Chipsmall

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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China
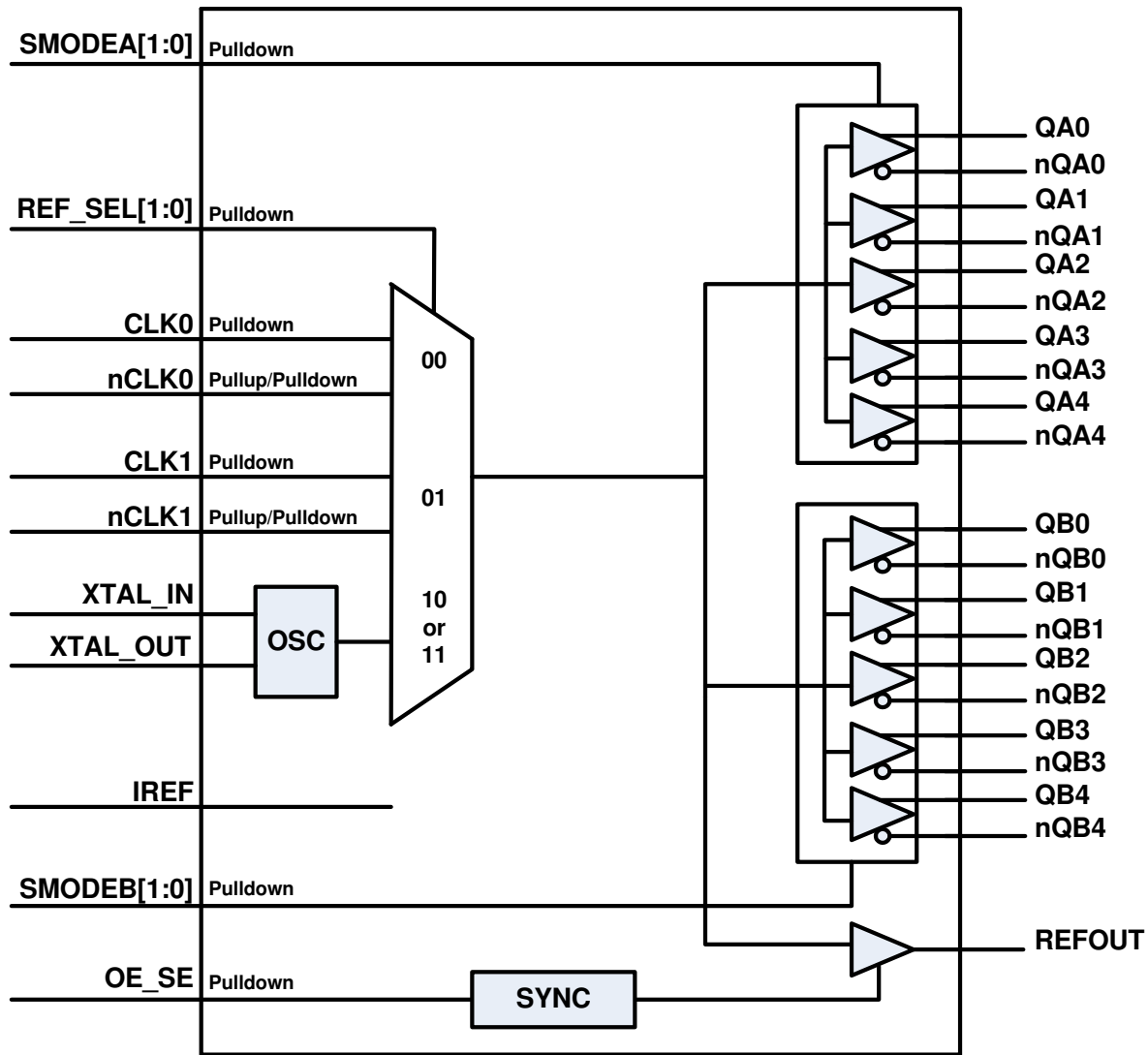
General Description

The IDT8T3910I is a high-performance clock fanout buffer. The input clock can be selected from two differential inputs or one crystal input. The internal oscillator circuit is automatically disabled if the crystal input is not selected. The selected signal is distributed to ten differential outputs which can be configured as LVPECL, LVDS or HSCL outputs. In addition, an LVCMOS output is provided. The user should always turn off this LVCMOS output when (the) clock is over 200MHz. The differential outputs can be disabled into an high-impedance state. The device is designed for signal fanout of high-frequency, low phase-noise clock and data signal. The outputs are at a defined level when inputs are open or shorted. It's designed to operate from a 3.3V core power supply, and either a 3.3V or 2.5V output operating supply.

Features

- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL
- Crystal Oscillator Interface
- Crystal input frequency range: 10MHz to 40MHz
- Two banks, each has five differential output pairs that can be configured as LVPECL or LVDS or HCSL
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: (Bank A and Bank B at the same output level) 32ps (typical)
- Part-to-part skew: 200ps (typical)
- Additive RMS phase jitter: 0.22ps (typical)
- Power supply modes:
- Output supply voltage modes:
  V_{CC}/V_{DDO}
  3.3V/3.3V
  3.3V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram

Pin Assignment

Top side pins (left to right): 36 QB0, 35 nQB0, 34 QB1, 33 nQB1, 32 V$_{DDO}$, 31 QB2, 30 nQB2, 29 V$_{DDO}$, 28 QB3, 27 nQB3, 26 QB4, 25 nQB4

Left side pins (top to bottom): 37 GND, 38 IREF, 39 SMODEB1, 40 nCLK1, 41 CLK1, 42 V$_{DD}$, 43 GND, 44 REFOUT, 45 V$_{DDO}$, 46 OE_SE, 47 SMODEA1, 48 GND

Right side pins (top to bottom): 24 GND, 23 SMODEB0, 22 REF_SEL1, 21 nCLK0, 20 CLK0, 19 REF_SEL0, 18 GND, 17 OSCO, 16 OSCI, 15 V$_{DD}$, 14 SMODEA0, 13 GND

Bottom side pins (left to right): 1 QA0, 2 nQA0, 3 QA1, 4 nQA1, 5 V$_{DDO}$, 6 QA2, 7 nQA2, 8 V$_{DDO}$, 9 QA3, 10 nQA3, 11 QA4, 12 nQA4

IDT8T3910I
48 Lead VFQFN
7.0mm x 7.0mm x 0.925mm, package body
NL Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QA0, nQA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
3, 4	QA1, nQA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
5, 8, 29, 32, 45	V_{DDO}	Power		Output supply pins.
6, 7	QA2, nQA2	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
9, 10	QA3, nQA3	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
11, 12	QA4, nQA4	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
13, 18, 24, 37, 43, 48	GND	Power		Power supply ground.
14, 47	SMODEA0, SMODEA1	Input	Pulldown	Output driver select for Bank A outputs. See Table 3D for function. LVCMOS/LVTTL interface levels.
15, 42	V_{DD}	Power		Power supply pins.
16, 17	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
19, 22	REF_SEL0, REF_SEL1	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3A for function.
20	CLK0	Input	Pulldown	Non-inverting differential clock.
21	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock. Internal resistor bias to $V_{DD}/2$.
23, 39	SMODEB0, SMODEB1	Input	Pulldown	Output driver select for Bank B outputs. See Table 3D for function. LVCMOS/LVTTL interface levels.
25, 26	nQB4, QB4	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
27, 28	nQB3, QB3	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
30, 31	nQB2, QB2	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
33, 34	nQB1, QB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
35, 36	nQB0, QB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
38	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QXx, nQXx clock outputs.
40	nCLK1	Input	Pullup/ Pulldown	Non-inverting differential clock. Internal resistor bias to $V_{DD}/2$.
41	CLK1	Input	Pulldown	Inverting differential clock.
44	REFOUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels
46	OE_SE	Input	Pulldown	Output enable. LVCMOS/LVTTL interface levels. See Table 3B.

NOTE: *Pulldown and Pullup* refer to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance	V_{DDO} = 3.3V		10		pF
		V_{DDO} = 2.5V		9		pF
R_{OUT}	Output Impedance	V_{DDO} = 3.3V		15		Ω
		V_{DDO} = 2.5V		18		Ω

Function Tables

Table 3A. REF_SELx Function Table

Control Input	
REF_SEL[1:0]	**Selected Input Reference Clock**
00 (default)	CLK0, nCLK0
01	CLK1, nCLK1
10	XTAL
11	XTAL

Table 3B. OE_SE Function Table

OE_SE	**REF_OUT**
0 (default)	High-Impedance
1	Enabled

NOTE: Synchronous output enable to avoid clock glitch.

Table 3C. Input/Output Operation Table, OE_SE

Input Status				Output State
OE_SE	REF_SEL [1:0]		CLKx and nCLKx	REFOUT
0	Not care		Don't Care	High Impedance
1	10 or 11		Don't Care	Fanout crystal oscillator
1	00		CLK0 and nCLK0 are both open circuit	Logic low
			CLK0 and nCLK0 are tied to ground	Logic low
			CLK0 is high, nCLK0 is low	Logic High
			CLK0 is low, nCLK0 is high	Logic Low
1	01		CLK1 and nCLK1 are both open circuit	Logic low
			CLK1 and nCLK1 are tied to ground	Logic low
			CLK1 is high, nCLK1 is low	Logic High
			CLK1 is low, nCLK1 is high	Logic Low

NOTE: The device output should support differential input being driven by a single-ended signal.

Table 3D. Input/Output Operation Table, SMODEA

Input Status			Output State
SMODEA[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QA[4:0], nQA[4:0]
11	Not care	Don't Care	High Impedance
00,01,or 10	10 or 11	Don't Care	Fanout crystal oscillator
00,01,or 10	00	CLK0 and nCLK0 are both open circuit	QA[4:0]=Low nQA4:0]=High
		CLK0 and nCLK0 are tied to ground	QA[4:0]=Low nQA[4:0]=High
		CLK0 is high, nCLK0 is low	QA[4:0]=High nQA[4:0]=Low
		CLK0 is low, nCLK0 is high	QA[4:0]=Low nQA[4:0]=High
00,01,or 10	01	CLK1 and nCLK1 are both open circuit	QA[4:0]=Low nQA4:0]=High
		CLK1 and CLK1 are tied to ground.	QA[4:0]=Low nQA[4:0]=High
		CLK1 is high, nCLK1 is low	QA[4:0]=High nQA[4:0]=Low
		CLK1 is low, nCLK1 is high	QA[4:0]=Low nQA4:0]=High

NOTE: The device output should support differential input being driven by a single-ended signal.

Table 3E. Input/Output Operation Table, SMODEB

Input Status			Output State
SMODEB[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QB[4:0], nQB[4:0]
11	Not care	Don't Care	High Impedance
00,01,or 10	10 or 11	Don't Care	Fanout crystal oscillator
00,01,or 10	00	CLK0 and nCLK0 are both open circuit	QB[4:0]=Low nQB4:0]=High
		CLK0 and nCLK0 are tied to ground	QB[4:0]=Low nQB[4:0]=High
		CLK0 is high, nCLK0 is low	QB[4:0]=High nQB[4:0]=Low
		CLK0 is low, nCLK0 is high	QB[4:0]=Low nQB[4:0]=High
00,01,or 10	01	CLK1 and nCLK1 are both open circuit	QB[4:0]=Low nQB[4:0]=High
		CLK1 and nCLK1 are tied to ground	QB[4:0]=Low nQB[4:0]=High
		CLK1 is high, nCLK1 is low	QB[4:0]=High nQB[4:0]=Low
		CLK1 is low, nCLK1 is high	QB[4:0]=Low nQB[4:0]=High

NOTE: The device output should support differential input being driven by a single-ended signal.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.
These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond
those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for
extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.6V
Inputs, V_I XTAL_IN Other Inputs	0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O, (HCSL, LVCMOS)	-0.5V to V_{DD} + 0.5V
Outputs, I_O, (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O, (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	29°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V\pm5\%$, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 01		67		mA
I_{DDO}	Output Supply Current	SMODEA/B[1:0] = 01		264		mA
I_{EE}	Power Supply Current	SMODEA/B[1:0] = 00 (default)		165		mA
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 10		80		mA
I_{DDO}	Power Supply Current	SMODEA/B[1:0] = 10		22		mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V\pm5\%$, $V_{DDO} = 2.5V\pm5\%$, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 01		67		mA
I_{DDO}	Output Supply Current	SMODEA/B[1:0] = 01		263		mA
I_{EE}	Power Supply Current	SMODEA/B[1:0] = 00 (default)		164		mA
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 10		80		mA
I_{DDO}	Power Supply Current	SMODEA/B[1:0] = 10		18		mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5% or 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V±5%	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V±5%	-0.3		0.8	V
I_{IH}	Input High Current	REF_SEL, SMODEA, SMODEB, OE_SE	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	OE_SE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1	REFOUT	V_{DDO} = 3.3V±5%	2.6			V
		REFOUT	V_{DDO} = 2.5V±5%	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	REFOUT	V_{DDO} = 3.3V±5% or 2.5V±5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

Table 4D. Differential DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5% or 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK[0:1], nCLK[0:1]	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK[0:1]	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK[0:1]	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.3		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} − 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2. Common mode voltage is defined as V_{IH}.

Table 4E. LVPECL DC Characteristics, V_{DD} = V_{DDO} = 3.3V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} − 1.4		V_{DDO} − 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} − 2.0		V_{DDO} − 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{DDO} − 2V.

Table 4F. LVPECL DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} − 1.4		V_{DDO} − 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} − 2.0		V_{DDO} − 1.4	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{DDO} − 2V.

Table 4G. LVDS DC Characteristics, V_{DD} = V_{DDO} = 3.3V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			405		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.26		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 4H. LVDS DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			405		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.26		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6A. AC Characteristics, V_{DD} = V_{DDO} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Using External Crystal	10		40	MHz
		LVDS, LVPECL output		500		MHz
		HCSL output			250	MHz
		LVCMOS output			200	MHz
tjit	Additive Phase Jitter:156.25MHz Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01	SMODEA/B[1:0] = 00		0.185		ps
		SMODEA/B[1:0] = 01		0.20		ps
		SMODEA/B[1:0] = 10		0.22		ps
tjit	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz	REF_SEL[1:0] = 10 or 11		0.375		ps
t_{PD}	Propagation Delay; CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs; NOTE 1	SMODEA/B[1:0] = 00		1.72		ns
		SMODEA/B[1:0] = 01		1.77		ns
		SMODEA/B[1:0] = 10		2.88		ns
$t$sk(o)	Output Skew; NOTE 2, 3			32		ps
$t$sk(pp)	Part-to-Part Skew; NOTE 3, 4			200		ps
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	HCSL Outputs	-100		100	mV
V_{MAX}	Voltage High; NOTE 7, 8	HCSL Outputs			1150	mV
V_{MIN}	Voltage Low; NOTE 7, 9	HCSL Outputs	-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	HCSL Outputs	250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	HCSL Outputs			140	mV
	Rise/Fall Edge Rate; NOTE 7, 13	HCSL Outputs; Measured between 150mV to +150mV	0.6		4.0	V/ns
t_R / t_F	Output Rise/Fall Time	SMODEA/B[1:0] = 00; 20% to 80%		430		ps
		SMODEA/B[1:0] = 01; 20% to 80%		515		
MUX_ISOLATION	MUX Isolation	156.25MHz		83		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: Measurement taken from differential waveform.
NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.
NOTE 7: Measurement taken from single-ended waveform.
NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.
Notes continued on next page.

NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
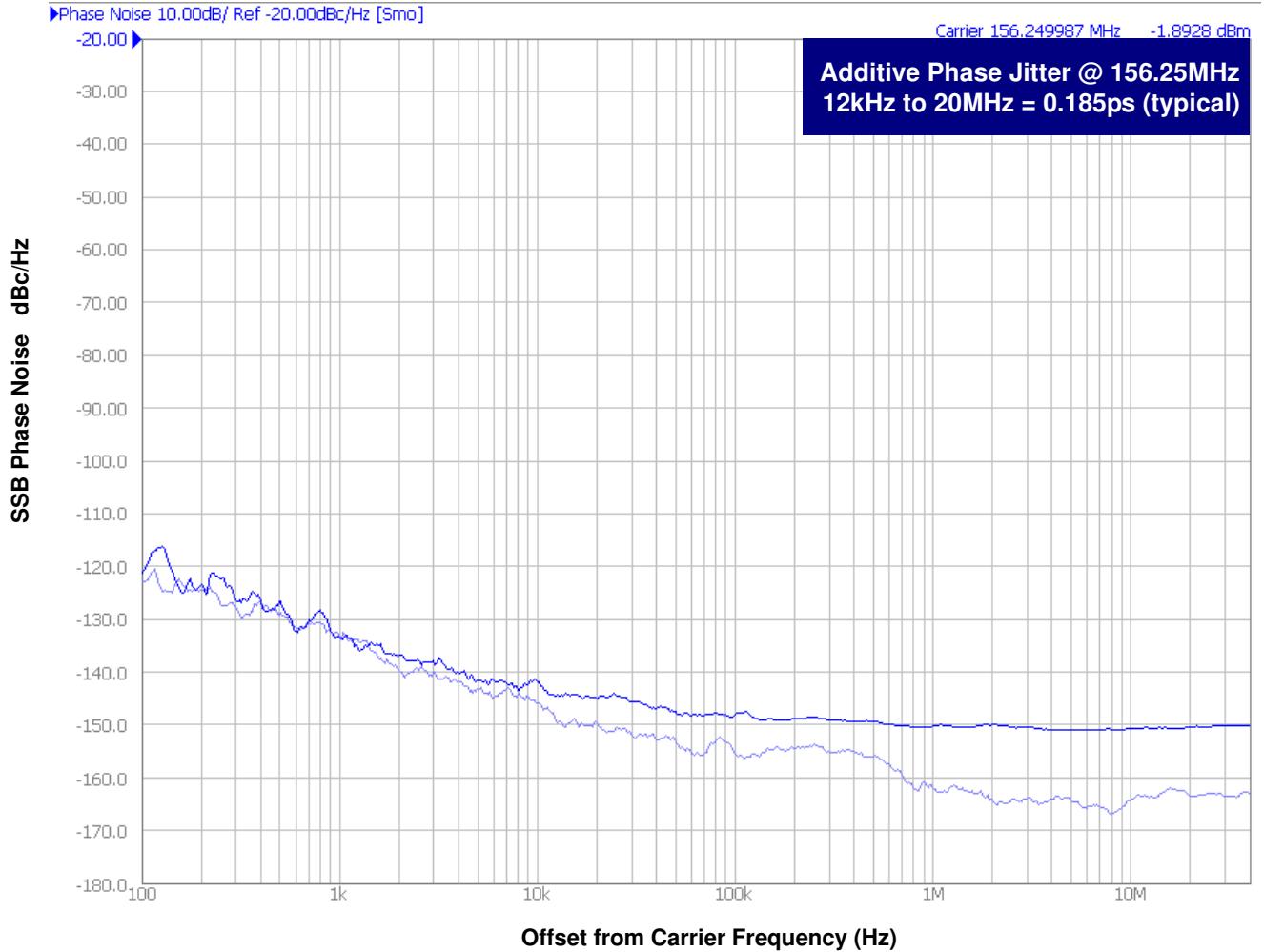Notes continue on next page.
NOTE 12: Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Table 6B. AC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Using External Crystal	10		40	MHz
		LVDS, LVPECL output		500		MHz
		HCSL output			250	MHz
		LVCMOS output			200	MHz
tjit	Additive Phase Jitter: 156.25 MHz Integration Range: 12kHz - 20 MHz REF_SEL[1:0] = 00 or 10					
		SMODEA/B[1:0] = 00		0.185		ps
		SMODEA/B[1:0] = 01		0.20		ps
		SMODEA/B[1:0] = 10		0.22		ps
tjit	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz	REF_SEL[1:0] = 10 or 11		0.375		ps
t_{PD}	Propagation Delay; CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs; NOTE 1	SMODEA/B[1:0] = 00		1.72		ns
		SMODEA/B[1:0] = 01		1.77		ns
		SMODEA/B[1:0] = 10		2.88		ns
$tsk(o)$	Output Skew; NOTE 2, 3			32		ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4			200		ps
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	HCSL Outputs	-100		100	mV
V_{MAX}	Voltage High; NOTE 7, 8	HCSL Outputs			1150	mV
V_{MIN}	Voltage Low; NOTE 7, 9	HCSL Outputs	-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	HCSL Outputs	250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	HCSL Outputs			140	mV
	Rise/Fall Edge Rate; NOTE 7, 13	HCSL Outputs; Measured between 150mV to +150mV	0.6		4.0	V/ns
t_R / t_F	Output Rise/Fall Time	SMODEA/B[1:0] = 00; 20% to 80%		430		ps
		SMODEA/B[1:0] = 01; 20% to 80%		570		
MUX_ISOLATION	MUX Isolation	156.25MHz		83		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
Notes continued on next page.

NOTE 5: Measurement taken from differential waveform.

NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.

NOTE 7: Measurement taken from single-ended waveform.

NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

NOTE 12: Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

NOTE 13: Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Additive Phase Jitter (LVPECL)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a

ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. The additive phase jitter is dependent on the input source and measurement equipment.

The above plot was measured using a Rohde & Schwarz SMA100A as the input source.

Additive Phase Jitter (HCSL)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a

ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. The additive phase jitter is dependent on the input source and measurement equipment.

The above plot was measured using a Rohde & Schwarz SMA100A as the input source.

Additive Phase Jitter (LVDS)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a

ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. The additive phase jitter is dependent on the input source and measurement equipment.

The above plot was measured using a Rohde & Schwarz SMA100A as the input source.

Typical Phase Noise at 25MHz Integration Range: 100Hz - 1MHz
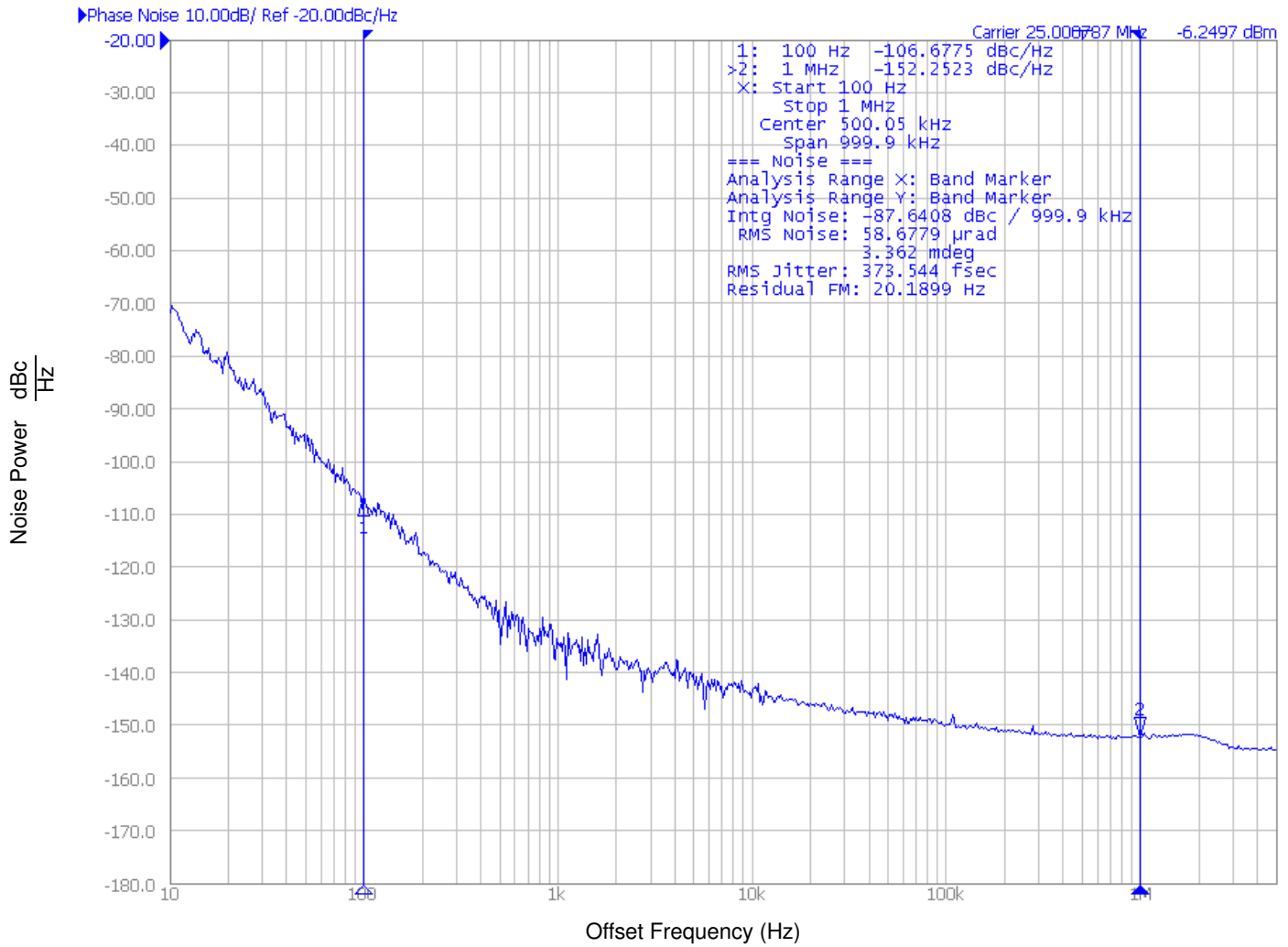
Parameter Measurement Information
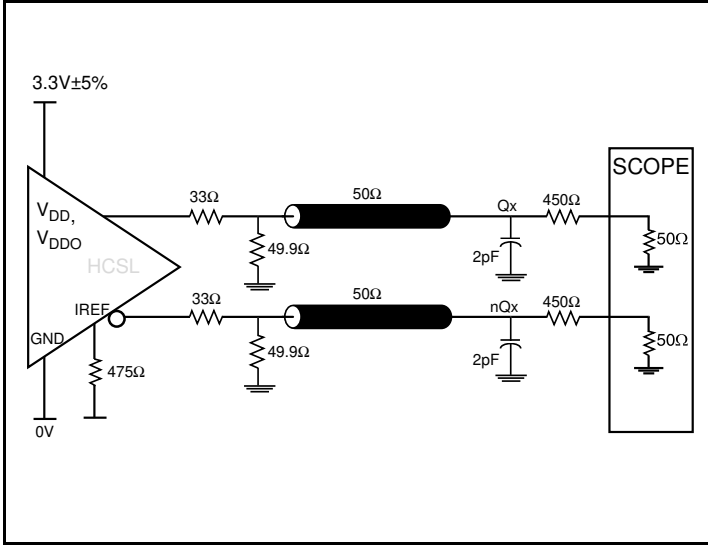
3.3V Core/3.3V HCSL Output Load AC Test Circuit
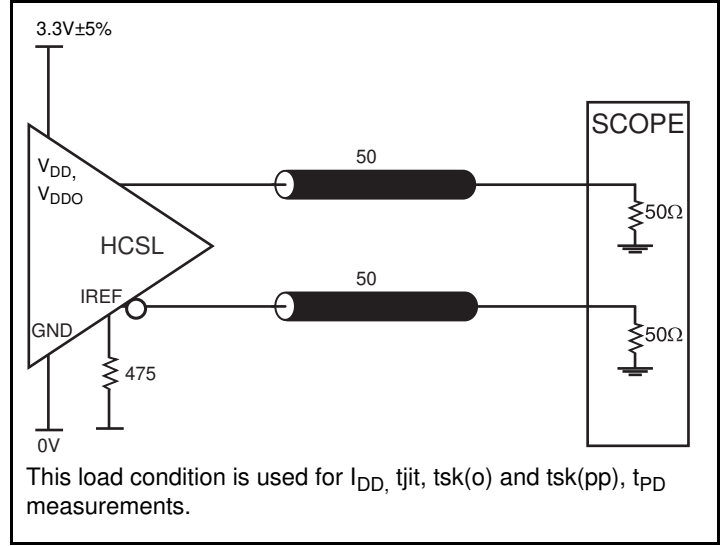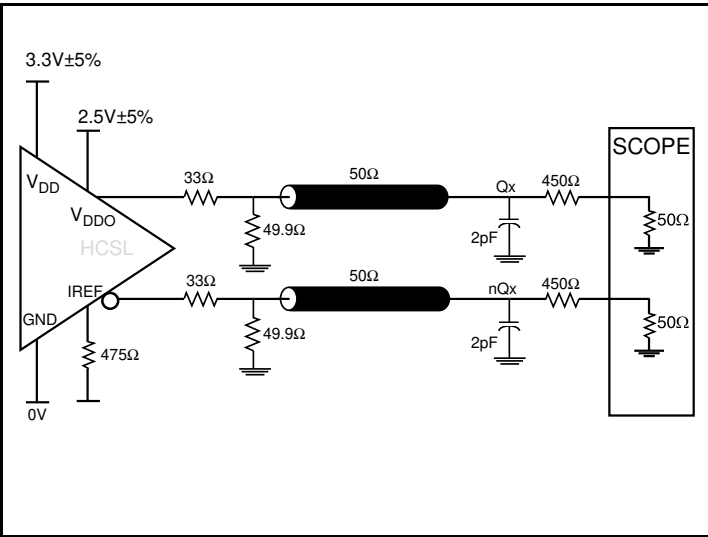
This load condition is used for I_{DD}, tjit, tsk(o) and tsk(pp), t_{PD} measurements.

3.3V Core/3.3V HCSL Output Load AC Test Circuit

3.3V Core/2.5V HCSL Output Load AC Test Circuit

This load condition is used for I_{DD}, tjit, tsk(o) and tsk(pp), t_{PD} measurements.
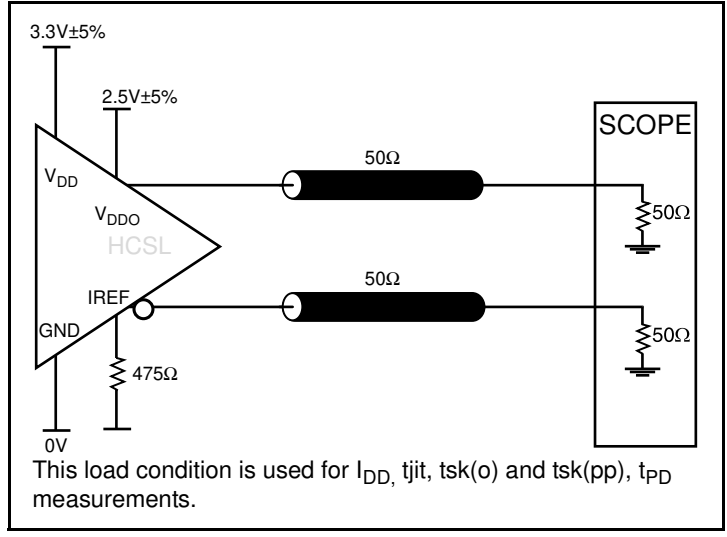
3.3V Core/2.5V HCSL Output Load AC Test Circuit
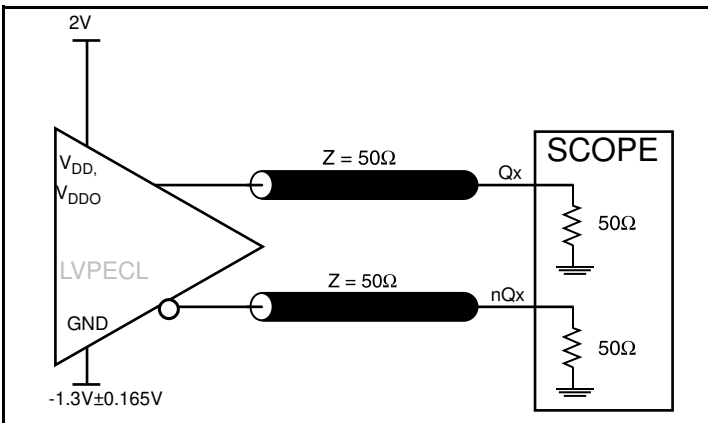
3.3V Core/3.3V LVPECL Output Load AC Test Circuit
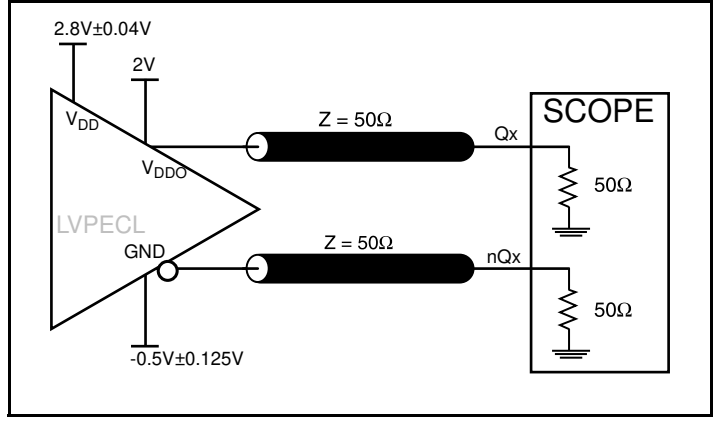
3.3V Core/2.5V LVPECL Output Load AC Test Circuit

Parameter Measurement Information, continued
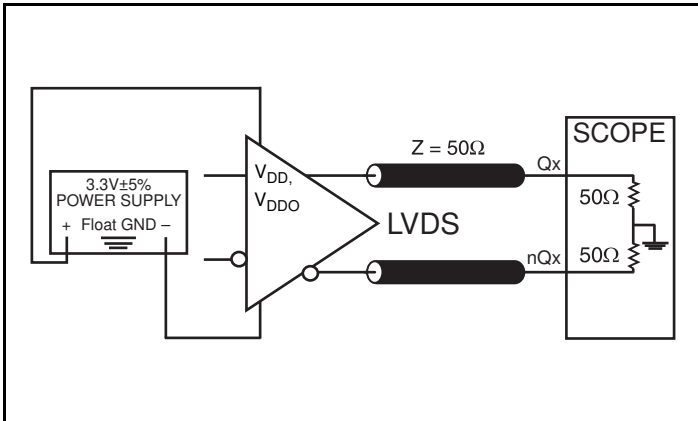
3.3V Core/3.3V LVDS Output Load AC Test Circuit
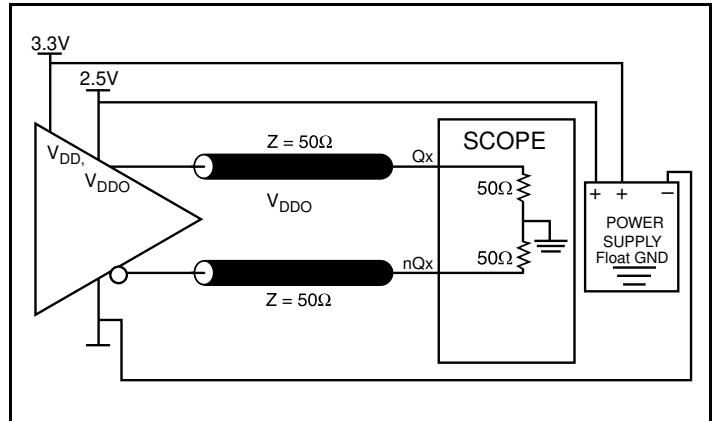
2.5V Core/2.5V LVDS Output Load AC Test Circuit
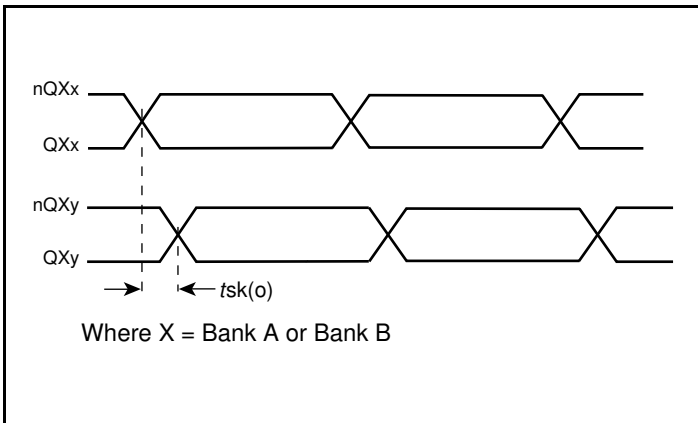
Output Skew
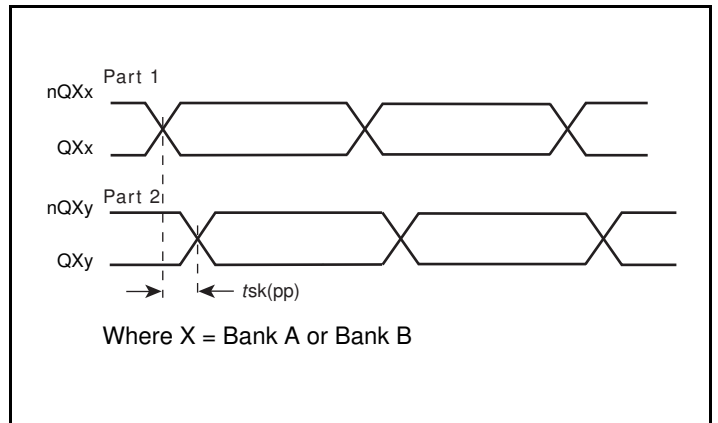
Part-to-Part Skew
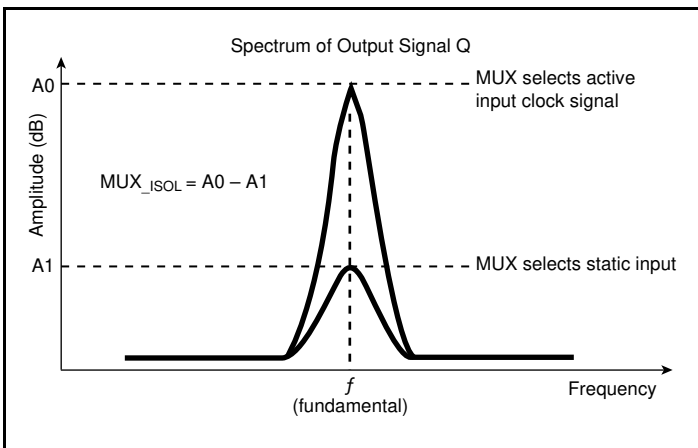
MUX Isolation
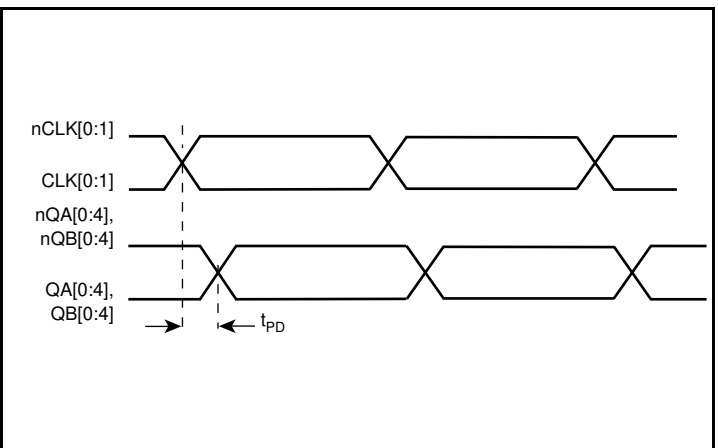
Propagation Delay

Parameter Measurement Information, continued
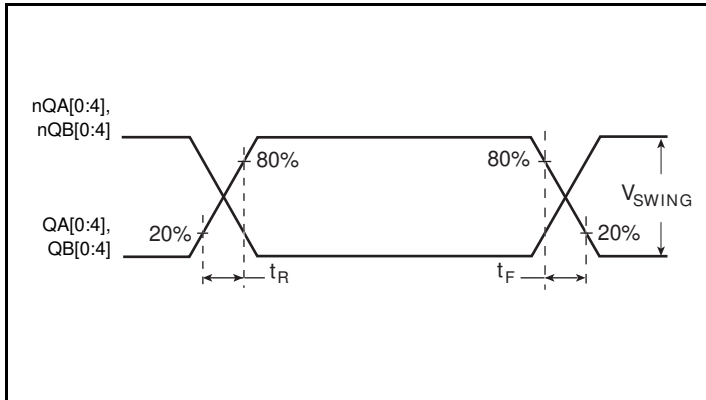
LVPECL Output Rise/Fall Time
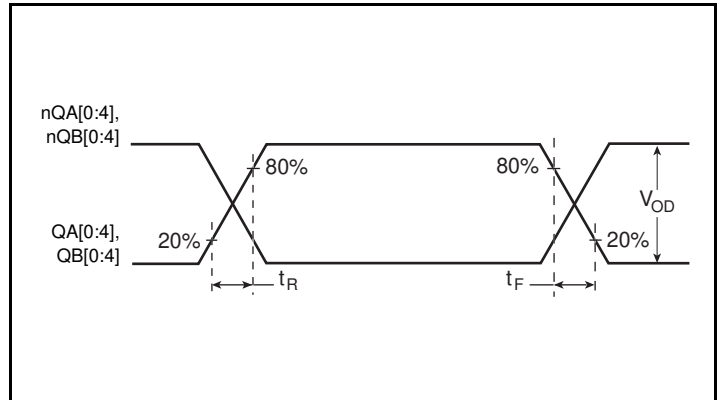
LVDS Output Rise/Fall Time
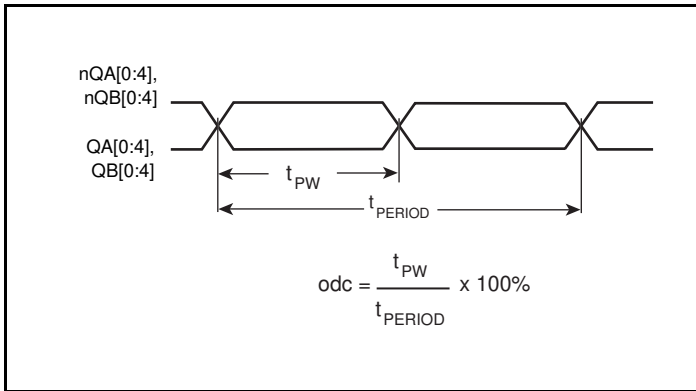
Output Duty Cycle/Pulse Width/Period
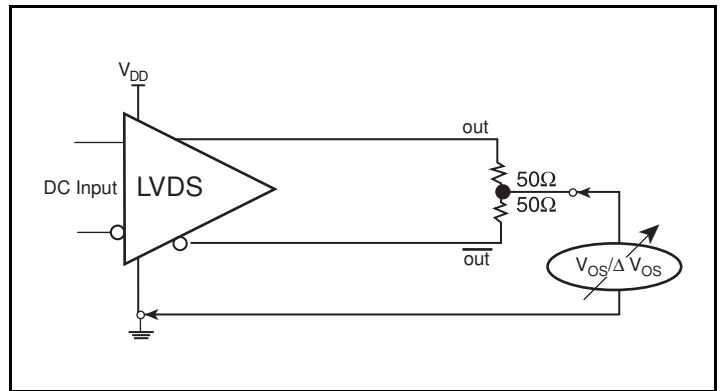
Offset Voltage Setup
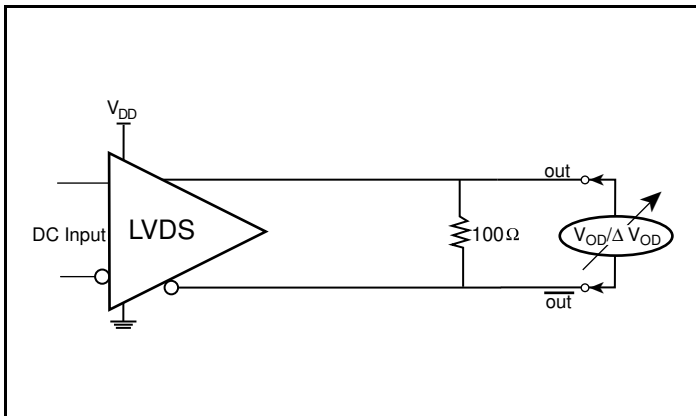
Differential Output Voltage Setup
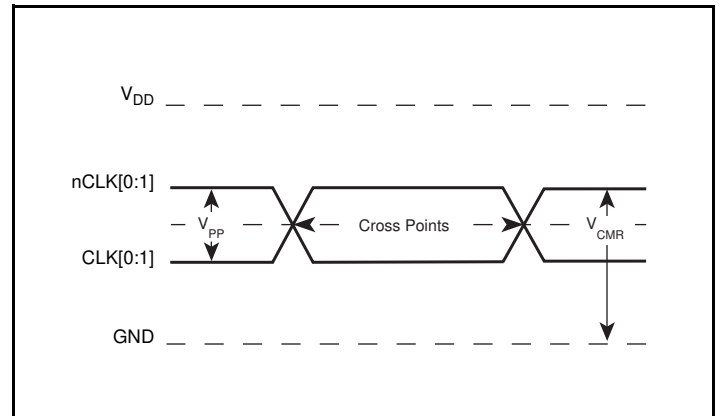
Differential Input Level

Parameter Measurement Information, continued
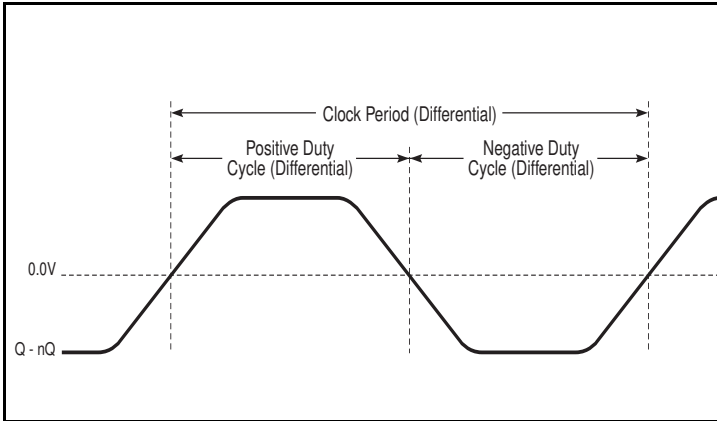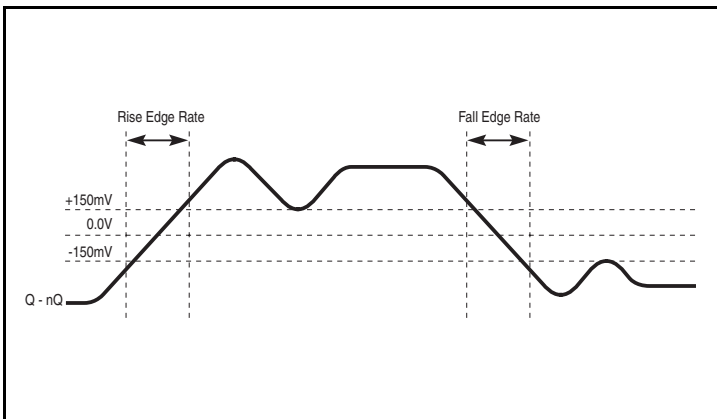

Differential Measurement Points for Duty Cycle/Period
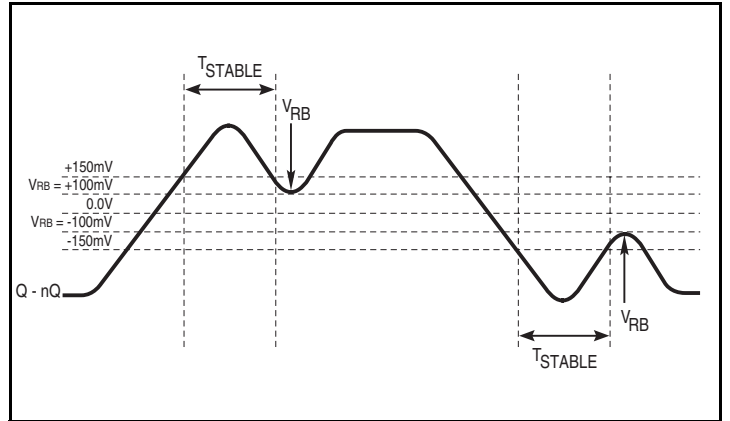
Differential Measurement Points for Ringback
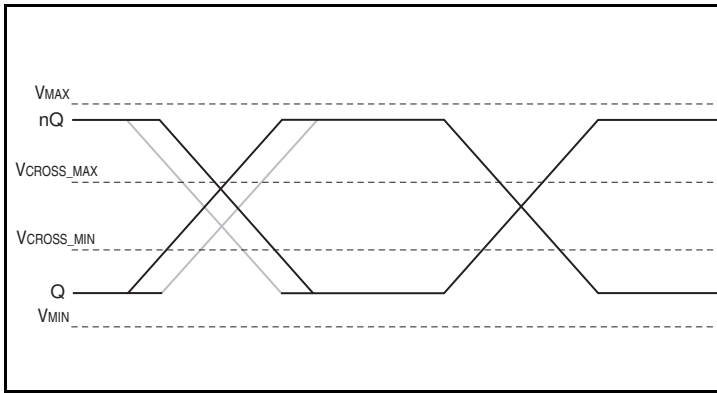
Single-ended Measurement Points for Absolute Cross Point/Swing
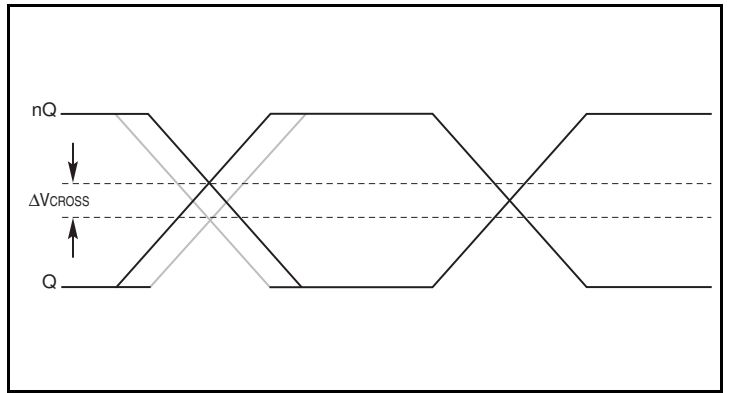
Single-ended Measurement Points for Delta Cross Point

Differential Measurement Points for Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating We recommend that there is no trace attached.

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.
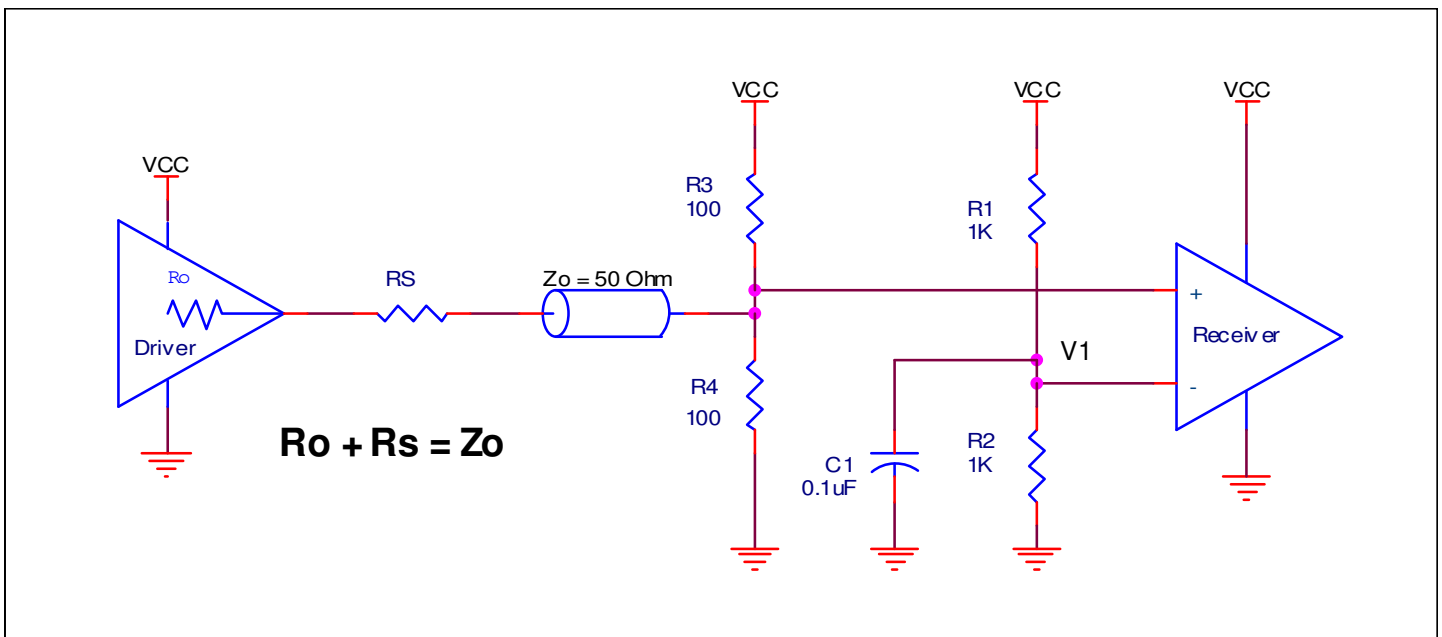

Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Crystal Input Interface

The IDT8T3910I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.
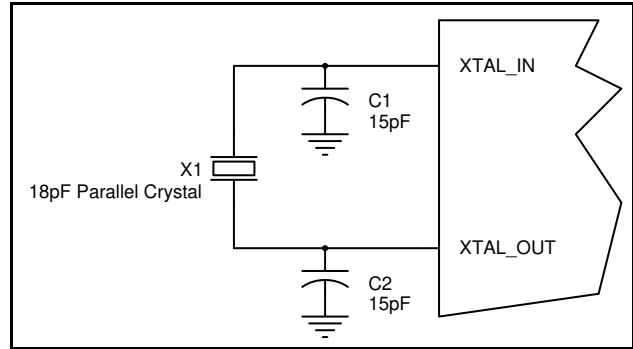
Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.
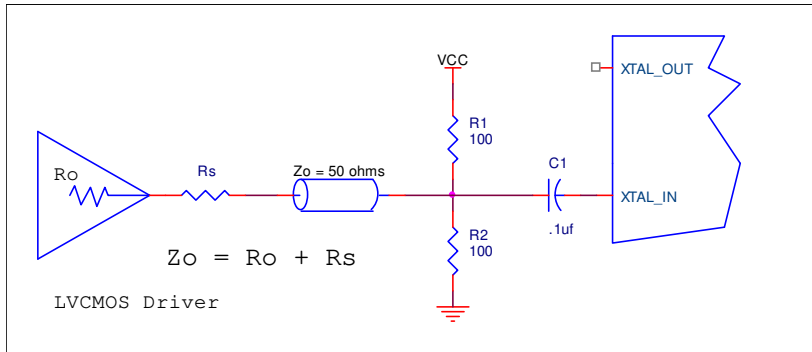
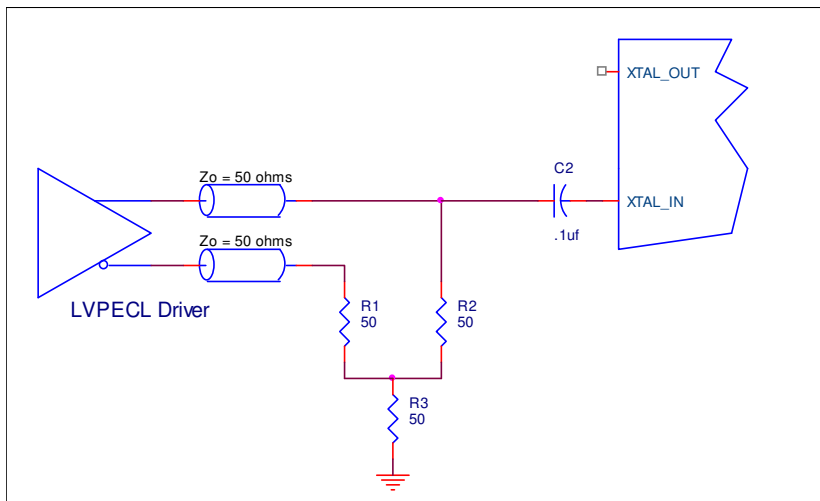**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**

Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface