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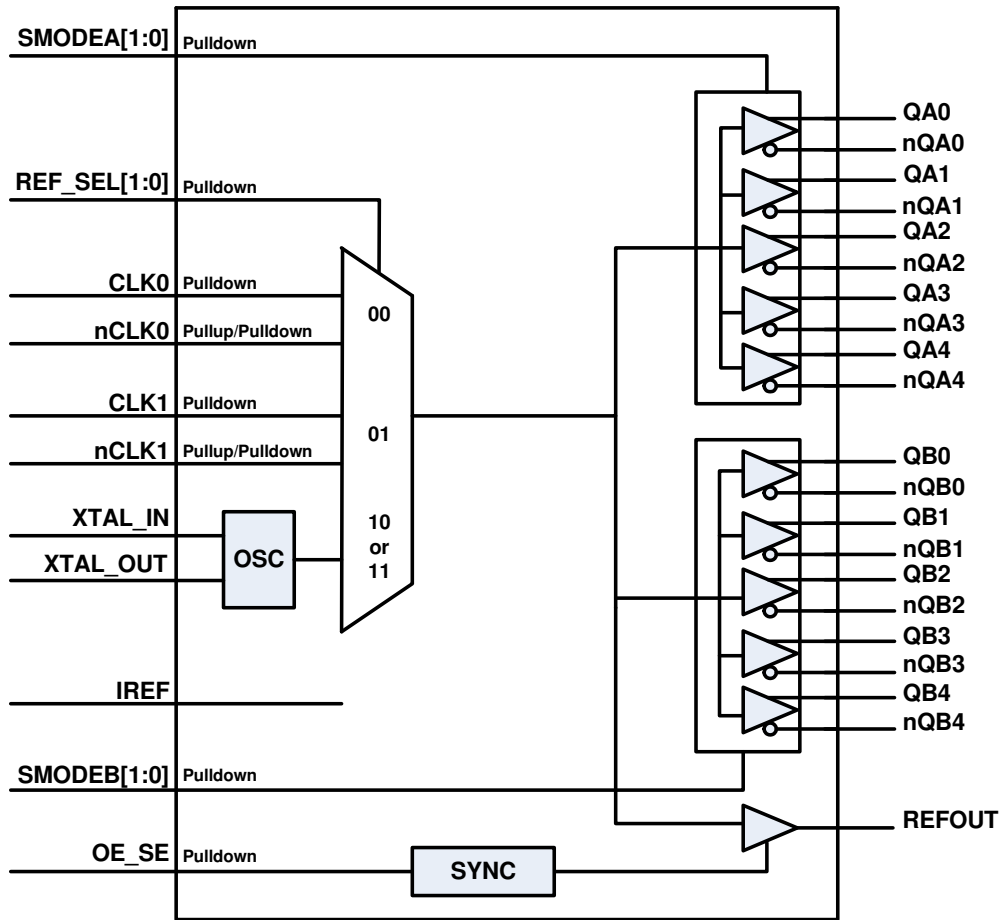
General Description

The IDT8T39S10I is a high-performance clock fanout buffer. The input clock can be selected from two differential inputs or one crystal input. The internal oscillator circuit is automatically disabled if the crystal input is not selected. The crystal pin can be driven by single-ended clock when crystal is bypassed. The selected signal is distributed to ten differential outputs which can be configured as LVPECL, LVDS or HSCL outputs. In addition, an LVCMOS output is provided. All outputs can be disabled into a high-impedance state. The device is designed for signal fanout of high-frequency, low phase-noise clock and data signal. The outputs are at a defined level when inputs are open circuit or tied to ground. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

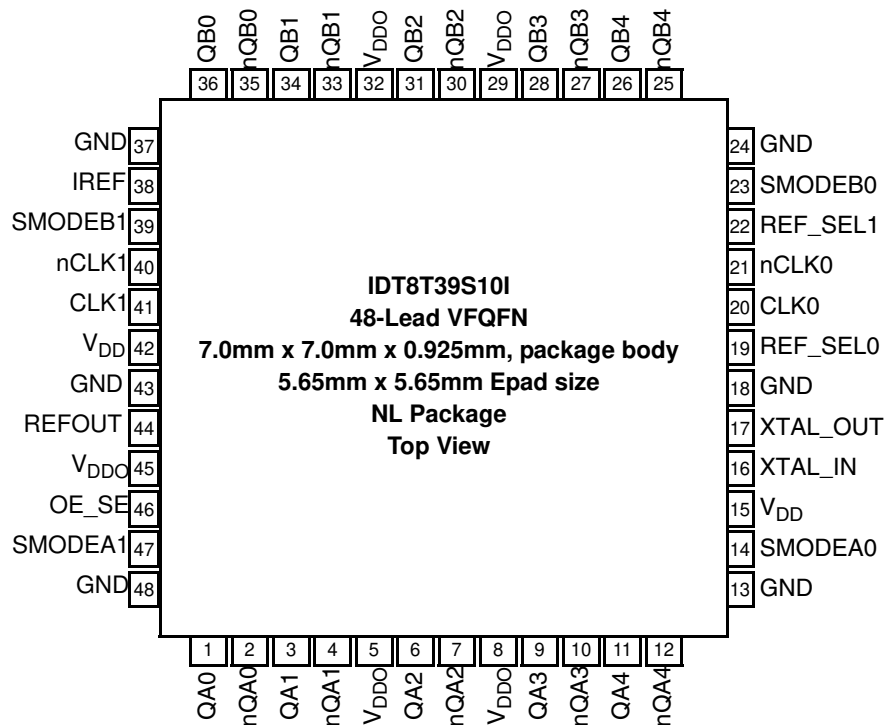
Features

- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL
- Crystal Oscillator Interface
- Crystal input frequency range: 10MHz to 40MHz
- Maximum Output Frequency
 - LVPECL - 2GHz
 - LVDS - 2GHz
 - HCSL - 250MHz
 - LVCMOS - 250MHz
- Two banks, each has five differential output pairs that can be configured as LVPECL or LVDS or HCSL
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: (Bank A and Bank B at the same output level) 70ps (max)
- Part-to-part skew: 250ps (max)
- Additive RMS phase jitter: 0.153ps (typical)
- Supply voltage modes:
 - V_{DD}/V_{DDO}
 - 3.3V/3.3V
 - 3.3V/2.5V
 - 2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QA0, nQA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
3, 4	QA1, nQA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
5, 8, 29, 32, 45	V _{DDO}	Power		Output supply pins.
6, 7	QA2, nQA2	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
9, 10	QA3, nQA3	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
11, 12	QA4, nQA4	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
13, 18, 24, 37, 43, 48	GND	Power		Power supply ground.
14, 47	SMODEA0, SMODEA1	Input	Pulldown	Output driver select for Bank A outputs. See Table 3D for function. LVCMOS/LVTTL interface levels.
15, 42	V _{DD}	Power		Power supply pins.
16, 17	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
19, 22	REF_SEL0, REF_SEL1	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3A for function.
20	CLK0	Input	Pulldown	Non-inverting differential clock.
21	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock. Internal resistor bias to V _{DD} /2.
23, 39	SMODEB0, SMODEB1	Input	Pulldown	Output driver select for Bank B outputs. See Table 3D for function. LVCMOS/LVTTL interface levels.
25, 26	nQB4, QB4	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
27, 28	nQB3, QB3	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
30, 31	nQB2, QB2	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
33, 34	nQB1, QB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
35, 36	nQB0, QB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
38	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for HCSL mode. QXx, nQXx clock outputs.
40	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock. Internal resistor bias to V _{DD} /2.
41	CLK1	Input	Pulldown	Non-inverting differential clock.
44	REFOUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels
46	OE_SE	Input	Pulldown	Output enable. LVCMOS/LVTTL interface levels. See Table 3B.

NOTE: *Pulldown* and *Pullup* refer to an internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance		SMODEx[0:1], REF_SEL[0:1], OE_SE pins		4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		k Ω
R_{PULLUP}	Input Pullup Resistor				51		k Ω
C_{PD}	Power Dissipation Capacitance	Qx, nQx	$V_{DDO} = 3.3V$		3.5		pF
C_{PD}	Power Dissipation Capacitance REFOUT		$V_{DDO} = 3.3V$		8		pF
			$V_{DDO} = 2.5V$		7		pF
R_{OUT}	Output Impedance	REFOUT	$V_{DDO} = 3.3V$		15		Ω
		REFOUT	$V_{DDO} = 2.5V$		20		Ω

Function Tables

Table 3A. REF_SELx Function Table

Control Input	Selected Input Reference Clock
REF_SEL[1:0]	
00 (default)	CLK0, nCLK0
01	CLK1, nCLK1
10	XTAL
11	XTAL

Table 3B. OE_SE Function Table

OE_SE	REFOUT
0 (default)	High-Impedance
1	Enabled

NOTE: Synchronous output enable to avoid clock glitch.

Table 3C. Input/Output Operation Table, OE_SE

Input Status			Output State
OE_SE	REF_SEL [1:0]	CLKx and nCLKx	REFOUT
0 (default)	Don't care	Don't Care	High Impedance
1	10 or 11	Don't Care	Fanout crystal oscillator
1	00 (default)	CLK0 and nCLK0 are both open circuit	Logic low
		CLK0 and nCLK0 are tied to ground	Logic low
		CLK0 is high, nCLK0 is low	Logic High
		CLK0 is low, nCLK0 is high	Logic Low
1	01	CLK1 and nCLK1 are both open circuit	Logic low
		CLK1 and nCLK1 are tied to ground	Logic low
		CLK1 is high, nCLK1 is low	Logic High
		CLK1 is low, nCLK1 is high	Logic Low

Table 3D. Input/Output Operation Table, SMODEA

Input Status			Output State
SMODEA[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QA[4:0], nQA[4:0]
11	Don't care	Don't Care	High Impedance
00, 01 or 10	10 or 11	Don't Care	Fanout crystal oscillator
00, 01 or 10	00 (default)	CLK0 and nCLK0 are both open circuit	QA[4:0] = Low nQA[4:0] = High
		CLK0 and nCLK0 are tied to ground	QA[4:0] = Low nQA[4:0] = High
		CLK0 is high, nCLK0 is low	QA[4:0] = High nQA[4:0] = Low
		CLK0 is low, nCLK0 is high	QA[4:0] = Low nQA[4:0] = High
00, 01 or 10	01	CLK1 and nCLK1 are both open circuit	QA[4:0] = Low nQA[4:0] = High
		CLK1 and nCLK1 are tied to ground.	QA[4:0] = Low nQA[4:0] = High
		CLK1 is high, nCLK1 is low	QA[4:0] = High nQA[4:0] = Low
		CLK1 is low, nCLK1 is high	QA[4:0] = Low nQA[4:0]=High

Table 3E. Input/Output Operation Table, SMODEB

Input Status			Output State
SMODEB[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QB[4:0], nQB[4:0]
11	Don't care	Don't Care	High Impedance
00, 01 or 10	10 or 11	Don't Care	Fanout crystal oscillator
00, 01 or 10	00 (default)	CLK0 and nCLK0 are both open circuit	QB[4:0] = Low nQB[4:0] = High
		CLK0 and nCLK0 are tied to ground	QB[4:0] = Low nQB[4:0] = High
		CLK0 is high, nCLK0 is low	QB[4:0] = High nQB[4:0] = Low
		CLK0 is low, nCLK0 is high	QB[4:0] = Low nQB[4:0] = High
00, 01 or 10	01	CLK1 and nCLK1 are both open circuit	QB[4:0] = Low nQB[4:0] = High
		CLK1 and nCLK1 are tied to ground	QB[4:0] = Low nQB[4:0] = High
		CLK1 is high, nCLK1 is low	QB[4:0] = High nQB[4:0] = Low
		CLK1 is low, nCLK1 is high	QB[4:0] = Low nQB[4:0] = High

Table 3F. Output Level Selection Table, QA[0:4], nQA[0:4]

SMODEA1	SMODEA0	Output Type
0	0	LVPECL (default)
0	1	LVDS
1	0	HCSSL
1	1	High-impedance

Table 3G. Output Level Selection Table, QB[0:4], nQB[0:4]

SMODEB1	SMODEB0	Output Type
0	0	LVPECL (default)
0	1	LVDS
1	0	HCSSL
1	1	High-impedance

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	0V to 2V -0.5V to $V_{DD} + 0.5V$
Outputs, V_O , (HCSL, LVCMOS)	-0.5V to $V_{DDO} + 0.5V$
Outputs, I_O , (LVPECL) Continuous Current Surge Current	50mA 100mA
Outputs, I_O , (LVDS) Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, θ_{JA}	30.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, GND = 0V, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 01		61	75	mA
I_{DDO}	Output Supply Current	SMODEA/B[1:0] = 01		211	255	mA
I_{EE}	Power Supply Current	SMODEA/B[1:0] = 00 (default)		151	184	mA
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 10		43	55	mA
I_{DDO}	Power Supply Current	SMODEA/B[1:0] = 10		25	35	mA

NOTE: Characterized with all outputs unloaded. I_{DDO} includes REFOUT.

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, GND = 0V, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 01		61	75	mA
I_{DDO}	Output Supply Current	SMODEA/B[1:0] = 01		210	255	mA
I_{EE}	Power Supply Current	SMODEA/B[1:0] = 00 (default)		147	184	mA
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 10		43	55	mA
I_{DDO}	Power Supply Current	SMODEA/B[1:0] = 10		25	35	mA

NOTE: Characterized with all outputs unloaded. I_{DDO} includes REFOUT.

Table 4C. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $GND = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 01		56	69	mA
I_{DDO}	Output Supply Current	SMODEA/B[1:0] = 01		202	245	mA
I_{EE}	Power Supply Current	SMODEA/B[1:0] = 00 (default)		141	173	mA
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 10		40	50	mA
I_{DDO}	Power Supply Current	SMODEA/B[1:0] = 10		24	32	mA

NOTE: Characterized with all outputs unloaded. I_{DDO} includes REFOUT.

Table 4D. LVCMOS/LVTTL DC Characteristics,

$V_{DD} = 3.3V \pm 5\%$, $2.5V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $GND = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	$V_{DD} = 3.3V \pm 5\%$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V \pm 5\%$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	$V_{DD} = 3.3V \pm 5\%$	-0.3		0.8	V
		$V_{DD} = 2.5V \pm 5\%$	-0.3		0.7	V
I_{IH}	Input High Current	REF_SEL, SMODEA, SMODEB, OE_SE $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	μA
I_{IL}	Input Low Current	OE_SE $V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage; NOTE 1	REFOUT $V_{DDO} = 3.3V \pm 5\%$: $I_{OH} = -8mA$	2.6			V
		REFOUT $V_{DDO} = 2.5V \pm 5\%$: $I_{OH} = -8mA$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	REFOUT $V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$: $I_{OL} = 8mA$			0.5	V

Table 4E. Differential DC Characteristics, $V_{DD} = 3.3V \pm 5\%$ or $2.625V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK[0:1], nCLK[0:1] $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	μA
I_{IL}	Input Low Current	CLK[0:1] $V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			μA
		nCLK[0:1] $V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			μA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.240		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		$GND + 0.5$		$V_{DD} - 0.85$	V

NOTE 1: V_{IL} should not be less than $-0.3V$.

NOTE 2: Common mode voltage is defined as the crosspoint.

Table 4F. LVPECL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $GND = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} - 1.4$		$V_{DDO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} - 2.0$		$V_{DDO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO} - 2V$.**Table 4G. LVPECL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$ or $2.625V$, $V_{DDO} = 2.5V \pm 5\%$, $GND = 0V$, $T_A = -40^\circ C$ to $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} - 1.4$		$V_{DDO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} - 2.0$		$V_{DDO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO} - 2V$.**Table 4H. LVDS DC Characteristics, $V_{DD} = 3.3V \pm 5\%$ or $2.625V$, $V_{DDO} = 2.5V \pm 5\%$, $GND = 0V$, $T_A = -40^\circ C$ to $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	400	462	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.00	1.16	1.25	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4I. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $GND = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	400	462	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.00	1.12	1.21	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Capacitive Loading (CL)			12	18	pF

AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Using External Crystal	10		40	MHz
		LVDS, LVPECL Outputs			2000	MHz
		HCSL Outputs			250	MHz
		LVC MOS Output			250	MHz
t_{jit}	Buffer Additive Phase Jitter, RMS: 156.25MHz Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01	SMODEA/B[1:0] = 00		0.153	0.200	ps
		SMODEA/B[1:0] = 01		0.163	0.200	ps
		SMODEA/B[1:0] = 10		0.198	0.250	ps
$t_{jit}(\emptyset)$	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz	REF_SEL[1:0] = 10 or 11		0.250	0.525	ps
t_{PD}	Propagation Delay; CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs; NOTE 1	SMODEA/B[1:0] = 00	0.65		1.10	ns
		SMODEA/B[1:0] = 01	0.59		1.15	ns
		SMODEA/B[1:0] = 10	1.70		2.65	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 3				70	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				250	ps
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	HCSL Outputs	-100		100	mV
V_{MAX}	Voltage High; NOTE 7, 8	HCSL Outputs			920	mV
V_{MIN}	Voltage Low; NOTE 7, 9	HCSL Outputs	-150		+150	mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	HCSL Outputs			520	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	HCSL Outputs			140	mV
	Rise/Fall Edge Rate; NOTE 13	HCSL Outputs	Measured between 150mV to +150mV	0.6	4.0	V/ns
t_R / t_F	Output Rise/Fall Time	SMODEA/B[1:0] = 00; 20% to 80%	60	200	310	ps
		SMODEA/B[1:0] = 01; 20% to 80%	40	170	300	ps
$MUX_ISOLATION$	MUX Isolation	156.25MHz		70		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All LVDS and LVPECL parameters characterized up to 1.5GHz. HCSL parameters characterized up to 250MHz.

NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint.

NOTE 5: Measurement taken from differential waveform.

Notes continued on next page.

NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum $\pm 150\text{mV}$ differential voltage after rising/falling edges before it is allowed to drop back into the $V_{\text{RB}} \pm 100\text{mV}$ differential range.

NOTE 7: Measurement taken from single-ended waveform.

NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 10: Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

NOTE 11: Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement.

NOTE 12: Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in V_{cross} for any particular system.

NOTE 13: Measured from -150mV to $+150\text{mV}$ on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Table 6B. AC Characteristics, $V_{\text{DD}} = 3.3\text{V} \pm 5\%$, $V_{\text{DDO}} = 2.5\text{V} \pm 5\%$, $T_{\text{A}} = -40^{\circ}\text{C}$ to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		Using External Crystal	10		40	MHz
		LVDS, LVPECL Outputs				2000	MHz
		HCSL Outputs				250	MHz
		LVC MOS Output				250	MHz
t_{jit}	Additive Phase Jitter: 156.25MHz Integration Range: 12kHz - 20MHz REF_SEL[1:0] = 00 or 10		SMODEA/B[1:0] = 00		0.181	0.235	ps
			SMODEA/B[1:0] = 01		0.181	0.235	ps
			SMODEA/B[1:0] = 10		0.200	0.250	ps
$t_{\text{jit}}(\emptyset)$	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz		REF_SEL[1:0] = 10 or 11		0.258	0.525	ps
t_{PD}	Propagation Delay; CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs; NOTE 1		SMODEA/B[1:0] = 00	0.40		1.60	ns
			SMODEA/B[1:0] = 01	0.57		1.10	ns
			SMODEA/B[1:0] = 10	1.75		2.85	ns
$t_{\text{sk}}(\text{o})$	Output Skew; NOTE 2, 3				70	ps	
$t_{\text{sk}}(\text{pp})$	Part-to-Part Skew; NOTE 3, 4				250	ps	
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	HCSL Outputs		-100		100	mV
V_{MAX}	Voltage High; NOTE 7, 8	HCSL Outputs				920	mV
V_{MIN}	Voltage Low; NOTE 7, 9	HCSL Outputs		-150		+150	mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	HCSL Outputs		250		520	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	HCSL Outputs				140	mV
	Rise/Fall Edge Rate; NOTE 13	HCSL Outputs	Measured between 150mV to +150mV	0.6		4.0	V/ns
$t_{\text{R}} / t_{\text{F}}$	Output Rise/Fall Time		SMODEA/B[1:0] = 00; 20% to 80%	60	200	310	ps
			SMODEA/B[1:0] = 01; 20% to 80%	40	170	300	ps
$\text{MUX}_{\text{ISOLATION}}$	MUX Isolation		156.25MHz		70		dB

Notes continued on next page.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All LVDS and LVPECL parameters characterized up to 1.5GHz. HCSL parameters characterized up to 250MHz.

NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint.

NOTE 5: Measurement taken from differential waveform.

NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum $\pm 150\text{mV}$ differential voltage after rising/falling edges before it is allowed to drop back into the $V_{\text{RB}} \pm 100\text{mV}$ differential range.

NOTE 7: Measurement taken from single-ended waveform.

NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 10: Measured at crosspoint where the instantaneous voltage value of the rising edge of Q_x equals the falling edge of nQ_x .

NOTE 11: Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement.

NOTE 12: Defined as the total variation of all crossing voltages of rising Q_x and falling nQ_x , This is the maximum allowed variance in V_{cross} for any particular system.

NOTE 13: Measured from -150mV to $+150\text{mV}$ on the differential waveform (Q_x minus nQ_x). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Table 6C. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		Using External Crystal	10		40	MHz
			LVDS, LVPECL Outputs			2000	MHz
			HCSL Outputs			250	MHz
			LVC MOS Output			250	MHz
t_{jit}	Additive Phase Jitter: 156.25MHz Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01		SMODEA/B[1:0] = 00		0.159	0.205	ps
			SMODEA/B[1:0] = 01		0.173	0.215	ps
			SMODEA/B[1:0] = 10		0.211	0.250	ps
$t_{jit}(\emptyset)$	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz		REF_SEL[1:0] = 10 or 11		0.254	0.510	ps
t_{PD}	Propagation Delay; CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs; NOTE 1		SMODEA/B[1:0] = 00	0.68		1.15	ns
			SMODEA/B[1:0] = 01	0.56		1.15	ns
			SMODEA/B[1:0] = 10	1.79		2.90	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 3				70	ps	
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				250	ps	
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	HCSL Outputs		-100		100	mV
V_{MAX}	Voltage High; NOTE 7, 8	HCSL Outputs				920	mV
V_{MIN}	Voltage Low; NOTE 7, 9	HCSL Outputs		-150		+150	mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	HCSL Outputs		250		520	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	HCSL Outputs				140	mV
	Rise/Fall Edge Rate; NOTE 13	HCSL Outputs	Measured between 150mV to +150mV	0.6		4.0	V/ns
t_R / t_F	Output Rise/Fall Time		SMODEA/B[1:0] = 00; 20% to 80%	60	200	310	ps
			SMODEA/B[1:0] = 01; 20% to 80%	40	170	300	ps
$MUX_{ISOLATION}$	MUX Isolation		156.25MHz		70		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All LVDS and LVPECL parameters characterized up to 1.5GHz. HCSL parameters characterized up to 250MHz.

NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint.

NOTE 5: Measurement taken from differential waveform.

NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum $\pm 150\text{mV}$ differential voltage after rising/falling edges before it is allowed to drop back into the $V_{RB} \pm 100\text{mV}$ differential range.

Notes continued on next page.

NOTE 7: Measurement taken from single-ended waveform.

NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

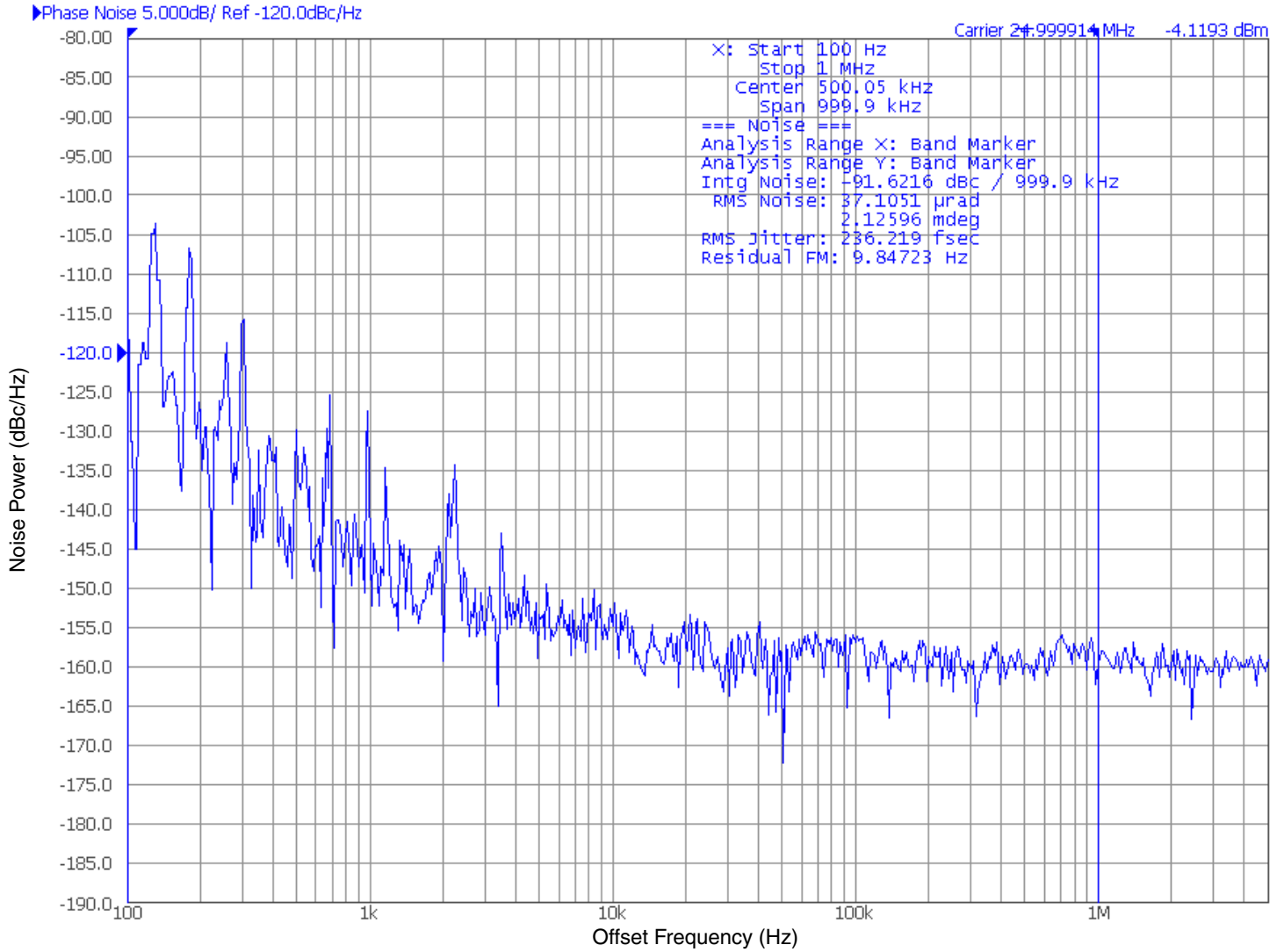
NOTE 10: Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

NOTE 11: Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement.

NOTE 12: Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

NOTE 13: Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing

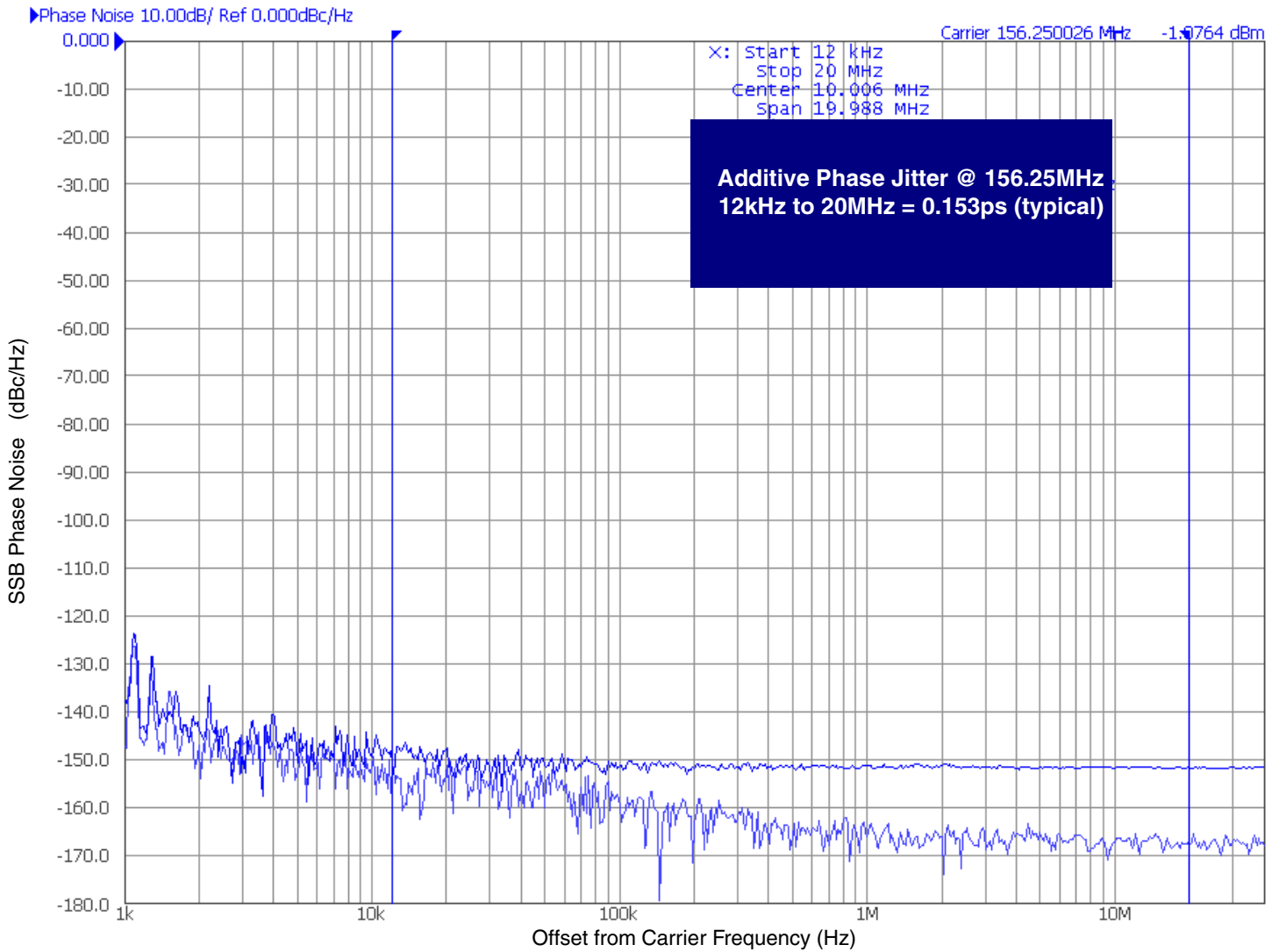
Typical Phase Noise at 25MHz



Additive Phase Jitter (LVPECL, 3.3V)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a

ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



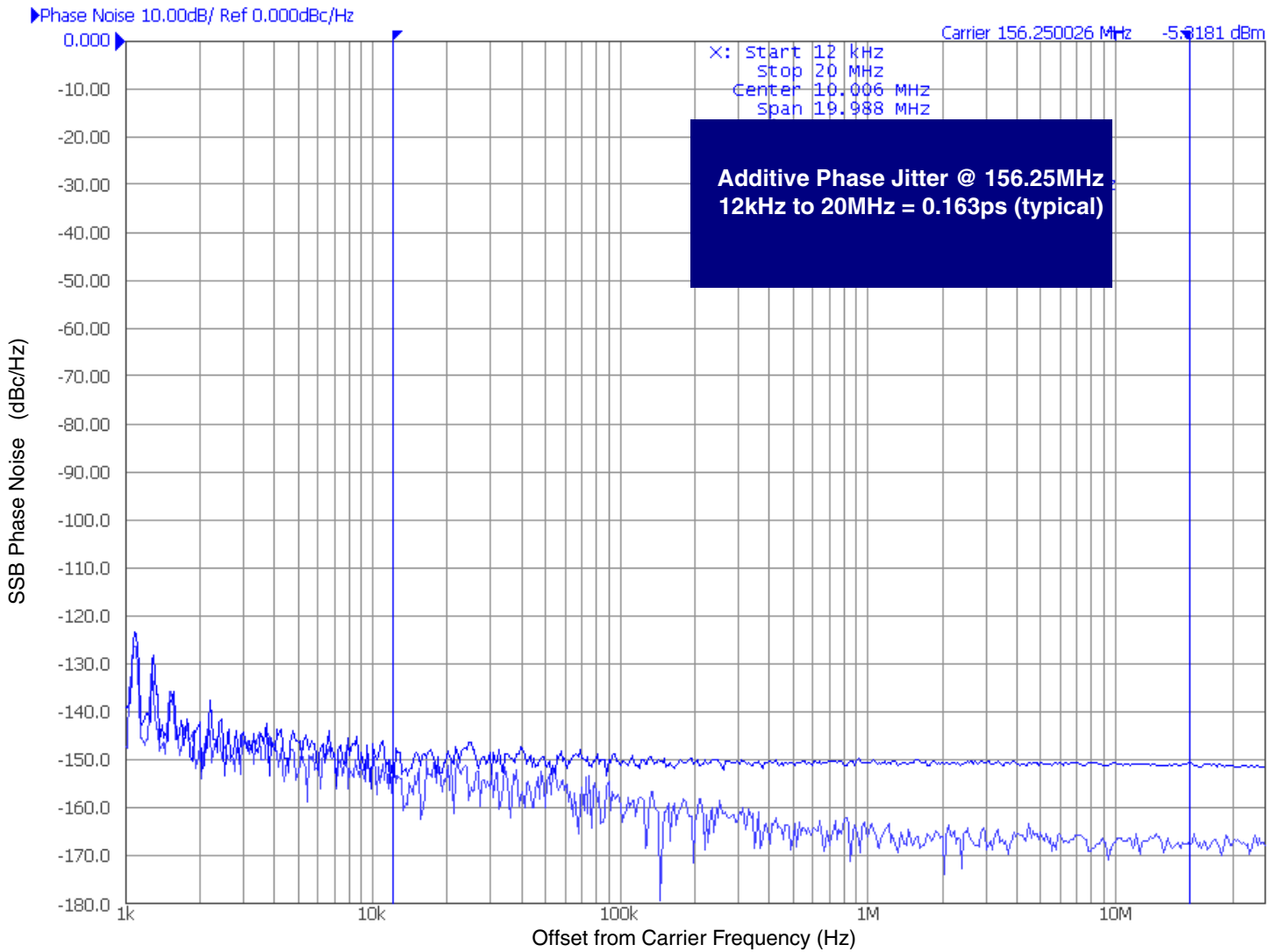
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. The additive phase jitter is dependent on the input source and measurement equipment.

The additive phase jitter for this device was measured using a Wenzel 156.25MHz oscillator as the input source and an Agilent E5052 Signal Source Analyzer.

Additive Phase Jitter (LVDS, 3.3V)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a

ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



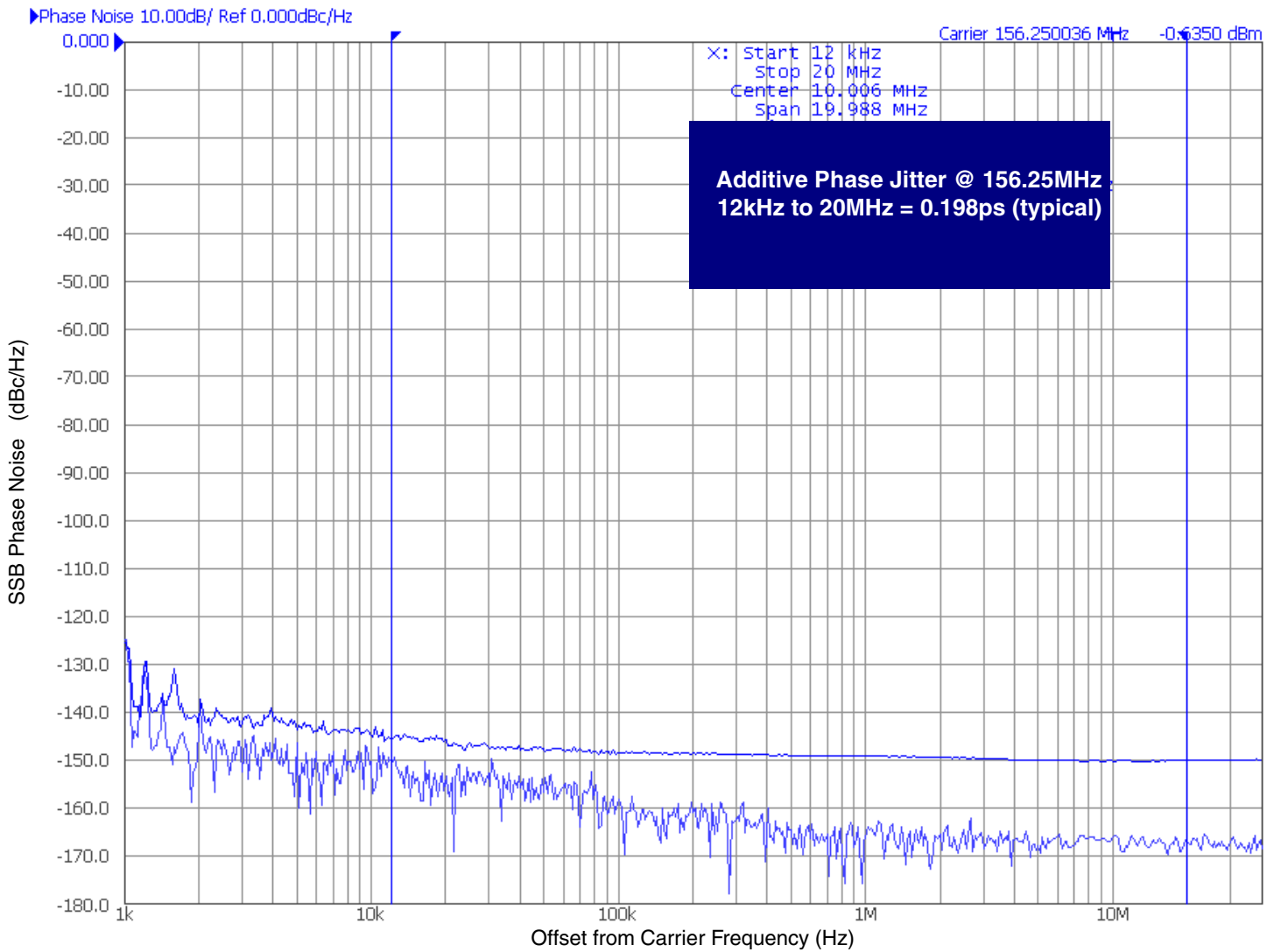
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. The additive phase jitter is dependent on the input source and measurement equipment.

The additive phase jitter for this device was measured using a Wenzel 156.25MHz oscillator as the input source and an Agilent E5052 Signal Source Analyzer.

Additive Phase Jitter (HCSL, 3.3V)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a

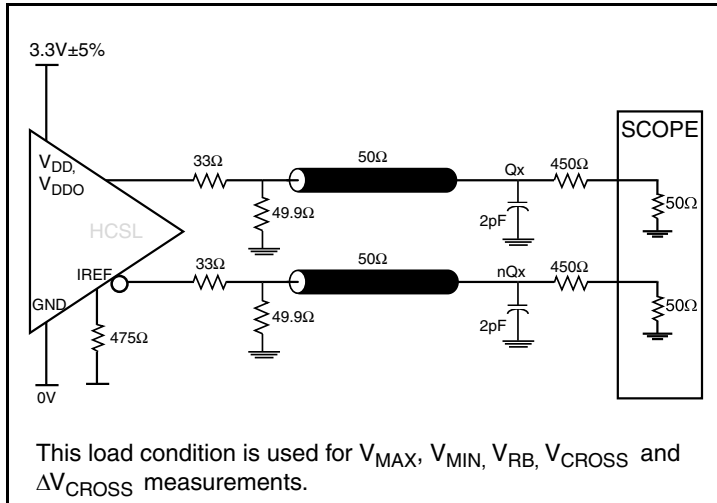
ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



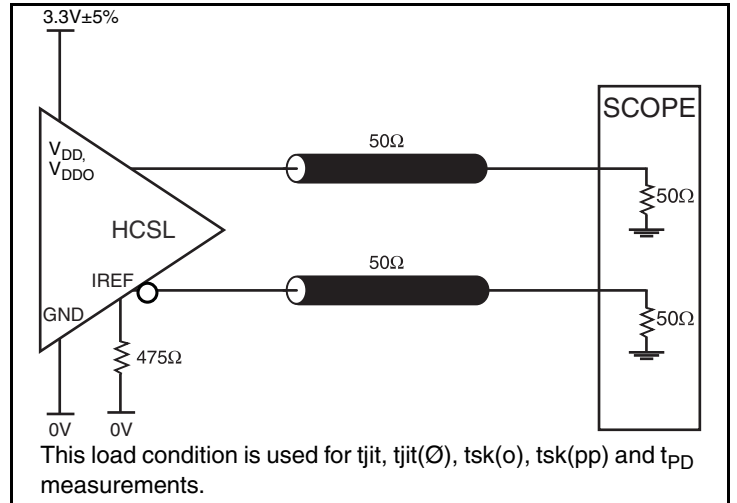
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. The additive phase jitter is dependent on the input source and measurement equipment.

The additive phase jitter for this device was measured using a Wenzel 156.25MHz oscillator as the input source and an Agilent E5052 Signal Source Analyzer.

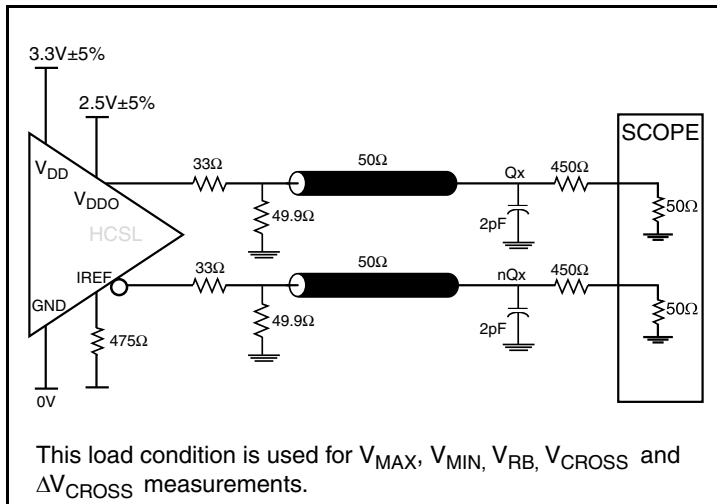
Parameter Measurement Information



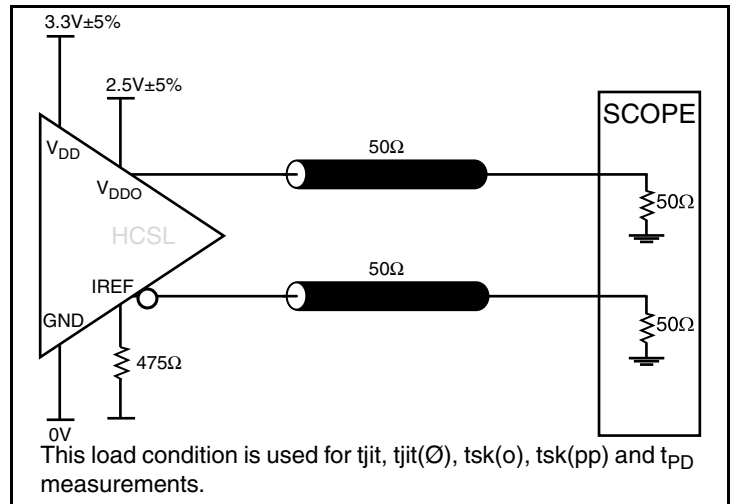
3.3V Core/3.3V HCSL Output Load Test Circuit



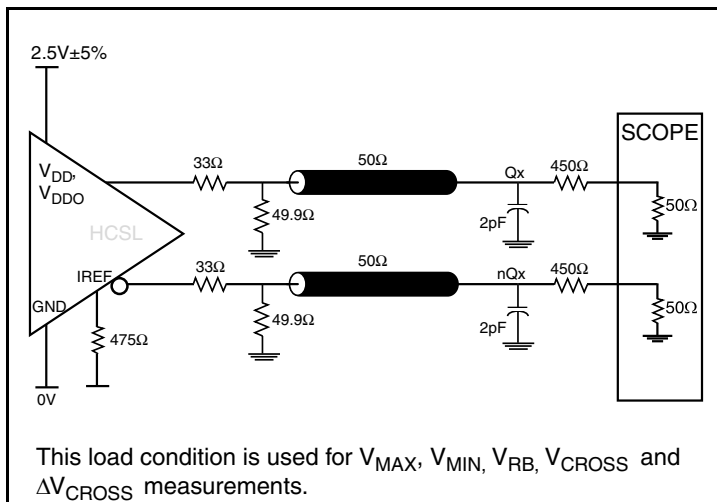
3.3V Core/3.3V HCSL Output Load Test Circuit



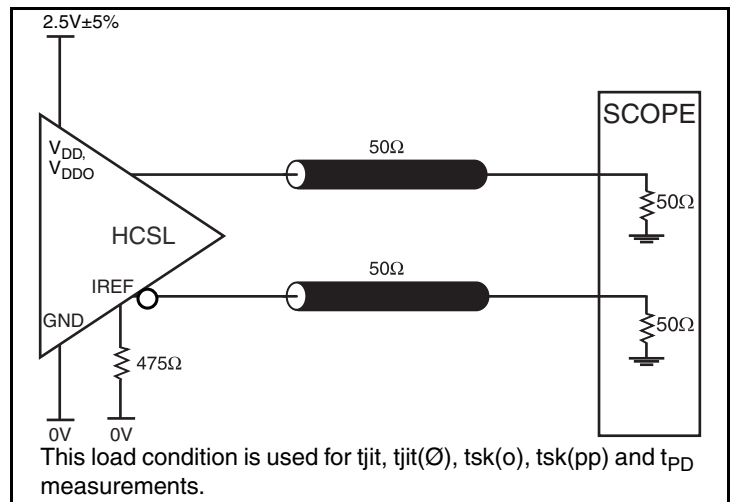
3.3V Core/2.5V HCSL Output Load Test Circuit



3.3V Core/2.5V HCSL Output Load Test Circuit

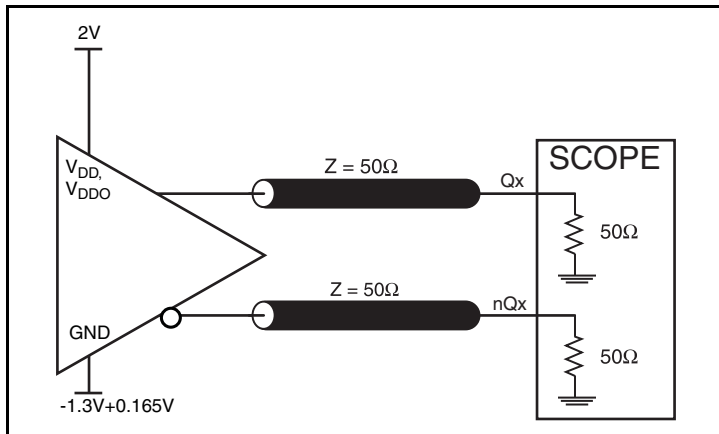


2.5V Core/2.5V HCSL Output Load Test Circuit

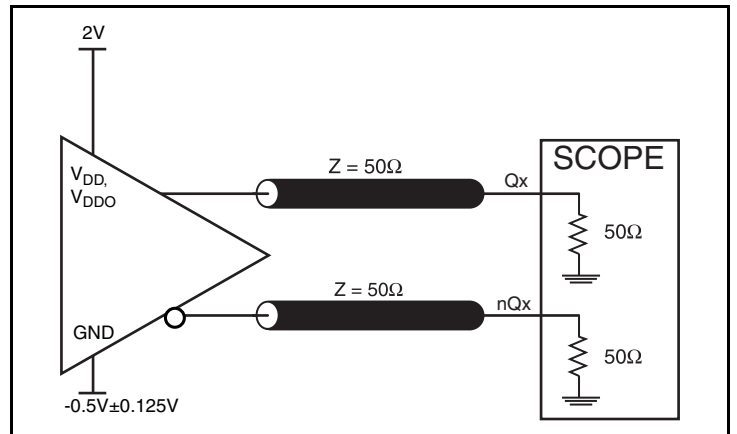


3.3V Core/2.5V HCSL Output Load Test Circuit

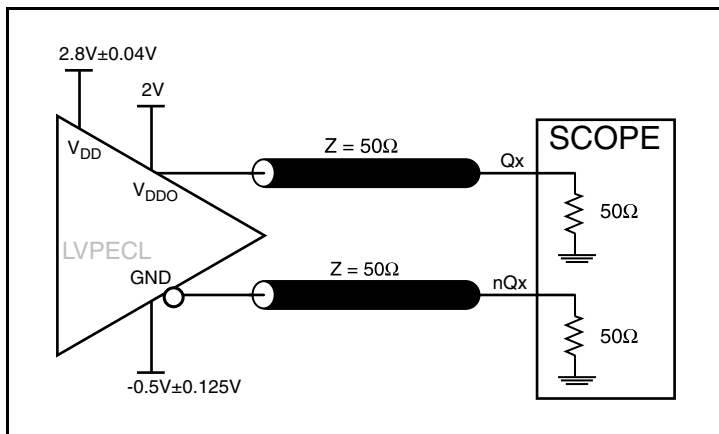
Parameter Measurement Information, continued



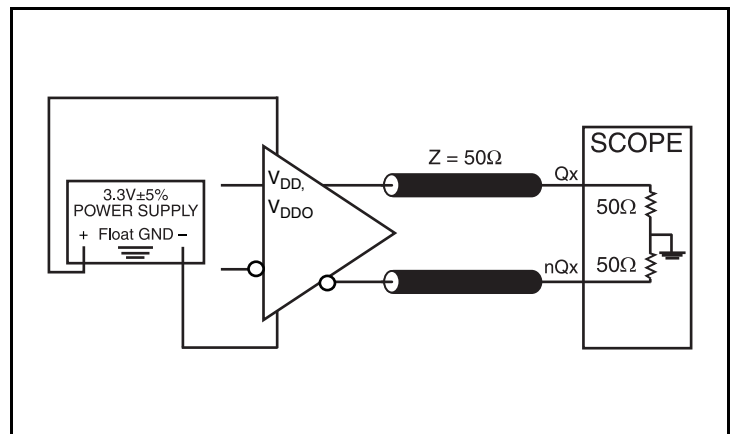
3.3V Core/3.3V LVPECL Output Load Test Circuit



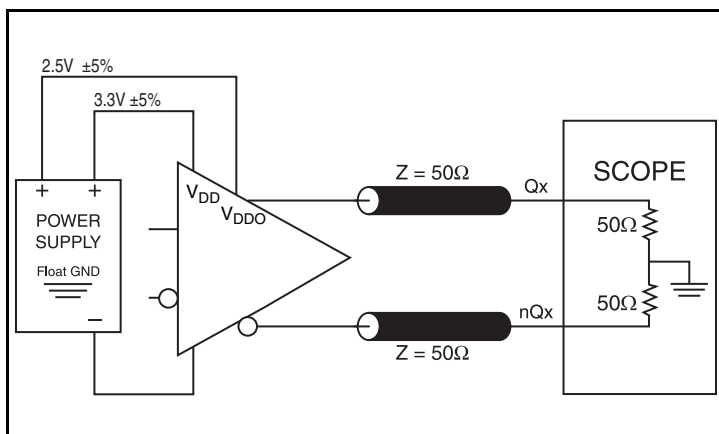
2.5V Core/2.5V LVPECL Output Load Test Circuit



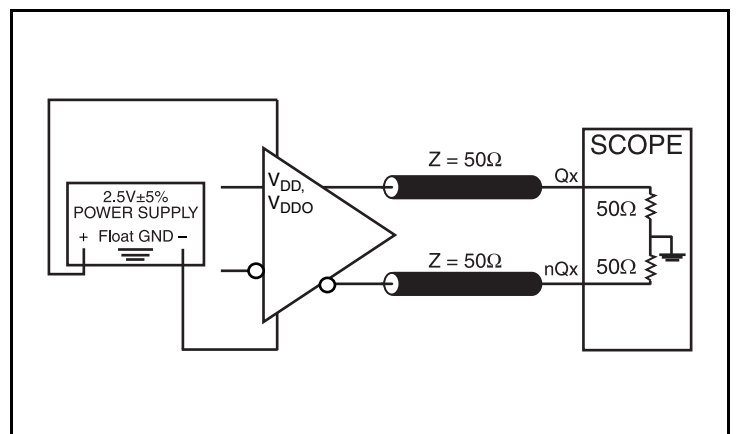
3.3V Core/2.5V LVPECL Output Load Test Circuit



3.3V Core/3.3V LVDS Output Load Test Circuit

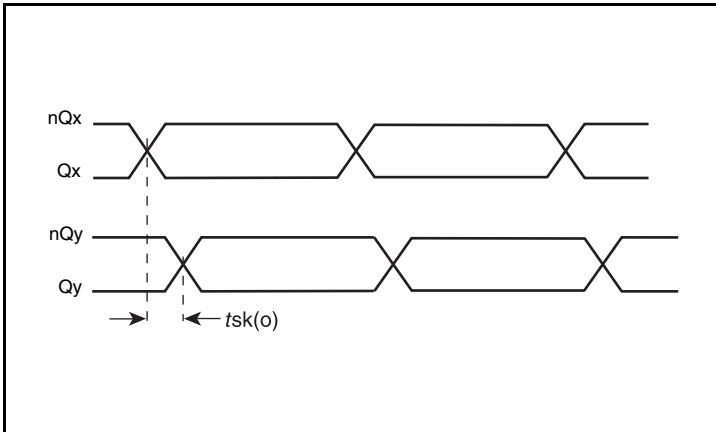


3.3V Core/2.5V LVDS Output Load Test Circuit

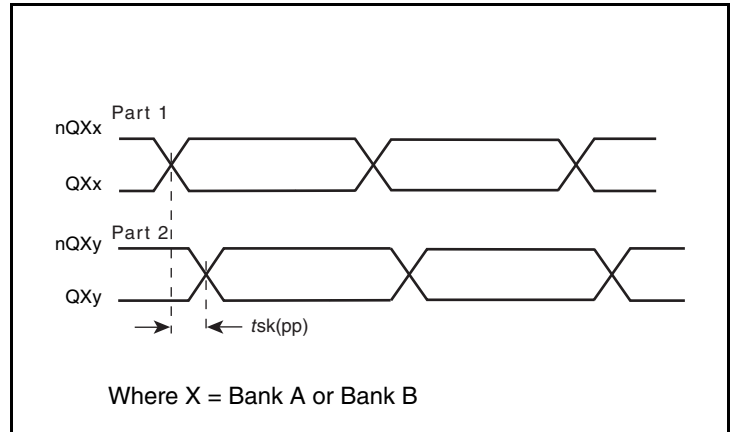


2.5V Core/2.5V LVDS Output Load Test Circuit

Parameter Measurement Information, continued

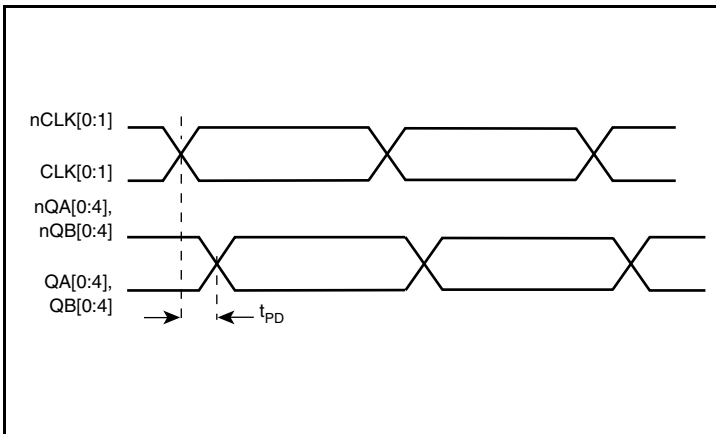


Output Skew

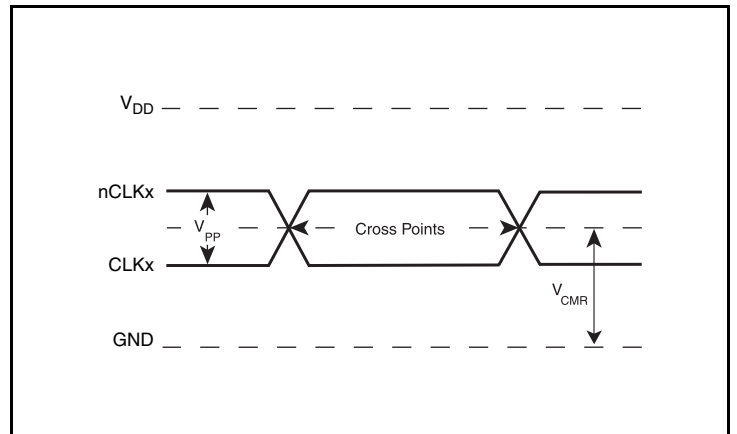


Where X = Bank A or Bank B

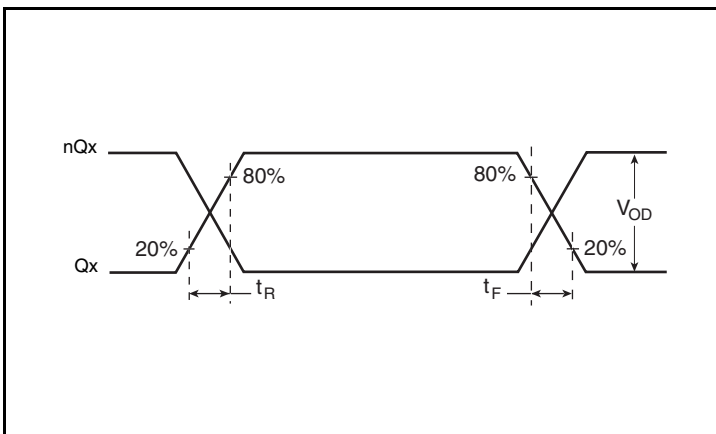
Part-to-Part Skew



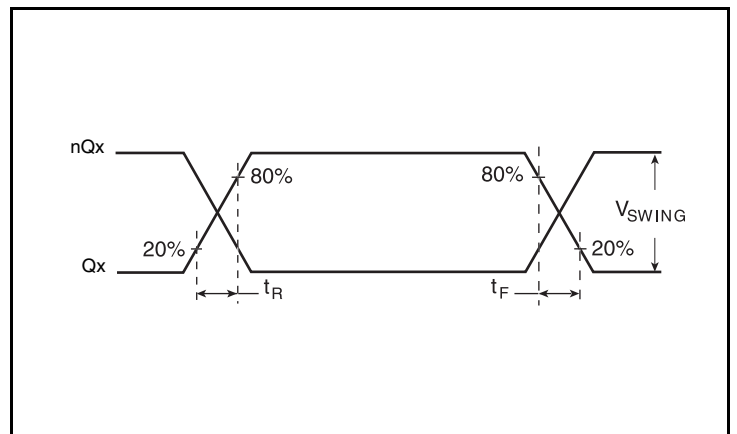
Propagation Delay



Differential Input Levels

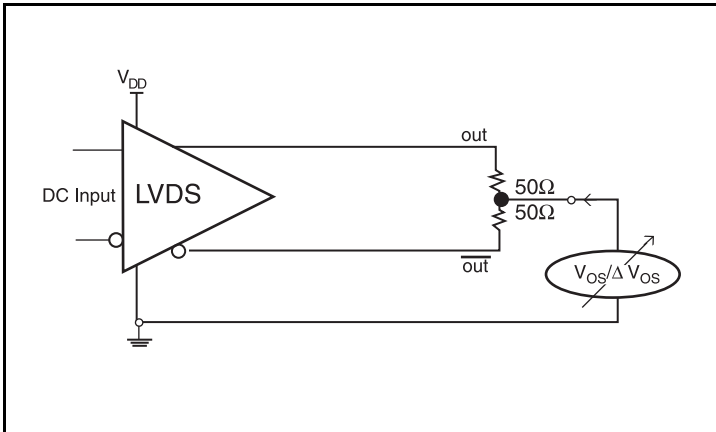


LVDS Output Rise/Fall Time

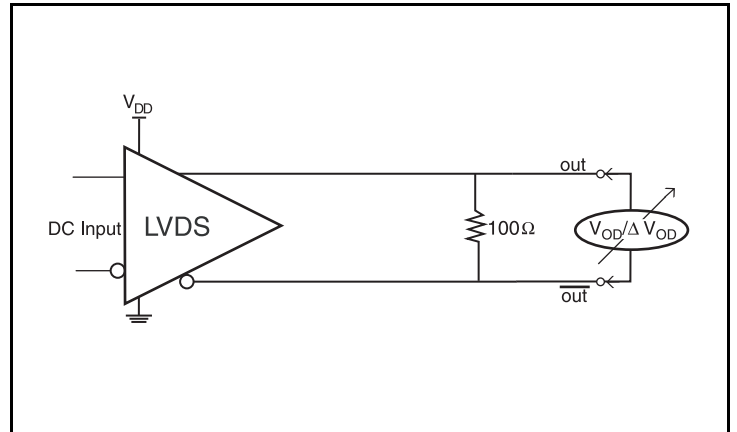


LVPECL Output Rise/Fall Time

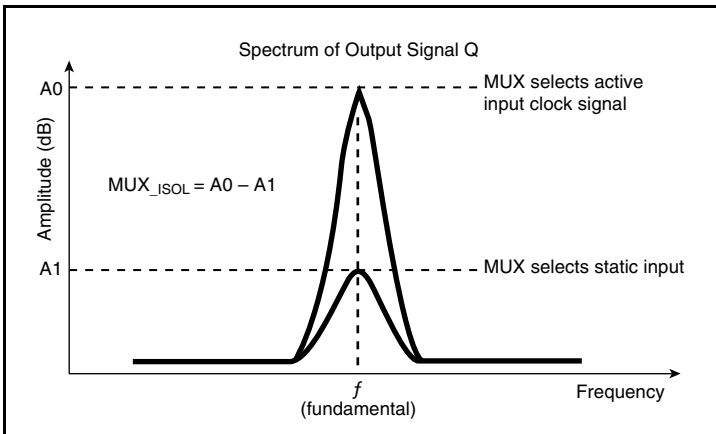
Parameter Measurement Information, continued



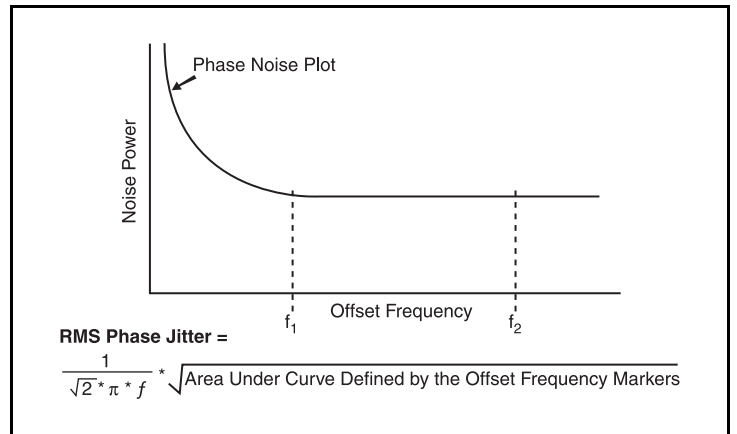
Offset Voltage Setup



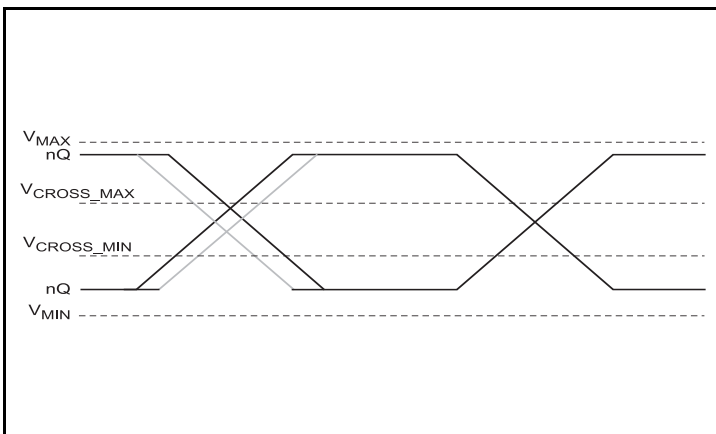
Differential Output Voltage Setup



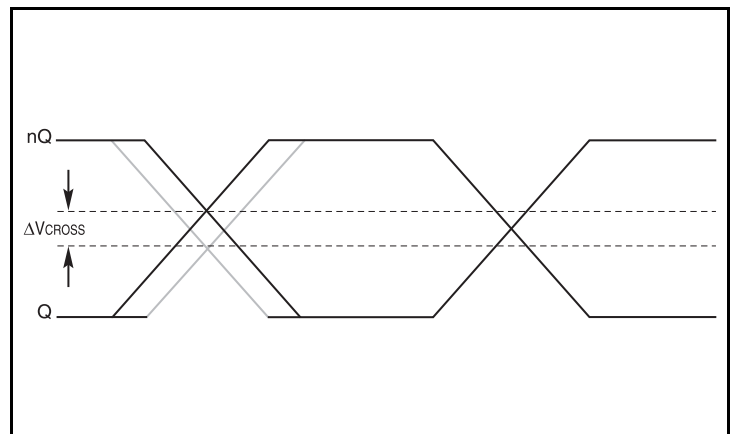
MUX Isolation



RMS Phase Jitter

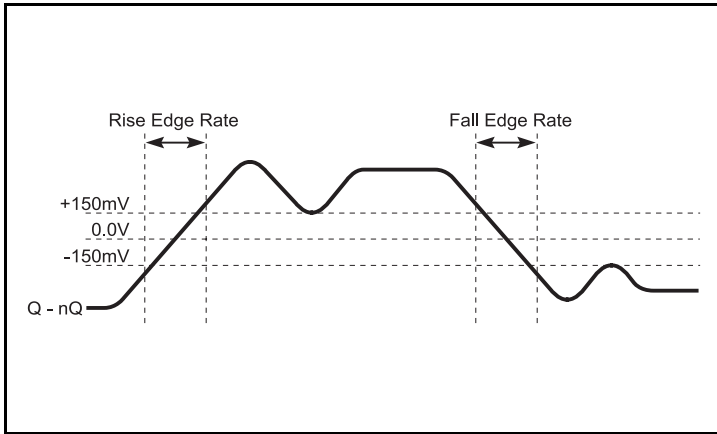


Single-ended Measurement Points for Absolute Crosspoint/Swing

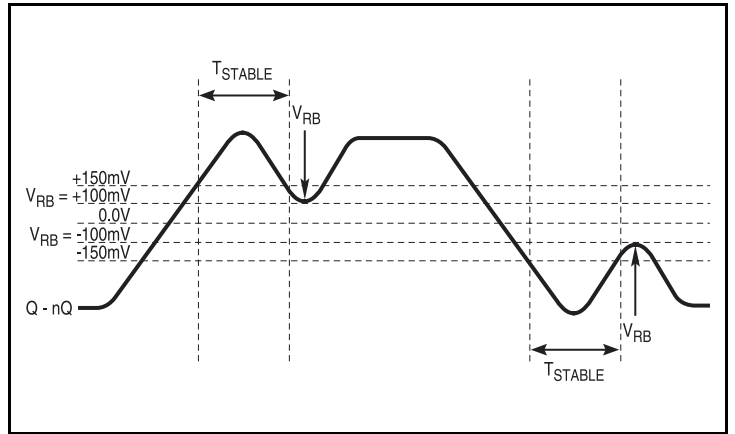


Single-ended Measurement Points for Delta Crosspoint

Parameter Measurement Information, continued



Differential Measurement Points for Rise/Fall Edge Rate



Differential Measurement Points for Ringback

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from XTAL_IN to ground.

LVC MOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Crystal Input Interface

The IDT8T39S10I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. In addition, the recommended 12pF parallel resonant crystal tuning is shown in *Figure 2*. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

Outputs:

LVC MOS Outputs

All unused LVC MOS output can be left floating. We recommend that there is no trace attached.

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If they are left floating, we recommend that there is no trace attached.

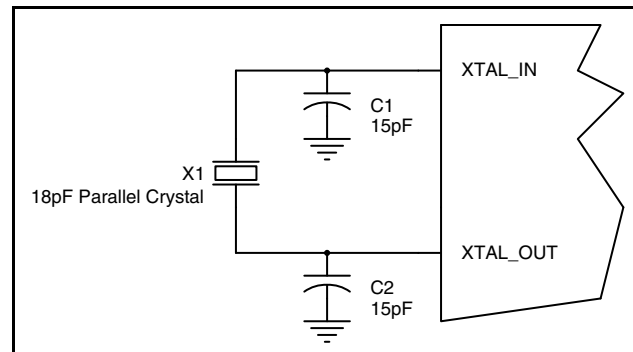


Figure 1. Crystal Input Interface

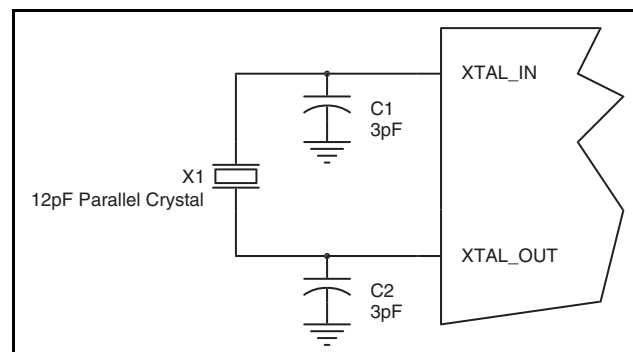


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50 Ω applications, R_1 and R_2 can be 100 Ω . This can also be accomplished by removing R_1 and changing R_2 to 50 Ω . The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

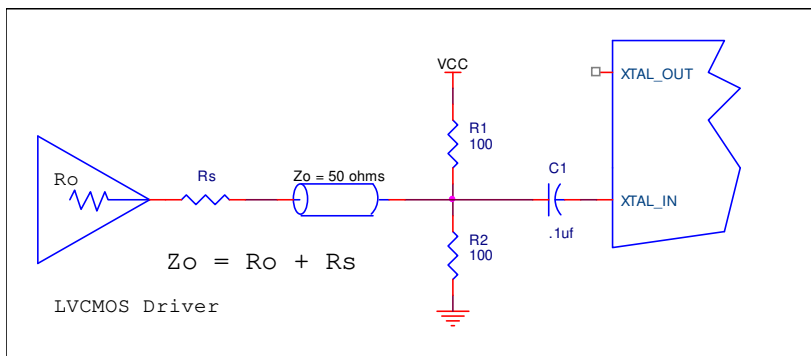


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

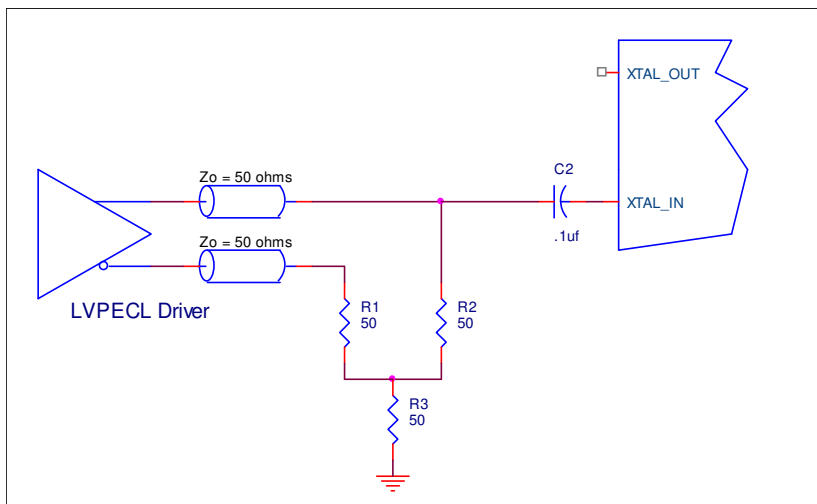


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface