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General Description

The 8T49N242 has one fractional-feedback PLL that can be used as a jitter attenuator and frequency translator. It is equipped with four integer output dividers, allowing the generation of up to four different output frequencies, ranging from 8kHz to 1GHz. These frequencies are completely independent of the input reference frequencies and the crystal reference frequency. The device places virtually no constraints on input to output frequency conversion, supporting all FEC rates, including the new revision of ITU-T Recommendation G.709 (2009), most with 0ppm conversion error. The outputs may select among LVPECL, LVDS, HCSL or LVCMOS output levels.

This makes it ideal to be used in any frequency synthesis application, including 1G, 10G, 40G and 100G Synchronous Ethernet, OTN, and SONET/SDH, including ITU-T G.709 (2009) FEC rates.

The 8T49N242 accepts up to two differential or single-ended input clocks and a fundamental-mode crystal input. The internal PLL can lock to either of the input reference clocks or just to the crystal to behave as a frequency synthesizer. The PLL can use the second input for redundant backup of the primary input reference, but in this case, both input clock references must be related in frequency.

The device supports hitless reference switching between input clocks. The device monitors both input clocks for Loss of Signal (LOS), and generates an alarm when an input clock failure is detected. Automatic and manual hitless reference switching options are supported. LOS behavior can be set to support gapped or un-gapped clocks.

The 8T49N242 supports holdover. The holdover has an initial accuracy of ±50ppB from the point where the loss of all applicable input reference(s) has been detected. It maintains a historical average operating point for the PLL that may be returned to in holdover at a limited phase slope.

The PLL has a register-selectable loop bandwidth from 0.2Hz to 6.4kHz.

The device supports Output Enable & Clock Select inputs and Lock, Holdover & LOS status outputs.

The device is programmable through an I^2C interface. It also supports I^2C master capability to allow the register configuration to be read from an external EEPROM.

Programming with IDT's *Timing Commander* software is recommended for optimal device performance. Factory pre-programmed devices are also available.

Applications

- OTN or SONET / SDH equipment
- Gigabit and Terabit IP switches / routers including Synchronous Ethernet
- Video broadcast

Features

- Supports SDH/SONET and Synchronous Ethernet clocks including all FEC rate conversions
- 0.35ps RMS Typical Jitter (including spurs): 12kHz to 20MHz
- Operating Modes: Synthesizer, Jitter Attenuator
- Operates from a 10MHz to 50MHz fundamental-mode crystal or a 10MHz to 125MHz external oscillator
- Initial holdover accuracy of ±50ppb.
- Accepts up to 2 LVPECL, LVDS, LVHSTL or LVCMOS input clocks
  - Accepts frequencies ranging from 8kHz to 875MHz
  - Auto and manual clock selection with hitless switching
  - Clock input monitoring including support for gapped clocks
- Phase-slope limiting and fully hitless switching options to control output clock phase transients
- Generates four LVPECL / LVDS / HCSL or eight LVCMOS output clocks
  - Output frequencies ranging from 8kHz up to 1.0GHz (differential)
  - Output frequencies ranging from 8kHz to 250MHz (LVCMOS)
  - Integer divider ranging from ÷4 to ÷786,420 for each output
- Programmable loop bandwidth settings from 0.2Hz to 6.4kHz
  - Optional fast-lock function
- Four General Purpose I/O pins with optional support for status & control:
  - Two Output Enable control inputs provide control over the four clocks
  - Manual clock selection control input
  - Lock, Holdover and Loss-of-Signal alarm outputs
- Open-drain Interrupt pin
- Register programmable through I^2C or via external I^2C EEPROM
- Full 2.5V or 3.3V supply modes, 1.8V support for LVCMOS outputs, GPIO and control pins
- -40°C to 85°C ambient operating temperature
- Package: 40QFN, lead-free (RoHS 6)

8T49N242 Block Diagram

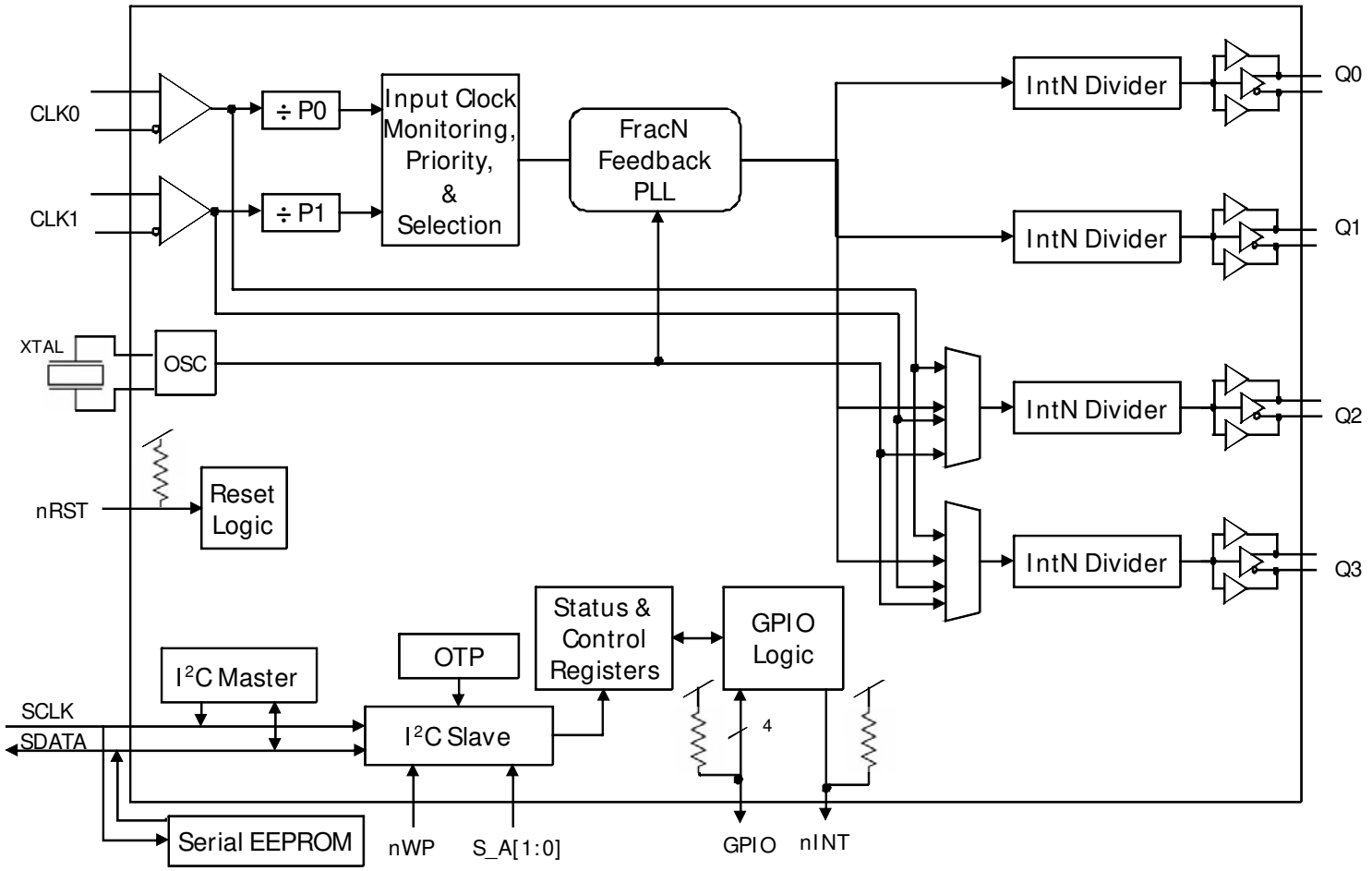
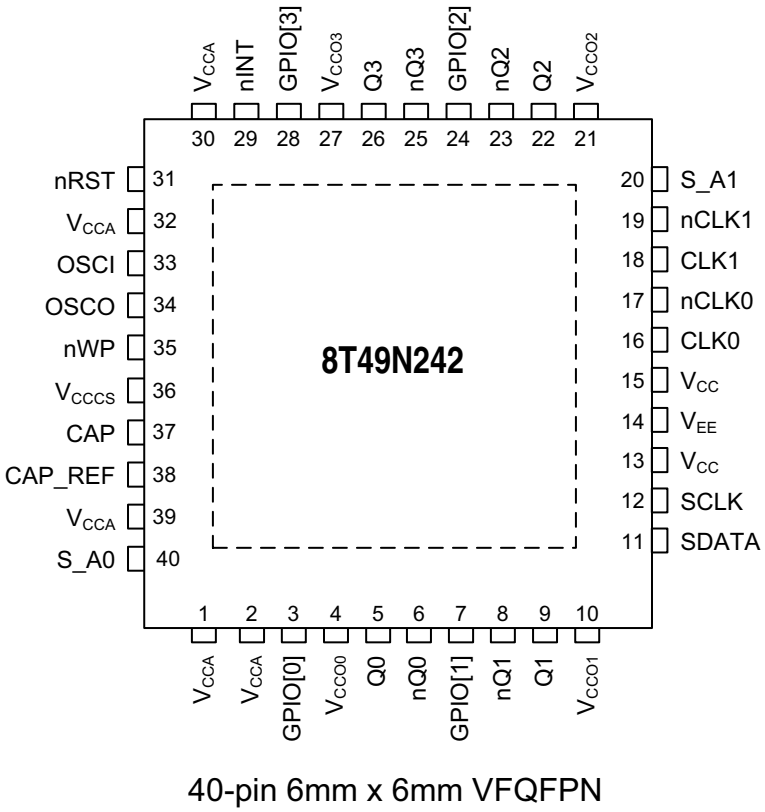


Figure 1. 8T49N242 Functional Block Diagram

Pin Assignment



40-pin 6mm x 6mm VFQFPN

Figure 2. 8T49N242 Pinout Drawing

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type[1]		Description
1	V_{CCA}	Power		Analog function supply for core analog functions. 2.5V or 3.3V supported.
2	V_{CCA}	Power		Analog function supply for analog functions associated with the PLL. 2.5V or 3.3V supported.
3	GPIO[0]	I/O	Pullup	General-purpose input-output. LVTTL / LVCMOS Input levels.
4	V_{CCO0}	Power		High-speed output supply for output pair Q0, nQ0. 2.5V or 3.3V supported for differential output types. LVCMOS outputs also support 1.8V.
5	Q0	O	Universal	Output Clock 0. Please refer to the Section, "Output Drivers" for more details.
6	nQ0	O	Universal	Output Clock 0. Please refer to the Section, "Output Drivers" for more details.
7	GPIO[1]	I/O	Pullup	General-purpose input-output. LVTTL / LVCMOS Input levels.
8	nQ1	O	Universal	Output Clock 1. Please refer to the Section, "Output Drivers" for more details.
9	Q1	O	Universal	Output Clock 1. Please refer to the Section, "Output Drivers" for more details.
10	V_{CCO1}	Power		High-speed output supply for output pair Q1, nQ1. 2.5V or 3.3V supported for differential output types. LVCMOS outputs also support 1.8V.
11	SDATA	I/O	Pullup	I^2C interface bi-directional data.
12	SCLK	I/O	Pullup	I^2C interface bi-directional clock.
13	V_{CC}	Power		Core digital function supply. 2.5V or 3.3V supported.
14	V_{EE}	Power		Negative supply voltage. All V_{EE} pins and EPAD must be connected before any positive supply voltage is applied.
15	V_{CC}	Power		Core digital function supply. 2.5V or 3.3V supported.
16	CLK0	I	Pulldown	Non-inverting differential clock input 0.
17	nCLK0	I	Pullup / Pulldown	Inverting differential clock input 0. V_{CC} / 2 when left floating (set by internal pullup / pulldown resistors)
18	CLK1	I	Pulldown	Non-inverting differential clock input 1.
19	nCLK1	I	Pullup / Pulldown	Inverting differential clock input 1. V_{CC} / 2 when left floating (set by internal pullup / pulldown resistors).
20	S_A1	I	Pulldown	I^2C Address Bit A1
21	V_{CCO2}	Power		High-speed output supply voltage for output pair Q2, nQ2. 2.5V or 3.3V supported for differential output types. LVCMOS outputs also support 1.8V.
22	Q2	O	Universal	Output Clock 2. Please refer to the Section, "Output Drivers" for more details.
23	nQ2	O	Universal	Output Clock 2. Please refer to the Section, "Output Drivers" for more details.
24	GPIO[2]	I/O	Pullup	General-purpose input-output. LVTTL / LVCMOS Input levels.
25	nQ3	O	Universal	Output Clock 3. Please refer to the Section, "Output Drivers" for more details.
26	Q3	O	Universal	Output Clock 3. Please refer to the Section, "Output Drivers" for more details.
27	V_{CCO3}	Power		High-speed output supply voltage for output pair Q3, nQ3. 2.5V or 3.3V supported for differential output types. LVCMOS outputs also support 1.8V.
28	GPIO[3]	I/O	Pullup	General-purpose input-output. LVTTL / LVCMOS Input levels.
29	nINT	O	Open-drain with pullup	Interrupt output.
30	V_{CCA}	Power		Analog function supply for analog functions associated with PLL. 2.5V or 3.3V supported.
31	nRST	I	Pullup	Master Reset input. LVTTL / LVCMOS interface levels: 0 = All registers and state machines are reset to their default values 1 = Device runs normally

Number	Name	Type[1]		Description
32	V_{CCA}	Power		Analog function supply for core analog functions. 2.5V or 3.3V supported.
33	OSCI	I		Crystal Input. Accepts a 10MHz – 50MHz reference from a clock oscillator or a 12pF fundamental mode, parallel-resonant crystal. For proper device functionality, a crystal or external oscillator must be connected to this pin.
34	OSCO	O		Crystal Output. This pin must be connected to a crystal. If an oscillator is connected to OSCI, then this pin must be left unconnected.
35	nWP	I	Pullup	Write Protect input. LVTTL / LVCMOS interface levels. 0 = Write operations on the serial port will complete normally, but will have no effect except on interrupt registers.
36	V_{CCCS}	Power		Output supply for Control & Status pins: GPIO[3:0], SDATA, SCLK, S_A1, S_A0, nINT, nWP, nRST 1.8V, 2.5V or 3.3V supported
37	CAP	Analog		PLL External Capacitance. A 0.1µF capacitance value across CAP and CAP_REF pins is recommended.
38	CAP_REF	Analog		PLL External Capacitance. A 0.1µF capacitance value across CAP and CAP_REF pins is recommended.
39	V_{CCA}	Power		Analog function supply for analog functions associated with PLL. 2.5V or 3.3V supported.
40	S_A0	I	Pulldown	I^2C Address Bit A0.
ePAD	Exposed Pad	Power		Negative supply voltage. All V_{EE} pins and ePAD must be connected before any positive supply voltage is applied.

NOTE 1: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics, $V_{CC} = V_{CCOX} = 3.3V±5\%$ or $2.5V±5\%$[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance[2]				3.5		pF
R_{PULLUP}	Input Pullup Resistor	GPIO[3:0], nRST, nWP, SDATA, SCLK			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor	S_A0, S_A1			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output pair)	LVCMOS	V_{CCOX} = 3.465V		11.5		pF
		LVCMOS	V_{CCOX} = 2.625V		10.5		pF
		LVCMOS	V_{CCOX} = 1.89V		11		pF
		LVDS, HCSL or LVPECL	V_{CCOX} = 3.465V or 2.625V		2.5		pF
R_{OUT}	Output Impedance	GPIO[3:0]	V_{CCCS} = 3.3V		26		Ω
			V_{CCCS} = 2.5V		30		
			V_{CCCS} = 1.8V		42		
		LVCMOS Q[3:0], nQ[3:0]	V_{CCOX} = 3.3V		18		Ω
			V_{CCOX} = 2.5V		22		
			V_{CCOX} = 1.8V		30		

NOTE 1: V_{CCOX} denotes: V_{CCO0}, V_{CCO1}, V_{CCO2} or V_{CCO3}.

NOTE 2: This specification does not apply to the OSCI or OSCO pins.

Principles of Operation

The 8T49N242 can be locked to either of the input clocks and generate a wide range of synchronized output clocks.

It could be used for example in either the transmit or receive path of Synchronous Ethernet equipment.

The 8T49N242 accepts up to two differential or single-ended input clocks ranging from 8kHz up to 875MHz. It generates up to four output clocks ranging from 8kHz up to 1.0GHz.

The PLL path within the 8T49N242 supports three states: Lock, Holdover and Free-run. Lock & holdover status may be monitored on register bits and pins. The PLL also supports automatic and manual hitless reference switching. In the locked state, the PLL locks to a valid clock input and its output clocks have a frequency accuracy equal to the frequency accuracy of the input clock. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. The PLL within the 8T49N242 has an initial holdover frequency offset of ±50ppb. In the Free-run state, the PLL outputs a clock with the same frequency accuracy as the external crystal.

Upon power up, the PLL will enter Free-run state, in this state it generates output clocks with the same frequency accuracy as the external crystal. The 8T49N242 continuously monitors each input for activity (signal transitions). If no input references are provided, the device will remain locked to the crystal in Free-run state and will generate output frequencies as a synthesizer.

When an input clock has been validated the PLL will transition to the Lock state. In automatic reference switching, if the selected input clock fails and there are no other valid input clocks, the PLL will quickly detect that and go into Holdover. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. If the selected input clock fails and another input clock is available then the 8T49N242 will hitlessly switch to that input clock. The reference switch can be either revertive or non-revertive. Manual switchover is also available with switchover only occurring on user command, either via register bit or via the Clock Select input function of the GPIO[3:0] pins.

The device supports conversion of any input frequencies to four different output frequencies: one independent output frequency on Q0 and three more integer-related frequencies on Q[1:3].

The 8T49N242 has a programmable loop bandwidth from 0.2Hz to 6.4kHz.

The device monitors all input clocks and generates an alarm when an input clock failure is detected.

The device is programmable through an I^2C and may also autonomously read its register settings from an internal One-Time Programmable (OTP) memory or an external serial I^2C EEPROM.

Crystal Input

The crystal input on the 8T49N242 is capable of being driven by a parallel-resonant, fundamental mode crystal with a frequency range of 10MHz – 50MHz.

The oscillator input also supports being driven by a single-ended crystal oscillator or reference clock.

The initial holdover frequency offset is set by the device, but the long term drift depends on the quality of the crystal or oscillator attached to this port.

This device provides the ability to double the crystal frequency input into the PLL for improved close-in phase noise performance. Refer to Figure 3.

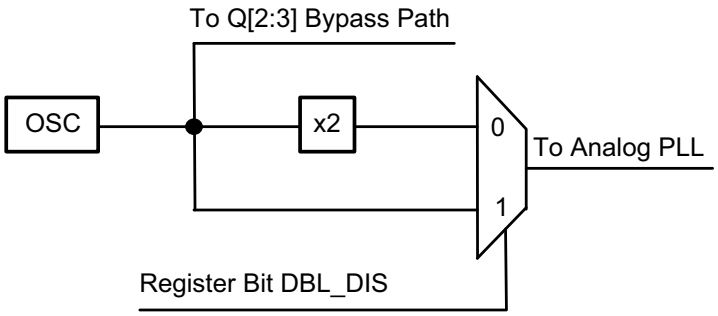


Figure 3. Doubler Block Diagram

Bypass Path

The crystal input, CLK0 or CLK1 may be used directly as a clock source for the Q[2:3] output dividers. This may only be done for input frequencies of 250MHz or less.

Input Clock Selection

The 8T49N242 accepts up to two input clocks with frequencies ranging from 8kHz up to 875MHz. Each input can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS inputs using 1.8V, 2.5V or 3.3V logic levels.

In Manual mode, only one of the inputs may be chosen and if that input fails that PLL will enter holdover.

Manual mode may be operated by directly selecting the desired input reference in the REFSEL register field. It may also operate via pin-selection of the desired input clock by selecting that mode in the REFSEL register field. In that case, GPIO[2] must be used as a Clock Select input (CSEL). CSEL = 0 will select the CLK0 input and CSEL = 1 will select the CLK1 input.

In addition, the crystal frequency may be passed directly to the output dividers Q[2:3] for use as a reference.

Inputs do not support transmission of spread-spectrum clocking sources. Since this family is intended for high-performance applications, it will assume input reference sources to have stabilities of ±100ppm or better, except where gapped clock inputs are used.

If the PLL is working in automatic mode, then one of the input reference sources is assigned as the higher priority. At power-up or if the currently selected input reference fails, the PLL will switch to the highest priority input reference that is valid at that time (see Section, "Input Clock Monitor" for details).

Automatic mode has two sub-options: revertive or non-revertive. In revertive mode, the PLL will switch to a reference with a higher priority setting whenever one becomes valid. In non-revertive mode the PLL remains with the currently selected source as long as it remains valid.

The clock input selection is based on the input clock priority set by the Clock Input Priority control bit.

Input Clock Monitor

Each clock input is monitored for Loss of Signal (LOS). If no activity has been detected on the clock input within a user-selectable time period then the clock input is considered to be failed and an internal Loss-of-Signal status flag is set, which may cause an input switchover depending on other settings. The user-selectable time period has sufficient range to allow a gapped clock missing many consecutive edges to be considered a valid input.

User-selection of the clock monitor time-period is based on a counter driven by a monitor clock. The monitor clock is fixed at the frequency of the PLL's VCO divided by 8. With a VCO range of 3GHz - 4GHz, the monitor clock has a frequency range of 375MHz to 500MHz.

The monitor logic for each input reference will count the number of monitor clock edges indicated in the appropriate Monitor Control register. If an edge is received on the input reference being monitored, then the count resets and begins again. If the target edge count is reached before an input reference edge is received, then an internal soft alarm is raised and the count re-starts. During the soft alarm period, the PLL tracking will not be adjusted. If an input reference edge is received before the count expires for the second time, then the soft alarm status is cleared and the PLL will resume adjustments. If the count expires again without any input reference edge being received, then a Loss-of-Signal alarm is declared.

It is expected that for normal (non-gapped) clock operation, users will set the monitor clock count for each input reference to be slightly longer than the nominal period of that input reference. A margin of 2-3 monitor clock periods should give a reasonably quick reaction time and yet prevent false alarms.

For gapped clock operation, the user will set the monitor clock count to a few monitor clock periods longer than the longest expected clock gap period. The monitor count registers support 17-bit count values, which will support at least a gap length of two clock periods for any supported input reference frequency, with longer gaps being supported for faster input reference frequencies. Since gapped clocks usually occur on input reference frequencies above 100MHz, gap lengths of thousands of periods can be supported.

Using this configuration for a gapped clock, the PLL will continue to adjust while the normally expected gap is present, but will freeze once the expected gap length has been exceeded and alarm after twice the normal gap length has passed.

Once a LOS on any of the input clocks is detected, the appropriate internal LOS alarm will be asserted and it will remain asserted until that input clock returns and is validated. Validation occurs once 8 rising edges have been received on that input reference. If another error condition on the same input clock is detected during the validation time then the alarm remains asserted and the validation period starts over.

Each LOS flag may also be reflected on one of the GPIO[3:0] outputs. Changes in status of any reference can also generate an interrupt if not masked.

Holdover

The 8T49N242 supports a small initial holdover frequency offset in non-gapped clock mode. When the input clock monitor is set to support gapped clock operation, this initial holdover frequency offset is indeterminate since the desired behavior with gapped clocks is for the PLL to continue to adjust itself even if clock edges are missing. In gapped clock mode, the PLL will not enter holdover until the input is missing for two LOS monitor periods.

The holdover performance characteristics of a clock are referred as its accuracy and stability, and are characterized in terms of the fractional frequency offset. The 8T49N242 can only control the initial frequency accuracy. Longer-term accuracy and stability are determined by the accuracy and stability of the external oscillator.

When the PLL loses all valid input references, it will enter the holdover state. In fast average mode, the PLL will initially maintain its most recent frequency offset setting and then transition at a rate dictated by its selected phase-slope limit setting to a frequency offset setting that is based on historical settings. This behavior is intended to compensate for any frequency drift that may have occurred on the input reference before it was detected to be lost.

The historical holdover value will have three options:

- Return to center of tuning range within the VCO band
- Instantaneous mode - the holdover frequency will use the DPLL current frequency 100msec before it entered holdover. The accuracy is shown in the *AC Characteristics Table,* Table 11.
- Fast average mode - an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3dB attenuation point corresponding to nominal a period of 20 minutes. The accuracy is shown in the *AC Characteristics Table,* Table 11.

When entering holdover, the PLL will set a separate internal HOLD alarm internally. This alarm may be read from internal status register, appear on the appropriate GPIO pin and/or assert the nINT output.

While the PLL is in holdover, its frequency offset is now relative to the crystal input and so the output clocks will be tracing their accuracy to the local oscillator or crystal. At some point in time, depending on the stability & accuracy of that source, the clock(s) will have drifted outside of the limits of the holdover state and be considered to be in a free-run state. Since this borderline is defined outside the PLL and dictated by the accuracy and stability of the external local crystal or oscillator, the 8T49N242 cannot know or influence when that transition occurs.

Input to Output Clock Frequency

The 8T49N242 is designed to accept any frequency within its input range and generate four different output frequencies that are integer-related to the PLL frequency and hence to each other, but not to the input frequencies. The internal architecture of the device ensures that most translations will result in the exact output frequency specified. Please contact IDT for configuration software or other assistance in determining if a desired configuration will be supported exactly.

Synthesizer Mode Operation

The device may act as a frequency synthesizer with the PLL generating its operating frequency from just the crystal input. By setting the SYN_MODE register bit and setting the STATE[1:0] field to Freerun, no input clock references are required to generate the desired output frequencies.

When operating as a synthesizer, the precision of the output frequency will be < 1ppb for any supported configuration.

Loop Filter and Bandwidth

The 8T49N242 uses one external capacitor of fixed value to support its loop bandwidth. When operating in Synthesizer mode a fixed loop bandwidth of approximately 200kHz is provided.

When not operating as a synthesizer, the 8T49N242 will support a range of loop bandwidths: 0.2Hz, 0.4Hz, 0.8Hz, 1.6Hz, 3.2Hz, 6.4Hz, 12Hz, 25Hz, 50Hz, 100Hz, 200Hz, 400Hz, 800Hz, 1.6kHz or 6.4kHz.

The device supports two different loop bandwidth settings: acquisition and locked. These loop bandwidths are selected from the list of options described above. If enabled, the acquisition bandwidth is used while lock is being acquired to allow the PLL to “fast-lock”. Once locked the PLL will use the locked bandwidth setting. If the acquisition bandwidth setting is not used, the PLL will use the locked bandwidth setting at all times.

Output Dividers

The 8T49N242 supports four integer output dividers. Each integer output divider block consists of two divider stages in a series to achieve the desired total output divider ratio. The first stage divider may be set to divide by 4, 5 or 6. In addition, the Q[2:3] first stage dividers may be bypassed if CLK0, CLK1 or the crystal are used as the clock source for them. The second stage of the divider may be bypassed (i.e. divide-by-1) or programmed to any even divider ratio from 2 to 131,070. The total divide ratios, settings and possible output frequencies are shown in Table 3.

An output synchronization via the PLL_SYN bit is necessary after programming the output dividers to ensure that the outputs are synchronized.

Table 3. Output Divide Ratios

1st-Stage Divide	2nd-Stage Divide	Total Divide	Minimum F_{OUT} MHz	Maximum F_{OUT} MHz
4	1	4	750	1000
5	1	5	600	800
6	1	6	500	666.7
4	2	8	375	500
5	2	10	300	400
6	2	12	250	333.3
4	4	16	187.5	250
5	4	20	150	200
6	4	24	125	166.7
...				
4	131,070	524,280	0.0057	0.0076
5	131,070	655,350	0.0046	0.0061
6	131,070	786,420	0.0038	0.0051

Output Divider Frequency Sources

Output dividers associated with the Q[0:1] outputs take their input frequency directly from the PLL.

Output dividers associated with the Q[2:3] outputs can take their input frequencies from the PLL, CLK0 or CLK1 input reference frequency or the crystal frequency.

Output Phase Control on Switchover

There are two options on how the output phase can be controlled when the 8T49N242 enters or leaves the holdover state, or the PLL switches between input references. Phase-slope limiting or fully hitless switching (sometimes called phase build-out) may be selected. The SWMODE bit selects which behavior is to be followed.

If fully hitless switching is selected, then the output phase will remain unchanged under any of these conditions. Note that fully hitless switching is not supported when external loopback is being used. Fully hitless switching should not be used unless all input references are in the same clock domain. Note that use of this mode may prevent an output frequency and phase from being able to trace its alignment back to a primary reference source.

If phase-slope limiting is selected, then the output phase will adjust from its previous value until it is tracking the new condition at a rate dictated by the SLEW[1:0] bits. Phase-slope limiting should be used if all input references are not in the same clock domain or users wish to retain traceability to a primary reference source.

Output Drivers

The Q0 to Q3 clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL, HCSL or LVDS logic levels.

The operating voltage ranges of each output is determined by its independent output power pin (V_{CCO}) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential operation and LVCMOS operation. In addition, LVCMOS output operation supports 1.8V V_{CCO}.

Each output may be enabled or disabled by register bits and/or GPIO pins.

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, voltage levels and enable / disable status apply to both the Q and nQ pins. When configured as LVCMOS, the Q & nQ outputs can be selected to be phase-aligned with each other or inverted relative to one another. Selection of phase-alignment may have negative effects on the phase noise performance of any part of the device due to increased simultaneous switching noise within the device.

Power-Saving Modes

To allow the device to consume the least power possible for a given application, the following functions can be disabled via register programming:

- Any unused output, including all output divider logic, can be individually powered-off.
- Any unused input, including the clock monitoring logic can be individually powered-off.
- The digital PLL can be powered-off when running in synthesizer mode.
- Clock gating on logic that is not being used.

Status / Control Signals and Interrupts

The status and control signals for the device, may be operated at 1.8V, 2.5V or 3.3V as determined by the voltage applied to the V_{CCCS} pins. All signals will share the same voltage levels.

Signals involved include: nWP, nINT, nRST, GPIO[3:0], S_A0, S_A1, SCLK and SDATA. The voltage used here is independent of the voltage chosen for the digital and analog core voltages and the output voltages selected for the clock outputs.

General-Purpose I/Os & Interrupts

The 8T49N242 provides four General Purpose Input / Output (GPIO) pins for miscellaneous status & control functions. Each GPIO may be configured as either an input or an output. Each GPIO may be directly controlled from register bits or be used as a predefined function as shown in Table 4. Note that the default state prior to configuration being loaded from internal OTP will be to set each GPIO to input direction to function as an Output Enable.

Table 4. GPIO Configuration[1]

GPIO Pin	Configured as Input		Configured as Output	
	Fixed Function (default)	General Purpose	Fixed Function	General Purpose
3	-	GPI[3]	LOL	GPO[3]
2	CSEL	GPI[2]	LOS[0]	GPO[2]
1	OSEL[1]	GPI[1]	LOS[1]	GPO[1]
0	OSEL[0]	GPI[0]	HOLD	GPO[0]

NOTE 1: GPI[x]: General Purpose Input. Logic state on GPIO[x] pin is directly reflected in GPI[x] register.

LOL: Loss-of-Lock Status Flag for Digital PLL. Logic-high indicates digital PLL not locked.

GPO[x]: General Purpose Output. Logic state is determined by value written in register GPO[x].

OSEL[n]: Output Enable Control Signals for Outputs Qx, nQx. Refer to Section, “Output Enable Operation”.

LOS[x]: Loss-of-Signal Status Flag for Input Reference x. Logic-high indicates input reference failure.

CSEL: Manual Clock Select Input for PLL. Logic-high selects differential clock input 1 (CLK1).

HOLD: Holdover Status Flag for Digital PLL. Logic-high indicates digital PLL in holdover status.

Refer to Section, “Register Descriptions” for additional details.

If used in the Fixed Function mode of operation, the GPIO bits will reflect the real-time status of their respective status bits as shown in Table 4.

The LOL alarm will support two modes of operation:

- De-asserts once PLL is locked, or
- De-asserts after PLL is locked and all internal synchronization operations that may destabilize output clocks are completed.

Interrupt Functionality

Interrupt functionality includes an interrupt status flag for each of PLL Loss-of-Lock status (LOL), PLL in holdover status (HOLD) and Loss-of-Signal status for each input (LOS[1:0]). Those Status Flags are set whenever there is an alarm on their respective functions. The Status Flag will remain set until the alarm has been cleared and a '1' has been written to the Status Flag's register location or if a reset occurs. Each Status Flag will also have an Interrupt Enable bit that will determine if that Status Flag is allowed to cause the Device Interrupt Status to be affected (enabled) or not (disabled). All Interrupt Enable bits will be in the disabled state after reset. The Device Interrupt Status Flag and nINT output pin are asserted if any of the enabled interrupt Status Flags are set.

Output Enable Operation

When GPIO[1:0] are used as Output Enable control signals, the function of the pins is to select one of four register-based maps that indicate which outputs should be enabled or disabled.

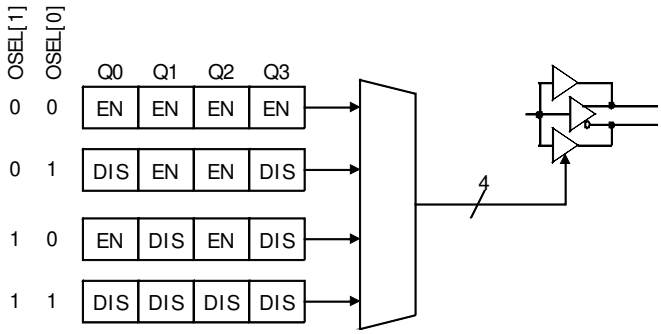


Figure 4. Output Enable Map Operation

Device Hardware Configuration

The 8T49N242 supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with one complete device configuration. Some or all of this pre-programmed configuration will be loaded into the device's registers on power-up or reset.

These default register settings can be over-written using the serial programming interface once reset is complete. Any configuration written via the serial programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

Device Start-up & Reset Behavior

The 8T49N242 has an internal power-up reset (POR) circuit and a Master Reset input pin nRST. If either is asserted, the device will be in the Reset State.

For highly programmable devices, it's common practice to reset the device immediately after the initial power-on sequence. IDT recommends connecting the nRST input pin to a programmable logic source for optimal functionality. It is recommended that a minimum pulse width of 10ns be used to drive the nRST input.

While in the reset state (nRST input asserted or POR active), the device will operate as follows:

- All registers will return to & be held in their default states as indicated in the applicable register description.
- All internal state machines will be in their reset conditions.
- The serial interface will not respond to read or write cycles.
- The GPIO signals will be configured as Output Enable inputs.
- All clock outputs will be disabled.
- All interrupt status and Interrupt Enable bits will be cleared, negating the nINT signal.

Upon the later of the internal POR circuit expiring or the nRST input negating, the device will exit reset and begin self-configuration.

The device will load an initial block of its internal registers using the configuration stored in the internal One-Time Programmable (OTP) memory. Once this step is complete, the 8T49N242 will check the register settings to see if it should load the remainder of its configuration from an external I^2C EEPROM at a defined address or continue loading from OTP, or both. See Section, "I2C Boot-up Initialization Mode" for details on how this is performed.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the crystal and begin operation. Once the PLL is locked, all the outputs derived from it will be synchronized and output phase adjustments can then be applied if desired.

Serial Control Port Description

Serial Control Port Configuration Description

The device has a serial control port capable of responding as a slave in an I^2C compatible configuration, to allow access to any of the internal registers for device programming or examination of internal status. All registers are configured to have default values. See the specifics for each register for details.

The device has the additional capability of becoming a master on the I^2C bus only for the purpose of reading its initial register configurations from a serial EEPROM on the I^2C bus. Writing of the configuration to the serial EEPROM must be performed by another device on the same I^2C bus or pre-programmed into the device prior to assembly.

I²C Mode Operation

The I²C interface is designed to fully support v1.2 of the I²C Specification for Normal and Fast mode operation. The device acts as a slave device on the I²C bus at 100kHz or 400kHz using the address defined in the Serial Interface Control register (0006h), as modified by the S_A0 & S_A1 input pin settings. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

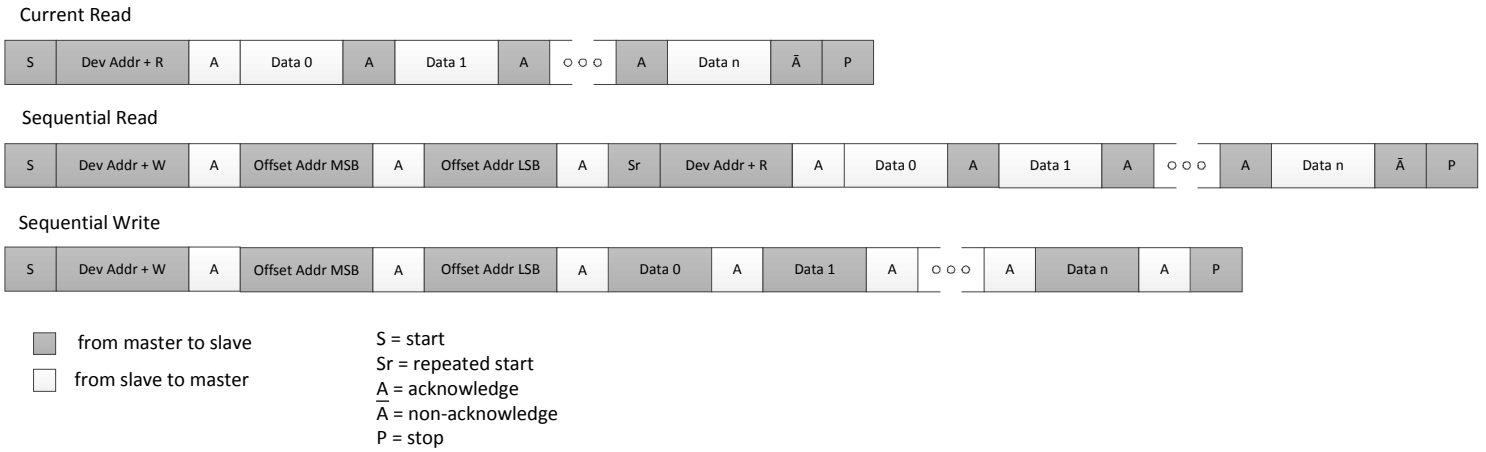


Figure 5. I²C Slave Read and Write Cycle Sequencing

I²C Master Mode

When operating in I²C mode, the 8T49N242 has the capability to become a bus master on the I²C bus for the purposes of reading its configuration from an external I²C EEPROM. Only a block read cycle will be supported.

As an I²C bus master, the 8T49N242 will support the following functions:

- 7-bit addressing mode
- Base address register for EEPROM
- Validation of the read block via CCITT-8 CRC check against value stored in last byte (84h) of EEPROM
- Support for 100kHz and 400kHz operation with speed negotiation. If bit d0 is set at Byte address 05h in the EEPROM, this will shift from 100kHz operation to 400kHz operation.
- Support for 1- or 2-byte addressing mode
- Master arbitration with programmable number of retries
- Fixed-period cycle response timer to prevent permanently hanging the I²C bus.
- Read will abort with an alarm (BOOTFAIL) if any of the following conditions occur: Slave NACK, Arbitration Fail, Collision during Address Phase, CRC failure, Slave Response time-out

The 8T49N242 will not support the following functions:

- I²C General Call
- Slave clock stretching
- I²C Start Byte protocol
- EEPROM Chaining
- CBUS compatibility
- Responding to its own slave address when acting as a master
- Writing to external I²C devices including the external EEPROM used for booting

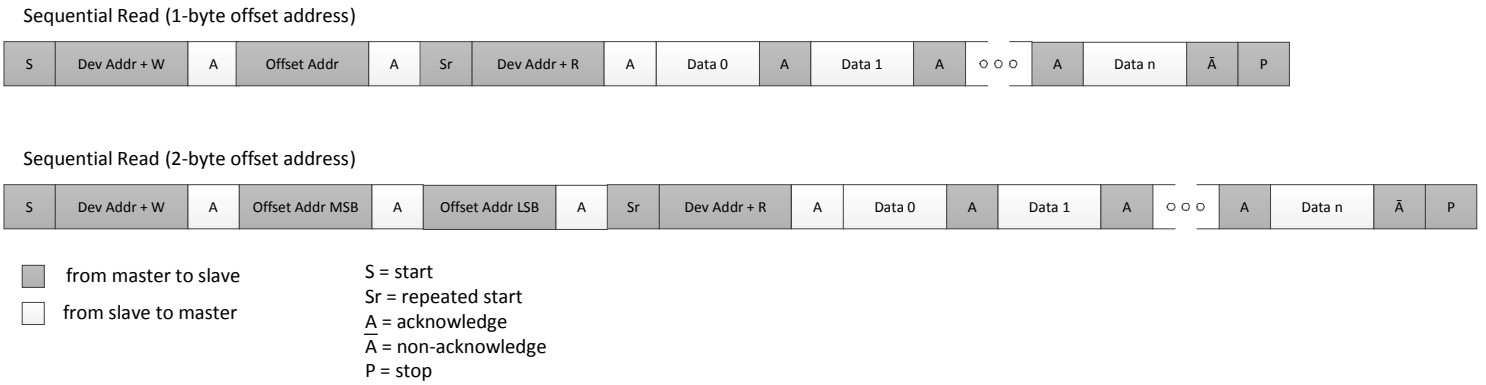


Figure 6. I²C Master Read Cycle Sequencing

I²C Boot-up Initialization Mode

If enabled (via the BOOT_EEP bit in the Startup register), once the nRST input has been deasserted (high) and its internal power-up reset sequence has completed, the device will contend for ownership of the I²C bus to read its initial register settings from a memory location on the I²C bus. The address of that memory location is kept in non-volatile memory in the Startup register. During the boot-up process, the device will not respond to serial control port accesses. Once the initialization process is complete, the contents of any of the device's registers can be altered. It is the responsibility of the user to make any desired adjustments in initial values directly in the serial bus memory.

If a NACK is received to any of the read cycles performed by the device during the initialization process, or if the CRC does not match the one stored in address 84h of the EEPROM the process will be aborted and any uninitialized registers will remain with their default values. The BOOTFAIL bit in the Global Interrupt Status register (0210h) will also be set in this event.

Contents of the EEPROM should be as shown in Table 5.

Table 5. External Serial EEPROM Contents

EEPROM Offset (Hex)	Contents							
	D7	D6	D5	D4	D3	D2	D1	D0
00	1	1	1	1	1	1	1	1
01	1	1	1	1	1	1	1	1
02	1	1	1	1	1	1	1	1
03	1	1	1	1	1	1	1	1
04	1	1	1	1	1	1	1	1
05	1	1	1	1	1	1	1	Serial EEPROM Speed Select 0 = 100kHz 1 = 400kHz
06	1	8T49N242 Device I²C Address [6:2]					1	1
07	0	0	0	0	0	0	0	0
08 - 83	Desired contents of Device Registers 08h - 83h							
84	Serial EEPROM CRC							
85 - FF	Unused							

Register Descriptions

Table 6. Register Blocks

Register Ranges Offset (Hex)	Register Block Description
0000 - 0001	Startup Control Registers
0002 - 0005	Device ID Control Registers
0006 - 0007	Serial Interface Control Registers
0008 - 002F	Digital PLL Control Registers
0030 - 0038	GPIO Control Registers
0039 - 003E	Output Driver Control Registers
003F - 004A	Output Divider Control Registers
004B - 0056	Reserved
0057 - 0062	Reserved
0063 - 0067	Output Divider Source Control Registers
0068- 006B	Analog PLL Control Registers
006C - 0070	Power-Down & Lock Alarm Control Registers
0071 - 0078	Input Monitor Control Registers
0079	Interrupt Enable Register
007A - 007B	Factory Setting Registers
007C - 01FF	Reserved
0200 - 0201	Interrupt Status Registers
0202 - 020B	Reserved
020C	General-Purpose Input Status Register
020D - 0212	Global Interrupt and Boot Status Register
0213 - 03FF	Reserved

Table 7A. Startup Control Register Bit Field Locations and Descriptions

Startup Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0000	EEP_RTY[4:0]					Rsvd	nBOOT_OTP	nBOOT_EEP
0001	EEP_A15	EEP_ADDR[6:0]						

Startup Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
EEP_RTY[4:0]	R/W	1h	Select number of times arbitration for the I^2C bus to read the serial EEPROM will be retried before being aborted. Note that this number does not include the original try.
nBOOT_OTP	R/W	NOTE[1]	Internal One-Time Programmable (OTP) memory usage on power-up: 0 = Load power-up configuration from OTP 1 = Only load 1st eight bytes from OTP
nBOOT_EEP	R/W	NOTE[1]	External EEPROM usage on power-up: 0 = Load power-up configuration from external serial EEPROM (overwrites OTP values) 1 = Don't use external EEPROM
EEP_A15	R/W	NOTE[1]	Serial EEPROM supports 15-bit addressing mode (multiple pages).
EEP_ADDR[6:0]	R/W	NOTE[1]	I^2C base address for serial EEPROM.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Please refer to the FemtoClock® NG Universal Frequency Translator Ordering Product Information guide or custom datasheet addendum for more details.

Table 7B. Device ID Control Register Bit Field Locations and Descriptions

Device ID Register Control Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0002	REV_ID[3:0]				DEV_ID[15:12]			
0003	DEV_ID[11:4]							
0004	DEV_ID[3:0]				DASH_CODE [10:7]			
0005	DASH_CODE [6:0]							1

Device ID Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
REV_ID[3:0]	R/W	0h	Device revision.
DEV_ID[15:0]	R/W	0607h	Device ID code.
DASH CODE [10:0]	R/W	NOTE[1]	Device Dash code. Decimal value assigned by IDT to identify the configuration loaded at the factory. May be over-written by users at any time.

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Please refer to the FemtoClock® NG Universal Frequency Translator Ordering Product Information guide or custom datasheet addendum for more details.

Table 7C. Serial Interface Control Register Bit Field Locations and Descriptions

Serial Interface Control Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0006	0	UFTADD[6:2]					UFTADD[1]	UFTADD[0]
0007	Rsvd							1

Device ID Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
UFTADD[6:2]	R/W	NOTE[1]	Configurable portion of I^2C base (bits 6:2) address for this device.
UFTADD[1]	R/O	0b	I^2C base address bit 1. This address bit reflects the status of the S_A1 external input pin. See Table 1.
UFTADD[0]	R/O	0b	I^2C base address bit 0. This address bit reflects the status of the S_A0 external input pin. See Table 1.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Generic dash codes -900 through -903, -998 and -999 are available and programmed with the default I^2C address of 1111100b (1101100b for -999). Please refer to the *FemtoClock NG Universal Frequency Translator Ordering Product Information guide* for more details.

Table 7D. Digital PLL Input Control Register Bit Field Locations and Descriptions

Digital PLL Input Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0008	REFSEL[2:0]			FBSEL[1:0]			RVRT	SWMODE
0009	Rsvd							REF_PRI
000A	Rsvd		REFDIS1	REFDIS0	Rsvd	Rsvd	STATE[1:0]	
000B	Rsvd			PRE0[20:16]				
000C	PRE0[15:8]							
000D	PRE0[7:0]							
000E	Rsvd			PRE1[20:16]				
000F	PRE1[15:8]							
0010	PRE1[7:0]							

Digital PLL Input Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
REFSEL[2:0]	R/W	000b	Input reference selection for Digital PLL: 000 = Automatic selection 001 = Manual selection by GPIO input 010 through 011 = Reserved 100 = Force selection of Input Reference 0 101 = Force selection of Input Reference 1 110 = Do not use 111 = Do not use
FBSEL[2:0]	R/W	000b	Feedback mode selection for Digital PLL: 000 through 011 = internal feedback divider 100 = external feedback from Input Reference 0 101 = external feedback from Input Reference 1 110 = do not use 111 = do not use
RVRT	R/W	1b	Automatic switching mode for Digital PLL: 0 = non-revertive switching 1 = revertive switching
SWMODE	R/W	1b	Controls how Digital PLL adjusts output phase when switching between input references: 0 = Absorb any phase differences between old & new input references 1 = Track to follow new input reference's phase using phase-slope limiting
REF_PRI	R/W	0b	Switchover priority for Input References when used by Digital PLL: 0 = CLK0 is primary input reference 1 = CLK1 is primary input reference
REFDIS0	R/W	0b	Input Reference 0 Switching Selection Disable for Digital PLL: 0 = Input Reference 0 is included in the switchover sequence 1 = Input Reference 0 is not included in the switchover sequence
REFDIS1	R/W	0b	Input Reference 1 Switching Selection Disable for Digital PLL: 0 = Input Reference 1 is included in the switchover sequence 1 = Input Reference 1 is not included in the switchover sequence
STATE[1:0]	R/W	00b	Digital PLL State Machine Control: 00 = Run automatically 01 = Force FREERUN state - set this if in Synthesizer Mode. 10 = Force NORMAL state 11 = Force HOLDOVER state

Digital PLL Input Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
PRE0[20:0]	R/W	000000h	Pre-divider ratio for Input Reference 0 when used by Digital PLL.
PRE1[20:0]	R/W	000000h	Pre-divider ratio for Input Reference 1 when used by Digital PLL.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7E. Digital PLL Feedback Control Register Bit Field Locations and Descriptions

Digital PLL Feedback Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0011	M1_0[23:16]							
0012	M1_0[15:8]							
0013	M1_0[7:0]							
0014	M1_1[23:16]							
0015	M1_1[15:8]							
0016	M1_1[7:0]							
0017	LCKBW[3:0]				ACQBW[3:0]			
0018	LCKDAMP[2:0]			ACQDAMP[2:0]			PLLGAIN[1:0]	
0019	Rsvd			Rsvd	Rsvd			Rsvd
001A	Rsvd							
001B	Rsvd							
001C	Rsvd							Rsvd
001D	Rsvd							
001E	Rsvd							
001F	FFh							
0020	FFh							
0021	FFh							
0022	FFh							
0023	SLEW[1:0]		Rsvd	HOLD[1:0]		Rsvd	HOLDAVG	FASTLCK
0024	LOCK[7:0]							
0025	Rsvd							DSM_INT[8]
0026	DSM_INT[7:0]							
0027	Rsvd							
0028	Rsvd			DSMFRAC[20:16]				
0029	DSMFRAC[15:8]							
002A	DSMFRAC[7:0]							
002B	Rsvd							
002C	01h							
002D	Rsvd							
002E	Rsvd							
002F	DSM_ORD[1:0]		DCXOGAIN[1:0]		Rsvd	DITHGAIN[2:0]		

Digital PLL Feedback Configuration Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
M1_0[23:0]	R/W	070000h	M1 Feedback divider ratio for Input Reference 0 when used by Digital PLL.
M1_1[23:0]	R/W	070000h	M1 Feedback divider ratio for Input Reference 1 when used by Digital PLL.
LCKBW[3:0]	R/W	0111b	Digital PLL Loop Bandwidth while locked: 0000 = 0.2Hz 0001 = 0.4Hz 0010 = 0.8Hz 0011 = 1.6Hz 0100 = 3.2Hz 0101 = 6.4Hz 0110 = 12Hz 0111 = 25Hz 1000 = 50Hz 1001 = 100Hz 1010 = 200Hz 1011 = 400Hz 1100 = 800Hz 1101 = 1.6kHz 1110 = 6.4kHz 1111 = Reserved
ACQBW[3:0]	R/W	0111b	Digital PLL Loop Bandwidth while in acquisition (not-locked): 0000 = 0.2Hz 0001 = 0.4Hz 0010 = 0.8Hz 0011 = 1.6Hz 0100 = 3.2Hz 0101 = 6.4Hz 0110 = 12Hz 0111 = 25Hz 1000 = 50Hz 1001 = 100Hz 1010 = 200Hz 1011 = 400Hz 1100 = 800Hz 1101 = 1.6kHz 1110 = 6.4kHz 1111 = Reserved
LCKDAMP[2:0]	R/W	011b	Damping factor for Digital PLL while locked: 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved

Digital PLL Feedback Configuration Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
ACQDAMP[2:0]	R/W	011b	Damping factor for Digital PLL while in acquisition (not locked): 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved
PLLGAIN[1:0]	R/W	01b	Digital Loop Filter Gain Settings for Digital PLL: 00 = 0.5 01 = 1 10 = 1.5 11 = 2
SLEW[1:0]	R/W	00b	Phase-slope control for Digital PLL: 00 = no limit - controlled by loop bandwidth of Digital PLL 01 = 64us/s 10 = 11us/s 11 = Reserved
HOLD[1:0]	R/W	00b	Holdover Averaging mode selection for Digital PLL: 00 = Instantaneous mode - uses historical value 100ms prior to entering holdover 01 = Fast Average Mode 10 = Reserved 11 = Return to Center of VCO Tuning Range
HOLDAVG	R/W	0b	Holdover Averaging Enable for Digital PLL: 0 = Holdover averaging disabled 1 = Holdover averaging enabled as defined in HOLD[1:0]
FASTLCK	R/W	0b	Enables Fast Lock operation for Digital PLL: 0 = Normal locking using LCKBW & LCKDAMP fields in all cases 1 = Fast Lock mode using ACQBW & ACQDAMP when not phase locked and LCKBW & LCKDAMP once phase locked
LOCK[7:0]	R/W	3Fh	Lock window size for Digital PLL. Unsigned 2's complement binary number in steps of 2.5ns, giving a total range of 640ns. Do not program to 0.
DSM_INT[8:0]	R/W	02Dh	Integer portion of the Delta-Sigma Modulator value.
DSMFRAC[20:0]	R/W	000000h	Fractional portion of Delta-Sigma Modulator value. Divide this number by 2^{21} to determine the actual fraction.
DSM_ORD[1:0]	R/W	11b	Delta-Sigma Modulator Order for Digital PLL: 00 = Delta-Sigma Modulator disabled 01 = 1st order modulation 10 = 2nd order modulation 11 = 3rd order modulation

Digital PLL Feedback Configuration Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
DCXOGAIN[1:0]	R/W	01b	Multiplier applied to instantaneous frequency error before it is applied to the Digitally Controlled Oscillator in Digital PLL: 00 = 0.5 01 = 1 10 = 2 11 = 4
DITHGAIN[2:0]	R/W	000b	Dither Gain setting for Digital PLL: 000 = no dither 001 = Least Significant Bit (LSB) only 010 = 2 LSBs 011 = 4 LSBs 100 = 8 LSBs 101 = 16 LSBs 110 = 32 LSBs 111 = 64 LSBs
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7F. GPIO Control Register Bit Field Locations and Descriptions

The values observed on any GPIO pins that are used as general purpose inputs are visible in the GPI[3:0] register that is located at location 0x020C near a number of other read-only registers.

GPIO Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0030	Rsvd				GPIO_DIR[3:0]			
0031	Rsvd				GPI3SEL[2]	GPI2SEL[2]	GPI1SEL[2]	GPI0SEL[2]
0032	Rsvd				GPI3SEL[1]	GPI2SEL[1]	GPI1SEL[1]	GPI0SEL[1]
0033	Rsvd				GPI3SEL[0]	GPI2SEL[0]	GPI1SEL[0]	GPI0SEL[0]
0034	Rsvd				GPO3SEL[2]	GPO2SEL[2]	GPO1SEL[2]	GPO0SEL[2]
0035	Rsvd				GPO3SEL[1]	GPO2SEL[1]	GPO1SEL[1]	GPO0SEL[1]
0036	Rsvd				GPO3SEL[0]	GPO2SEL[0]	GPO1SEL[0]	GPO0SEL[0]
0037	Rsvd							
0038	Rsvd				GPO[3:0]			

GPIO Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
GPIO_DIR[3:0]	R/W	0000b	Direction control for General-Purpose I/O Pins GPIO[3:0]: 0 = input mode 1 = output mode
GPI0SEL[2:0]	R/W	001b	Function of GPIO[0] pin when set to input mode by GPIO_DIR[0] register bit: 000 = General Purpose Input (value on GPIO[0] pin directly reflected in GPI[0] register bit) 001 = Output Enable control bit 0: OSEL[0], (Refer to Figure 4 for more details.) 010 = reserved 011 = reserved 100 through 111 = reserved
GPI1SEL[2:0]	R/W	001b	Function of GPIO[1] pin when set to input mode by GPIO_DIR[1] register bit: 000 = General Purpose Input (value on GPIO[1] pin directly reflected in GPI[1] register bit) 001 = Output Enable control bit 1: OSEL[1], (Refer to Figure 4 for more details.) 010 through 111 = reserved
GPI2SEL[2:0]	R/W	001b	Function of GPIO[2] pin when set to input mode by GPIO_DIR[2] register bit: 000 = General Purpose Input (value on GPIO[2] pin directly reflected in GPI[2] register bit) 001 = CSEL: Manual Clock Select Input for PLL 010 = reserved 011 = reserved 100 = reserved 101 through 111 = reserved
GPI3SEL[2:0]	R/W	001b	Function of GPIO[3] pin when set to input mode by GPIO_DIR[3] register bit: 000 = General Purpose Input (value on GPIO[3] pin directly reflected in GPI[3] register bit) 001 = reserved 010 = reserved 011 = reserved 100 through 111 = reserved

GPIO Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
GPO0SEL[2:0]	R/W	000b	Function of GPIO[0] pin when set to output mode by GPIO_DIR[0] register bit: 000 = General Purpose Output (value in GPO[0] register bit driven on GPIO[0] pin 001 = Holdover Status Flag for Digital PLL reflected on GPIO[0] pin 010 = reserved 011 = reserved 100 = reserved 101 = reserved 110 through 111 = reserved
GPO1SEL[2:0]	R/W	000b	Function of GPIO[1] pin when set to output mode by GPIO_DIR[1] register bit: 000 = General Purpose Output (value in GPO[1] register bit driven on GPIO[1] pin 001 = Loss-of-Signal Status Flag for Input Reference 1 reflected on GPIO[1] pin 010 = reserved 011 = reserved 100 = reserved 101 = reserved 110 = reserved 111 = reserved
GPO2SEL[2:0]	R/W	000b	Function of GPIO[2] pin when set to output mode by GPIO_DIR[2] register bit: 000 = General Purpose Output (value in GPO[2] register bit driven on GPIO[2] pin 001 = Loss-of-Signal Status Flag for Input Reference 0 reflected on GPIO[2] pin 010 = reserved 011 = reserved 100 = reserved 101 through 111 = reserved
GPO3SEL[2:0]	R/W	000b	Function of GPIO[3] pin when set to output mode by GPIO_DIR[3] register bit: 000 = General Purpose Output (value in GPO[3] register bit driven on GPIO[3] pin 001 = Loss-of-Lock Status Flag for Digital PLL reflected on GPIO[3] pin 010 = reserved 011 = reserved 100 through 111 = reserved
GPO[3:0]	R/W	0000b	Output Values reflect on pin GPIO[3:0] when General-Purpose Output Mode selected.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7G. Output Driver Control Register Bit Field Locations and Descriptions

Output Driver Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0039	Rsvd				OUTEN[3:0]			
003A	Rsvd				POL_Q[3:0]			
003B	Rsvd							
003C	Rsvd							
003D	OUTMODE3[2:0]			SE_MODE3	OUTMODE2[2:0]			SE_MODE2
003E	OUTMODE1[2:0]			SE_MODE1	OUTMODE0[2:0]			SE_MODE0

Output Driver Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
OUTEN[3:0]	R/W	0000b	Output Enable control for Clock Outputs Q[3:0], nQ[3:0]: 0 = Qn is in a high-impedance state 1 = Qn is enabled as indicated in appropriate OUTMODEn[2:0] register field
POL_Q[3:0]	R/W	0000b	Polarity of Clock Outputs Q[3:0], nQ[3:0]: 0 = Qn is normal polarity 1 = Qn is inverted polarity
OUTMODEm[2:0]	R/W	001b	Output Driver Mode of Operation for Clock Output Pair Qm, nQm: 000 = High-impedance 001 = LVPECL 010 = LVDS 011 = LVCMOS 100 = HCSL 101 - 111 = reserved
SE_MODEm	R/W	0b	Behavior of Output Pair Qm, nQm when LVCMOS operation is selected: (Must be 0 if LVDS or LVPECL output style is selected) 0 = Qm and nQm are both the same frequency but inverted in phase 1 = Qm and nQm are both the same frequency and phase
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7H. Output Divider Control Register Bit Field Locations and Descriptions

Output Divider Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
003F	Rsvd						NS1_Q0[1:0]	
0040	NS2_Q0[15:8]							
0041	NS2_Q0[7:0]							
0042	Rsvd						NS1_Q1[1:0]	
043	NS2_Q1[15:8]							
0044	NS2_Q1[7:0]							
0045	Rsvd						NS1_Q2[1:0]	
0046	NS2_Q2[15:8]							
0047	NS2_Q2[7:0]							
0048	Rsvd						NS1_Q3[1:0]	
0049	NS2_Q3[15:8]							
004A	NS2_Q3[7:0]							

Output Divider Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
NS1_Qm[1:0]	R/W	10b	1st Stage Output Divider Ratio for Output Clock Qm, nQm (m = 0, 1, 2, 3): 00 = /5 01 = /6 10 = /4 11 = /1 (Do not use this selection if PLL is the source since the 2nd-stage divider has a limit of 1GHz).
NS2_Qm[15:0]	R/W	0002h	2nd Stage Output Divider Ratio for Output Clock Qm, nQm (m = 0, 1, 2, 3). Actual divider ratio is 2x the value written here. A value of 0 in this register will bypass the second stage of the divider.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.