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Description

The 8T49N286 has two independent, fractional-feedback PLLs that can be used as jitter attenuators and frequency translators. It is equipped with six integer and two fractional output dividers, allowing the generation of up to eight different output frequencies, ranging from 8kHz to 1GHz. Four of these frequencies are completely independent of each other and the inputs. The other four are related frequencies. The eight outputs may select among LVPECL, LVDS, HCSL or LVCMOS output levels.

This functionality makes it ideal to be used in any frequency translation application, including 1G, 10G, 40G and 100G Synchronous Ethernet, OTN, and SONET/SDH, including ITU-T G.709 (2009) FEC rates. The device may also behave as a frequency synthesizer.

The 8T49N286 accepts up to four differential or single-ended input clocks and a crystal input. Each of the two internal PLLs can lock to different input clocks which may be of independent frequencies. The other two input clocks are intended for redundant backup of the primary clocks and must be related in frequency to their primary.

The device supports hitless reference switching between input clocks. The device monitors all input clocks for Loss of Signal (LOS), and generates an alarm when an input clock failure is detected. Automatic and manual hitless reference switching options are supported. LOS behavior can be set to support gapped or ungapped clocks.

The 8T49N286 supports holdover for each PLL. The holdover has an initial accuracy of ±50ppB from the point where the loss of all applicable input reference(s) has been detected. It maintains a historical average operating point for each PLL that may be returned to in holdover at a limited phase slope.

The device places no constraints on input to output frequency conversion, supporting all FEC rates, including the new revision of ITU-T Recommendation G.709 (2009), most with 0ppm conversion error.

Each PLL has a register-selectable loop bandwidth from 1.4Hz to 360Hz.

Each output supports individual phase delay settings to allow output-output alignment.

The device supports Output Enable inputs and Lock, Holdover and LOS status outputs.

The device is programmable through an I^2C interface. It also supports I^2C master capability to allow the register configuration to be read from an external EEPROM. The user may select whether the programming interface uses I^2C protocols or SPI protocols, however in SPI mode, read from the external EEPROM is not supported.

Typical Applications

- OTN or SONET / SDH equipment Line cards (up to OC-192, and supporting FEC ratios)
- OTN de-mapping (Gapped Clock and DCO mode)
- Gigabit and Terabit IP switches / routers including support of Synchronous Ethernet
- SyncE (G.8262) applications
- Wireless base station baseband
- Data communications
- 100G Ethernet

Features

- Supports SDH/SONET and Synchronous Ethernet clocks including all FEC rate conversions
- <0.3ps RMS Typical Jitter (including spurs), 12kHz to 20MHz
- Operating modes: locked to input signal, holdover and free-run
- Initial holdover accuracy of ±50ppb
- Accepts up to four LVPECL, LVDS, LVHSTL, HCSL or LVCMOS input clocks
  - Accepts frequencies ranging from 8kHz up to 875MHz
  - Auto and manual input clock selection with hitless switching
  - Clock input monitoring, including support for gapped clocks
- Phase-Slope Limiting and Fully Hitless Switching options to control output phase transients
- Operates from a 10MHz to 40MHz fundamental-mode crystal
- Generates 8 LVPECL / LVDS / HCSL or 16 LVCMOS output clocks
  - Output frequencies ranging from 8kHz up to 1.0GHz (diff)
  - Output frequencies ranging from 8kHz to 250MHz (LVCMOS)
- Eight General Purpose I/O pins with optional support for status and control
  - Eight Output Enable control inputs
  - Lock, Holdover and Loss-of-Signal status outputs
- Open-drain Interrupt pin
- Write-protect pin to prevent configuration registers being altered
- Nine programmable loop bandwidth settings for each PLL from 1.4Hz to 360Hz.
  - Optional Fast Lock function
- Programmable output phase delays in steps as small as 16ps
- Register programmable through I^2C / SPI or via external I^2C EEPROM
- Bypass clock paths for system tests
- Power supply modes:
  V_{CC} / V_{CCA} / V_{CCO}
  3.3V / 3.3V / 3.3V
  3.3V / 3.3V / 2.5V
  3.3V / 3.3V / 1.8V (LVCMOS)
  2.5V / 2.5V / 3.3V
  2.5V / 2.5V / 2.5V
  2.5V / 2.5V / 1.8V (LVCMOS)
- -40°C to 85°C ambient operating temperature
- Package: 72QFN, lead-free RoHs (6)

8T49N286 Block Diagram

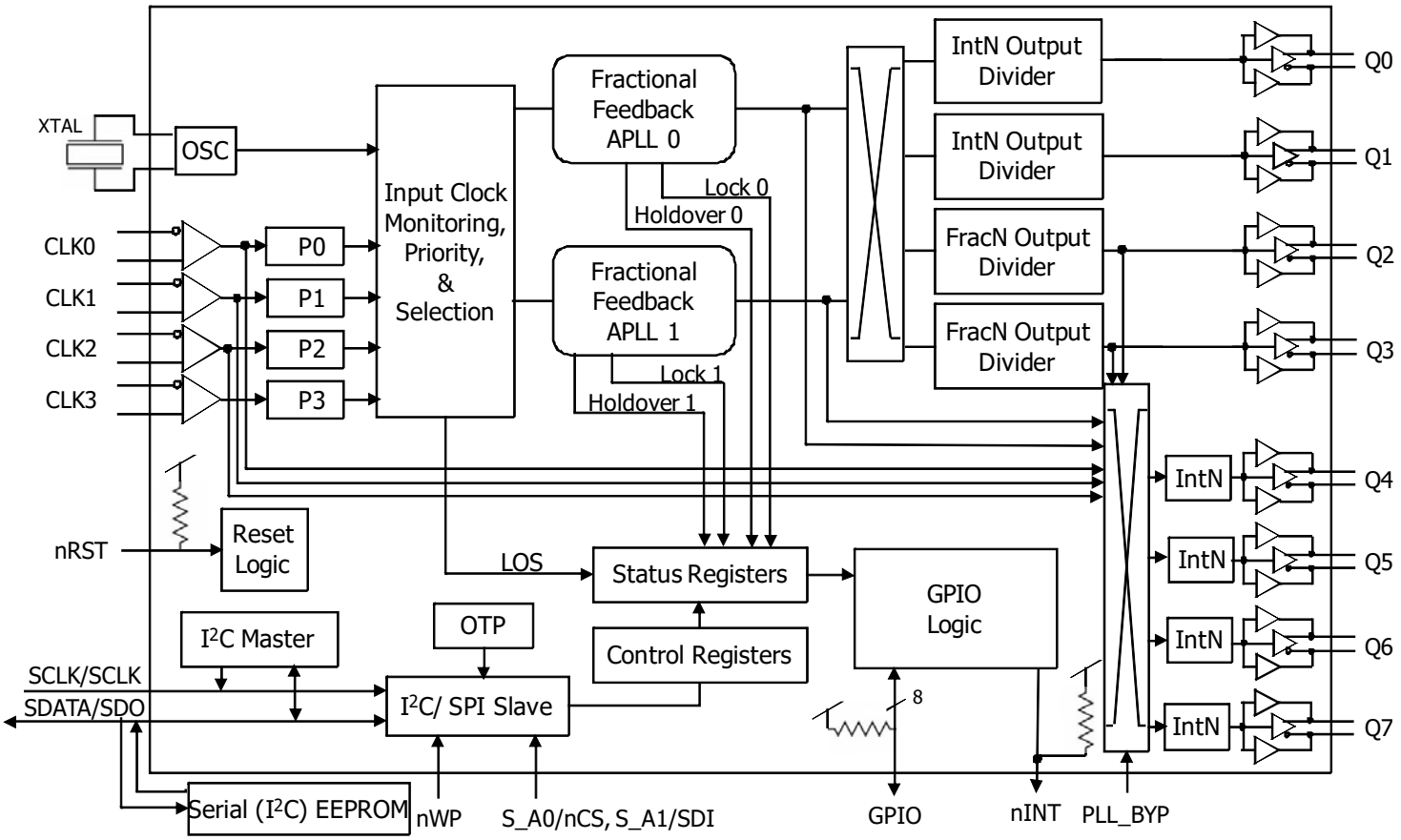
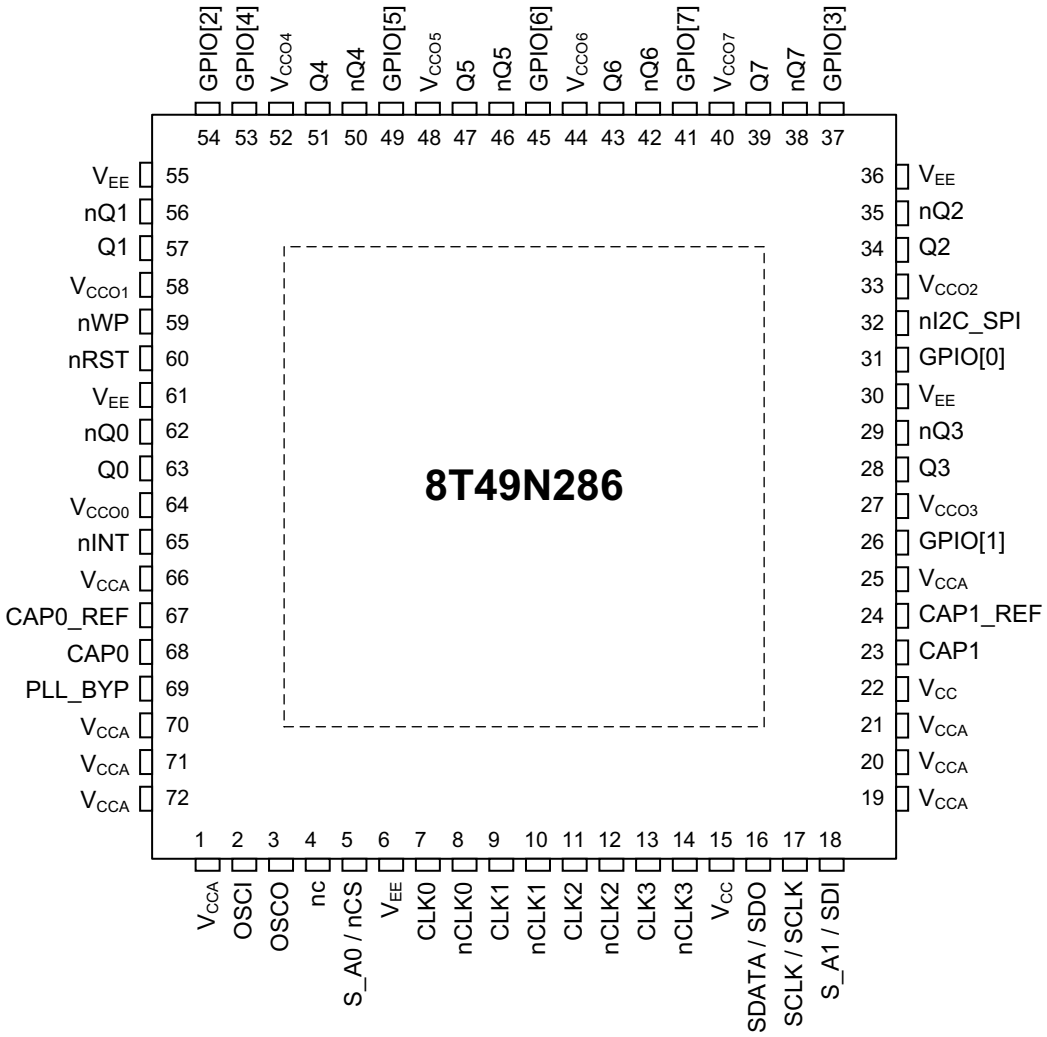


Figure 1. 8T49N286 Functional Block Diagram

Pin Assignment



72-pin, 10mm x 10mm VFQFN Package

Figure 2. Pinout Drawing

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
2	OSCI	I		Crystal Input. Accepts a 10MHz - 40MHz reference from a clock oscillator or a 12pF fundamental mode, parallel-resonant crystal.
3	OSCO	O		Crystal Output. This pin should be connected to a crystal. If an oscillator is connected to OSCI, then this pin must be left unconnected.
5	S_A0 / nCS	I	Pulldown	I^2C lower address bit A0 / SPI interface chip select signal.
16	SDATA / SDO	I/O	Pullup	I^2C interface bi-directional Data / SPI interface serial data output signal.
17	SCLK / SCLK	I/O	Pullup	I^2C interface bi-directional Clock / SPI interface clock input signal.
18	S_A1 / SDI	I	Pulldown	I^2C lower address bit A1 / SPI interface serial data input signal.
32	nI2C_SPI	I	Pulldown	Serial Interface Mode Selection. LVCMOS Input Levels: 0 = I^2C Mode 1 = SPI Mode
7	CLK0	I	Pulldown	Non-inverting differential clock input.
8	nCLK0	I	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors.)
9	CLK1	I	Pulldown	Non-inverting differential clock input.
10	nCLK1	I	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors.)
11	CLK2	I	Pulldown	Non-inverting differential clock input.
12	nCLK2	I	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors.)
13	CLK3	I	Pulldown	Non-inverting differential clock input.
14	nCLK3	I	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors.)
63, 62	Q0, nQ0	O	Universal	Output Clock 0. Please refer to Output Drivers for more details.
57, 56	Q1, nQ1	O	Universal	Output Clock 1. Please refer to Output Drivers for more details.
34, 35	Q2, nQ2	O	Universal	Output Clock 2. Please refer to Output Drivers for more details.
28, 29	Q3, nQ3	O	Universal	Output Clock 3. Please refer to Output Drivers for more details.
51, 50	Q4, nQ4	O	Universal	Output Clock 4. Please refer to Output Drivers for more details.
47, 46	Q5, nQ5	O	Universal	Output Clock 5. Please refer to Output Drivers for more details.
43, 42	Q6, nQ6	O	Universal	Output Clock 6. Please refer to Output Drivers for more details.
39, 38	Q7, nQ7	O	Universal	Output Clock 7. Please refer to Output Drivers for more details.
60	nRST	I	Pullup	Master Reset input. LVTTL / LVCMOS interface levels. 0 = All registers and state machines are reset to their default values 1 = Device runs normally
65	nINT	O	Open-drain with pullup	Interrupt output.
59	nWP	I	Pullup	Write protect input. LVTTL / LVCMOS interface levels: 0 = Write operations on the serial port will complete normally, but will have no effect except on interrupt registers 1 = Serial port writes may change any register
41, 45, 49, 53, 37, 54, 26, 31	GPIO[7:0]	I/O	Pullup	General-purpose input-outputs. LVTTL / LVCMOS Input levels Open-drain output. Pulled-up with 5.1kΩ resistor to V_{CC}.
69	PLL_BYP	I	Pulldown	Bypass Selection. Allow input references to bypass both PLLs. LVTTL / LVCMOS interface levels.

Number	Name	Type		Description
6, 30, 36, 55, 61, ePAD	V_{EE}	Power		Negative supply voltage. All V_{EE} pins and EPAD must be connected before any positive supply voltage is applied.
15	V_{CC}	Power		Core and digital function supply voltage.
22	V_{CC}	Power		Core and digital functions supply voltage.
1	V_{CCA}	Power		Analog function supply voltage for core analog functions.
19, 20, 21, 25	V_{CCA}	Power		Analog function supply voltage for analog functions associated with PLL1.
66, 70, 71, 72	V_{CCA}	Power		Analog function supply voltage for analog functions associated with PLL0.
64	V_{CCO0}	Power		High-speed output supply voltage for output pair Q0, nQ0.
58	V_{CCO1}	Power		High-speed output supply voltage for output pair Q1, nQ1.
33	V_{CCO2}	Power		High-speed output supply voltage for output pair Q2, nQ2.
27	V_{CCO3}	Power		High-speed output supply voltage for output pair Q3, nQ3.
52	V_{CCO4}	Power		High-speed output supply voltage for output pair Q4, nQ4.
48	V_{CCO5}	Power		High-speed output supply voltage for output pair Q5, nQ5.
44	V_{CCO6}	Power		High-speed output supply voltage for output pair Q6, nQ6.
40	V_{CCO7}	Power		High-speed output supply voltage for output pair Q7, nQ7.
68, 67	CAP0, CAP0_REF	Analog		PLL0 External Capacitance.
23, 24	CAP1, CAP1_REF	Analog		PLL1 External Capacitance.
4	nc	Unused		No connect.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See *Table 2*, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics, V_{CC} = V_{CCOX} = 3.3V±5% or 2.5V±5%

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance; NOTE 1				3.5		pF
R_{PULLUP}	Internal Pullup Resistor	nRST, nWP, SDATA / SDO, SCLK / SCLK			51		kΩ
		nINT			50		kΩ
		GPIO[7:0]			5.1		kΩ
$R_{PULLDOWN}$	Internal Pulldown Resistor				51		kΩ
C_{PD}	Power Dissipation Capacitance (per output pair)	LVCMOS Q[0:1], Q[4:7]	V_{CCOX} = 3.465V		14.5		pF
		LVCMOS Q[2:3]	V_{CCOX} = 3.465V		18.5		pF
		LVCMOS Q[0:1], Q[4:7]	V_{CCOX} = 2.625V		13		pF
		LVCMOS Q[2:3]	V_{CCOX} = 2.625V		17.5		pF
		LVCMOS Q[0:1], Q[4:7]	V_{CCOX} = 1.89V		12.5		pF
		LVCMOS Q[2:3]	V_{CCOX} = 1.89V		17		pF
		LVDS, HCSL or LVPECL Q[0:1], Q[4:7]	V_{CCOx} = 3.465V or 2.625V		2		pF
		LVDS, HCSL or LVPECL Q[2:3]	V_{CCOx} = 3.465V or 2.625V		4.5		pF
R_{OUT}	Output Impedance	GPIO[7:0]	Output HIGH		5.1		kΩ
			Output LOW		25		Ω
		LVCMOS Q[7:0], nQ[7:0]			20		Ω

NOTE: V_{CCOX} denotes: V_{CCO0} through V_{CCO7}.
NOTE 1: This specification does not apply to OSCI and OSCO pins.

Principles of Operation

The 8T49N286 has two PLLs that can each independently be locked to any of the input clocks and generate a wide range of synchronized output clocks.

It incorporates two completely independent PLLs. These could be used for example in the transmit and receive path of Synchronous Ethernet equipment. Any of the input clocks can be selected as the reference for either PLL. From the output of the two PLLs a wide range of output frequencies can be simultaneously generated.

The 8T49N286 accepts up to four differential input clocks ranging from 8kHz up to 875MHz. It generates up to eight output clocks ranging from 8kHz up to 1.0GHz.

Each PLL path within the 8T49N286 supports three states: Lock, Holdover and Free-run. Lock and holdover status may be monitored on register bits and pins. Each PLL also supports automatic and manual hitless reference switching. In the locked state, the PLL locks to a valid clock input and its output clocks have a frequency accuracy equal to the frequency accuracy of the input clock. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. Each of the PLL paths within the 8T49N286 has an initial holdover frequency offset of ±50ppb. In the Free-run state, the PLL outputs a clock with the same frequency accuracy as the external crystal.

Upon power up, each PLL will enter Free-run state, in this state it generates output clocks with the same frequency accuracy as the external crystal. The 8T49N286 continuously monitors each input for activity (signal transitions).

In automatic reference switching, when an input clock has been validated the PLL will transition to the locked state. If the selected input clock fails and there are no other valid input clocks, the PLL will quickly detect that and go into holdover. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. If the selected input clock fails and another input clock is available then the 8T49N286 will hitlessly switch to that input clock. The reference switch can be either revertive or non-revertive.

The device supports conversion of any input frequency to four different, independent output frequencies on the Q[0:3] outputs. Additionally, a further four output frequencies may be generated that are integer-related to the four independent frequencies. These additional four frequencies are on the Q[4:7] outputs.

The 8T49N286 has a programmable loop bandwidth from 1.4Hz to 360Hz.

The device monitors all input clocks and generates an alarm when an input clock failure is detected.

The device supports programmable individual output phase adjustments in order to allow control of input to output phase adjustments and output to output phase alignment.

The device is programmable through an I^2C or SPI interface and may also autonomously read its register settings from an internal One-Time Programmable (OTP) memory or an external serial I^2C EEPROM.

Bypass Path

For system test purposes, each of PLL0 and PLL1 may be bypassed. When PLL_BYP is asserted the CLK0 input reference will be presented to the Q4 dividers. The CLK1 input reference will be presented to the Q5 dividers.

Additionally, CLK0, CLK1 or CLK2 may be used as a clock source for the output dividers of Q[4:7]. This may only be done for input frequencies of 250MHz or less.

Input Clock Selection

The 8T49N286 accepts up to four input clocks with frequencies ranging from 8kHz up to 875MHz. Each input can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS inputs using 1.8V, 2.5V or 3.3V logic levels. To use LVCMOS inputs, please refer to the Application Note, Wiring the Differential Input to Accept Single-Ended Levels for biasing instructions.

The device has independent input clock selection control for each PLL. In Manual mode, only one of these inputs may be chosen per PLL and if that input fails that PLL will enter holdover.

Manual mode may be operated by directly selecting the desired input reference in the REFSEL register field. It may also operate via pin-selection of the desired input clock by selecting that mode in the REFSEL register field. In that case, GPIOs must be used as Clock Select inputs (CSELn[1:0]) for PLLn.

CSELn[1]	CSELn[0]	Selected Input Reference
0	0	CLK0
0	1	CLK1
1	0	CLK2
1	1	CLK3

In addition, the crystal frequency may be passed directly to the output dividers for Q[4:7] for use as a reference.

Inputs do not support transmission of spread-spectrum clocking sources. Since this family is intended for high-performance applications, it will assume input reference sources to have stabilities of ±100ppm or better.

If the PLL is working in automatic mode, then each of the input reference sources is assigned a priority of 1-4. At power-up or if the currently selected input reference fails, the PLL will switch to the highest priority input reference that is valid at that time (see section, Input Clock Monitor for details).

Automatic mode has two sub-options: revertive or non-revertive. In revertive mode, the PLL will switch to a reference with a higher priority setting whenever one becomes valid. In non-revertive mode the PLL remains with the currently selected source as long as it remains valid.

The clock input selection is based on the input clock priority set by the Clock Input Priority control registers. It is recommended that all input references for a PLL be given different priority settings in the Clock Input Priority control registers for that PLL.

Input Clock Monitor

Each clock input is monitored for Loss of Signal (LOS). If no activity has been detected on the clock input within a user-selectable time period then the clock input is considered to be failed and an internal Loss-of-Signal status flag is set, which may cause an input switchover depending on other settings. The user-selectable time period has sufficient range to allow a gapped clock missing many consecutive edges to be considered a valid input.

User-selection of the clock monitor time-period is based on a counter driven by a monitor clock. The monitor clock is fixed at the frequency of PLL0's VCO divided by 8. With a VCO range of 3GHz - 4GHz, the monitor clock has a frequency range of 375MHz to 500MHz.

The monitor logic for each input reference will count the number of monitor clock edges indicated in the appropriate Monitor Control register. If an edge is received on the input reference being monitored, then the count resets and begins again. If the target edge count is reached before an input reference edge is received, then an internal soft alarm is raised and the count re-starts. During the soft alarm period, the PLL(s) tracking this input will not be adjusted. If an input reference edge is received before the count expires for the second time, then the soft alarm status is cleared and the PLL(s) will resume adjustments. If the count expires again without any input reference edge being received, then a Loss-of-Signal alarm is declared.

It is expected that for normal (non-gapped) clock operation, users will set the monitor clock count for each input reference to be slightly longer than the nominal period of that input reference. A margin of 2-3 monitor clock periods should give a reasonably quick reaction time and yet prevent false alarms.

For gapped clock operation, the user will set the monitor clock count to a few monitor clock periods longer than the longest expected clock gap period. The monitor count registers support 17-bit count values, which will support at least a gap length of two clock periods for any supported input reference frequency, with longer gaps being supported for faster input reference frequencies. Since gapped clocks usually occur on input reference frequencies above 100MHz, gap lengths of thousands of periods can be supported.

Using this configuration for a gapped clock, the PLL will continue to adjust while the normally expected gap is present, but will freeze once the expected gap length has been exceeded and alarm after twice the normal gap length has passed.

Once a LOS on any of the input clocks is detected, the appropriate internal LOS alarm will be asserted and it will remain asserted until that input clock returns and will be validated by the receipt of 8 rising clock edges on that input reference. If another error condition on the same input clock is detected during the validation time then the alarm remains asserted and the validation time starts over.

Each LOS flag may also be reflected on one of the GPIO[7:0] outputs. Changes in status of any reference can also generate an interrupt if not masked.

Holdover

8T49N286 supports a small initial holdover frequency offset for each PLL path in non-gapped clock mode. When the input clock monitor is set to support gapped clock operation, this initial holdover frequency offset is indeterminate since the desired behavior with gapped clocks is for the PLL to continue to adjust itself even if clock edges are missing. In gapped clock mode, the PLL will not enter holdover until the input is missing for at least 2 LOS monitor periods.

The holdover performance characteristics of a clock are referred as its accuracy and stability, and are characterized in terms of the fractional frequency offset. The 8T49N286 can only control the initial frequency accuracy. Longer-term accuracy and stability are determined by the accuracy and stability of the external oscillator.

When a PLL loses all valid input references, it will enter the holdover state. In fast average mode, the PLL will initially maintain its most recent frequency offset setting and then transition at a rate dictated by its selected phase-slope limit setting to a frequency offset setting that is based on historical settings. This behavior is intended to compensate for any frequency drift that may have occurred on the input reference before it was detected to be lost.

The historical holdover value will have three options:

- Return to center of tuning range within the V_{CO} band
- Instantaneous mode - the holdover frequency will use the DPLL current frequency 100msec before it entered holdover. The accuracy is shown in *Table 12*, AC Characteristics Table.
- Fast average mode - an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3dB attenuation point corresponding to a nominal period of 20 minutes. The accuracy is shown in *Table 12*, AC Characteristics Table.

When entering holdover, each PLL will set a separate internal HOLD alarm internally. This alarm may be read from internal status register, appear on the appropriate GPIO pin and/or assert the nINT output.

While a PLL is in holdover, its frequency offset is now relative to the crystal input and so the output clocks derived from that PLL will be tracing their accuracy to the local oscillator or crystal. At some point in time, depending on the stability & accuracy of that source, the clock(s) derived from that PLL will have drifted outside of the limits of the holdover state and the system will be considered to be in a free-run state. Since this borderline is defined outside the PLL and dictated by the accuracy and stability of the external local crystal or oscillator, the 8T49N286 cannot know or influence when that transition occurs. As a result, the 8T49N286 will remain in the holdover state internally.

Input to Output Clock Frequency

The 8T49N286 is designed to accept any frequency within its input range and generate eight different output frequencies that are independent from the input frequencies. The internal architecture of the device ensures that most translations will result in the exact output frequency specified. Where exact frequency translation is not possible, the frequency translation error will be minimized. Please contact IDT for configuration software or other assistance in determining if a desired configuration will be supported exactly.

Synthesizer Mode Operation

The device may also act as a frequency synthesizer with either or both PLL's generating their operating frequency from just the crystal input. By setting the SYN_MODEn register bit and setting the STATEn[1:0] field to Freerun, no input clock references are required to generate the desired output frequencies.

Loop Filter and Bandwidth

When operating in Synthesizer Mode as described above, the 8T49N286 has a fixed loop bandwidth of approximately 200kHz. When operating in all other modes, the following information applies:

The 8T49N286 uses no external components to support a range of loop bandwidths:1.40625Hz, 2.8125Hz, 5.625Hz, 11.25Hz, 22.5Hz, 45Hz, 90Hz, 180Hz or 360Hz. Each PLL shall support separate loop filter settings.

The device supports two different loop bandwidth settings for each PLL: acquisition and locked. These loop bandwidths are selected from the list of options described above. If enabled, the acquisition bandwidth is used while lock is being acquired to allow the PLL to `fast-lock'. Once locked the PLL will use the locked bandwidth setting. If the acquisition bandwidth setting is not used, the PLL will use the locked bandwidth setting at all times.

Output Dividers and Mapping to PLLs

Each integer output divider block consists of two divider stages in a series to achieve the desired total output divider ratio. The first stage divider may be set to divide by 4, 5 or 6. The second stage of the divider may be bypassed (i.e. divide-by-1) or programmed to any even divider ratio from 2 to 131,070. The total divide ratios, settings and possible output frequencies are shown in *Table 3*.

In addition, the first divider stage for the Q[4:7] outputs supports a bypass (i.e. divide-by-1) operation for some clock sources.

Table 3. Q[0:1], Q[4:7] Output Divide Ratios

1st-Stage Divide	2nd-Stage Divide	Total Divide	Minimum F_{OUT} MHz	Maximum F_{OUT} MHz
4	1	4	750	1000
5	1	5	600	800
6	1	6	500	666.7
4	2	8	375	500
5	2	10	300	400
6	2	12	250	333.3
4	4	16	187.5	250
5	4	20	150	200
6	4	24	125	166.7
...				
4	131,070	524,280	0.0057	0.0076
5	131,070	655,350	0.0046	0.0061
6	131,070	786,420	0.0038	0.0051

NOTE: Above frequency ranges for Q[4:7] apply when driven directly from PLL0 or PLL1.

Fractional Output Divider Programming (Q2, Q3 only)

For the FracN output dividers Q[2:3], the output divide ratio is given by:

Output Divide Ratio = (N.F)x2

N = Integer Part: 4, 5, ...(2^{18}-1)

F = Fractional Part: [0, 1, 2, ...(2^{28}-1)]/(2^{28})

For integer operation of these outputs dividers, N = 3 is also supported.

Output Divider Frequency Sources

Output dividers associated with the Q[0:3] outputs can take their input frequencies from either PLL0 or PLL1.

Output dividers associated with the Q[4:7] outputs can take their input frequencies from PLL0, PLL1, Q2 or Q3 output dividers, the CLK0, CLK1 or CLK2 input reference frequencies or the crystal frequency.

Output Banks

Outputs of the 8T49N286 are divided into three banks for purposes of output skew measurement.

- Q0, nQ0, Q1, nQ1
- Q4, nQ4, Q5, nQ5
- Q6, nQ6, Q7, nQ7

Output Phase Control on Switchover

There are two options on how the output phase can be controlled when the 8T49N286 enters or leaves the holdover state, or either PLL switches between input references. Phase-slope limiting or fully hitless switching (sometimes called phase build-out) may be selected. The SWMODEn bit selects which behavior is to be followed for PLLn.

If fully hitless switching is selected, then the output phase will remain unchanged under any of these conditions. Note that fully hitless switching is not supported when external loopback is being used. Fully hitless switching should not be used unless all input references are in the same clock domain. Note that use of this mode may prevent an output frequency and phase from being able to trace its alignment back to a primary reference source.

If phase-slope limiting is selected, then the output phase will adjust from its previous value until it is tracking the new condition at a rate dictated by the SLEWn[1:0] bits. Phase-slope limiting should be used if all input references are not in the same clock domain or users wish to retain traceability to a primary reference source.

Input-Output Delay Control

When using the 8T49N286 in external loopback or in a situation where input-output delay needs to be known and controlled, it is necessary to examine the exact signal path through the device. Due to the flexibility of the device, there are a large number of potential signal paths from input to output through it that depend on the desired configuration. Each of those potential paths may include or exclude logic blocks from the path and change the absolute value of the delay (Static Phase Offset or SPO) through the device. Considering the range of SPO values to cover all those potential paths would not be useful in achieving the target delays for any specific user configuration. Please contact IDT for the specific SPO value associated with a desired input-output path. Note that events such as switch-overs, entering or leaving holdover or re-configuring the signal path can result in one-time changes to the SPO due to that path re-configuration. The AC Characteristics table (*Table 12*) indicates the maximum variation in SPO that could be expected for a particular path through the device.

Output Phase Alignment

The device has a programmable output to output phase alignment for each of the eight output dividers. After power-up and the PLLs have achieved lock, the device will be in a state where the outputs are synchronized with a deterministic offset relative to each other. After synchronization, the output alignment will depend on the particular configuration of each output according to the following rules. The step size is defined as the period of the clock to that divider:

1) Only outputs derived from the same source will be aligned with each other. 'Source' means the reference selected to drive the output divider as controlled by the CLK_SELn bit for each output.

2) For integer dividers (Q[0:1], Q[4:7]) when both divider stages are active, edges are aligned. This case is used as a baseline to compare the other cases here.

3) For integer dividers where the 1st-stage divider is bypassed (only Q[4:7] support this), coarse delay adjustments can't be performed. The output phase will be one step earlier than in Case 2.

4) Fractional output dividers (Q2 or Q3) do not guarantee any specific phase on power-up or after a synchronization event.

5) Integer dividers using Q2 or Q3 as a source (Q[4:7] support this option) will be aligned to their source divider's output (Q2 or Q3).

6) Phase alignments listed above may differ by the output-output skews in *Table 12*, AC Characteristics Table.

Once the device is in operation, the outputs associated with each PLL may have their phase adjustments re-synced in one of two ways:

1) If the PLL becomes unlocked, the coarse phase adjustments will be reset and the fine phase adjustments will be re-loaded once it becomes locked again.

2) Toggling of PLLn_SYN bit may also be used to force a re-sync / re-load for outputs associated with that PLL.

The user may apply adjustments that are proportional to the period of the clock source driving each output divider. For example, if the divider associated with output Q3 is running off PLL0, which has a VCO frequency of 4GHz, then the appropriate period would be 250ps. The output phase may be adjusted in these steps across the full period of the output.

- Coarse Adjustment: all Output Dividers may have their phase adjusted in steps of the source clock period. For example a 4GHz VCO gives a step size of 250ps. The user may request an adjustment of phase of up to 31 steps using a single register write. The phase will be adjusted by lengthening the period of the output by 250ps at a time. This process will be repeated every 4 output clock periods until the full requested adjustment has been achieved. A busy signal will remain asserted in the phase delay register until the requested adjustment is complete. Then a further adjustment may be setup and triggered by toggling the trigger bit.
- Fine Adjustment: For the Fractional Output Dividers associated with the Q2 and Q3 outputs, the phase of those outputs may be further adjusted with a granularity of 1/16th of the VCO period. For example a 4GHz VCO frequency gives a granularity of 16ps. This is performed by directly writing the required offset (from the nominal rising edge position) in units of $1/16^{th}$ of the output period into a register. Then the appropriate PLLn_SYN bit must be toggled to load the new value. Note that toggling this bit will clear all Coarse Delays for all outputs associated with that PLL, so Fine Delays should be set first, before Coarse Delays. The output will then jump directly to that new offset value. For this reason, this adjustment should be made as the input is initially programmed or in high-impedance.

Each output has the capability of being inverted (180 degree phase shift).

Jitter and Wander Tolerance

The 8T49N286 can be used as a line card device and therefore is expected to tolerate the jitter and wander output of a timing card PLL (e.g. 82P33714).

Output Drivers

The Q0 to Q7 clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL, HCSL or LVDS logic levels.

The operating voltage ranges of each output is determined by its independent output power pin (V_{CCO}) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential operation and LVCMOS operation. In addition, LVCMOS output operation supports 1.8V V_{CCO}.

Each output may be enabled or disabled by register bits and/or GPIO pins configured as Output Enables. The outputs will be enabled if the register bit and the associated OE pin are both asserted (high). When disabled an output will be in a high impedance state.

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, phase alignment, voltage levels and enable / disable status apply to both the Q and nQ pins. When configured as LVCMOS, the Q and nQ outputs can be selected to be phase-aligned with each other or inverted relative to one another. Phase-aligned outputs will have increased simultaneous switching currents which can negatively affect phase noise performance and power consumption. It is recommended that use of this selection be kept to a minimum.

Power-Saving Modes

To allow the device to consume the least power possible for a given application, the following functions are included under register control:

- PLL1 may be shut down.
- Any unused output, including all output divider and phase adjustment logic, can be individually powered-off.
- Clock gating on logic that is not being used.

Status / Control Signals and Interrupts

General-Purpose I/Os and Interrupts

The 8T49N286 provides eight General Purpose Input / Output (GPIO) pins for miscellaneous status & control functions. Each GPIO may be configured as an input or an output. Each GPIO may be directly controlled from register bits or be used as a predefined function as shown in *Table 4*. Note that the default state prior to configuration being loaded from internal OTP or external EEPROM will be to set each GPIO to function as an Output Enable.

Table 4. GPIO Configuration

GPIO Pin	Configured as Input			Configured as Output	
	Fixed Function				
	Output Enable (default)	Clock Select	General Purpose	Fixed Function	General Purpose
7	OE[7]	CSEL1[1]	GPI[7]	LOS[3]	GPO[7]
6	OE[6]	CSEL0[1]	GPI[6]	LOS[2]	GPO[6]
5	OE[5]	-	GPI[5]	LOS[1]	GPO[5]
4	OE[4]	-	GPI[4]	HOLD[1]	GPO[4]
3	OE[3]	CSEL1[0]	GPI[3]	LOL[1]	GPO[3]
2	OE[2]	CSEL0[0]	GPI[2]	LOS[0]	GPO[2]
1	OE[1]	-	GPI[1]	HOLD[0]	GPO[1]
0	OE[0]	-	GPI[0]	LOL[0]	GPO[0]

If used in the Fixed Function mode of operation, the GPIO bits will reflect the real-time status of their respective status bits as shown in *Table 4*. Note that the LOL signal represents the lock status of the PLL. It does not account for the process of synchronization of the output dividers associated with that PLL. The output dividers programmed to operate from that PLL will automatically go through a re-synchronization process when the PLL locks or re-locks or if the user triggers a re-sync manually via register bit PLLn_SYN. This synchronization process may result in a period of instability on the affected outputs for a duration of up to 350ns after the re-lock (LOL de-asserts) or the PLLn_SYN bit is de-asserted.

Interrupt Functionality

Interrupt functionality includes an interrupt status flag for each of PLL Loss-of-Lock Status (LOL[1:0]), PLL Holdover Status (HOLD[1:0]) and Input Reference Status (LOS[3:0]) that is set whenever there is an alarm on any of those signals. The Status Flag will remain set until the alarm has been cleared and a '1' has been written to the Status Flag's register location or if a reset occurs. Each Status Flag will also have an Interrupt Enable bit that will determine if that Status Flag is allowed to cause the Interrupt Status to be affected (enabled) or not (disabled). All Interrupt Enable bits will be in the disabled state after reset. The Device Interrupt Status flag and nINT output pin are asserted if any of the enabled Interrupt Status flags are set.

Device Hardware Configuration

The 8T49N286 supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with one complete device configuration. If the device is set to read a configuration from an external, serial EEPROM, then the values read will overwrite the OTP-defined values.

This configuration can be over-written using the serial interface once reset is complete. Any configuration written via the programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

Device Start-up and Reset Behavior

The 8T49N286 has an internal power-up reset (POR) circuit and a Master Reset input pin nRST. If either is asserted, the device will be in the Reset State.

For highly programmable devices, it is common practice to reset the device immediately after the initial power-on sequence. IDT recommends connecting the nRST input pin to a programmable logic source for optimal functionality. It is recommended that a minimum pulse width of 10ns be used to drive the nRST input pin.

While in the reset state (nRST input asserted or POR active), the device will operate as follows:

- All registers will return to & be held in their default states as indicated in the applicable register description.
- All internal state machines will be in their reset conditions.
- The serial interface will not respond to read or write cycles.
- The GPIO signals will be configured as OE[7:0] inputs.
- All clock outputs will be disabled.
- All interrupt status and Interrupt Enable bits will be cleared, negating the nINT signal.

Upon the latter of the internal POR circuit expiring or the nRST input negating, the device will exit reset and begin self-configuration.

The device will load an initial block of its internal registers using the configuration stored in the internal One-Time Programmable (OTP) memory. Once this step is complete, the 8T49N286 will check the register settings to see if it should load the remainder of its configuration from an external I^2C EEPROM at a defined address or continue loading from OTP. See the section on I2C Boot-up Initialization Mode for details on how this is performed.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock both PLLs to the selected sources and begin operation. Once the PLLs are locked, all the outputs derived from a given PLL will be synchronized and output phase adjustments can then be applied if desired.

Serial Control Port Description

Serial Control Port Configuration Description

The device has a serial control port capable of responding as a slave in an I^2C or SPI compatible configuration, to allow access to any of the internal registers for device programming or examination of internal status. All registers are configured to have default values. See the specifics for each register for details. Selection of I^2C versus SPI protocol will be done via an input pin.

The device has the additional capability of becoming a master on the I^2C bus only for the purpose of reading its initial register configurations from a serial EEPROM on the I^2C bus. Writing of the configuration to the serial EEPROM must be performed by another device on the same I^2C bus or pre-programmed into the device prior to assembly. This capability is unavailable if SPI protocols are selected for the programming interface.

SPI Mode Operation

In a read operation (R/$\overline{W}$ bit is '1') data on SDO will be clocked out on the falling edge of SCLK.

In a write operation (R/$\overline{W}$ bit is '0'), data on SDI will be clocked in on the rising edge of SCLK.

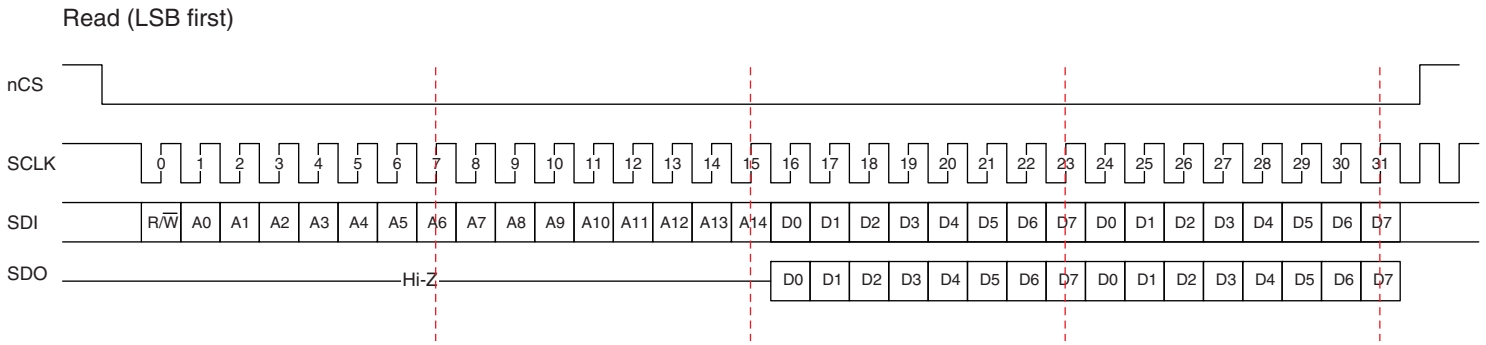


Figure 3. SPI Read Sequencing Diagram

During SPI Write operations, the user may continue to hold nCS low and provide further bytes of data for up to a total of 32,767 bytes in a single block write. Once nCS is driven high, then all data will be written into sequential registers starting at the address given.

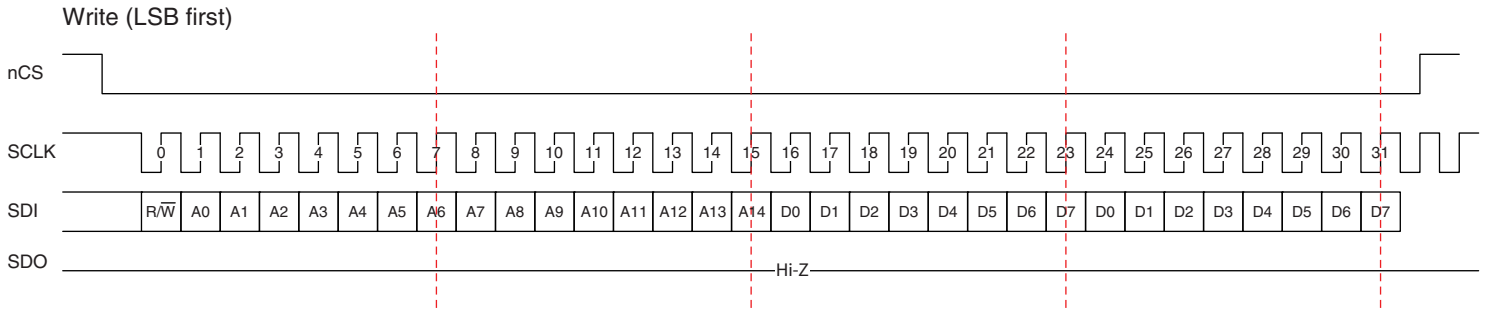


Figure 4. SPI Write Sequencing Diagram

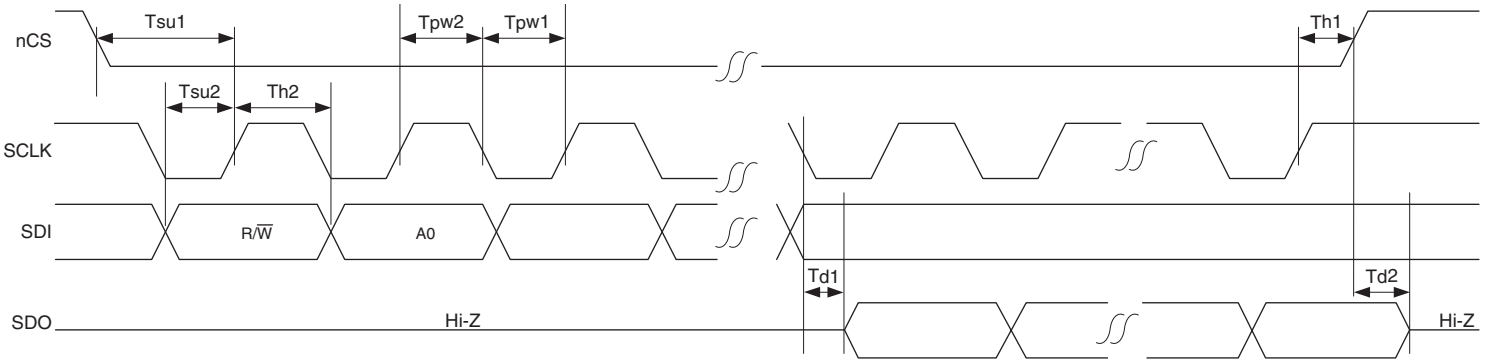


Figure 5. SPI Read/Write Timing Diagram

Table 5. Timing Characteristics in SPI Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	Internal timing parameter used to calculate SPI timing specs	T = PLL0 period * 64			ns
t_{su1}	Valid nCS to SCLK rising setup time	2T			ns
t_{su2}	Valid SDI to SCLK rising setup time	5			ns
t_{d1}	SCLK falling to valid data delay time			4T + 5	ns
t_{d2}	nCS rising edge to SDO high impedance delay time			15	ns
t_{pw1}	SCLK pulse width low	5T			ns
t_{pw2}	SCLK pulse width high	5T			ns
t_{h1}	Valid nCS after valid SCLK hold time	2T			ns
t_{h2}	Valid SDI after valid SCLK hold time	3T			ns
t_{csh}	Time between consecutive Read-Read or Read-Write accesses (nCS rising edge to nCS falling edge)	3T			ns

NOTE: Specifications guaranteed by design and characterization.

I²C Mode Operation

The I²C interface is designed to fully support v2.1 of the I²C Specification for Normal and Fast mode operation. The device acts as a slave device on the I²C bus at 100kHz or 400kHz using the address defined in the Serial Interface Control register (0006h), as modified by the S_A0 & S_A1 input pin settings. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

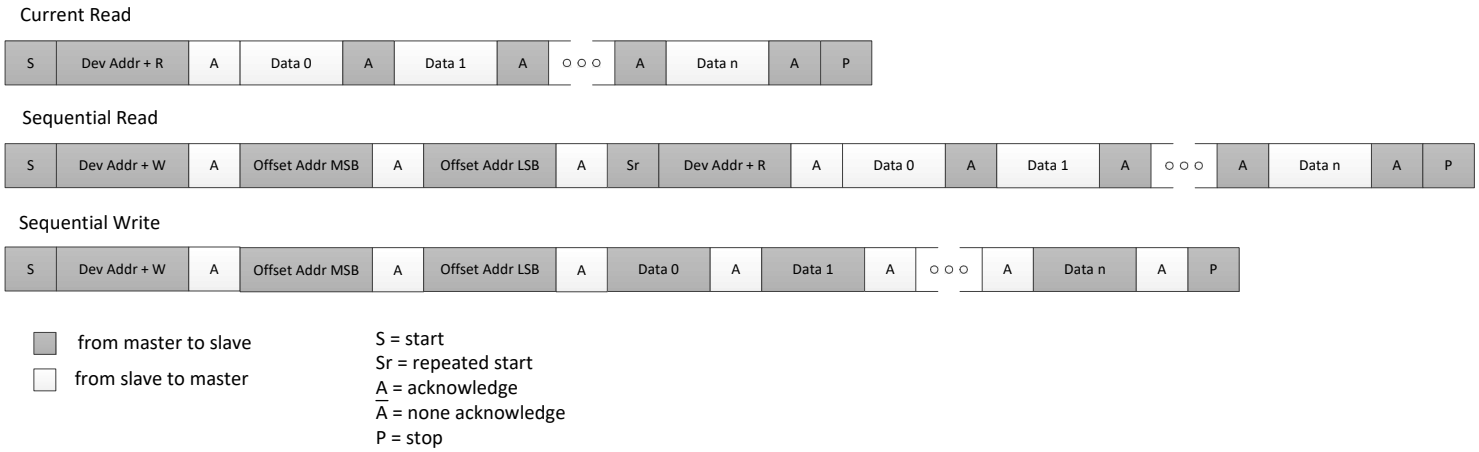


Figure 6. I²C Slave Read and Write Cycle Sequencing

I²C Master Mode

When operating in I²C mode, the 8T49N286 has the capability to become a bus master on the I²C bus for the purposes of reading its configuration from an external I²C EEPROM. Only a block read cycle will be supported.

As an I²C bus master, the 8T49N286 will support the following functions:

- 7-bit addressing mode
- Base address register for EEPROM
- Validation of the read block via CCITT-8 CRC check against value stored in last byte (E0h) of EEPROM
- Support for 100kHz and 400kHz operation with speed negotiation. If bit d0 is set at Byte address 05h in the EEPROM, this will shift from 100kHz operation to 400kHz operation.
- Support for 1- or 2-byte addressing mode
- Master arbitration with programmable number of retries
- Fixed-period cycle response timer to prevent permanently hanging the I²C bus.
- Read will abort with an alarm (BOOTFAIL) if any of the following conditions occur: Slave NACK, Arbitration Fail, Collision during Address Phase, CRC failure, Slave Response time-out

The 8T49N286 will not support the following functions:

- I²C General Call
- Slave clock stretching
- I²C Start Byte protocol
- EEPROM Chaining
- CBUS compatibility
- Responding to its own slave address when acting as a master
- Writing to external I²C devices including the external EEPROM used for booting

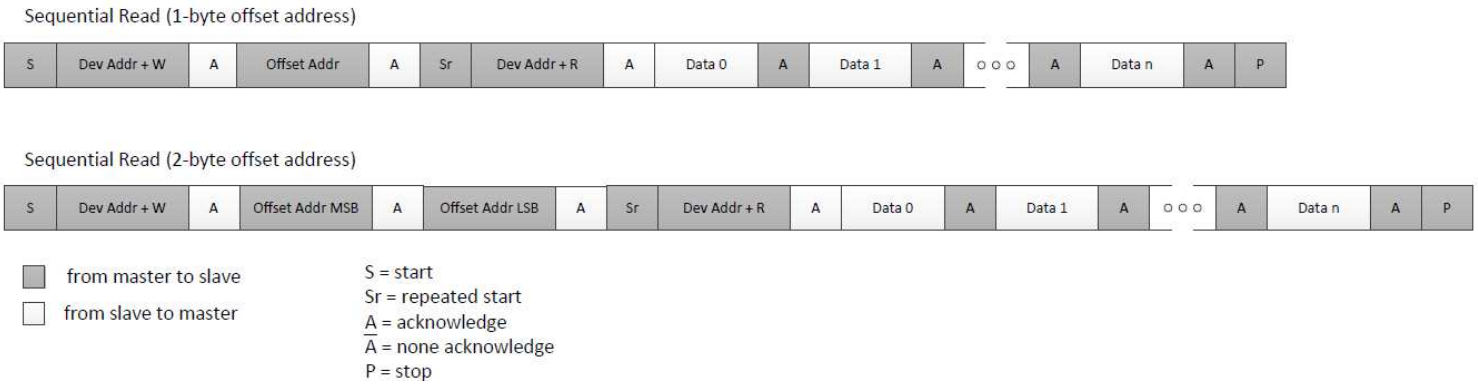


Figure 7. I²C Master Read Cycle Sequencing

I²C Boot-up Initialization Mode

If enabled (via the BOOT_EEP bit in the Startup register), once the nRST input has been de-asserted (high) and its internal power-up reset sequence has completed, the device will contend for ownership of the I²C bus to read its initial register settings from a memory location on the I²C bus. The address of that memory location is kept in non-volatile memory in the Startup register. During the boot-up process, the device will not respond to serial control port accesses. Once the initialization process is complete, the contents of any of the device's registers can be altered. It is the responsibility of the user to make any desired adjustments in initial values directly in the serial bus memory.

If a NACK is received to any of the read cycles performed by the device during the initialization process, or if the CRC does not match the one stored in address E0h of the EEPROM the process will be aborted and any uninitialized registers will remain with their default values. The BOOTFAIL bit (021Eh) in the Global Interrupt Status register will also be set in this event.

If the BOOTFAIL bit is set, then both LOL[n] indicators will be set.

Contents of the EEPROM should be as shown in *Table 6*.

Table 6. External Serial EEPROM Contents

EEPROM Offset (Hex)	Contents							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00	1	1	1	1	1	1	1	1
01	1	1	1	1	1	1	1	1
02	1	1	1	1	1	1	1	1
03	1	1	1	1	1	1	1	1
04	1	1	1	1	1	1	1	1
05	1	1	1	1	1	1	1	Serial EEPROM Speed Select 0 = 100kHz 1 = 400kHz
06	1	8T49N286 Device I²C Address [6:2]					1	1
07	0	0	0	0	0	0	0	0
08 - DF	Desired contents of Device Registers 08h - DFh							
E0	Serial EEPROM CRC							
E1 - FF	Unused							

Register Descriptions

Table 7A. Register Blocks

Register Ranges Offset (Hex)	Register Block Description
0000 - 0001	Startup Control Registers
0002 - 0005	Device ID Control Registers
0006 - 0007	Serial Interface Control Registers
0008 - 003A	Digital PLL0 Control Registers
003B - 006D	Digital PLL1 Control Registers
006E - 0076	GPIO Control Registers
0077 - 00AB	Output Clock Control Registers
00AC - 00AF	Analog PLL0 Control Registers
00B0 - 00B3	Analog PLL1 Control Registers
00B4 - 00B8	Power-Down Control Registers
00B9 - 00C6	Input Monitor Control Registers
00C7	Interrupt Enable Register
00C8 - 00CB	Digital Phase Detector Control Registers
00CC - 01FF	Reserved[1]
0200 - 0203	Interrupt Status Registers
0204	Output Phase Adjustment Status Register
0205 - 020E	Digital PLL0 Status Registers
020F - 0218	Digital PLL1 Status Registers
0219	General-Purpose Input Status Register
021A - 021F	Global Interrupt and Boot Status Register
0220 - 03FF	Reserved[1]

NOTE 1: Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7B. Startup Control Register Bit Field Locations and Descriptions

Startup Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0000	EEP_RTY[4:0]					Rsvd	nBOOT_OTP	nBOOT_EEP
0001	EEP_A15	EEP_ADDR[6:0]						

Startup Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
EEP_RTY[4:0]	R/W	00001b	Select number of times arbitration for the I^2C bus to read the serial EEPROM will be retried before being aborted. Note that this number does not include the original try.
nBOOT_OTP	R/W	NOTE 1	Internal One-Time Programmable (OTP) memory usage on power-up: 0 = Load power-up configuration from OTP 1 = Only load 1st eight bytes from OTP
nBOOT_EEP	R/W	NOTE 1	External EEPROM usage on power-up: 0 = Load power-up configuration from external serial EEPROM (overwrites OTP values) 1 = Don't use external EEPROM
EEP_A15	R/W	NOTE 1	Serial EEPROM supports 15-bit addressing mode (multiple pages).
EEP_ADDR[6:0]	R/W	NOTE 1	I^2C base address for serial EEPROM.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Please refer to the FemtoClock NG Universal Frequency Translator Ordering Product Information guide for more details.

Table 7C. Device ID Control Register Bit Field Locations and Descriptions

Device ID Register Control Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0002	REV_ID[3:0]				DEV_ID[15:12]			
0003	DEV_ID[11:4]							
0004	DEV_ID[3:0]				DASH_CODE[10:7]			
0005	DASH_CODE[6:0]							1

Device ID Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
REV_ID[3:0]	R/W	0000b	Device revision.
DEV_ID[15:0]	R/W	0604h	Device ID code.
DASH_CODE [10:0]	R/W	NOTE 1	Device Dash Code: Decimal value assigned by IDT to identify the configuration loaded at the factory. May be over-written by users at any time. Refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information* to identify major configuration parameters associated with this Dash Code value.

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Please refer to the FemtoClock NG Universal Frequency Translator Ordering Product Information guide or custom datasheet addendum for more details.

Table 7D. Serial Interface Control Register Bit Field Locations and Descriptions

Serial Interface Control Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0006	SPI_SEL	UFTADD[6:2]					UFTADD[1]	UFTADD[0]
0007	Rsvd							1

Device ID Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
SPI_SEL	R/O	0b	Select Mode for serial interface as read from the nI2C_SPI pin: 0 = I^2C 1 = SPI
UFTADD[6:2]	R/W	NOTE 1	Configurable portion of I^2C Base Address (bits 6:2) for this device.
UFTADD[1]	R/O	0b	I^2C Base Address bit 1. This address bit reflects the status of the S_A1 / SDI external input pin. See *Table 1*, Pin Descriptions.
UFTADD[0]	R/O	0b	I^2C Base Address bit 0. This address bit reflects the status of the S_A0 / nCS external input pin. See *Table 1*, Pin Descriptions.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Generic dash codes -900 through -908, -998 and-999 are available and programmed with the default I^2C address of 1111100b. Please refer to the FemtoClock NG Universal Frequency Translator Ordering Product Information guide for more details.

Table 7E. Digital PLL0 Input Control Register Bit Field Locations and Descriptions

Digital PLL0 Input Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0008	REFSEL0[2:0]			FBSEL0[2:0]			RVRT0	SWMODE0
0009	PRI0_3[1:0]		PRI0_2[1:0]		PRI0_1[1:0]		PRI0_0[1:0]	
000A	REFDIS0_3	REFDIS0_2	REFDIS0_1	REFDIS0_0	Rsvd	Rsvd	STATE0[1:0]	
000B	Rsvd			PRE0_0[20:16]				
000C	PRE0_0[15:8]							
000D	PRE0_0[7:0]							
000E	Rsvd			PRE0_1[20:16]				
000F	PRE0_1[15:8]							
0010	PRE0_1[7:0]							
0011	Rsvd			PRE0_2[20:16]				
0012	PRE0_2[15:8]							
0013	PRE0_2[7:0]							
0014	Rsvd			PRE0_3[20:16]				
0015	PRE0_3[15:8]							
0016	PRE0_3[7:0]							

Digital PLL0 Input Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
REFSEL0[2:0]	R/W	000b	Input reference selection for Digital PLL0: 000 = Automatic selection 001 = Manual selection by GPIO inputs 010 through 011 = Reserved 100 = Force selection of Input Reference 0 101 = Force selection of Input Reference 1 110 = Force selection of Input Reference 2 111 = Force selection of Input Reference 3
FBSEL0[2:0]	R/W	000b	Feedback mode selection for Digital PLL0: 000 - 011 = internal feedback divider 100 = external feedback from Input Reference 0 101 = external feedback from Input Reference 1 110 = external feedback from Input Reference 2 111 = external feedback from Input Reference 3
RVRT0	R/W	1b	Automatic switching mode for Digital PLL0: 0 = non-revertive switching 1 = revertive switching
SWMODE0	R/W	1b	Controls how Digital PLL0 adjusts output phase when switching between input references: 0 = Absorb any phase differences between old and new input references at the PLL output. Recommended for use when both input references are in the same clock domain. 1 = Limit the maximum rate of phase change at the PLL output when adjusting to a new input reference's phase/frequency using phase-slope limiting as set in the SLEWn bits. Recommended for use when the input references are not in the same clock domain.
PRI0_0[1:0]	R/W	00b	Switchover priority for Input Reference 0 when used by Digital PLL0: 00 = 1st priority 01 = 2nd priority 10 = 3rd priority 11 = 4th priority

Digital PLL0 Input Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
PRI0_1[1:0]	R/W	01b	Switchover priority for Input Reference 1 when used by Digital PLL0: 00 = 1st priority 01 = 2nd priority 10 = 3rd priority 11 = 4th priority
PRI0_2[1:0]	R/W	10b	Switchover priority for Input Reference 2 when used by Digital PLL0: 00 = 1st priority 01 = 2nd priority 10 = 3rd priority 11 = 4th priority
PRI0_3[1:0]	R/W	11b	Switchover priority for Input Reference 3 when used by Digital PLL0: 00 = 1st priority 01 = 2nd priority 10 = 3rd priority 11 = 4th priority
REFDIS0_0	R/W	0b	Input Reference 0 Switching Selection Disable for Digital PLL0: 0 = Input Reference 0 is included in the switchover sequence for Digital PLL0 1 = Input Reference 0 is not included in the switchover sequence for Digital PLL0
REFDIS0_1	R/W	0b	Input Reference 1 Switching Selection Disable for Digital PLL0: 0 = Input Reference 1 is included in the switchover sequence for Digital PLL0 1 = Input Reference 1 is not included in the switchover sequence for Digital PLL0
REFDIS0_2	R/W	0b	Input Reference 2 Switching Selection Disable for Digital PLL0: 0 = Input Reference 2 is included in the switchover sequence for Digital PLL0 1 = Input Reference 2 is not included in the switchover sequence for Digital PLL0
REFDIS0_3	R/W	0b	Input Reference 3 Switching Selection Disable for Digital PLL0: 0 = Input Reference 3 is included in the switchover sequence for Digital PLL0 1 = Input Reference 3 is not included in the switchover sequence for Digital PLL0
STATE0[1:0]	R/W	00b	Digital PLL0 State Machine Control: 00 = Run automatically 01 = Force FREERUN state - set this if in Synthesizer Mode for PLL0. 10 = Force NORMAL state 11 = Force HOLDOVER state
PRE0_0[20:0]	R/W	000000h	Pre-divider ratio for Input Reference 0 when used by Digital PLL0.
PRE0_1[20:0]	R/W	000000h	Pre-divider ratio for Input Reference 1 when used by Digital PLL0.
PRE0_2[20:0]	R/W	000000h	Pre-divider ratio for Input Reference 2 when used by Digital PLL0.
PRE0_3[20:0]	R/W	000000h	Pre-divider ratio for Input Reference 3 when used by Digital PLL0.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7F. Digital PLL0 Feedback Control Register Bit Field Locations and Descriptions

Digital PLL0 Feedback Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0017	M1_0_0[23:16]							
0018	M1_0_0[15:8]							
0019	M1_0_0[7:0]							
001A	M1_0_1[23:16]							
001B	M1_0_1[15:8]							
001C	M1_0_1[7:0]							
001D	M1_0_2[23:16]							
001E	M1_0_2[15:8]							
001F	M1_0_2[7:0]							
0020	M1_0_3[23:16]							
0021	M1_0_3[15:8]							
0022	M1_0_3[7:0]							
0023	LCKBW0[3:0]				ACQBW0[3:0]			
0024	LCKDAMP0[2:0]			ACQDAMP0[2:0]			PLLGAIN0[1:0]	
0025	Rsvd			Rsvd	Rsvd			Rsvd
0026	Rsvd							
0027	Rsvd							
0028	Rsvd							Rsvd
0029	Rsvd							
002A	Rsvd							
002B	FFh							
002C	FFh							
002D	FFh							
002E	FFh							
002F	SLEW0[1:0]		Rsvd	HOLD0[1:0]		Rsvd	HOLDAVG0	FASTLCK0
0030	LOCK0[7:0]							
0031	Rsvd							DSM_INT0[8]
0032	DSM_INT0[7:0]							
0033	Rsvd			DSMFRAC0[20:16]				
0034	DSMFRAC0[15:8]							
0035	DSMFRAC0[7:0]							
0036	Rsvd							
0037	01h							
0038	Rsvd							
0039	Rsvd							
003A	DSM_ORD0[1:0]		DCXOGAIN0[1:0]		Rsvd	DITHGAIN0[2:0]		

Digital PLL0 Feedback Configuration Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
M1_0_0[23:0]	R/W	070000h	M1 Feedback divider ratio for Input Reference 0 when used by Digital PLL0.
M1_0_1[23:0]	R/W	070000h	M1 Feedback divider ratio for Input Reference 1 when used by Digital PLL0.
M1_0_2[23:0]	R/W	070000h	M1 Feedback divider ratio for Input Reference 2 when used by Digital PLL0.
M1_0_3[23:0]	R/W	070000h	M1 Feedback divider ratio for Input Reference 3 when used by Digital PLL0.
LCKBW0[3:0]	R/W	0111b	Digital PLL0 Loop Bandwidth while locked: 0000 = Reserved 0001 = Reserved 0010 = Reserved 0011 = 1.40625Hz 0100 = 2.8125Hz 0101 = 5.625Hz 0110 = 11.25Hz 0111 = 22.5Hz 1000 = 45Hz 1001 = 90Hz 1010 = 180Hz 1011 = 360Hz 1100 through 1111 = Reserved
ACQBW0[3:0]	R/W	0111b	Digital PLL0 Loop Bandwidth while in acquisition (not-locked): 0000 = Reserved 0001 = Reserved 0010 = Reserved 0011 = 1.40625Hz 0100 = 2.8125Hz 0101 = 5.625Hz 0110 = 11.25Hz 0111 = 22.5Hz 1000 = 45Hz 1001 = 90Hz 1010 = 180Hz 1011 = 360Hz 1100 through 1111 = Reserved
LCKDAMP0[2:0]	R/W	011b	Damping factor for Digital PLL0 while locked: 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved
ACQDAMP0[2:0]	R/W	011b	Damping factor for Digital PLL0 while in acquisition (not locked): 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved

Digital PLL0 Feedback Configuration Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
PLLGAIN0[1:0]	R/W	01b	Digital Loop Filter Gain Settings for Digital PLL0: 00 = 0.5 01 = 1 10 = 1.5 11 = 2
SLEW0[1:0]	R/W	00b	Phase-slope control for Digital PLL0: 00 = no limit - controlled by loop bandwidth of Digital PLL0, NOTE1. 01 = 83 µsec/sec 10 = 13 µsec/sec 11 = Reserved
HOLD0[1:0]	R/W	00b	Holdover Averaging mode selection for Digital PLL0: 00 = Instantaneous mode - uses historical value 100ms prior to entering holdover 01 = Fast Average Mode 10 = Reserved 11 = Set VCO control voltage to $V_{CC}/2$
HOLDAVG0	R/W	0b	Holdover Averaging Enable for Digital PLL0: 0 = Holdover averaging disabled 1 = Holdover averaging enabled as defined in HOLD0[1:0]
FASTLCK0	R/W	0b	Enables Fast Lock operation for Digital PLL0: 0 = Normal locking using LCKBW0 & LCKDAMP0 fields in all cases 1 = Fast Lock mode using ACQBW0 & ACQDAMP0 when not phase locked and LCKBW0 & LCKDAMP0 once phase locked
LOCK0[7:0]	R/W	3Fh	Lock window size for Digital PLL0. Unsigned 2's complement binary number in steps of 2.5ns, giving a total range of 640ns. Do not program to 0.
DSM_INT0[8:0]	R/W	02Dh	Integer portion of the Delta-Sigma Modulator value. Do not set higher than FFh. This implies that for crystal frequencies lower than 16MHz, the doubler circuit must be enabled.
DSMFRAC0[20:0]	R/W	000000h	Fractional portion of Delta-Sigma Modulator value. Divide this number by 2^{21} to determine the actual fraction.
DSM_ORD0[1:0]	R/W	11b	Delta-Sigma Modulator Order for Digital PLL0: 00 = Delta-Sigma Modulator disabled 01 = 1st order modulation 10 = 2nd order modulation 11 = 3rd order modulation
DCXOGAIN0[1:0]	R/W	01b	Multiplier applied to instantaneous frequency error before it is applied to the Digitally Controlled Oscillator in Digital PLL0: 00 = 0.5 01 = 1 10 = 2 11 = 4
DITHGAIN0[2:0]	R/W	000b	Dither Gain setting for Digital PLL0: 000 = no dither 001 = Least Significant Bit (LSB) only 010 = 2 LSBs 011 = 4 LSBs 100 = 8 LSBs 101 = 16 LSBs 110 = 32 LSBs 111 = 64 LSBs
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

NOTE 1: Settings other than "00" may result in a significant increase in initial lock time.

Table 7G. Digital PLL1 Input Control Register Bit Field Locations and Descriptions

Digital PLL1 Input Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
003B	REFSEL1[2:0]			FBSEL1[2:0]			RVRT1	SWMODE1
003C	PRI1_3[1:0]		PRI1_2[1:0]		PRI1_1[1:0]		PRI1_0[1:0]	
003D	REFDIS1_3	REFDIS1_2	REFDIS1_1	REFDIS1_0	Rsvd	Rsvd	STATE1[1:0]	
003E	Rsvd			PRE1_0[20:16]				
003F	PRE1_0[15:8]							
0040	PRE1_0[7:0]							
0041	Rsvd			PRE1_1[20:16]				
0042	PRE1_1[15:8]							
0043	PRE1_1[7:0]							
0044	Rsvd			PRE1_2[20:16]				
0045	PRE1_2[15:8]							
0046	PRE1_2[7:0]							
0047	Rsvd			PRE1_3[20:16]				
0048	PRE1_3[15:8]							
0049	PRE1_3[7:0]							

Digital PLL1 Input Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
REFSEL1[2:0]	R/W	000b	Input reference selection for Digital PLL1: 000 = Automatic selection 001 = Manual selection by GPIO inputs 010 through 011 = Reserved 100 = Force selection of Input Reference 0 101 = Force selection of Input Reference 1 110 = Force selection of Input Reference 2 111 = Force selection of Input Reference 3
FBSEL1[2:0]	R/W	000b	Feedback mode selection for Digital PLL1: 000 through 011 = internal feedback divider 100 = external feedback from Input Reference 0 101 = external feedback from Input Reference 1 110 = external feedback from Input Reference 2 111 = external feedback from Input Reference 3
RVRT1	R/W	1b	Automatic switching mode for Digital PLL1: 0 = non-revertive switching 1 = revertive switching
SWMODE1	R/W	1b	Controls how Digital PLL1 adjusts output phase when switching between input references: 0 = Absorb any phase differences between old and new input references at the PLL output. Recommended for use when both input references are in the same clock domain. 1 = Limit the maximum rate of phase change at the PLL output when adjusting to a new input reference's phase/frequency using phase-slope limiting as set in the SLEWn bits. Recommended for use when the input references are not in the same clock domain.
PRI1_0[1:0]	R/W	00b	Switchover priority for Input Reference 0 when used by Digital PLL1: 00 = 1st priority 01 = 2nd priority 10 = 3rd priority 11 = 4th priority