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Description

The 8V79S680 is a fully integrated, clock and SYSREF signal fanout buffer for JESD204B applications. It is designed as a high-performance clock and converter synchronization solution for wireless basestation radio equipment boards with JESD204B subclass 0, 1, and 2 compliance. The main function of the device is the distribution and fanout of high-frequency clocks and low-frequency system reference signals generated by a JESB204B clock generator such as the IDT 8V19N480, extending its fanout capabilities and providing additional phase-delay.

The 8V79S680 is optimized to deliver very low phase noise clocks and precise, phase-adjustable SYSREF synchronization signals as required in GSM, WCDMA, LTE, and LTE-A radio board implementations. Low-skew outputs, low device-to-device skew characteristics and fast output rise/fall times help the system design to achieve deterministic clock and SYSREF phase relationship across devices.

The device distributes the input clock (CLK) and JESD204B SYSREF signals (REF) to four fanout channels. In each channel, both input clock and SYSREF signals are fanned-out to multiple clock (QCLK) and SYSREF (QREF) outputs. Clock signals can be frequency-divided in each channel. Configurable phase-delay circuits are available for both clock and SYSREF signals. The propagation delays in all signal paths are fully deterministic to support fixed phase relationships between clock and SYSREF signals within one device. The clock divider can be bypassed for low-latency clock paths. The 8V79S680 facilitates synchronization between frequency dividers within the device and across multiple devices, removing phase ambiguity introduced in dividers between power and configuration cycles.

Each channel supports clock frequencies up to 3GHz. In an alternative configuration (e.g., JESD204B subclass 0 and 2) the SYSREF (QREF) outputs can be configured as regular clock outputs adding additional clock fanout to the device.

All outputs are very flexible in amplitude configuration, output signal termination, and allow both DC and AC coupling. Outputs can be disabled and powered down when not used. The SYSREF output pre-bias feature supports prevention of power-on glitches and enables AC-coupling of the system synchronization signals.

The device is configured through a 3-wire SPI serial interface. The device is packaged in a lead-free (RoHS 6) 64-lead VFQFN package. The extended temperature range supports wireless infrastructure, telecommunication, and networking end equipment requirements. The 8V79S680 is a member of the high-performance clock family from IDT.

Typical Applications

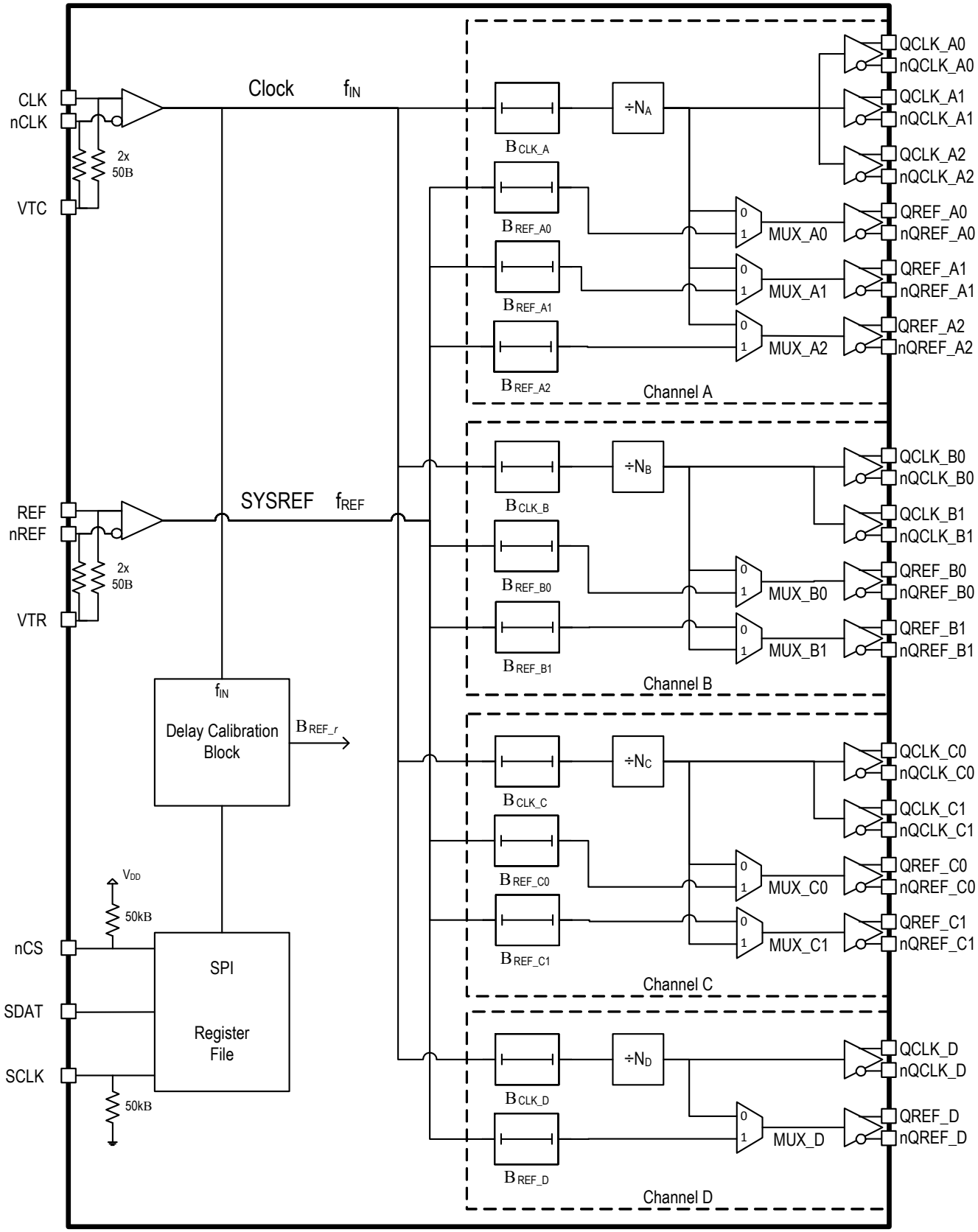
- JESD204B low phase noise clock and SYSREF signal distribution
- Supports JESD204 subclass 0, 1 and 2
- Clock distribution device for jitter-sensitive ADC and DAC circuits
- Wireless infrastructure
- Radar and imaging
- Instrumentation and medical

Features

- Supports high-speed, low phase noise converter clocks
- Distribution, fanout, phase-delay of clock and SYSREF signals
- Very low output noise floor: -158.8dBc/Hz noise floor (245.76MHz)
- Supports clock frequencies up to 3GHz, including clock output frequencies of 983.04MHz, 491.52MHz, 245.76MHz, and 122.88MHz
- Four output channels with a total of 16 differential outputs, organized in:
  - 8 dedicated clock outputs
  - 8 outputs configurable as SYSREF outputs with individual phase delay stages, or configurable as additional clock outputs
- Each channel contains:
  - frequency dividers: ÷1, ÷2, ÷4, ÷6, ÷8, ÷12, ÷16
  - clock phase delay circuits
- Clock phase delay circuits
  - Clock: delay unit is the clock period; 256 steps
  - SYSREF: Configurable precision phase delay circuits: 8 steps of 131ps, 262ps, 393ps, or 524ps
- Flexible differential outputs:
  - LVDS/LVPECL configurable
  - Amplitude configurable
  - Power-down modes for unused outputs
  - Supports DC and AC coupling
  - QREF (SYSREF) output pre-bias feature to prevent glitches when turning output on or off
- Supply voltage:
  - 3.3V core and signal I/O
  - 1.8V Digital control SPI I/O (3.3V-tolerant inputs)
- 64-VFQFN-P package (9 x 9 x 0.85mm)
- Ambient temperature range: -40°C to +85°C

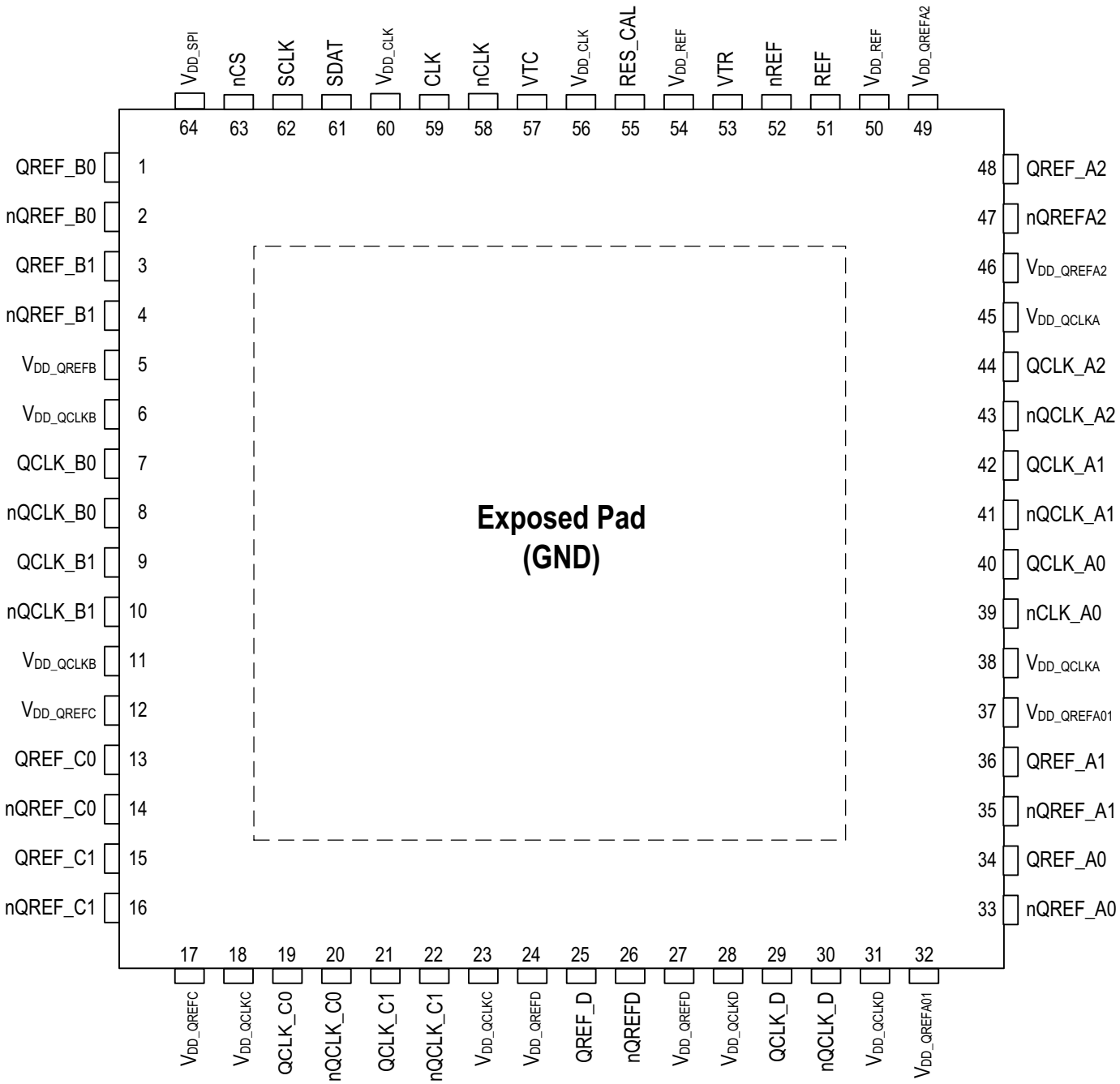
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments 9mmx9mmx0.85mm 64-VFQFN-P Package (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type[a]		Description
1, 2	QREF_B0, nQREF_B0	Output		Differential SYSREF/clock output QREF_B0. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
3, 4	QREF_B1, nQREF_B1	Output		Differential SYSREF/clock output QREF_B1. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
5	V_{DD_QREFB}	Power		Positive supply voltage (3.3V) for the QREF_B[1:0] outputs.
6	V_{DD_QCLKB}	Power		Positive supply voltage (3.3V) for the QCLK_B[1:0] outputs.
7, 8	QCLK_B0, nQCLK_B0	Output		Differential clock output QCLK_B0. Configurable LVPECL/LVDS style and amplitude.
9, 10	QCLK_B1, nQCLK_B1	Output		Differential clock output QCLK_B1. Configurable LVPECL/LVDS style and amplitude.
11	V_{DD_QCLKB}	Power		Positive supply voltage (3.3V) for the QCLK_B[1:0] outputs.
12	V_{DD_QREFC}	Power		Positive supply voltage (3.3V) for the QREF_C[1:0] outputs.
13, 14	QREF_C0, nQREF_C0	Output		Differential SYSREF/clock output QREF_C0. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
15, 16	QREF_C1, nQREF_C1	Output		Differential SYSREF/clock output QREF_C1. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
17	V_{DD_QREFC}	Power		Positive supply voltage (3.3V) for the QREF_C[1:0] outputs.
18	V_{DD_QCLKC}	Power		Positive supply voltage (3.3V) for the QCLK_C[1:0] outputs.
19, 20	QCLK_C0, nQCLK_C0	Output		Differential clock output QCLK_C0. Configurable LVPECL/LVDS style and amplitude.
21, 22	QCLK_C1, nQCLK_C1	Output		Differential clock output QCLK_C1. Configurable LVPECL/LVDS style and amplitude.
23	V_{DD_QCLKC}	Power		Positive supply voltage (3.3V) for the QCLK_C[1:0] outputs.
24	V_{DD_QREFD}	Power		Positive supply voltage (3.3V) for the QREF_D outputs.
25, 26	QREF_D, nQREF_D	Output		Differential SYSREF/clock output QREF_D. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
27	V_{DD_QREFD}	Power		Positive supply voltage (3.3V) for the QREF_D outputs.
28	V_{DD_QCLKD}	Power		Positive supply voltage (3.3V) for the QCLK_D outputs.
29, 30	QCLK_D, nQCLK_D	Output		Differential clock output QCLK_D. Configurable LVPECL/LVDS style and amplitude.
31	V_{DD_QCLKD}	Power		Positive supply voltage (3.3V) for the QCLK_D outputs.
32	$V_{DD\_QREFA01}$	Power		Positive supply voltage (3.3V) for the QREF_A[1:0] outputs.
33, 34	nQREF_A0, QREF_A0	Output		Differential SYSREF/clock output QREF_A0. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
35, 36	nQREF_A1, QREF_A1	Output		Differential SYSREF/clock output QREF_A1. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
37	$V_{DD\_QREFA01}$	Power		Positive supply voltage (3.3V) for the QREF_A[1:0] outputs.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type[a]		Description
38	V_{DD_QCLKA}	Power		Positive supply voltage (3.3V) for the QCLK_A[2:0] outputs.
39, 40	nQCLK_A0, QCLK_A0	Output		Differential clock output QCLK_A0. Configurable LVPECL/LVDS style and amplitude.
41, 42	nQCLK_A1, QCLK_A1	Output		Differential clock output QCLK_A1. Configurable LVPECL/LVDS style and amplitude.
43, 44	nQCLK_A2, QCLK_A2	Output		Differential clock output QCLK_A2. Configurable LVPECL/LVDS style and amplitude.
45	V_{DD_QCLKA}	Power		Positive supply voltage (3.3V) for the QCLK_A[2:0] outputs.
46	V_{DD_QREFA2}	Power		Positive supply voltage (3.3V) for the QREF_A2 output.
47, 48	nQREF_A2, QREF_A2	Output		Differential SYSREF/clock output QREF_A2. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
49	V_{DD_QREFA2}	Power		Positive supply voltage (3.3V) for the QREF_A2 output.
50	V_{DD_REF}	Power		Positive supply voltage (3.3V) for the differential SYSREF input REF, nREF
51, 52	REF, nREF	Input		SYSREF inverting and non-inverting differential input. Compatible with LVPECL and LVDS signals. REF and nREF are internally 50Ω terminated to the VTR pin
53	VTR	–		Internal termination for the differential clock input REF, nREF. Both REF and nREF inputs are internally terminated 50Ω to this pin. See input termination information in Application Information.
54	V_{DD_REF}	Power		Positive supply voltage (3.3V) for the differential SYSREF input REF, nREF
55	RES_CAL	Analog		Connect a 2.8 kΩ (1%) resistor to GND for output current calibration.
56	V_{DD_CLK}	Power		Positive supply voltage (3.3V) for the differential device clock input CLK, nCLK.
57	VTC	–		Internal termination for the differential clock input CLK, nCLK. Both CLK and nCLK inputs are internally 50Ω terminated to the VTR pin. See input termination information in Application Information.
58, 59	nCLK, CLK	Input		Device clock inverting and non-inverting differential clock input. Compatible with LVPECL and LVDS signals. CLK and nCLK are internally terminated to VTC through 50Ω.
60	V_{DD_CLK}	Power		Positive supply voltage (3.3V) for the differential device clock input CLK, nCLK.
61	SDAT	Input/ Output		Serial Control Port SPI Mode Data Input and Output. 1.8V LVCMOS/LVTTL interface levels. 3.3V tolerant when input.
62	SCLK	Input	PD	Serial Control Port SPI Mode Clock Input. 1.8V LVCMOS/LVTTL interface levels. 3.3V-tolerant when input.
63	nCS	Input	PU	Serial Control Port SPI Chip Select Input. 1.8V LVCMOS/LVTTL interface levels and 3.3V tolerant.
64	V_{DD_SPI}	Power		Positive supply voltage (3.3V) for the SPI interface.
Exposed Pad (EP)	GND	Power		Ground supply voltage (GND) and ground return path. Connect to board GND (0V).

[a] Internal pull-up (PU) and pull-down (PD) resistors are indicated in parentheses (see Table 22 for values).

Principles of Operation

Overview

The 8V79S680 is a JESD204B Fanout Buffer with Configurable Phase Delay. The device supports the division, phase-delay and distribution of high-frequency clocks (input: CLK, nCLK) and the fanout and phase-delay of low-frequency synchronization (SYSREF) signals (input: REF/nREF). Clock and SYSREF signal paths are independent and are organized in channels, with each channel consisting of several clock and SYSREF outputs. Outputs are configurable with support for LVPECL, LVDS and four amplitude settings. Individual channels and unused circuit blocks support a powered-down state for reduced power consumption operation. The register map, accessible through a SPI interface with read-back capability controls the main device settings.

Signal Flow

The device offers four channels with the names A, B, C and D. Each channel supports individual frequency-division, phase-delay and fan-out functions of the input clock to a total of eight QCLK_y clock outputs; each channel also distributes the SYSREF input signal to multiple QREF_r outputs with individual per-output phase delay capability.

The central clock distribution ensures low skew clock outputs within each channel; outputs are synchronous across channels (independent on the divider setting) on the incident rising clock edge for all outputs with equal phase delay settings.

SYSREF output are synchronous with each other for equal phase-delay settings. QCLK_y and QREF_r outputs will be phase-locked to each other if the CLK and REF inputs are phase-locked. The phase-delay capability in each signal path can be used to establish repeatable and deterministic clock to SYSREF phase relationships at the outputs.

The CLK and QREF signal paths are optimized for channel isolation. allowing high-speed clocks of 983.04MHz, 1474.56MHz or 1966.08MHz (up to 3GHz) and lower-speed SYSREF signals at e.g. 7.68MHz or 9.6MHz with a minimum of signal crosstalk and spurious signals.

Clock Channel Divider

Each of the four independent frequency dividers N_A-N_D can be individually set to the divider values ÷1, ÷2, ÷4, ÷6, ÷8, ÷12, ÷16. The dividers are synchronous and have an equal propagation delay on the incident edge. See Table 2 for the supported frequency divider settings.

Table 2. N_{A-D} Frequency Divider Settings

N_{A-D}	Clock Divider
000	÷1 Divider bypass and powered down
001	÷2
010	÷4
011	÷6
100	÷8
101	÷12
110	÷16
111	Not defined

Phase Delay

Output phase delay is independently supported on each clock channel and each SYSREF output. The delay unit of the clock channel phase-delay circuits Φ_{CLK_x} is a function of the frequency f_{IN} applied to CLK input: $1 \div f_{IN}$.

The delay unit of the SYSREF phase-delay circuits Φ_{REF_r} is a function of an internal oscillator frequency f_{DCO} and the DLC multiplier setting. The oscillator is fully self-contained and located in delay calibration block (DCB). At startup, this oscillator is calibrated with the input frequency f_{IN} as reference. After the calibration, the oscillator is turned-off to save power and to eliminate noise. See Table 3 for details on the delay unit, number of available steps and the delay range.

Table 3. Delay Circuit Characteristics

Delay Circuit	Unit	Steps	Range
Clock channel Φ_{CLK_x}	$1 \div f_{IN}$ 1.017ns at f_{IN} = 983.04MHz	256	$256 \div f_{IN}$ [a] 0 to 259.3ns at f_{IN} = 983.04MHz
SYSREF Φ_{REF_r}	T_{DCB}[b] DLC = 0: 131ps DLC = 1: 262ps DLC = 2: 393ps DLC = 3: 524ps	8	$0...7 * T_{DCB}$[c] DLC = 0: 0 to 0.917ns DLC = 1: 0 to 1.834ns DLC = 2: 0 to 2.751ns DLC = 3: 0 to 3.668ns

[a] At f_{IN} = 983.04MHz, the clock channel delay range is equal to 260.416ns and encompasses 32 periods of a 122.88MHz clock signal.

[b] $T_{DCB} \sim DLC \div (8 \cdot f_{DCO})$. f_{DCO} = 983.04MHz. DLC = 1, 2, 3 or 4.

[c] SYSREF phase delay supports ≥8 delay stops within one input reference period for f_{IN} = 254.76MHz to f_{IN} = 983.04MHz.

Delay Calibration Block (DCB)

The DCB sets the *SYSREF* delay unit by providing a reference signal to the QREF_*r* delay circuits. Figure 3 shows the functional diagram. The DCB requires configuration and calibration. Verification of the calibration is optional.

Description. The DCB consists of an internal DCO running at f_{DCO} = 983.04±20MHz, three frequency dividers P_{DCB}, M_{DCB} and N_{DCB} and a digital hold circuit. The DCB input frequency is the device input frequency f_{IN} at the differential CLK, nCLK input. The input frequency acts as a reference to lock the oscillator to a stable and known frequency.

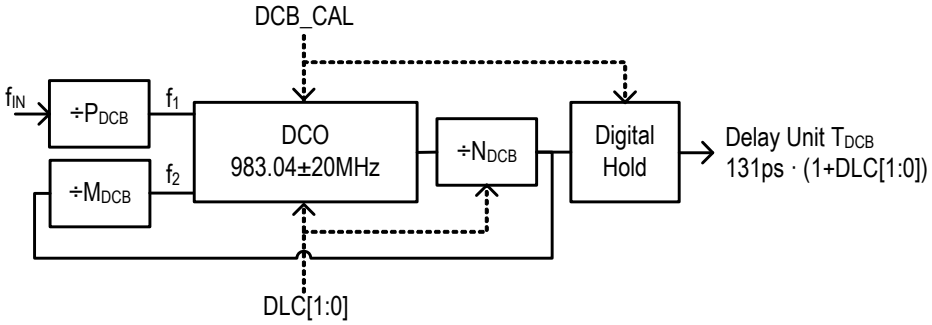
The output of the DCB is the effective delay unit T_{DCB} which is approx. one eighth of the oscillator period multiplied by the DLC multiplier. The DLC multiplier extends the delay unit by a factor of 1, 2, 3 or 4. For instance, at a DCO frequency of 983.04MHz, DLC = 1 sets the SYSREF delay unit to 131ps; DLC = 2 sets the delay unit to 262ps, etc.

Configuration. Select a desired delay unit and corresponding DLC multiplier from Table 4. DLC[1:0] also sets the N_{DCB} divider. Then, find a P_{DCB} and M_{DCB} divider configuration to locate the oscillator frequency into the range of f_{DCO} = 983.04MHz according to the formula in Figure 3. The DCO lock condition is $f_1 = f_2$ while both f_1 and f_2 must be lower than 200MHz. For instance, if f_{IN} = 245.76MHz and the smallest possible SYSREF delay unit is desired, set DLC = 1 (DLC[1:0] = 00; also sets N_{DCB} = ÷1). Then, set P_{DCB} = ÷24 and M_{DCB} = ÷96. As a result, $f_1 = f_2$ = 10.24MHz, f_{DCO} = 983.04MHz. This example configuration results in a delay unit of measured: 131ps. Figure 5 shows more configuration examples.

Calibration. Calibration requires a valid DCB configuration with the DCO locking to an input frequency. Setting DCB_CAL = 1 starts an automatic calibration. At the end, the DCB_CAL bit will clear, the delay unit value is stored digitally and the DCO, P_{DCB}, M_{DCB} and N_{DCB} frequency dividers turn off. The QREF_r delay circuits now use the stored constant delay unit. The delay unit remains digitally stored until the next power cycle. The DCB calibration must run once as part of the device startup procedure and must be re-run after each input frequency or DCB configuration change.

Verification. Verify a successful calibration by reading the DAC_CODE value. 0 < DAC_CODE< 32767 indicates a successful calibration. If DAC_CODE = 0 or DAC_CODE = 32767, the DCB calibration should be re-run with an alternative P_{DCB}, M_{DCB} setting while maintaining the desired $M_{DCB} \cdot N_{DCB}/P_{DCB}$ ratio for locking the DCO to the input frequency.

Figure 3. DCB Functional Diagram



$$\frac{f_{IN}}{P_{DCB}} = \frac{f_{DCO}}{M_{DCB} \cdot N_{DCB}}$$

$$f_{DCO} = 983MHz \pm 20MHz$$

Table 4. DCB Delay Unit at f_{DCO} = 983.04MHz

T_{DCB} Delay Unit (ps)	DLC		N_{DCB}
	DLC[1:0] Setting	Numeric Value	
131	00	1	1
262	01	2	2
393	10	3	3
524	11	4	4

Table 5. DCB Divider Configuration Examples[a]

f_{IN} (MHz)	T_{DCB} Delay Unit in ps	DLC	P_{DCB}	M_{DCB}
245.76	131	1	24	96
	262	2	24	48
	393	3	24	32
	524	4	24	24
491.52	131	1	48	96
	262	2	48	48
	393	3	48	32
	524	4	48	24
983.04	131	1	96	96
	262	2	96	48
	393	3	96	32
	524	4	96	24

[a] f_{DCO} = 983.04MHz.

QCLK to SYSREF Phase Alignment

To achieve an output phase alignment between the QCLK_*y* clock and the QREF_*r* SYSREF outputs, the CLK and REF input signals must be phase aligned or have a known, deterministic phase relationship. Figure 4 shows an example output phase alignment for aligned clock and SYREF inputs. The closest (smallest phase error) output alignment is achieved by setting the clock phase delay register Φ_{QCLK_Y} to 0x00 (clock) and the SYSREF phase delay register Φ_{QCLK_Y} to 0x04. With a SYSREF phase delay setting of 0x03 or less, the QREF_*r* output phase is in advance of the QCLK_y phase, which is applicable in JESD204B application. Phase delay settings and propagation delays are independent on the clock and SYSREF frequencies. Table 6 shows recommended phase delay setting several device configurations.

Figure 4. QCLK to QREF Phase Alignment

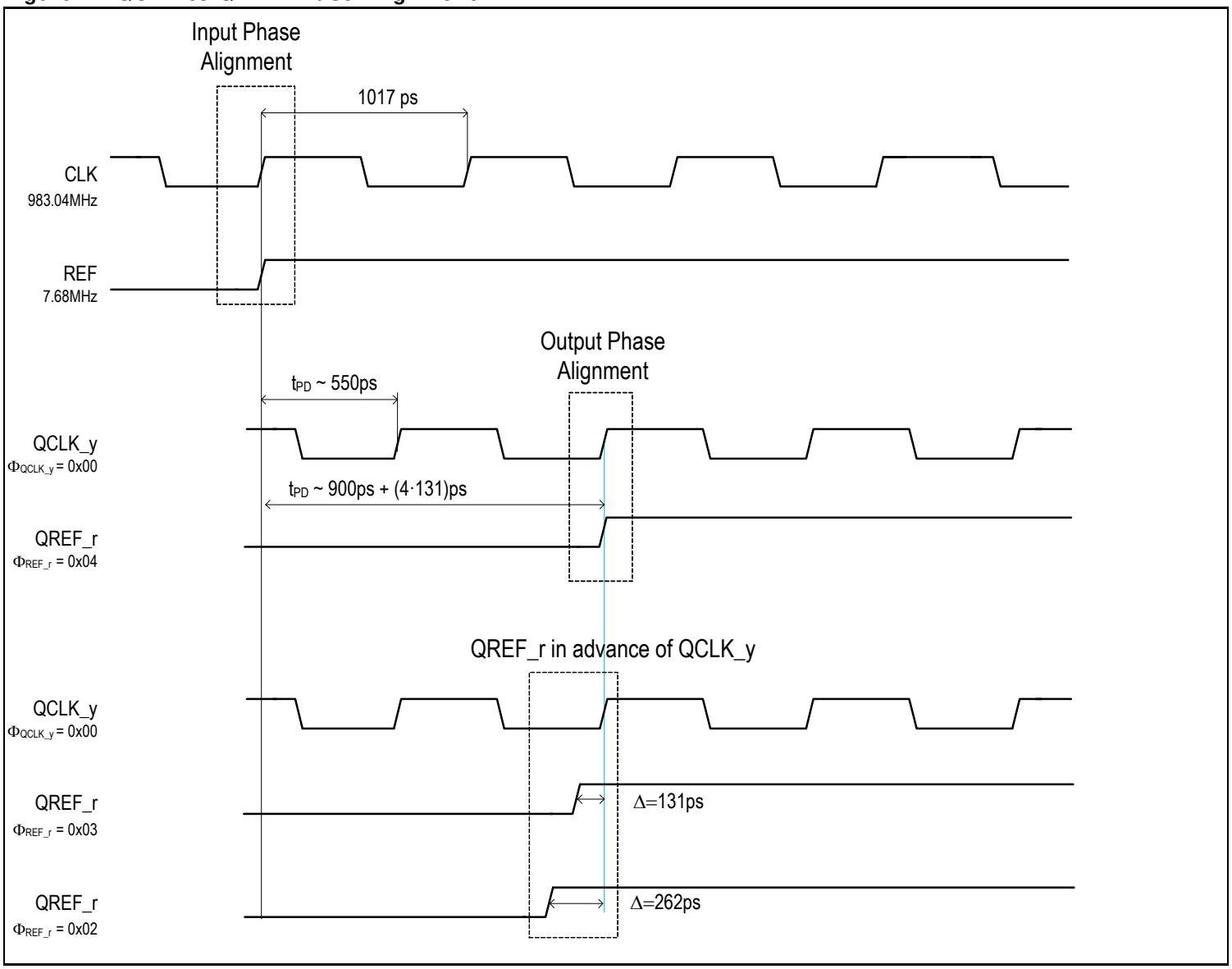


Table 6. Recommended Delay Settings for Closest Clock-SYSREF Output Phase Alignment[a]

Divider Configuration	ΦCLK_y	ΦREF_r
N = ÷1	0x00	0x04

[a] QCLK and QREF outputs are aligned on the incident edge.

Differential Outputs

Table 7. Output Features

Output	Style	Ampl.[a]	Disable	Power Down	DC Bias	Termination
QCLK_y[b], QREF_r[c] (Clock)	LVPECL	250-1000mV 4 steps	Yes	Yes	–	50Ω to V_T[d]
	LVDS					100Ω differential[e] [f]
QREF_r (SYSREF)	LVPECL	250-1000mV 4 steps	Yes	Yes	–	50Ω to V_T[d]
	LVDS				Yes[g]	100Ω differential[e] [f]

[a] Amplitudes are measured single-ended. Differential amplitudes supported are 500mV, 1000mV, 1500mV and 2000mV.

[b] y = A0, A1, A2, B0, B1, C0, C1 and D.

[c] r = A0, A1, A2, B0, B1, C0, C1 and D.

[d] $V_T = V_{DD\_V} – 1.5V$ (250mV amplitude setting), $V_{DD\_V} – 1.75V$ (500mV amplitude setting), $V_{DD\_V} – 2.0V$ (750mV amplitude setting), $V_{DD\_V} – 2.25V$ (1000mV amplitude setting).

[e] AC coupling and DC coupling supported.

[f] See Application Information for output termination information.

[g] In JESD204B applications, it is recommended to use QREF_r (SYSREF) outputs configured to LVDS and 500mV amplitude. AC-coupling and DC-coupling is supported.

Table 8. Individual Clock Output (QCLK_y) Settings[a]

PD	STYLE	EN	A[1:0]	Output Power	Termination[b]	State	Amplitude (mV)
1	X	X	X	Off	100Ω differential (LVDS) or no termination	Off	X
0	0	0	XX	On	100Ω differential (LVDS)	Disable[c]	X
		1	00			Enable	250
			01				500
			10				750
			11				1000
	1	0	XX		50Ω to V_T (LVPECL)	Disable	X
		1	00			Enable	250
			01				500
			10				750
			11				1000

[a] Applicable to clock outputs: QCLK_*y* and QREF_*r* outputs in clock mode (MUX_*r* = 0).

[b] See Application Information for output termination information.

[c] Differential output is disabled in static low state: QCLK_*y* = L, nQCLK_*y* = H.

Table 9. Individual SYSREF Output (QREF_r) Settings[a]

PD	STYLE	Enable	A[1:0]	nBIAS	Output Power	Termination[b]	State	Amplitude (mV)
1	X	X	X	X	Off	100Ω differential or no termination	Off	X
0	0	0	XX	0	On	100Ω differential (LVDS)	Disable[c]	X
		1	00	0			Enabled	250
			01	0			See Table 10	500
				1			Enabled	
			10	0				750
			11	0				1000
	1	0	XX	0		50Ω to V_T (LVPECL)	Disable	X
		1	00				Enable	250
			01					500
			10					750
			11					1000

[a] Applicable QREF_*r* outputs when configured as SYSREF output (MUX_*r* = 1).

[b] See Application Information for output termination information.

[c] Differential output is disabled in static low state: QCLK_*y* = L, nQCLK_*y* = H.

Table 10. QREF_r Setting for JESD204B Applications

BIAS_TYPE	nBIAS_*r*	QREF_r Outputs (LVDS, 500mV amplitude)			Application
		Initial	Active Rising Edge on the REF Input	SYSREF Completed	
0	1	Static Low (QREF = L, nQREF_*r* = H)			QREF_*r* DC coupled
	0	Static Low (QREF = L, nQREF_*r* = H)	Start switching for the number of received SYSREF pulses	Released to static low (QREF = L, nQREF_*r* = H)	
1	0	Static LVDS crosspoint level (QREF = nQREF_*r* = VOS)	Start switching for the number of received SYSREF pulses	Released to static LVDS crosspoint level (QREF = nQREF_*r* = VOS)	QREF_*r* AC coupled
	1	Static LVDS crosspoint level (QREF = nQREF_*r* = VOS)			

Device Startup, Reset, and Synchronization

At startup, an internal POR (power-on reset) resets the device and sets all register bits to its default value. In the default configuration the QCLK_*y* and QREF_*r* outputs are disabled at startup.

Recommended configuration sequence (in order):

1. (Optional) set the value of the CPOL register bit to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. Configure the channel circuits and the outputs to the desired values and configure the DCB:
   - Output source MUX_r, output divider N_{A-D}, clock delay $\Phi_{A-D;}$ MUX-output style, amplitude and power down mode for QCLK_*y* and QREF_*r* outputs
   - For synchronization between multiple devices: Set N_{A-D} = ÷1 and set BYP_INIT = 1)
   - (Optional) the global BIAS_TYPE bit and nBIAS_*r* for each QREF_r in preparation for JESD204B/SYSREF operation
   - Phase delay for Φ_{REF_r} values for the QREF_*r* outputs
   - Setup the DCB settings DLC, P_{DCB} and M_{DCB} as described in the paragraph *Configuration*, see Delay Calibration Block (DCB)
3. If not already applied: apply a valid input frequency to CLK. Set the PB_CAL bit and the DCB_CAL bit to start the calibration of the precision bias current circuit and the DCB calibration. Both bits will auto-clear. *See* paragraph *Configuration* in section Delay Calibration Block (DCB).
   - (Optional): verify the success of the DCB calibration by reading the DAC_CODE value. *See* paragraph *Verification* in section Delay Calibration Block (DCB)
4. Set the initialization bit INIT_CLK. This will initiate the N_*x* divider and ΦCLK_*x* delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear.
5. At this point, the configuration of the registers 0x00 to 0x73 should be completed and the SPI transfer ended. Set nCS to high level.
6. In a separate SPI write access, enable the outputs as desired by accessing the output-enable registers 0x74 and 0x76.

Registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

Changing Frequency Dividers and Phase Delay Values

Clock Frequency Divider and Delay

Following procedure has to be applied for a change of a clock divider and phase delay value $N_{A-D,}$ and $\Phi_{CLKA-D:}$

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. (Optional) disable the outputs whose frequency divider or delay value is changed.
3. Configure the N_{A-D} dividers and the delay circuits Φ_{CLKA-D} to the desired new values.
   - For synchronization between multiple devices: Set N_{A-D} = ÷1 and set BYP_INIT = 1)
4. Set the initialization bit INIT_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear. During this initialization step, all QCLK_y and QREF_*r* outputs are reset to the logic low state.
5. (Optional) Enable the outputs whose frequency divider was changed.

SYSREF Delay

Following procedure has to be applied for a change of any SYSREF phase delay value $\Phi_{REF\_r:}$

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. Configure any delay circuits Φ_{REF_r} to their desired new values. During configuration of Φ_{REF_r} outputs are not stopped or interrupted.

SPI Interface

The 8V79S680 has a 3-wire serial control port capable of responding as a slave in an SPI configuration to allow read and write access to any of the internal registers for device programming or read back. The SPI interface consists of the SCLK (clock), SDAT (serial data input and output), and nCS (chip select) pins. A data transfer consists of any integer multiple of 8 bits and is always initiated by the SPI master on the bus. Internal register data is organized in SPI bytes of 8 bits each. If nCS is at logic high, the SDAT data I/O is in high-impedance state and the SPI interface of the 8V79S680 is disabled. In a write operation, data on SDAT will be clocked in on the rising edge of SCLK. In a read operation, data on SDAT will be clocked out on the falling or rising edge of SCLK depending on the CPOL setting (CPOL = 0: output data changes on the falling edge, CPOL = 1: output data changes on the rising edge).

Starting a data transfer requires nCS to set and hold at logic low level during the entire transfer. Setting nCS = 0 will enable the SPI interface with SDAT in data input mode. The master must initiate the first 8-bit transfer. The first bit presented to the slave is the direction bit R/nW (1 = Read,
0 = Write) and the following seven bits are the address bits A[0:6] pointing to an internal register in the address space 0 to 127. Data is presented with the LSB (least significant bit) first.

Read operation from an internal register: a read operation starts with an 8 bit transfer from the master to the slave: SDAT is clocked on the rising edge of SCLK. The first bit is the direction bit R/nW which must be to 1 to indicate a read transfer, followed by 7 address bits A[0:6]. After the first 8 bits are clocked into SDAT, the SDAT I/O changes to output: the register content addressed by A[0:6] is loaded into the shift register and the next 8 SCLK falling clock cycles (if CPOL = 0) will then present the loaded register data on the SDAT output and transfer these to the master. Transfers must be completed by de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. SPI byte (8 bit) and back-to-back read transfers of multiple registers are supported with an address auto-increment. During multiple transfers, nCS must stay at logic low level and SDAT will present multiple registers (A), (A+1), (A+2), etc. with each 8 SCLK cycles. During SPI Read operations, the user may continue to hold nCS low and provide further bytes in a single block read.

Write operation to a 8V79S680 register: During a write transfer, a SPI master transfers one or more bytes of data into the internal registers of the 8V79S680. A write transfer starts by asserting nCS to low logic level. The first bit presented by the master must set the direction bit R/nW to 0 (Write) and the 7 address bits A[0:6] must contain the 7-bit register address. Bits D0 to D7 contain 8 bit of payload data, which is written into the register addressed by A[0:6] at the end of a 8-bit write transfer. Multiple, subsequent register transfers from the master to the slave are supported by holding nCS asserted at logic low level during write transfers. The 7 bit register address will auto-increment. Transfers must be completed by de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined.

End of transfer: After de-asserting nCS, the SPI bus is available to transfers to other slaves on the SPI bus. See also the READ diagram (Figure 5) and WRITE diagram (Figure 6) displaying the transfer of two bytes of data from and into registers.

Registers 0x78 to 0xFF: Registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

Figure 5. Logic Diagram: READ Data from 8V79S680 Registers for CPOL = 0 and CPOL = 1

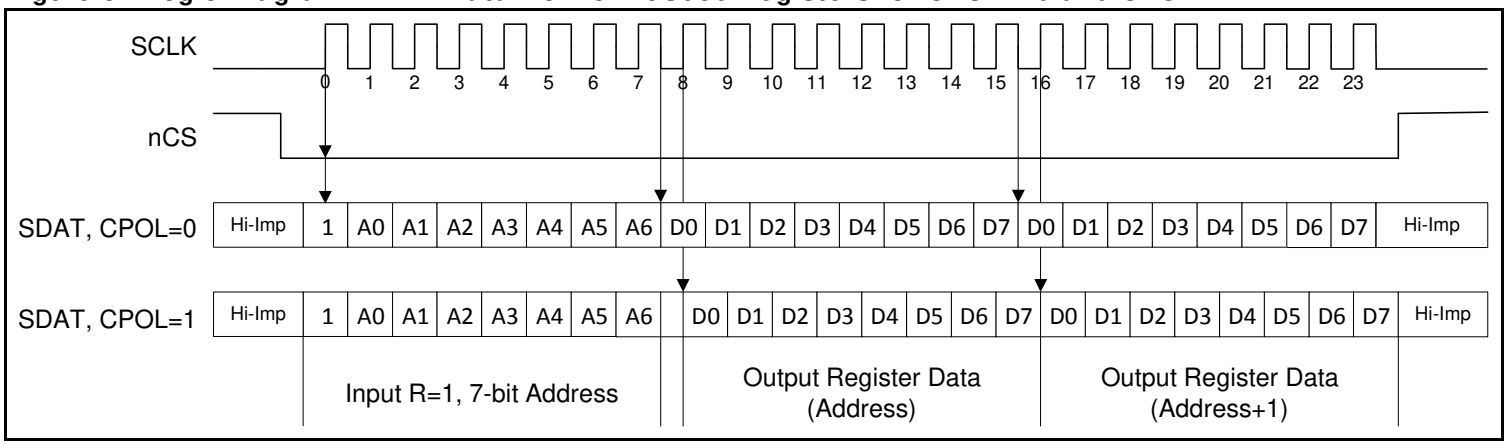


Figure 6. Logic Diagram WRITE Data into 8V79S680 Registers

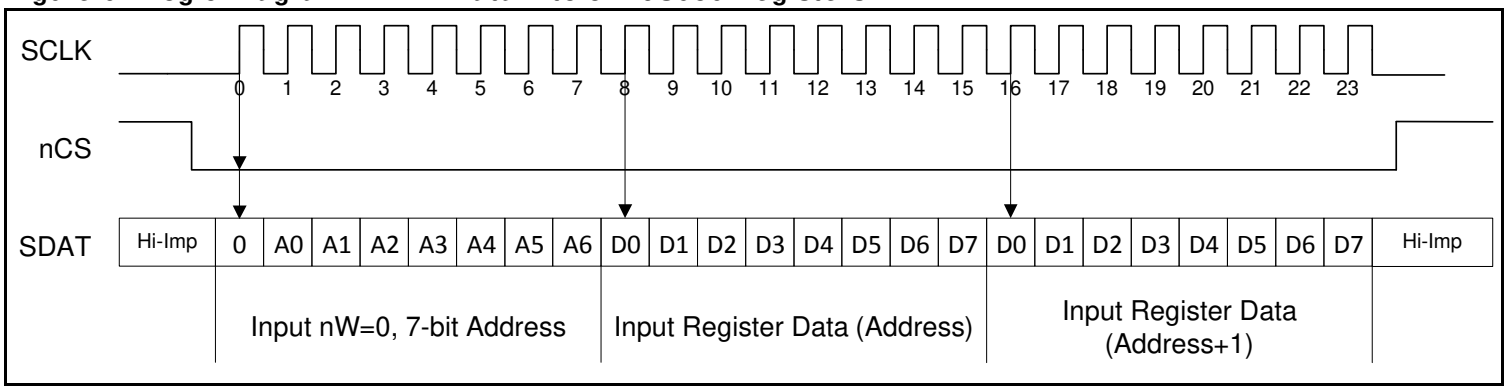
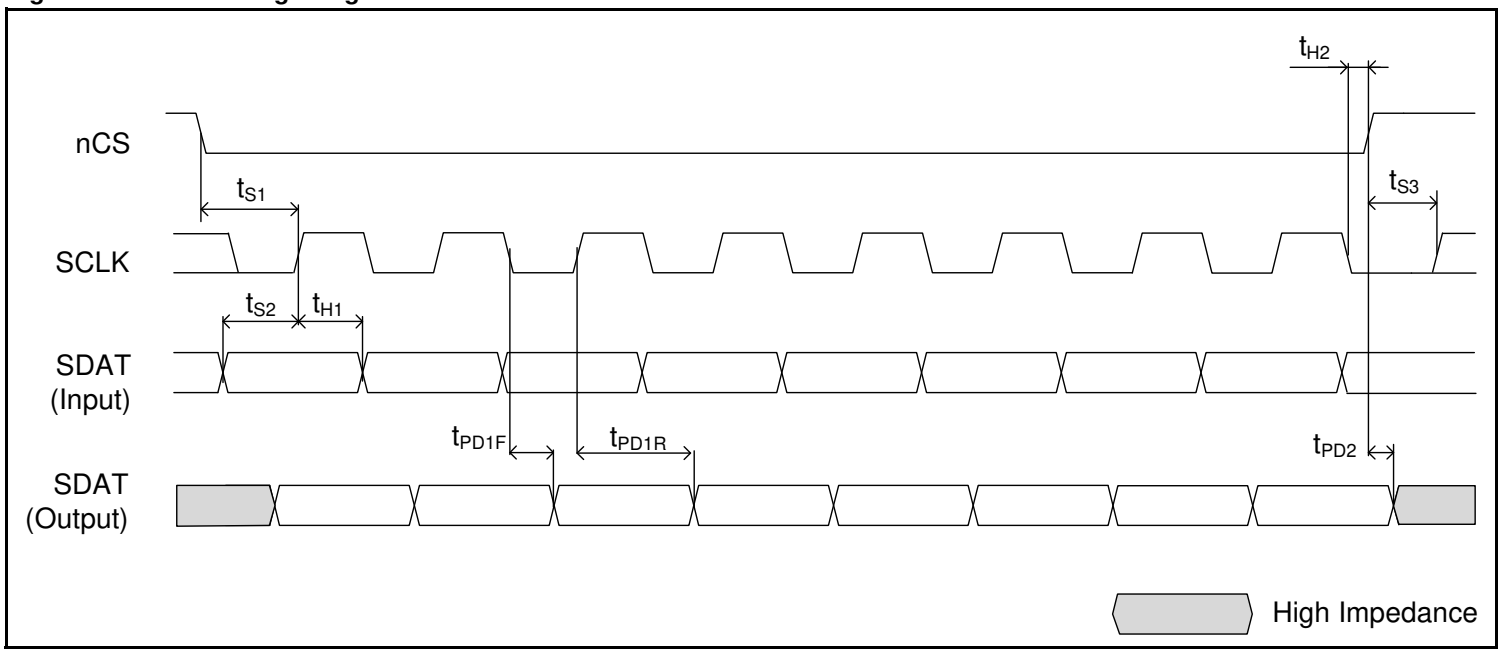


Table 11. SPI Read / Write Cycle Timing Parameters

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
f_{SCLK}	SCLK frequency			20	MHz
t_{S1}	Setup time, nCS (falling) to SCLK (rising)		5		ns
t_{S2}	Setup time, SDAT (input) to SCLK (rising)		5		ns
t_{S3}	Setup time, nCS (rising) to SCLK (rising)		5		ns
t_{H1}	Hold time, SCLK (rising) to SDAT (input)		5		ns
t_{H2}	Hold time, SCLK (falling) to nCS (rising)		5		ns
t_{PD1F}	Propagation delay, SCLK (falling) to SDAT	CPOL = 0		12	ns
t_{PD1R}	Propagation delay, SCLK (rising) to SDAT	CPOL = 1		12	ns
t_{PD2}	Propagation delay, nCS to SDAT disable			12	ns

Figure 7. SPI Timing Diagram



Register Descriptions

This section contains a list of all addressable registers and a register description, sorted by function, followed for a detailed description of each bit field for each register. Several functional blocks with multiple instances in this device have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once, but with an additional table to indicate their addresses and default values. All writable register fields will come up with a default values as indicated in the Factory Defaults column unless altered by values loaded from non-volatile storage during the initialization sequence.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are Reserved. Reserved bit fields will be unaffected by writes and are undefined on reads.

Table 12. Configuration Registers

Register Address	Register Description
0x00–0x17	Reserved
0x18–0x1B	SYSREF Control
0x1C–0x1F	Reserved
0x20	Channel A, Output Divider
0x21	Channel A Delay ΦCLK_*A*
0x22	Channel A PD
0x23	Reserved
0x24	Output State QCLK_*A0*
0x25	Output State QCLK_*A1*
0x26	Output State QCLK_*A2*
0x27	Reserved
0x28	ΦREF_A0 Delay, MUX, PD
0x29	ΦREF_A1 Delay, MUX, PD
0x2A	ΦREF_A2 Delay, MUX, PD
0x2B	Reserved
0x2C	Output State QREF_A0
0x2D	Output State QREF_A1
0x2E	Output State QREF_A2
0x2F	Reserved
0x30	Channel B, Output Divider
0x31	Channel B Delay ΦCLK_*B*
0x32	Channel B PD
0x33	Reserved
0x34	Output State QCLK_*B0*
0x35	Output State QCLK_*B1*
0x36–0x37	Reserved
0x38	ΦREF_B0 Delay, MUX, PD

Table 12. Configuration Registers (Cont.)

Register Address	Register Description
0x39	ΦREF_B1 Delay, MUX, PD
0x3A–0x3B	Reserved
0x3C	Output State QREF_B0
0x3D	Output State QREF_B1
0x3E–0x3F	Reserved
0x40	Channel C, Output Divider
0x41	Channel C Delay ΦCLK_*C*
0x42	Channel C PD
0x43	Reserved
0x44	Output State QCLK_*C0*
0x45	Output State QCLK_*C1*
0x46–0x47	Reserved
0x48	ΦREF_C0 Delay, MUX, PD
0x49	ΦREF_C1 Delay, MUX, PD
0x4A–0x4B	Reserved
0x4C	Output State QREF_C0
0x4D	Output State QREF_C1
0x4E–0x4F	Reserved
0x50	Channel D, Output Divider
0x51	Channel D Delay ΦCLK_*D*
0x52	Channel D PD
0x53	Reserved
0x54	Output State QCLK_*D*
0x55–0x57	Reserved
0x58	ΦREF_D Delay, MUX, PD
0x59–0x5B	Reserved
0x5C	Output State QREF_D
0x5D–0x6B	Reserved
0x6C–0x6D	DAC_CODE
0x6E–0x6F	General Control
0x70	Reserved
0x71–0x73	General Control
0x74	Output State QCLK
0x75	Reserved
0x76	Output State QREF

Table 12. Configuration Registers (Cont.)

Register Address	Register Description
0x77	Reserved
0x78	Do not use
0x79	Do not use
0x7A	Do not use
0x7B	Do not use
0x7C–0x7D	Do not use
0x7E	Do not use
0x7F	Do not use
0x80–0xFF	Do not use

Channel and Clock Output Registers

The content of the channel register and clock output registers set the clock divider, output style, amplitude, power down state, enable state and the clock phase delay.

Table 13. Channel and Clock Output Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x20 0x30 0x40 0x50	Reserved	Reserved	Reserved	Reserved	Reserved	N_*A*[2:0] N_*B*[2:0] N_*C*[2:0] N_*D*[2:0]		
0x21 0x31 0x41 0x51	ΦCLK_*A*[7:0] ΦCLK_*B*[7:0] ΦCLK_*C*[7:0] ΦCLK_*D*[7:0]							
0x22 0x32 0x42 0x52	PD_*A* PD_*B* PD_*C* PD_*D*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x24: QCLK_A0 0x25: QCLK_A1 0x26: QCLK_A2	PD_*A0* PD_*A1* PD_*A2*	Reserved	Reserved	STYLE_*A0* STYLE_*A1* STYLE_*A2*	A_*A0*[1:0] A_*A1*[1:0] A_*A2*[1:0]		Reserved	
0x34: QCLK_B0 0x35: QCLK_B1	PD_*B0* PD_*B1*	Reserved	Reserved	STYLE_*B0* STYLE_*B1*	A_*B0*[1:0] A_*B1*[1:0]		Reserved	
0x44: QCLK_C0 0x45: QCLK_C1	PD_*C0* PD_*C1*	Reserved	Reserved	STYLE_*C0* STYLE_*C1*	A_*C0*[1:0] A_*C1*[1:0]		Reserved	
0x54: QCLK_D	PD_*D*	Reserved	Reserved	STYLE_*D*	A_*D*[1:0]		Reserved	
0x74	EN_QCLK_A0	EN_QCLK_A1	EN_QCLK_A2	EN_QCLK_B0	EN_QCLK_B1	EN_QCLK_C0	EN_QCLK_C1	EN_QCLK_D

Table 14. Channel and Clock Output Register Descriptions[a]

Register Description				
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**	
N_*x*[2:0]	R/W	000 Value: ÷1	Output Frequency Divider N	
			N_*x*[2:0]	Frequency Divider
			000 001 010 011 100 101 110 111	÷1 (Divider bypassed and powered-down) ÷2 ÷4 ÷6 ÷8 ÷12 ÷16 Not defined If N_x[2:0] = 000 (÷1), set BYP_INIT = 1 to exclude the divider from initialization.
PD_*x*	R/W	0	0 = Channel *x* is powered up 1 = Channel *x* is powered down	
PD_*y*	R/W	0	0 = Output QCLK_*y* is powered up 1 = Output QCLK_*y* is powered down	
ΦCLK_*x*[7:0]	R/W	0000 0000 Value: 0ns	CLK_*x* Phase Delay	
			ΦCLK_*x*[7:0]	Phase Delay in units of the input period: ΦCLK_*x*[7:0] ÷ f_{IN} (256 steps).
			0000 0000 0000 0001 … 1111 1111	0ps 1 ÷ f_{IN} … 255 ÷ f_{IN}

Table 14. Channel and Clock Output Register Descriptions[a]

Register Description				
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**	
A_*y*[1:0]	R/W	00 Value: 250mV	QCLK_*y* Output Amplitude	
			Setting for STYLE = 0 (LVDS) Termination: 100Ω across	Setting for STYLE = 1 (LVPECL) Termination: 50Ω to VT
			A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 750mV A[1:0] = 11:1000mV	
STYLE_*y*		0 Value: LVDS	QCLK_*y* Output Format: 0 = Output is LVDS (requires LVDS 100Ω output termination) 1 = Output is LVPECL (requires LVPECL 50Ω output termination to the specified recommended termination voltage)	
EN_*y*		0 Value: disabled	QCLK_*y* Output Enable: 0 = QCLK_*y* Output is disabled at the logic low state 1 = QCLK_*y* Output is enabled	

[a] *x* = A, B, C, D; *y* = A0, A1, A2, B0, B1, C0, C1, D.

QREF Output State Registers

The content of the QREF output registers selects the source signal of the QREF outputs, set the phase delay, the style, the amplitude, the power state, the enable state and the output bias.

Table 15. QREF Output State Register Bit Field Locations[a]

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x28: QREF_A0 0x29: QREF_A1 0x2A:QREF_A2	Reserved	Reserved	Reserved	MUX_*A0* MUX_*A1* MUX_*A2*	ΦREF_*A0*[2:0] ΦREF_*A1*[2:0] ΦREF_*A2*[2:0]			Reserved
0x38: QREF_B0 0x39: QREF_B1	Reserved	Reserved	Reserved	MUX_*B0* MUX_*B1*	ΦREF_*B0*[2:0] ΦREF_*B1*[2:0]			Reserved
0x48: QREF_C0 0x49: QREF_C1	Reserved	Reserved	Reserved	MUX_*C0* MUX_*C1*	ΦREF_*C0*[2:0] ΦREF_*C1*[2:0]			Reserved
0x58: QREF_D	Reserved	Reserved	Reserved	MUX_*D*	ΦREF_*D*[2:0]			Reserved
0x2C: QREF_A0 0x2D: QREF_A1 0x2E: QREF_A2	PD_*A0* PD_*A1* PD_*A2*	Reserved	nBIAS_*A0* nBIAS_*A1* nBIAS_*A2*	STYLE_*A0* STYLE_*A1* STYLE_*A2*	A_*A0*[1:0] A_*A1*[1:0] A_*A2*[1:0]		Reserved	Reserved
0x3C: QREF_B0 0x3D: QREF_B1	PD_*B0* PD_*B1*	Reserved	nBIAS_*B0* nBIAS_*B1*	STYLE_*B0* STYLE_*B1*	A_*B0*[1:0] A_*B1*[1:0]		Reserved	Reserved
0x4C: QREF_C0 0x4D: QREF_C1	PD_*C0* PD_*C1*	Reserved	nBIAS_*C0* nBIAS_*C1*	STYLE_*C0* STYLE_*C1*	A_*C0*[1:0] A_*C1*[1:0]		Reserved	Reserved
0x5C: QREF_D	PD_*D*	Reserved	nBIAS_*D*	STYLE_*D*	A_*D*[1:0]		Reserved	Reserved
0x76	EN_QREF_A0	EN_QREF_A1	EN_QREF_A2	EN_QREF_B0	EN_QREF_B1	EN_QREF_C0	EN_QREF_C1	EN_QCLK_D

[a] r = A0, A1, A2, B0, B1, C0, C1, D.

Table 16. QREF Output State Register Descriptions[a]

<table>
<tr><th colspan="7">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="4">Description</th></tr>
<tr><td>MUX_r</td><td>R/W</td><td>1

Value: QREF = SYSREF</td><td colspan="4">0 = QREF_r output signal source is the channel’s clock signal
1 = QREF_r output signal source is the centrally generated SYSREF signal</td></tr>
<tr><td>ΦREF_r[2:0]</td><td>R/W</td><td>000

Value: 0ps</td><td colspan="4">SYSREF Phase Delay:
QREF_r delay = ΦREF_r[2:0] · T_{DCB}.
Delay values for f_{DCO} = 983.04MHz. Delay values are a function of T_{DCB}.</td></tr>
<tr><td></td><td></td><td></td><td>ΦREF_r[2:0]</td><td colspan="3">QREF_r delay in ps for a DLC[1:0] setting of:</td></tr>
<tr><td></td><td></td><td></td><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td></td><td></td><td></td><td>000</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td></td><td></td><td></td><td>001</td><td>131</td><td>262</td><td>393</td><td>524</td></tr>
<tr><td></td><td></td><td></td><td>010</td><td>262</td><td>524</td><td>786</td><td>1048</td></tr>
<tr><td></td><td></td><td></td><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td></td><td></td><td></td><td>111</td><td>917</td><td>1834</td><td>2751</td><td>3668</td></tr>
<tr><td>nBIAS_r</td><td>R/W</td><td>0</td><td colspan="4">QREF_r Output Bias Voltage:
Individual QREF_r output LVDS output bias operation. Not applicable to QREF_r outputs set to LVPECL mode.
0 = Normal operation
1 = Output is biased to the LVDS cross-point voltage if BIAS_TYPE (register 0x19, bit 7) is set to 1. Bit has no effect if BIAS_TYPE = 0.
Output bias = 1 requires AC coupling and LVDS style on the corresponding output.</td></tr>
<tr><td></td><td></td><td></td><td>BIAS_TYPE</td><td>nBIAS_r</td><td colspan="2">QREF_r output operation if set to LVDS.</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>0</td><td colspan="2">QREF_r outputs are initially logic low (QREF_r = L, nQREF_r = H) and will start switching on the first rising edge of the REF input. Use in DC-coupled applications.</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td colspan="2">Disabled with static low/high levels. During a SYSREF event, the output remains at static low levels (QREF_r = L, nQREF_r = H).</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>0</td><td colspan="2">Both QREF_r and nQREF_r outputs are initially set to the LVDS crosspoint level (VOS) and will start switching on the first rising edge of the REF input. Use in AC-coupled applications.</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td colspan="2">Output is statically set to the LVDS crosspoint voltage. During a SYSREF event, the output remains at the LVDS crosspoint level (VOS).</td></tr>
</table>

Table 16. QREF Output State Register Descriptions[a] (Cont.)

Register Description				
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**	
A_*r*[1:0]	R/W	00 Value: 250mV	QREF_*r* Output Amplitude	
			Setting for STYLE = 0 (LVDS) Termination: 100Ω across	Setting for STYLE = 1 (LVPECL) Termination: 50Ω to VT
			A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 750mV A[1:0] = 11:1000mV	
PD_*r*	R/W	0 Value: Powered up	QREF_*r* Output Power Down: 0 = Output is powered up 1 = Output is powered down. STYLE, EN and A[1:0] settings have no effect	
STYLE_*r*	R/W	0 Value: LVDS	QREF_*r* Output Format: 0 = Output is LVDS (requires LVDS 100Ω output termination) 1 = Output is LVPECL (requires LVPECL 50Ω output termination of to the specified recommended termination voltage)	
EN_*r*	R/W	0 Value: Disabled	QREF_*r* Output Enable: 0 = Output is disabled at the logic low state 1 = Output is enabled	

[a] r = A0, A1, A2, B0, B1, C0, C1, D.

SYSREF Control Registers

Table 17. SYSREF Control Register Bit Field Locations

Bit Field Location								
Register Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x18	PD_S	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x19	BIAS_TYPE	DLC[1:0		Reserved	Reserved	Reserved	Reserved	M_DCB[8]
0x1A	M_DCB[7:0]							
0x1B	Reserved	P_DCB[6:0]						

Table 18. SYSREF Control Register Descriptions

Register Description					
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**		
PD_S	R/W	1 Value: Powered down	SYSREF Global Power-down: 0 = SYSREF functional blocks are powered-up 1 = SYSREF functional blocks are powered-down		
BIAS_TYPE	R/W	1	SYSREF Output Voltage Bias: Global to all QREF_*r* outputs bit to control the LVDS output operation. Not applicable to QREF_*r* outputs set to LVPECL mode.		
			BIAS_TYPE	nBIAS_*r*	QREF_*r* output operation if set to LVDS.
			0	0	QREF_*r* outputs are initially logic low (QREF_r = L, nQREF_*r* = H) and will start switching on the first rising edge of the REF input. Use in DC-coupled applications.
			0	1	Disabled with static low/high levels. During a SYSREF event, the output remains at static low levels (QREF_r = L, nQREF_*r* = H).
			1	0	Both QREF_*r* and nQREF_*r* outputs are initially set to the LVDS crosspoint level (VOS) and will start switching on the first rising edge of the REF input. Use in AC-coupled applications.
			1	1	Output is statically set to the LVDS crosspoint voltage. During a SYSREF event, the output remains at the LVDS crosspoint level (VOS).

Table 18. SYSREF Control Register Descriptions (Cont.)

Register Description				
Bit Field Name	**Field Type**	**Default (Binary)**	**Description**	
DLC[1:0]	R/W	00 Value: 131ps	Delay Unit Multiplier: Effective delay unit for the SYSREF outputs is (1 + DLC[1:0]) ÷ (8 · f_{DCO}).	
			DLC[1:0]	Effective SYSREF Delay Unit for f_{DCO} = 983.04MHz
			00	131ps
			01	262ps
			10	393ps
			11	524ps
M_DCB[8:0]	R/W	0 0000 1000 Value: 8	Delay Calibration Block (DCB) DCO feedback divider. Set in conjunction with f_{IN} and P_DCB to achieve a DCO frequency of 983.04±20MHz: $f_{DCO} = f_{IN} \div P_{DCB} \cdot M_{DCB}$.	
P_DCB[6:0]	R/W	000 1000 Value: 8	Delay Calibration Block (DCB) DCO input divider. Set in conjunction with f_{IN} and M_DCB to achieve DCO frequency of 983.04±20MHz: $f_{DCO} = f_{IN} \div P_{DCB} \cdot M_{DCB}$. DCO phase detector frequency should not exceed 200MHz.	