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Stratix V GX FPGA Development Board

Reference Manual

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MNL-01063-1.6

Contents

Appendix A. Board Revision History

Additional Information

1. Overview

This document describes the hardware features of the Stratix® V GX FPGA development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Stratix V GX FPGA development board provides a hardware platform for developing and prototyping high-performance and high-bandwidth application designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Stratix V GX FPGA designs.

Two High-Speed Mezzanine Card (HSMC) connectors are available to add additional functionality via a variety of HSMC cards available from both Altera and various partners.

To see a list of the latest HSMC cards available or to download a copy of the HSMC specification, refer to the Development Board Daughtercards page of the Altera website.

Design advancements and innovations, such as the PCI Express hard IP implementation, partial reconfiguration, and programmable power technology ensure that designs implemented in the Stratix V GX FPGAs operate faster, with lower power than in previous FPGA families.

For more information on the following topics, refer to the respective documents:

- Stratix V device family, refer to the *Stratix V Device Handbook*.
- PCI Express hard IP implementation, refer to the *Stratix V Hard IP for PCI Express User Guide*.
- HSMC Specification, refer to the *High Speed Mezzanine Card (HSMC) Specification*.

Board Component Blocks

The board features the following major component blocks:

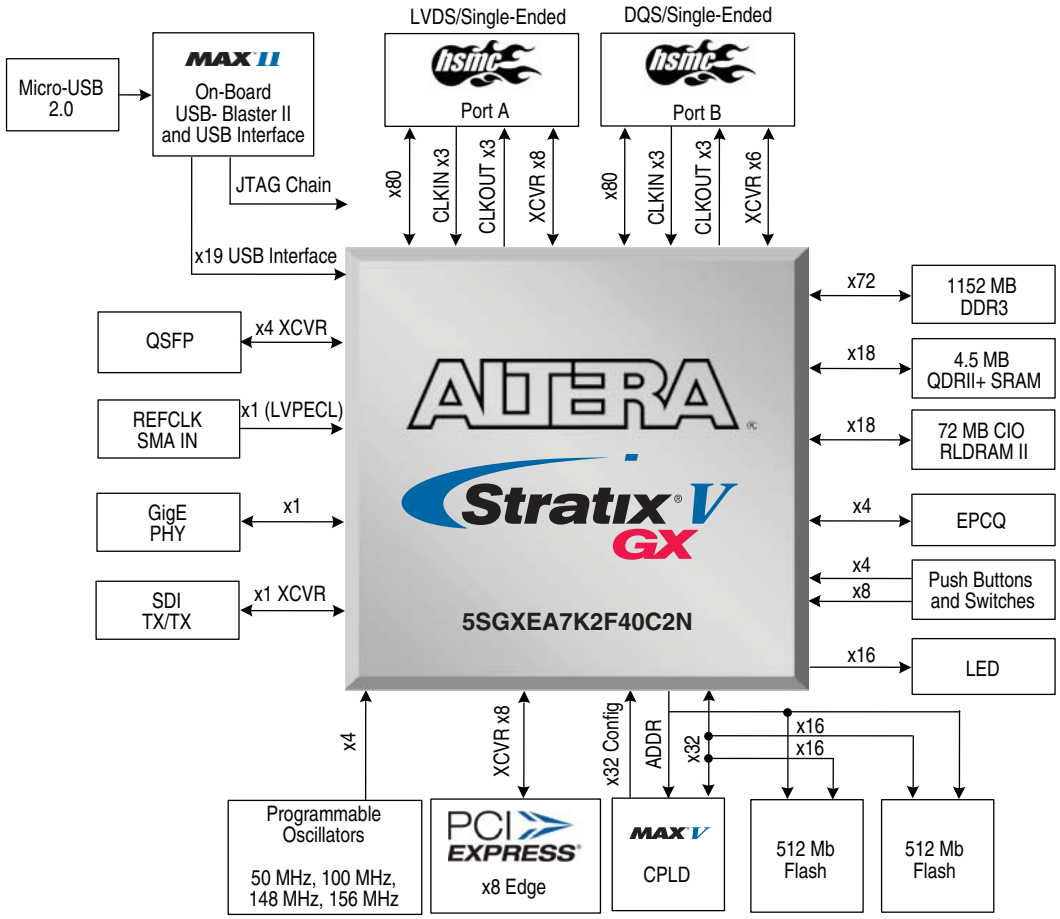
- Altera Stratix V FPGA (5SGXEA7K2F40C2N) in the 1517-pin FineLine BGA Package
  - 622,000 LEs
  - 234,720 adaptive logic modules (ALMs)
  - 50-Mbits (Mb) embedded memory
  - 36 transceivers (12.5 Gbps)
  - 174 full-duplex LVDS channels
  - 28 phase locked loops (PLLs)
  - 512 18x18-bit multipliers
  - 900-mV core voltage
  - 696 user I/Os
  - 2 PCI Express hard IP blocks
- MAX® V CPLD (5M2210ZF256C4) System Controller in the 256-pin FineLine BGA Package
  - 2,210 LEs
  - 203 user I/Os
  - 1.8-V core voltage
- FPGA Configuration Circuitry
  - MAX II CPLD (EPM570GM100) and Flash Fast Passive Parallel (FPP) configuration
  - On-Board USB-Blaster™ II for use with the Quartus® II Programmer, Nios® II Software Build Tools, and System Console.
- On-Board Clocking Circuitry
  - 50-MHz, 100-MHz, 125-MHz, and programmable oscillators
  - SMA connector for clock input (LVPECL)
- Memory devices
  - 1152-Mbyte (MB) DDR3 SDRAM with a 72-bit data bus
  - 72-MB CIO RLDRAM II with a 18-bit data bus
  - 4.5-MB QDRII+ SRAM with a 18-bit data bus (footprint is compatible for 9-Mbyte QDRII with a 18-bit data bus)
  - Two 512-Mb synchronous flash with a 16-bit data bus

- Communication Ports
  - PCI Express (PCIe) x8 edge connector
  - Two HSMC ports
    - One universal HSMC port A
    - One DQS-type HSMC port B
  - SMB for SDI input and output
  - QSFP
  - USB 2.0
  - Gigabit Ethernet
  - LCD header
- General User I/O
  - 16 user LEDs
  - Two-line character LCD display
  - Six configuration status LEDs
  - One transmit/receive LED (TX/RX) per HSMC interface
  - Five PCI Express LEDs
  - Four Ethernet LEDs
- Push Buttons and DIP Switches
  - One CPU reset push button
  - Three general user push buttons
  - Two configuration push buttons
  - Eight user DIP switches
  - Four MAX V control DIP switches
- Power
  - 19-V (laptop) DC input
  - PCI Express edge connector power
  - On-Board power measurement circuitry
- System Monitoring
  - Power—voltage, current, wattage
  - Temperature—FPGA die, local board
- Mechanical
  - PCI Express short form factor
  - PCI Express chassis or bench-top operation

Development Board Block Diagram

Figure 1–1 shows the block diagram of the Stratix V GX FPGA Development Board.

Figure 1–1. Stratix V GX FPGA Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

This chapter introduces all the important components on the Stratix V GX FPGA Development Board. Figure 2–1 illustrates major component locations and Table 2–1 provides a brief description of all features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the Stratix V GX FPGA development kit documents directory.

For information about powering up the board and installing the demo software, refer to the *Stratix V GX FPGA Development Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Stratix V GX FPGA development board, including an annotated board image and component descriptions. Figure 2–1 provides an overview of the development board features.

Figure 2–1. Overview of the Stratix V GX FPGA Development Board Features

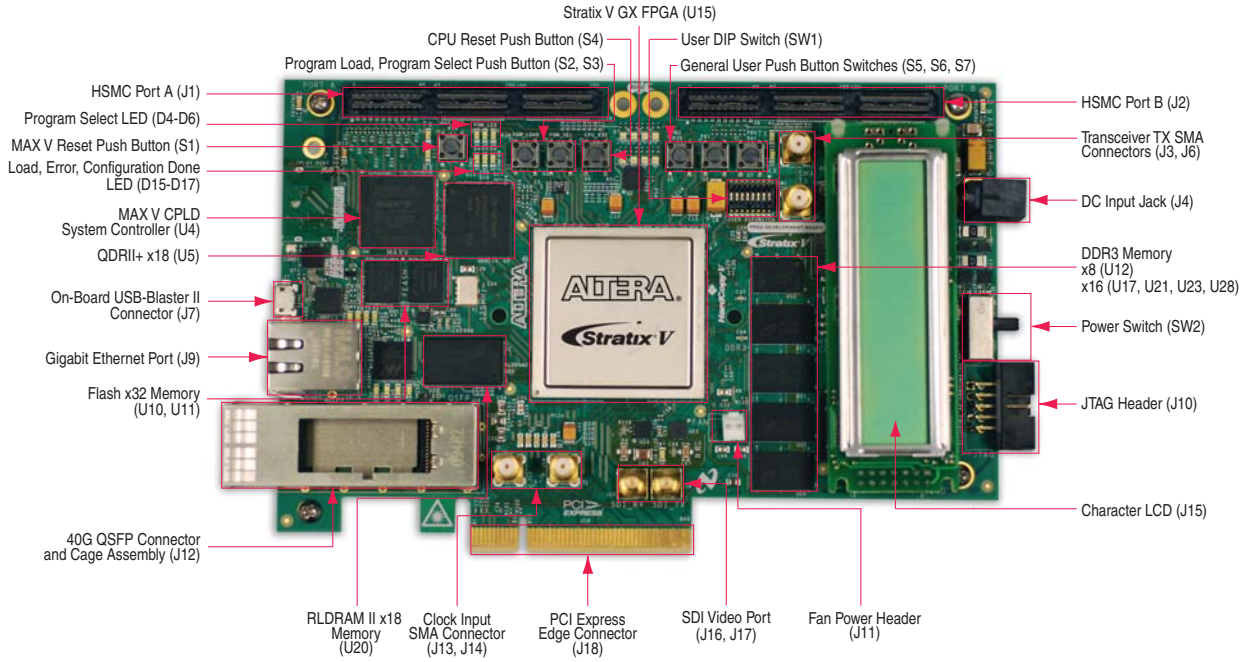


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Stratix V GX FPGA Development Board Components (Part 1 of 4)

Board Reference	Type	Description
Featured Devices		
U15	FPGA	5SGXEA7K2F40C2N, 1517-pin BGA.
U4	CPLD	5M2210ZF256C4, 256-pin BGA.
Configuration, Status, and Setup Elements		
J10	JTAG header	Provides access to the JTAG chain by using an external USB-Blaster cable (disables the on-board USB-Blaster II).
J7	On-Board USB-Blaster II	Micro-USB 2.0 connector for programming and debugging the FPGA.
SW3	JTAG DIP switch	Enables and disables devices in the JTAG chain. This switch is located on the back of the board.
SW4	FPGA mode select DIP switch	Sets the Stratix V `MSEL[4:0]` pins.
SW5	Board settings DIP switch	Controls the MAX V CPLD System Controller functions such as clock select, clock enable, factory or user design load from flash and `FACTORY` signal command sent at power up. This switch is located at the bottom of the board.

Table 2–1. Stratix V GX FPGA Development Board Components (Part 2 of 4)

Board Reference	Type	Description
SW6	PCI Express DIP switch	Controls the PCI Express lane width by connecting prsnt pins together on the PCI Express edge connector. This switch is located at the back of the board.
S3	Program select push button	Toggles the program LEDs which selects the program image that loads from flash memory to the FPGA.
S2	Program load push button	Configures the FPGA from flash memory image based on the program LEDs.
D4, D5, D6	Program LEDs	Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when you press the program load push button.
D17	Configuration done LED	Illuminates when the FPGA is configured.
D15	Load LED	Illuminates during FPGA configuration.
D16	Error LED	Illuminates when the FPGA configuration from flash fails.
D24	Power LED	Illuminates when 5-V power is present.
D25, D26	System Console TX/RX LEDs	Indicate the transmit or receive activity of the System Console USB interface. The TX and RX LEDs would flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle.
D27, D28	JTAG TX/RX LEDs	Indicate the transmit or receive activity of the JTAG chain. The TX and RX LEDs would flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle.
D29, D30, D31, D32	Ethernet LEDs	Indicate the connection speed as well as transmit or receive activity.
D3, D13	HSMC port A LEDs	You can configure these LEDs to indicate transmit or receive activity.
D1	HSMC port A Present LED	Illuminates when a daughtercard is plugged into the HSMC port A.
D11, D14	HSMC port B LEDs	You can configure these LEDs to indicate transmit or receive activity.
D2	HSMC port B Present LED	Illuminates when a daughtercard is plugged into the HSMC port B.
D33, D34	PCI Express Gen2/Gen3 LED	You can configure these LEDs to illuminate when PCI Express is in Gen2 or Gen3 mode.
D35, D36, D37	PCI Express Link LEDs	You can configure these LEDs to display the PCI Express link width (x1, x4, x8).
Clock Circuitry		
X1	125 M oscillator	125.000-MHz crystal oscillator for Gigabit Ethernet, Serial RapidIO™ (SRIO), or PCI Express.
U38	Quad-output oscillator	Programmable oscillator with default frequencies of 100 MHz, 156.25 MHz, 625 MHz, and 270 MHz.
U46	Quad-output oscillator	Programmable oscillator with default frequencies of 125 MHz, 644.53125 MHz, 282.5 MHz, and 125 MHz.
X6	148.5 M oscillator	148.500-MHz voltage controlled crystal oscillator for SDI video. This oscillator is programmable to any frequency between 20-810 MHz.
X4	100 M oscillator	100.000-MHz (programmable to any frequency between 20–810 MHz) crystal oscillator for PCI Express or general use such as memories. Multiplex with CLKIN_SMA_P or CLKIN_SMA_N based on CLK_SEL switch value.

Table 2–1. Stratix V GX FPGA Development Board Components (Part 3 of 4)

Board Reference	Type	Description
X3	50 M oscillator	50.000-MHz crystal oscillator for general purpose logic.
J13, J14	Clock input SMAs	Drives LVPECL-compatible clock inputs into the clock multiplexer buffer.
U4	100 M oscillator	100-MHz crystal oscillator for the MAX V CPLD System Controller.
General User Input and Output		
D7-D10, D18-D21	User LEDs	Eight bi-color LEDs (green and red) for 16 user LEDs. Illuminates when driven low.
SW1	User DIP switch	Octal user DIP switches. When the switch is ON, a logic 0 is selected.
S1	MAX V reset push button	The default reset for the MAX V CPLD System Controller.
S4	CPU reset push button	The default reset for the FPGA logic.
S5, S6, S7	General user push button	Three user push buttons. Driven low when pressed.
Memory Devices		
U12, U17, U21, U23, U28	DDR3 x72	A 1152-MB DDR3 SDRAM with a 72-bit data bus. The 72-bit data bus consists of four x16 devices and one x8 device with a single address or command bus.
U5	QDRII+ x18	A 4.5-MB QDRII+ SRAM with a 18-bit data bus. The device has a separate 18-bit read and 18-bit write port with DDR signalling at up to 550 MHz.
U20	RLDRAM II x18	A 72-MB CIO RLDRAM II with a 18-bit data bus. The 18-bit data bus consists of a single x18 device with a single address or command bus.
U10, U11	Flash x32	Two 512-Mb synchronous flash devices with a 16-bit data buses for non-volatile memory. The board supports two flash devices of 16-bit interface each, which combine to allow for 1-Gbyte (GB) synchronous flash with a 32-bit data bus.
Communication Ports		
J18	PCI Express edge connector	Made of gold-plated edge fingers for up to ×8 signaling in either Gen1, Gen2, or Gen3 mode.
J12	QSFP connector	Provides four transceiver channels for a 40G QSFP module.
J1	HSMC port A	Provides eight transceiver channels and 84 CMOS or 17 LVDS channels per the HSMC specification.
J2	HSMC port B	Provides four transceiver channels and 84 CMOS or a DQ/DQS interface.
J9	Gigabit Ethernet port	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MAC MegaCore function in SGMII mode.
Video and Display Ports		
J16, J17	SDI video port	Two 75-Ω system management bus (SMB) connectors which provide a full-duplex SDI interface through a LMH0303 driver and LMH0384 cable equalizer.
J15	Character LCD header	A single 14-pin 0.1" pitch dual-row header which interfaces to the 16 character × 2 line LCD module.

Table 2–1. Stratix V GX FPGA Development Board Components (Part 4 of 4)

Board Reference	Type	Description
Power Supply		
J18	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard.
J4	DC input jack	Accepts a 19-V DC power supply.
SW2	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Stratix V GX FPGA

The Stratix V GX FPGA development board features the Stratix V GX FPGA 5SGXEA7K2F40C2N device (U15) in a 1517-pin FineLine BGA package.

For more information about the Stratix V device family, refer to the *Stratix V Device Handbook*.

Table 2–2 describes the features of the Stratix V GX FPGA 5SGXEA7K2F40C2N device.

Table 2–2. Stratix V GX FPGA 5SGXEA7K2F40C2N Features

ALMs	Equivalent LEs	Registers	M20K Blocks	MLAB Blocks (Mb)	18-bit × 18-bit Multipliers	PLLs	Transceiver Channels (12.5 Gbps)	Package Type
234,720	622,000	939,000	2,560	7.16	512	28	36	1517-pin FineLine BGA

Table 2–3 lists the Stratix V GX FPGA component reference and manufacturing information.

Table 2–3. Stratix V GX FPGA Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U15	FPGA, Stratix V GX F1517, 622K LEs, lead free	Altera Corporation	5SGXEA7K2F40C2N	www.altera.com

I/O Resources

Table 2–4 lists the Stratix V GX FPGA device pin count and usage by function on the development board.

Table 2–4. Stratix V GX FPGA Pin Count and Usage (Part 1 of 2)

Function	I/O Standard	I/O Count	Special Pins
DDR3	1.5-V SSTL	126	1 Diff ×9DQS
RLDRAM II	1.8-V SSTL	57	1 Diff ×2 DQS
QDRII+ SRAM	1.8-V HSTL	67	1 Diff ×2 DQS
MAX V System Controller	1.5-V CMOS	8	—

Table 2–4. Stratix V GX FPGA Pin Count and Usage (Part 2 of 2)

Function	I/O Standard	I/O Count	Special Pins
Flash	1.8-V CMOS	68	—
PCI Express ×8	2.5-V CMOS + XCVR	43	1 REFCLK
HSMC Port A	2.5-V CMOS + LVDS + XCVR	118	1 REFCLK
HSMC Port B	2.5-V CMOS + DQS + XCVR	104	1 REFCLK
Gigabit Ethernet	2.5-V CMOS + LVDS	8	—
On-Board USB-Blaster II	1.5-V CMOS	18	—
	3.3-V CMOS	1	—
SDI Video	2.5-V CMOS + XCVR	8	1 REFCLK
QSFP	2.5-V CMOS + XCVR	23	1 REFCLK
Buttons	1.8/2.5-V CMOS	4	1 DEV_CLRn
Switches	1.8-V CMOS	8	—
Character LCD	2.5-V CMOS	11	—
LEDs	1.8/2.5-V CMOS	16	—
Clocks or Oscillators	1.8-V CMOS + LVDS	25	9 REFCLK
Device I/O Total:		**713**	

MAX V CPLD System Controller

The board utilizes the 5M2210ZF256C4 System Controller, an Altera MAX V CPLD, for the following purposes:

- FPGA configuration from flash memory
- Power consumption monitoring
- Temperature monitoring
- Fan control
- Control registers for clocks
- Control registers for remote system update

Figure 2–2 illustrates the MAX V CPLD System Controller's functionality and external circuit connections as a block diagram.

Figure 2–2. MAX V CPLD System Controller Block Diagram

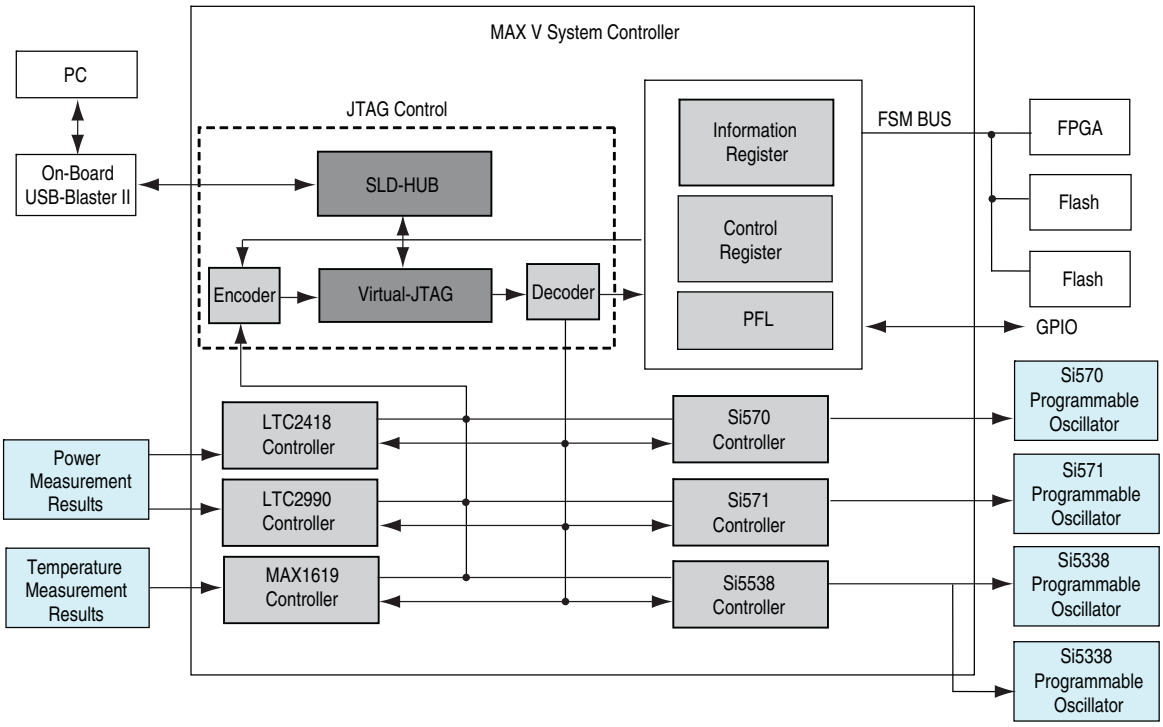


Table 2–5 lists the I/O signals present on the MAX V CPLD System Controller. The signal names and functions are relative to the MAX V device (U4).

Table 2–5. MAX V CPLD System Controller Device Pin-Out (Part 1 of 6)

Schematic Signal Name	MAX V CPLD Pin Number	Stratix V GX FPGA Pin Number	I/O Standard	Description
5M2210_JTAG_TMS	N4	—	2.5-V	MAX V JTAG TMS
CLK125_EN	B9	—	2.5-V	125 MHz oscillator enable
CLK50_EN	E9	—	2.5-V	50 MHz oscillator enable
CLK_CONFIG	J5	—	2.5-V	100 MHz configuration clock input
CLK_ENABLE	A15	—	2.5-V	DIP switch for clock oscillator enable
CLK_SEL	A13	—	2.5-V	DIP switch for clock select SMA or oscillator
CLKIN_50	J12	AN6	1.8-V	50 MHz clock input
CLOCK_SCL	C9	—	2.5-V	Programmable oscillator I2C clock
CLOCK_SDA	D9	—	2.5-V	Programmable oscillator I2C data
CPU_RESETn	D10	AM34	2.5-V	FPGA reset push button
FACTORY_LOAD	A2	—	2.5-V	DIP - load factory image or user1 image from flash at power-up
FACTORY_REQUEST	R14	—	1.8-V	On-Board USB-Blaster II request to send FACTORY command

Table 2–5. MAX V CPLD System Controller Device Pin-Out (Part 2 of 6)

Schematic Signal Name	MAX V CPLD Pin Number	Stratix V GX FPGA Pin Number	I/O Standard	Description
FACTORY_STATUS	N12	—	1.8-V	On-Board USB-Blaster II FACTORY command status
FLASH_ADVn	N7	AP7	1.8-V	FM bus flash memory address valid
FLASH_CEn0	R5	AV14	1.8-V	FM bus flash memory chip enable 0
FLASH_CEn1	M7	AW13	1.8-V	FM bus flash memory chip enable 1
FLASH_CLK	R6	AM8	1.8-V	FM bus flash memory clock
FLASH_OEn	M6	AJ7	1.8-V	FM bus flash memory output enable
FLASH_RDYBSYN0	T5	AL6	1.8-V	FM bus flash memory chip ready 0
FLASH_RDYBSYN1	R7	AN7	1.8-V	FM bus flash memory chip ready 1
FLASH_RESETn	P7	AJ6	1.8-V	FM bus flash memory reset
FLASH_WEn	N6	AN8	1.8-V	FM bus flash memory write enable
FM_A0	E14	AW19	1.8-V	FM address bus
FM_A1	C14	AV19	1.8-V	FM address bus
FM_A2	C15	AM16	1.8-V	FM address bus
FM_A3	E13	AL16	1.8-V	FM address bus
FM_A4	E12	AF16	1.8-V	FM address bus
FM_A5	D15	AG16	1.8-V	FM address bus
FM_A6	F14	AN17	1.8-V	FM address bus
FM_A7	D16	AM17	1.8-V	FM address bus
FM_A8	F13	AP16	1.8-V	FM address bus
FM_A9	E15	AN16	1.8-V	FM address bus
FM_A10	E16	AT17	1.8-V	FM address bus
FM_A11	F15	AR17	1.8-V	FM address bus
FM_A12	G14	AU16	1.8-V	FM address bus
FM_A13	F16	AU17	1.8-V	FM address bus
FM_A14	G13	AW16	1.8-V	FM address bus
FM_A15	G15	AV16	1.8-V	FM address bus
FM_A16	G12	AW17	1.8-V	FM address bus
FM_A17	G16	AV17	1.8-V	FM address bus
FM_A18	H14	AU6	1.8-V	FM address bus
FM_A19	H15	AT6	1.8-V	FM address bus
FM_A20	H13	AL17	1.8-V	FM address bus
FM_A21	H16	AK17	1.8-V	FM address bus
FM_A22	J13	AE16	1.8-V	FM address bus
FM_A23	R3	AE17	1.8-V	FM address bus
FM_A24	P5	AH16	1.8-V	FM address bus
FM_A25	T2	AP21	1.8-V	FM address bus
FM_D0	J14	AN21	1.8-V	FM data bus
FM_D1	J15	AD21	1.8-V	FM data bus

Table 2–5. MAX V CPLD System Controller Device Pin-Out (Part 3 of 6)

Schematic Signal Name	MAX V CPLD Pin Number	Stratix V GX FPGA Pin Number	I/O Standard	Description
FM_D2	K16	AD20	1.8-V	FM data bus
FM_D3	K13	AG21	1.8-V	FM data bus
FM_D4	K15	AH21	1.8-V	FM data bus
FM_D5	K14	AE21	1.8-V	FM data bus
FM_D6	L16	AE20	1.8-V	FM data bus
FM_D7	L11	AL22	1.8-V	FM data bus
FM_D8	L15	AK21	1.8-V	FM data bus
FM_D9	L12	AJ21	1.8-V	FM data bus
FM_D10	M16	AJ20	1.8-V	FM data bus
FM_D11	L13	AL21	1.8-V	FM data bus
FM_D12	M15	AL20	1.8-V	FM data bus
FM_D13	L14	AN25	1.8-V	FM data bus
FM_D14	N16	AM25	1.8-V	FM data bus
FM_D15	M13	AP24	1.8-V	FM data bus
FM_D16	N15	AN24	1.8-V	FM data bus
FM_D17	N14	AC24	1.8-V	FM data bus
FM_D18	P15	AB24	1.8-V	FM data bus
FM_D19	P14	AF25	1.8-V	FM data bus
FM_D20	D13	AE25	1.8-V	FM data bus
FM_D21	D14	AE24	1.8-V	FM data bus
FM_D22	F11	AD24	1.8-V	FM data bus
FM_D23	J16	AG24	1.8-V	FM data bus
FM_D24	F12	AH24	1.8-V	FM data bus
FM_D25	K12	AK24	1.8-V	FM data bus
FM_D26	M14	AJ24	1.8-V	FM data bus
FM_D27	N13	AL24	1.8-V	FM data bus
FM_D28	R1	AL25	1.8-V	FM data bus
FM_D29	P4	AW25	1.8-V	FM data bus
FM_D30	N5	AV25	1.8-V	FM data bus
FM_D31	P6	AT24	1.8-V	FM data bus
FPGA_CONF_DONE	K1	AH6	2.5-V	FPGA configuration done
FPGA_CONFIG_D0	D3	AP33	2.5-V	FPGA configuration data
FPGA_CONFIG_D1	C2	AT33	2.5-V	FPGA configuration data
FPGA_CONFIG_D2	C3	AR33	2.5-V	FPGA configuration data
FPGA_CONFIG_D3	E3	AU34	2.5-V	FPGA configuration data
FPGA_CONFIG_D4	D2	AU33	2.5-V	FPGA configuration data
FPGA_CONFIG_D5	E4	AN31	2.5-V	FPGA configuration data
FPGA_CONFIG_D6	D1	AM31	2.5-V	FPGA configuration data
FPGA_CONFIG_D7	E5	AU32	2.5-V	FPGA configuration data

Table 2–5. MAX V CPLD System Controller Device Pin-Out (Part 4 of 6)

Schematic Signal Name	MAX V CPLD Pin Number	Stratix V GX FPGA Pin Number	I/O Standard	Description
FPGA_CONFIG_D8	F3	AT32	2.5-V	FPGA configuration data
FPGA_CONFIG_D9	E1	AR31	2.5-V	FPGA configuration data
FPGA_CONFIG_D10	F4	AP31	2.5-V	FPGA configuration data
FPGA_CONFIG_D11	F2	AW34	2.5-V	FPGA configuration data
FPGA_CONFIG_D12	F1	AV34	2.5-V	FPGA configuration data
FPGA_CONFIG_D13	F6	AW31	2.5-V	FPGA configuration data
FPGA_CONFIG_D14	G2	AV31	2.5-V	FPGA configuration data
FPGA_CONFIG_D15	G3	AW32	2.5-V	FPGA configuration data
FPGA_CONFIG_D16	G1	AV32	2.5-V	FPGA configuration data
FPGA_CONFIG_D17	G4	AJ33	2.5-V	FPGA configuration data
FPGA_CONFIG_D18	H2	AH33	2.5-V	FPGA configuration data
FPGA_CONFIG_D19	G5	AL33	2.5-V	FPGA configuration data
FPGA_CONFIG_D20	H3	AK33	2.5-V	FPGA configuration data
FPGA_CONFIG_D21	J1	AK32	2.5-V	FPGA configuration data
FPGA_CONFIG_D22	J2	AJ32	2.5-V	FPGA configuration data
FPGA_CONFIG_D23	H5	AH31	2.5-V	FPGA configuration data
FPGA_CONFIG_D24	K2	AG31	2.5-V	FPGA configuration data
FPGA_CONFIG_D25	K5	AF31	2.5-V	FPGA configuration data
FPGA_CONFIG_D26	L1	AE31	2.5-V	FPGA configuration data
FPGA_CONFIG_D27	L2	AJ30	2.5-V	FPGA configuration data
FPGA_CONFIG_D28	K3	AH30	2.5-V	FPGA configuration data
FPGA_CONFIG_D29	M2	AR30	2.5-V	FPGA configuration data
FPGA_CONFIG_D30	L4	AP30	2.5-V	FPGA configuration data
FPGA_CONFIG_D31	L3	AU30	2.5-V	FPGA configuration data
FPGA_CVP_CONFDONE	N3	AT29	2.5-V	FPGA configuration via protocol done
FPGA_DCLK	J3	AC31	2.5-V	FPGA configuration clock
FPGA_nCONFIG	N1	AK35	2.5-V	FPGA configuration active
FPGA_nSTATUS	J4	AM5	2.5-V	FPGA configuration ready status
FPGA_PR_DONE	H1	AT30	2.5-V	FPGA partial reconfiguration done
FPGA_PR_ERROR	P2	AU29	2.5-V	FPGA partial reconfiguration error
FPGA_PR_READY	E2	AN29	2.5-V	FPGA partial reconfiguration ready
FPGA_PR_REQUEST	F5	AN30	2.5-V	FPGA partial reconfiguration request
HSMA_PRSNTn	B8	AW8	2.5-V	HSMC port A present
HSMB_PRSNTn	A8	AU7	2.5-V	HSMC port B present
M570_CLOCK	P11	—	1.8-V	25-MHz clock to on-board USB-Blaster for sending FACTORY command
M570_PCIE_JTAG_EN	P12	—	1.8-V	A low signal disables the on-board USB-Blaster when PCIe masters the JTAG
MAX5_BEN0	P10	U31	1.8-V	MAX V byte enable 0

Table 2–5. MAX V CPLD System Controller Device Pin-Out (Part 5 of 6)

Schematic Signal Name	MAX V CPLD Pin Number	Stratix V GX FPGA Pin Number	I/O Standard	Description
MAX5_BEN1	R11	T31	1.8-V	MAX V byte enable 1
MAX5_BEN2	T12	N33	1.8-V	MAX V byte enable 2
MAX5_BEN3	N11	M33	1.8-V	MAX V byte enable 3
MAX5_CLK	T11	E34	1.8-V	MAX V clock
MAX5_CSN	R10	B32	1.8-V	MAX V chip select
MAX5_OEN	M10	A32	1.8-V	MAX V output enable
MAX5_WEN	N10	A34	1.8-V	MAX V write enable
MAX_CONF_DONE	E11	—	1.8-V	FPGA configuration done LED
MAX_ERROR	A4	—	1.8-V	FPGA configuration error LED
MAX_LOAD	A6	—	1.8-V	FPGA configuration active LED
MAX_RESETn	M9	—	1.8-V	MAX V reset push button
MSEL0	B10	AA9	2.5-V	DIP switch for FPGA mode select 0
MSEL1	B3	AA10	2.5-V	DIP switch for FPGA mode select 1
MSEL2	C10	AD8	2.5-V	DIP switch for FPGA mode select 2
MSEL3	C12	AG8	2.5-V	DIP switch for FPGA mode select 3
MSEL4	C6	AH7	2.5-V	DIP switch for FPGA mode select 4
OVERTEMP	B7	—	2.5-V	Temperature monitor fan enable
OVERTEMPn	C8	—	2.5-V	Temperature monitor over-temperature indicator LED
PCIE_JTAG_EN	C7	—	2.5-V	DIP switch to enable the PCIe JTAG master
PGM_CONFIG	D12	—	2.5-V	Loads the flash memory image identified by the PGM LEDs
PGM_LED0	B14	—	2.5-V	Flash memory PGM select indicator 0
PGM_LED1	C13	—	2.5-V	Flash memory PGM select indicator 1
PGM_LED2	B16	—	2.5-V	Flash memory PGM select indicator 2
PGM_SEL	B13	—	2.5-V	Toggles the PGM_LED[0:2] sequence
SDI_RX_BYPASS	D5	AB30	2.5-V	SDI equalization bypass
SDI_RX_EN	E8	AB28	2.5-V	SDI receive enable
SDI_TX_EN	D11	AK27	2.5-V	SDI transmit enable
SECURITY_MODE	R12	—	1.8-V	DIP switch for on-board USB-Blaster II to send FACTORY command at power up.
SENSE_CS0n	E7	—	2.5-V	Power monitor chip select
SENSE_SCK	A5	—	2.5-V	Power monitor SPI clock
SENSE_SDI	D7	—	2.5-V	Power monitor SPI data in
SENSE_SDO	B6	—	2.5-V	Power monitor SPI data out
SENSE_SMB_CLK	D8	—	2.5-V	Temperature monitor SMB clock
SENSE_SMB_DATA	A7	—	2.5-V	Temperature monitor SMB data
SI570_EN	A10	—	2.5-V	Si570 programmable oscillator enable

Table 2–5. MAX V CPLD System Controller Device Pin-Out (Part 6 of 6)

Schematic Signal Name	MAX V CPLD Pin Number	Stratix V GX FPGA Pin Number	I/O Standard	Description
SI571_EN	D4	—	2.5-V	Si571 programmable VCXO enable
TSENSE_ALERTn	B5	—	2.5-V	Temperature monitor alert

Table 2–6 lists the MAX V CPLD System Controller component reference and manufacturing information.

Table 2–6. MAX V CPLD EPM2210 System Controller Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U4	MAX V CPLD 2210 LE 256FBGA LF 1.8V VCCINT	Altera Corporation	5M2210ZF256C4N	www.altera.com

Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements.

Configuration

This section describes the FPGA, flash memory, and MAX V CPLD System Controller device programming methods that the Stratix V GX FPGA development board supports.

The Stratix V GX FPGA development board supports three configuration methods:

- On-Board USB-Blaster II is the default method for configuring the FPGA at any time using the Quartus II Programmer in JTAG mode with the supplied micro-USB cable.
- Flash memory download for configuring the FPGA using stored images from the flash memory on either power-up or pressing the program load push button (S2).
- External USB-Blaster for configuring the FPGA using the external USB-Blaster.

FPGA Programming over On-Board USB-Blaster II

The on-board USB-Blaster II is implemented using a micro-USB type-B connector (J7), a USB 2.0 PHY device, and an Altera MAX II CPLD EPM570GM100 (U14). This allows the configuration of the FPGA using a USB cable which connects directly between the USB port on the board (J7) and a USB port on a PC running the Quartus II software. The on-board USB-Blaster II normally masters the JTAG chain.

For more information about the on-board USB-Blaster II, refer to the on-board USB-Blaster II page of the Altera Wiki website.

MAX II CPLD EPM570GM100

The MAX II CPLD is dedicated to the on-board USB-Blaster II functionality. The CPLD connects to the CY7C68013A USB 2.0 PHY device on one side and drives the JTAG and System Console direct USB signals out the other side through the general purpose I/O (GPIO) pins.

Table 2–7 lists the I/O signals present on the MAX II CPLD EPM570GM100.

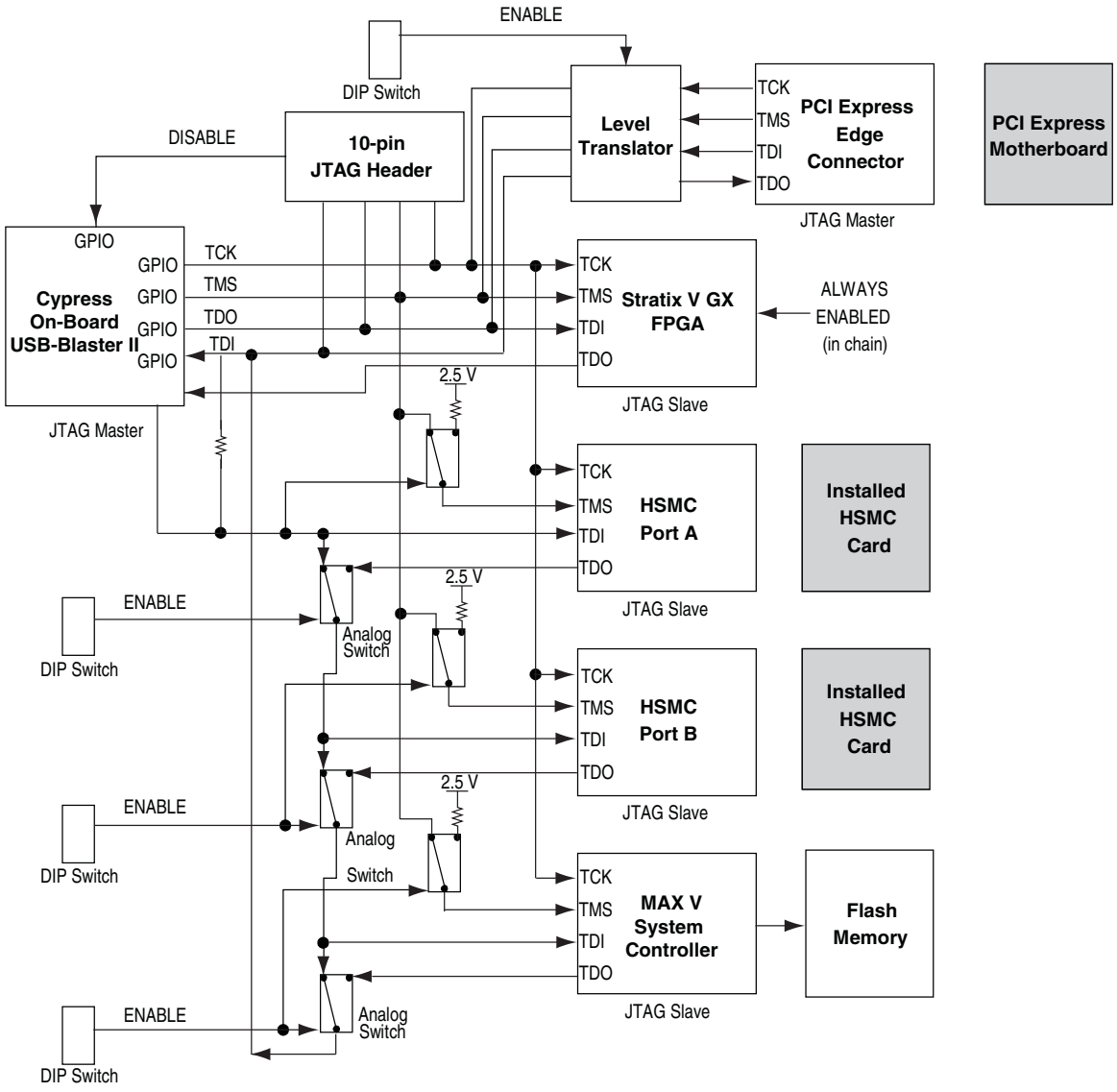
Table 2–7. MAX II CPLD EPM570GM100 On-Board USB-Blaster II I/O Signals

Schematic Signal Name	Type	Description
SC_RX	1.5-V CMOS output	USB system console receive LED
SC_TX	1.5-V CMOS output	USB system console transmit LED
JTAG_RX	1.5-V CMOS output	USB-Blaster II JTAG receive LED
JTAG_TX	1.5-V CMOS output	USB-Blaster II JTAG transmit LED
C_JTAG_TCK	2.5-V CMOS output	GPIO for on-board JTAG chain clock
C_JTAG_TMS	2.5-V CMOS output	GPIO for on-board JTAG chain mode
C_JTAG_TDI	2.5-V CMOS output	GPIO for on-board JTAG chain data in
C_JTAG_TDO	2.5-V CMOS input	GPIO for on-board JTAG chain data out
USB_CLK	3.3-V CMOS input	USB System Console clock
USB_OEn	1.5-V CMOS output	USB System Console FPGA output enable
USB_RESETn	1.5-V CMOS output	USB System Console reset
USB_DATA(7:0)	1.5-V CMOS inout (8 bits)	USB System Console FIFO data bus
USB_RDn	1.5-V CMOS output	USB System Console read from FIFO
USB_WRn	1.5-V CMOS output	USB System Console write to FIFO
USB_EMPTY	1.5-V CMOS input	USB System Console FIFO empty
USB_FULL	1.5-V CMOS input	USB System Console FIFO full
USB_ADDR(1:0)	1.5-V CMOS input/output	USB System Console address bus
USB_SCL	1.5-V CMOS input/output	USB System Console configuration clock
USB_SDA	1.5-V CMOS input/output	USB System Console configuration data
FACTORY_REQUEST	1.5-V CMOS output	Send FACTORY command
FACTORY_STATUS	1.5-V CMOS input	FACTORY command status
M570_CLOCK	1.5-V CMOS output	25-MHz input clock for FACTORY command

JTAG Chain

The on-board USB-Blaster II is automatically disabled when you connect an external USB-Blaster to the JTAG chain or when you enable JTAG from the PCI Express edge connector. Figure 2–3 illustrates the JTAG chain.

Figure 2–3. JTAG Chain



Each jumper shown in Figure 2–3 is located in the JTAG DIP switch (SW3) on the back of the board. To connect a device or interface in the chain, their corresponding switch must be in the OFF position. Push all the switches in the ON position to only have the FPGA in the chain. Note that the MAX V CPLD System Controller must be in the chain to use some of the GUI interfaces.

By default, the on-board USB-Blaster II clocks TCK at 24 MHz. For the on-board USB-Blaster II to function correctly, you must set the Quartus II clock constraint on the internal_tck input signal to 24 MHz.

System Console USB Interface

The System Console USB interface is a fast parallel interface. Together with the soft logic supplied by Altera, this interface provides a System Console master for debug access.

The System Console controls the debug master via signals shown in Table 2–8 to give fast access to an Avalon® Memory-Mapped (Avalon-MM) master bus that the Qsys system integration tool generates.

For more information about the System Console, refer to the *Analyzing and Debugging Designs with the System Console* chapter in volume 3 of the *Quartus II Handbook*.

Table 2–8 lists the System Console USB interface pin connections relative to the FPGA.

Table 2–8. System Console USB Interface Pin Connections

Stratix V GX FPGA Device Pin Number	Schematic Signal Name	Direction	Note
AV28	usb_clk	input	48 MHz
H34	usb_reset_n	input	—
G32, G33, F32, E32, A37, A36, C34, A35	usb_data[7:0]	bidirectional	G32(MSB), A35 (LSB)
N34	usb_full	output	—
P34	usb_empty	output	—
J33	usb_wr_n	input	—
K33	usb_rd_n	input	—
E33	usb_oe_n	input	—
G34, K34	usb_addr	bidirectional	Reserved
J34	usb_scl	bidirectional	—
F33	usb_sda	bidirectional	—

Flash Programming

Flash programming is possible through a variety of methods using the Stratix V GX FPGA device.

The first method is to use the factory design called the Board Update Portal. This design is an embedded web server, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (**.flash**) and write the design to the user hardware page (page 1) of the flash over the network.

The secondary method is to use the pre-built PFL design included in the development kit. The development board implements the Altera PFL megafunction for flash programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash over the USB interface using the Quartus II software. Use this method to restore the development board to its factory default settings.

Other methods to program the flash can be used as well, including the Nios II processor.

For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website.

FPGA Programming from Flash Memory

On either power-up or by pressing the program load push button (S2), the MAX V CPLD System Controller's parallel flash loader configures the FPGA from the flash memory. The system controller uses the Altera Parallel Flash Loader (PFL) megafunction which reads 32-bit data from the flash memory and converts it to fast passive parallel (FPP) format. This 32-bit data is then written to the FPGA's dedicated configuration pins during configuration.

After a power-up or reset event, the MAX V CPLD (U4) automatically configures the FPGA in FPP mode with either the pre-installed factory **.pof** file or a user **.pof** file depending on the setting of the `PGM_SEL` push-button (S3). There are three pages reserved for the FPGA configuration data—factory hardware (page 0), user hardware 1 (page 1), and user hardware 2 (page 2). Three green configuration status LEDs, `PGM_LED[2:0]` (D4, D5, D6) indicates the status of the FPP configuration. Table 2–9 lists the configuration status LEDs settings.

Table 2–9. Configuration LED settings *(1)*

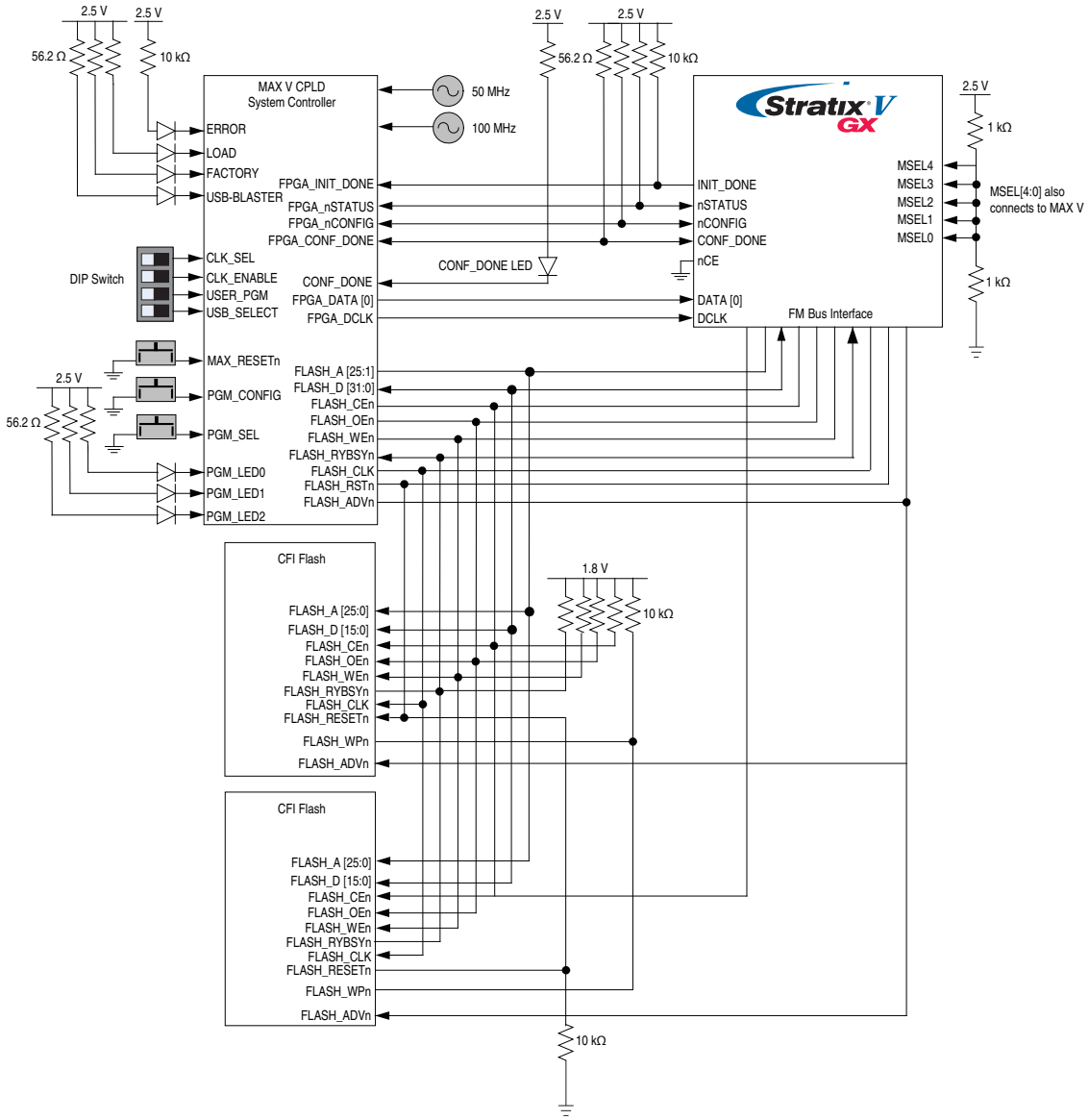
LED			Design
PGM_LED0	PGM_LED1	PGM_LED2	
✓	—	—	Factory
—	✓	—	User hardware 1
—	—	✓	User hardware 2

Note to Table 2–9:

(1) A checkmark (✓) indicates that the LED is ON (logic 0) while a dash (—) indicates that the LED is OFF (logic 1).

Figure 2–4 shows the PFL configuration.

Figure 2–4. PFL Configuration



For more information on the flash memory map storage, refer to the *Stratix V GX FPGA Development Kit User Guide*.

FPGA Programming over External USB-Blaster

The JTAG programming header provides another method for configuring the FPGA (U15) using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster connects to the board through the JTAG header (J10).