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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Single-Phase High-Performance Wide-Span Energy Metering IC 90E21/22/23/24

Version 6
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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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FEATURES

Metering Features

- Metering features fully in compliance with the requirements of IEC62052-11, IEC62053-21 and IEC62053-23; applicable in class 1 or class 2 single-phase watt-hour meter or class 2 single-phase var-hour meter.
- Accuracy of 0.1% for active energy and 0.2% for reactive energy over a dynamic range of 5000:1.
- Temperature coefficient is 15 ppm/ ℃ (typical) for on-chip reference voltage
- Single-point calibration over a dynamic range of 5000:1 for active energy; no calibration needed for reactive energy.
- Energy Meter Constant doubling at low current to save verification time.
- Electrical parameters measurement: less than ±0.5% fiducial error for Vrms, Irms, mean active/ reactive/ apparent power, frequency, power factor and phase angle.
- Forward/ reverse active/ reactive energy with independent energy registers. Active/ reactive energy can be output by pulse or read through energy registers to adapt to different applications.
- Programmable startup and no-load power threshold.
- Dedicated ADC and different gains for L line and N line current sampling circuits. Current sampled over shunt resistor or current transformer (CT); voltage sampled over resistor divider network or potential transformer (PT).
- Programmable L line and N line metering modes: anti-tampering mode (larger power), L line mode (fixed L line), L+N mode (applicable for single-phase three-wire system) and flexible mode (configure through register).
- Programmable L line and N line power difference threshold in anti-tampering mode.

Other Features

- 3.3V single power supply. Operating voltage range: 2.8~3.6V. Metering accuracy guaranteed within 3.0V~3.6V. 5V compatible for digital input.
- Built-in hysteresis for power-on reset.
- Four-wire SPI interface or simplified three-wire SPI interface with fixed 24 cycles for all registers operation
- Parameter diagnosis function and programmable interrupt output of the IRQ interrupt signal and the WarnOut signal.
- Programmable voltage sag detection and zero-crossing output.
- Channel input range
  - Voltage channel (when gain is '1'): 120μVrms~600mVrms.
  - L line current channel (when gain is '24'): 5μVrms~25mVrms.
  - N line current channel (when gain is '1'): 120μVrms~600mVrms.
- Programmable L line current gain: 1, 4, 8, 16, 24; Programmable N line gain: 1, 2, 4.
- Support L line and N line offset compensation.
- CF1 and CF2 output active and reactive energy pulses respectively which can be used for calibration or energy accumulation.
- Crystal oscillator frequency: 8.192 MHz. On-chip 10pF capacitors and no need of external capacitors.
- Green SSOP28 package.
- Operating temperature: -40 ℃ ~ +85 ℃ .

APPLICATION

- The 90E21/22/23/24 series are used for active and reactive energy metering for single-phase two-wire, single-phase three-wire or anti-tampering energy meters. With the measurement function, the 90E21/22/23/24 series can also be used in power instruments which need to measure voltage, current, etc.

DESCRIPTION

The 90E21/22/23/24 series are high-performance wide-span energy metering chips. The ADC and DSP technology ensure the chips' long-term stability over variations in grid and ambient environmental conditions.

Table-1 Function List

Part Number	Active Energy Metering	Reactive Energy Metering	N Line Metering	Electrical Parameters Measurement
90E21	√			√
90E22	√	√		√
90E23	√		√	√
90E24	√	√	√	√

90E21/22/23/24 are all of green SSOP28 package with the same pin alignment. In this datasheet, all reactive energy metering parts are only applicable for the 90E22/24, and all N line metering and measurement parts are only applicable for the 90E23/24.

BLOCK DIAGRAM

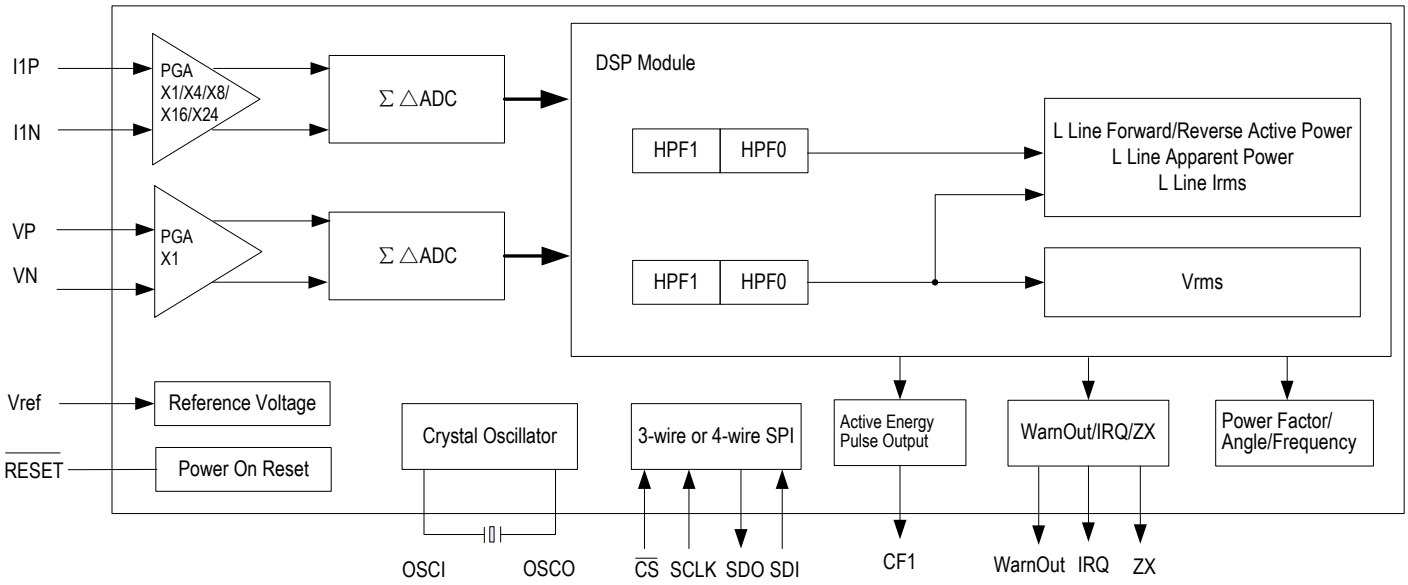

Figure-1 90E21 Block Diagram

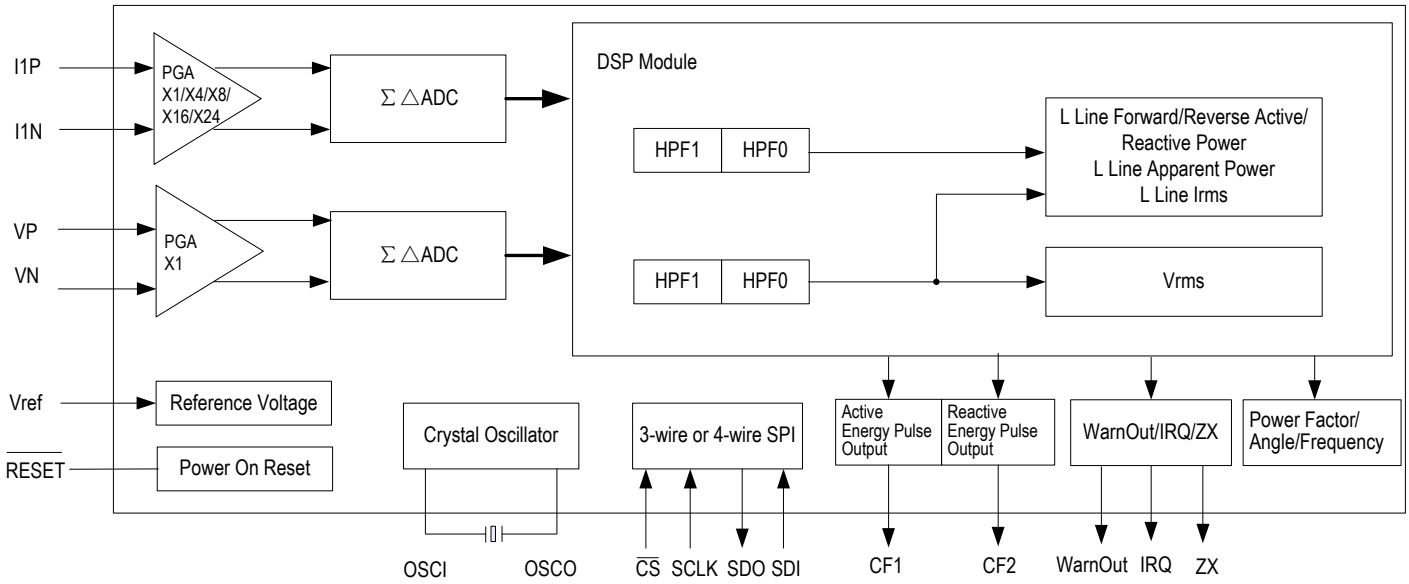

Figure-2 90E22 Block Diagram

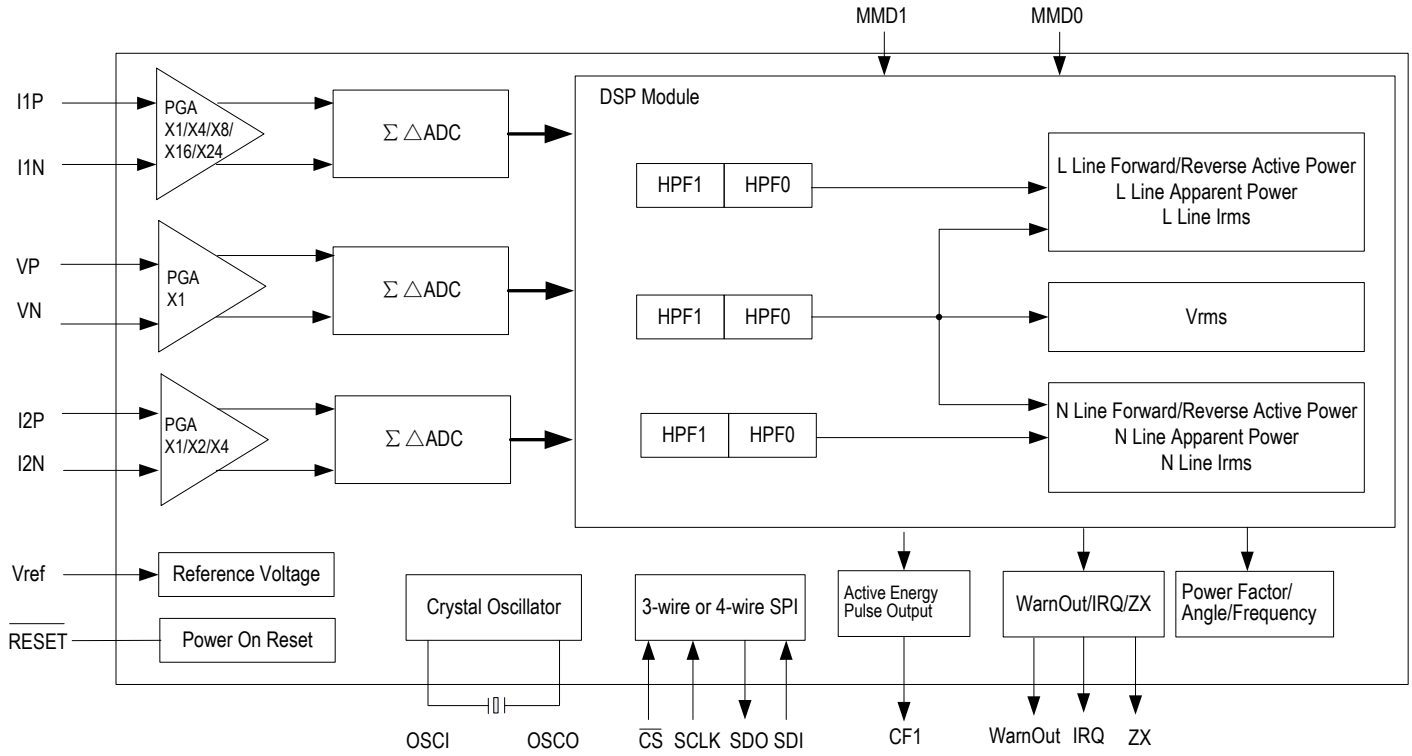

Figure-3 90E23 Block Diagram

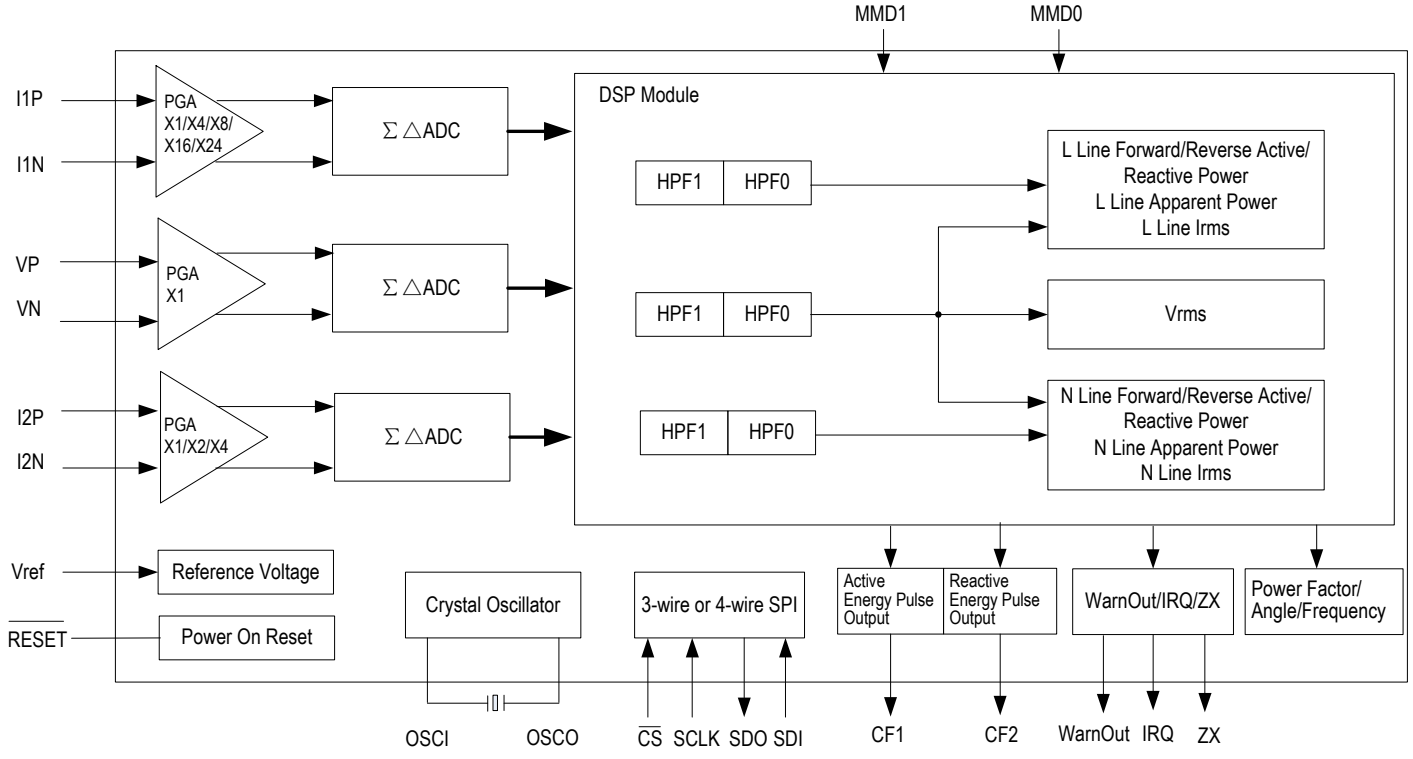

Figure-4 90E24 Block Diagram

1 PIN ASSIGNMENT

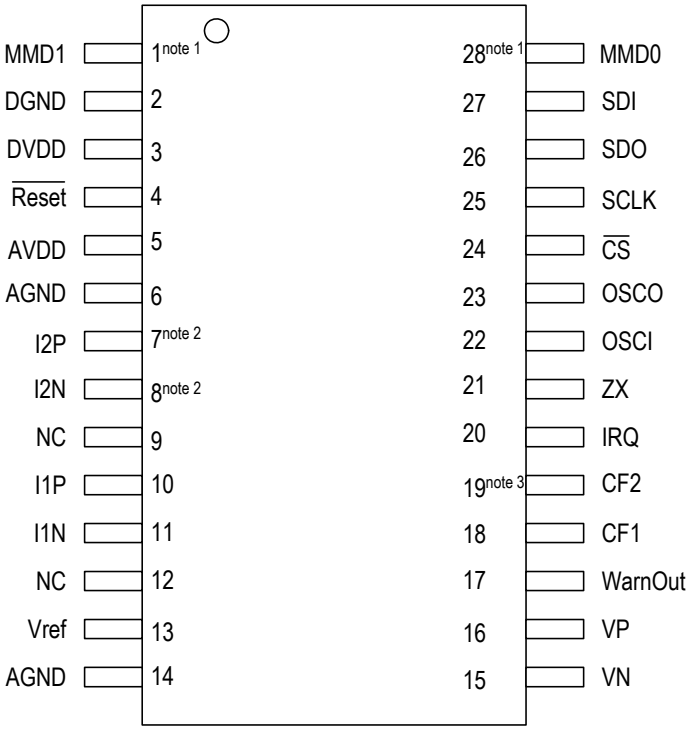

Figure-5 Pin Assignment (Top View)

Note 1: Pin 1 and 28 are dedicated for the 90E23/24. Pin 1 should connect to DGND and pin 28 should connect to DVDD for 90E21/22.

Note 2: Pin 7 and 8 are dedicated for the 90E23/24. They should be left open for the 90E21/22.

Note 3: Pin 19 is dedicated for the 90E22/24. It should be left open for the 90E21/23.

2 PIN DESCRIPTION

Table-2 Pin Description

Name	Pin No.	I/O [note 1]	Type	Description
$\overline{\text{Reset}}$	4	I	LVTTL	**$\overline{\text{Reset}}$: Reset Pin (active low)** This pin should connect to ground through a 0.1μF filter capacitor. In application it can also directly connect to one output pin from microcontroller (MCU).
DVDD	3	I	Power	**DVDD: Digital Power Supply** This pin provides power supply to the digital part. It should be decoupled with a 10μF electrolytic capacitor and a 0.1μF capacitor.
DGND	2	I	Power	**DGND: Digital Ground**
AVDD	5	I	Power	**AVDD: Analog Power Supply** This pin provides power supply to the analog part. This pin should connect to DVDD through a 10Ω resistor and be decoupled with a 0.1μF capacitor.
Vref	13	O	Analog	**Vref: Output Pin for Reference Voltage** This pin should be decoupled with a 1μF capacitor and a 1nF capacitor.
AGND	6, 14	I	Power	**AGND: Analog Ground**
I1P I1N	10 11	I	Analog	**I1P: Positive Input for L Line Current** **I1N: Negative Input for L Line Current** These pins are differential inputs for L line current. Input range is 5μVrms~25mVrms when gain is '24'.
I2P I2N	7 8	I	Analog	**I2P: Positive Input for N Line Current** **I2N: Negative Input for N Line Current** These pins are differential inputs for N line current. Input range is 120μVrms~600mVrms when gain is '1'. **Note:** I2P and I2N are dedicated for the 90E23/24. They should be left open for the 90E21/22.
VP VN	16 15	I	Analog	**VP: Positive Input for Voltage** **VN: Negative Input for Voltage** These pins are differential inputs for voltage. Input range is 120μVrms~600mVrms.
NC	9, 12			**NC: This pin should be left open.**
$\overline{\text{CS}}$	24	I	LVTTL	**$\overline{\text{CS}}$: Chip Select (Active Low)** In 4-wire SPI mode, this pin must be driven from high to low for each read/write operation, and maintain low for the entire operation. In 3-wire SPI mode, this pin must be low all the time. Refer to section 4.1.
SCLK	25	I	LVTTL	**SCLK: Serial Clock** This pin is used as the clock for the SPI interface. Data on SDI is shifted into the chip on the rising edge of SCLK while data on SDO is shifted out of the chip on the falling edge of SCLK.
SDO	26	OZ	LVTTL	**SDO: Serial Data Output** This pin is used as the data output for the SPI interface. Data on this pin is shifted out of the chip on the falling edge of SCLK.
SDI	27	I	LVTTL	**SDI: Serial Data Input** This pin is used as the data input for the SPI interface. Address and data on this pin is shifted into the chip on the rising edge of SCLK.
MMD1 MMD0	1 28	I	LVTTL	**MMD1/0: Metering Mode Configuration** 00: anti-tampering mode (larger power); 01: L line mode (fixed L line); 10: L+N mode (applicable for single-phase three-wire system); 11: flexible mode (line specified by the LNSel bit (MMode, 2BH)) **Note:** The MMD1/0 pins are dedicated for the 90E23/24. For the 90E21/22, the metering mode is fixed as L line mode, and MMD1 should connect to DGND and MMD0 should connect to DVDD.

Table-2 Pin Description (Continued)

Name	Pin No.	I/O note 1	Type	Description
OSCI	22	I	LVTTL	**OSCI: External Crystal Input** An 8.192 MHz crystal is connected between OSCI and OSCO. There is an on-chip 10pF capacitor, therefore no need of external capacitors.
OSCO	23	O	LVTTL	**OSCO: External Crystal Output** An 8.192 MHz crystal is connected between OSCI and OSCO. There is an on-chip 10pF capacitor, therefore no need of external capacitors.
CF1 CF2	18 19	O	LVTTL	**CF1: Active Energy Pulse Output** **CF2: Reactive Energy Pulse Output** These pins output active/reactive energy pulses. **Note:** CF2 is dedicated for the 90E22/24. It should be left open for the 90E21/23.
ZX	21	O	LVTTL	**ZX: Voltage Zero-Crossing Output** This pin is asserted when voltage crosses zero. Zero-crossing mode can be configured to positive zero-crossing, negative zero-crossing or all zero-crossing by the Zxcon[1:0] bits (MMode, 2BH).
IRQ	20	O	LVTTL	**IRQ: Interrupt Output** This pin is asserted when one or more events in the SysStatus register (01H) occur. It is deasserted when there is no bit set in the SysStatus register (01H).
WarnOut	17	O	LVTTL	**WarnOut: Fatal Error Warning** This pin is asserted when there is metering parameter calibration error or voltage sag. Refer to section 4.2.
Note 1: All digital inputs are 5V tolerant except for the OSCI pin.				

3 FUNCTIONAL DESCRIPTION

3.1 DYNAMIC METERING RANGE

Accuracy is 0.1% for active energy metering and 0.2% for reactive energy metering over a dynamic range of 5000:1 (typical). Refer to Table-3 and Table-4.

Table-3 Active Energy Metering Error

Current	Power Factor	Error(%)
20mA ⩽ I < 50mA	1.0	±0.2
50mA ⩽ I ⩽ 100A		±0.1
50mA ⩽ I < 100mA	0.5 (Inductive) 0.8 (Capacitive)	±0.2
100mA ⩽ I ⩽ 100A		±0.1
Note: Shunt resistor is 250 μΩ or CT ratio is 1000:1 and load resistor is 6Ω.		

Table-4 Reactive Energy Metering Error

Current	sinϕ (Inductive or Capacitive)	Error(%)
20mA ⩽ I < 50mA	1.0	±0.4
50mA ⩽ I ⩽ 100A		±0.2
50mA ⩽ I < 100mA	0.5	±0.4
100mA ⩽ I ⩽ 100A		±0.2
Note: Shunt resistor is 250 μΩ or CT ratio is 1000:1 and load resistor is 6Ω.		

3.2 STARTUP AND NO-LOAD POWER

Startup and no-load power thresholds are programmable, both for active and reactive power. The related registers are listed in Table-5.

Table-5 Threshold Configuration for Startup and No-Load Power

Threshold	Register
Threshold for Active Startup Power	PStartTh, 27H
Threshold for Active No-load Power	PNolTh, 28H
Threshold for Reactive Startup Power	QStartTh, 29H
Threshold for Reactive No-load Power	QNolTh, 2AH

The chip will start within 1.2 times of the theoretical startup time of the configured startup power, if startup power is less than the corresponding power of 20mA when power factor or sinϕ is 1.0.

The chip has no-load status bits, the Pnoload/Qnoload bit (EnStatus, 46H). The chip will not output any active pulse (CF1) in active no-load state. The chip will not output any reactive pulse (CF2) in reactive no-load state.

3.3 ENERGY REGISTERS

The 90E21/22/23/24 provides energy pulse output CFx (CF1/CF2) which is proportionate to active/reactive energy. Energy is usually accumulated by adding the CFx pulses in system applications. Alternatively, the 90E21/22/23/24 provides energy registers. There are forward (inductive), reverse (capacitive) and absolute energy registers for both active and reactive energy. Refer to Table-6.

Table-6 Energy Registers

Energy	Register
Forward Active Energy	APenergy, 40H
Reverse Active Energy	ANenergy, 41H
Absolute Active Energy	ATenergy, 42H
Forward (Inductive) Reactive Energy	RPenergy, 43H
Reverse (Capacitive) Reactive Energy	RNenergy, 44H
Absolute Reactive Energy	RTenergy, 45H

Each energy register is cleared after read. The resolution of energy registers is 0.1CF, i.e. one LSB represents 0.1 energy pulse.

3.4 N LINE METERING AND ANTI-TAMPERING

3.4.1 METERING MODE AND L/N LINE CURRENT SAMPLING GAIN CONFIGURATION

The 90E23 and 90E24 have two current sampling circuits with N line metering and anti-tampering functions. The MMD1 and MMD0 pins are used to configure the metering mode. Refer to Table-7.

Table-7 Metering Mode

MMD1	MMD0	Metering Mode	CFx (CF1 or CF2) Output
0	0	Anti-tampering Mode (larger power)	CFx represents the larger energy line. Refer to section 3.4.2.
0	1	L Line Mode (fixed L line)	CFx represents L line energy all the time.
1	0	L+N Mode (applicable for single-phase three-wire system)	CFx represents the arithmetic sum of L line and N line energy
1	1	Flexible Mode (line specified by the LNSel bit (MMode, 2BH))	CFx represents energy of the specified line.

The 90E23 and 90E24 have two current sampling circuits with different gain configurations. L line gain can be 1, 4, 8, 16 and 24, and N line gain can be 1, 2 and 4. The configuration is made by the MMode register (2BH). Generally L line can be sampled over shunt resistor or CT. N line can be sampled over CT for isolation consideration. Note that Rogowski coil is not supported.

3.4.2 ANTI-TAMPERING MODE

Threshold

In anti-tampering mode, the power difference threshold between L line and N line can be: 1%, 2%,... 12%, 12.5%, 6.25%, 3.125% and 1.5625%, altogether 16 choices. The configuration is made by the Pthresh[3:0] bits (MMode, 2BH) and the default value is 3.125%. The threshold is applicable for active energy. The metering line of the reactive energy follows that of the active energy.

Compare Method

In anti-tampering mode, the compare method is as follows:

If current metering line is L line and

$$\frac{\text{N Line Active Power - L Line Active Power}}{\text{L Line Active Power}} * 100\% > \text{Threshold}$$

N line is switched as the metering line, otherwise L line keeps as the metering line.

If current metering line is N line and

$$\frac{\text{L Line Active Power - N Line Active Power}}{\text{N Line Active Power}} * 100\% > \text{Threshold}$$

L line is switched as the metering line, otherwise N line keeps as the metering line.

This method can achieve hysteresis around the threshold automatically. L line is employed after reset by default.

Special Treatment at Low Power

When power is low, general factors such as the quantization error or calibration difference between L line and N line might cause the power difference to be exceeded. To ensure L line and N line to start up normally, special treatment as follows is adopted:

The line with higher power is selected as the metering line when both L line and N line power are lower than 8 times of the startup power but higher than the startup power.

3.5 MEASUREMENT AND ZERO-CROSSING

3.5.1 MEASUREMENT

The 90E21/22/23/24 has the following measurements:

- voltage rms
- current rms (L line/N line)
- mean active power (L line/N line)
- mean reactive power (L line/N line)
- voltage frequency
- power factor (L line/N line)
- phase angle between voltage and current (L line/N line)
- mean apparent power (L line/N line)

The above measurements are all calculated with fiducial error except for frequency. The frequency accuracy is 0.01Hz, and the other measurement accuracy is 0.5%. Fiducial error is calculated as follow:

$$\text{Fiducial\_Error} = \frac{U_{mea} - U_{real}}{U_{FV}} * 100\%$$

Where U_{mea} is the measured voltage, U_{real} is the actual voltage and U_{FV} is the fiducial value.

Table-8 The Measurement Format

Measurement	Fiducial Value (FV)	90E21/22/23/24 Defined Format	Range	Comment
Voltage rms	Un	XXX.XX	0~655.35V	
Current rms[note 1, note 2]	Imax as 4Ib	XX.XXX	0~65.535A	
Active/ Reactive Power[note 1]	maximum power as Un*4Ib	XX.XXX	-32.768~+32.767 kW/kvar	Complement, MSB as the sign bit
Apparent Power[note 1]	Un*4Ib	XX.XXX	0~+32.767 kVA	Complement, MSB always '0'
Frequency	fn	XX.XX	45.00~65.00 Hz	
Power Factor[note 3]	1.000	X.XXX	-1.000~+1.000	Signed, MSB as the sign bit
Phase Angle[note 4]	180°	XXX.X	-180°~+180°	Signed, MSB as the sign bit

Note 1: All registers are of 16 bits. For cases when the current and active/reactive/apparent power goes beyond the above range, it is suggested to be handled by microcontroller (MCU) in application. For example, register value can be calibrated to 1/2 of the actual value during calibration, then multiply 2 in application. Note that if the actual current is twice of that of the 90E21/22/23/24, the actual active/reactive/apparent power is also twice of that of the chip.
Note 2: The accuracy is not guaranteed when the current is lower than 15mA. Note that the tolerance is 25 mA at I_{FV} of 5A and fiducial accuracy of 0.5%.
Note 3: Power factor is obtained by active power dividing apparent power
Note 4: Phase angle is obtained when voltage/current crosses zero at the frequency of 256kHz. Precision is not guaranteed at small current.

3.5.2 ZERO-CROSSING

The ZX pin is asserted when the sampling voltage crosses zero. Zero-crossing mode can be configured to positive zero-crossing, negative zero-crossing and all zero-crossing by the Zxcon[1:0] bits (MMode, 2BH). Refer to section 6.4.

The zero-crossing signal can facilitate operations such as relay operation and power line carrier transmission in typical smart meter applications.

3.6 CALIBRATION

Metering Calibration

Only single-point calibration is needed over the entire dynamic range.

Metering calibration is realized by first calibrating gain at unity power factor and then calibrating phase angle compensation at 0.5 inductive power factor.

However, due to very small signal in L line current sampling circuits, any external interference, e.g., a tens of nano volts influence voltage on shunt resistor conducted by transformer in the energy meter's power supply may cause perceptible metering error, especially in low current state. For this nearly constant external interference, the 90E21/22/23/24 also provides power offset compensation.

L line and N line need to be calibrated sequentially. Reactive does not need to be calibrated.

Measurement Calibration

Measurement calibration is realized by calibrating the gains for voltage rms and current rms. Considering the possible nonlinearity around zero caused by external components, the chip also provides offset compensation for voltage rms, current rms, mean active power and mean reactive power.

Frequency, phase angle and power factor do not need calibration.

For more calibration details, please refer to Application Note AN-641.

3.7 RESET

The 90E21/22/23/24 has an on-chip power supply monitor circuit with built-in hysteresis. The 90E21/22/23/24 only works within the voltage range.

The 90E21/22/23/24 has three means of reset: power-on reset, hardware reset and software reset. All registers resume to their default value after reset.

Power-on Reset: Power-on reset is initiated during power-up. Refer to section 6.3.

Hardware Reset: Hardware Reset is initiated when the $\overline{\text{reset}}$ pin is pulled low. The width of the reset signal should be over 200μs.

Software Reset: Software Reset is initiated when '789AH' is written to the software reset register (SoftReset, 00H).

4 INTERFACE

4.1 SERIAL PERIPHERAL INTERFACE (SPI)

SPI is a full-duplex, synchronous channel. There are two SPI modes: four-wire mode and three-wire mode. In four-wire mode, four pins are used: $\overline{CS}$, SCLK, SDI and SDO. In three-wire mode, three pins are used: SCLK, SDI and SDO. Data on SDI is shifted into the chip on the rising edge of SCLK while data on SDO is shifted out of the chip on the falling edge of SCLK. The LastSPIData register (06H) stores the 16-bit data that is just read or written.

4.1.1 FOUR-WIRE MODE

In four-wire mode, the $\overline{CS}$ pin must be driven low for the entire read or write operation. The first bit on SDI defines the access type and the lower 7-bit is decoded as address.

Read Sequence

As shown in Figure-6, a read operation is initiated by a high on SDI followed by a 7-bit register address. A 16-bit data in this register is then shifted out of the chip on SDO. A complete read operation contains 24 cycles.

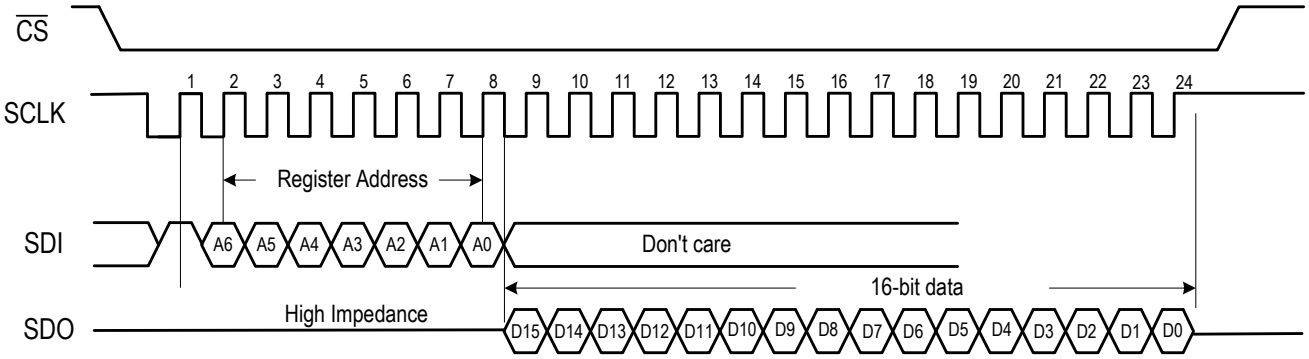

Figure-6 Read Sequence in Four-Wire Mode

Write Sequence

As shown in Figure-7, a write operation is initiated by a low on SDI followed by a 7-bit register address. A 16-bit data is then shifted into the chip on SDI. A complete write operation contains 24 cycles.

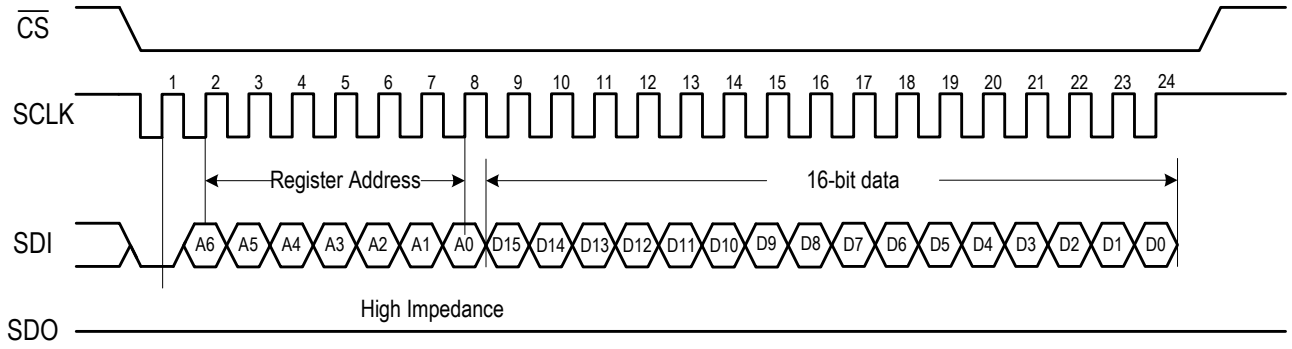

Figure-7 Write Sequence in Four-Wire Mode

4.1.2 THREE-WIRE MODE

In three-wire mode, $\overline{CS}$ is always at low level. When there is no operation, SCLK keeps at high level. The start of a read or write operation is triggered if SCLK is consistently low for at least 400µs. The subsequent read or write operation is similar to that in four-wire mode. Refer to Figure-8 and Figure-9.

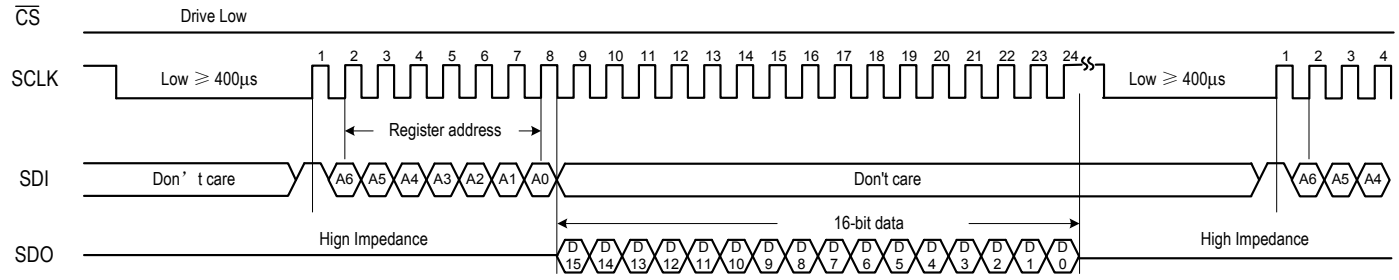

Figure-8 Read Sequence in Three-Wire Mode

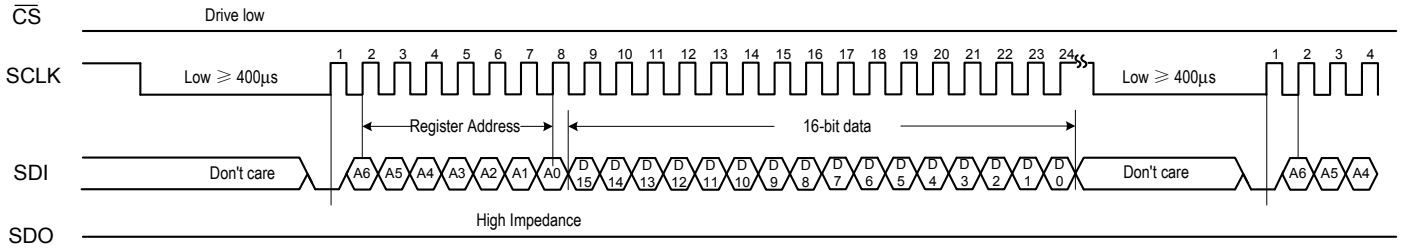

Figure-9 Write Sequence in Three-Wire Mode

4.1.3 TIMEOUT AND PROTECTION

Timeout occurs if SCLK does not toggle for 6ms in both four-wire and three-wire modes. When timeout, the read or write operation is aborted.

If there are more than 24 SCLK cycles when $\overline{CS}$ is driven low in four-wire mode or between two starts in three-wire mode, writing operation is prohibited while normal reading operation can be completed by taking the first 24 SCLK cycles as the valid ones. However, the reading result might not be the intended one.

A read access to an invalid address returns all zero. A write access to an invalid address is discarded.

Table-9 and Table-10 list the read or write result in different conditions.

Table-9 Read / Write Result in Four-Wire Mode

Condition			Result	
Operation	Timeout	SCLK Cycles[note 1]	Read/Write Status	LastSPIData Register Update
Read	-[note 2]	>=24	Normal Read	Yes
	-[note 2]	<24	Partial Read	No
Write	No	=24	Normal Write	Yes
	No	!=24	No Write	No
	Yes	-	No Write	No

Note 1: The number of SCLK cycles when $\overline{CS}$ is driven low or the number of SCLK cycles before timeout if any.
Note 2: '-' stands for Don't Care.

Table-10 Read / Write Result in Three-Wire Mode

Condition			Result	
Operation	Timeout	SCLK Cycles[note 1]	Read/Write Status	LastSPIData Register Update
Read	No	>=24[note 2]	Normal Read	Yes
	Timeout after 24 cycles	>24	Normal Read	Yes
	Timeout before 24 cycles	-[note 3]	Partial Read	No
	Timeout at 24 cycles	=24	Normal Read	Yes
Write	No	=24	Normal Write	Yes
	No	!=24	No Write	No
	Yes	-	No Write	No

Note 1: The number of SCLK cycles between 2 starts or the number of SCLK cycles before timeout if any.
Note 2: There is no such case of less than 24 SCLK cycles when there is no timeout in three-wire mode, because the first few SCLK cycles in the next operation is counted into this operation. In this case, data is corrupted.
Note 3: '-' stands for Don't Care.

4.2 WARNOUT PIN FOR FATAL ERROR WARNING

Fatal error warning is raised through the WarnOut pin in two cases: checksum calibration error and voltage sag.

Calibration Error

The 90E21/22/23/24 performs diagnosis on a regular basis for important parameters such as calibration parameters and metering configuration. When checksum is not correct, the CalErr[1:0] bits (SysStatus, 01H) are set, and both the WarnOut pin and the IRQ pin are asserted. When checksum is not correct, the metering part does not work to prevent a large number of pulses during power-on or any abnormal situation upon incorrect parameters.

Voltage Sag

Voltage sag is detected when voltage is continuously below the voltage sag threshold for one cycle which starts from any zero-crossing point. Voltage threshold is configured by the SagTh register (03H). Refer to section 6.5.

When voltage sag occurs, the SagWarn bit (SysStatus, 01H) is set and the WarnOut pin is asserted if the FuncEn register (02H) enables voltage sag warning through the WarnOut pin. This function helps reduce power-down detection circuit in system design. In addition, the method of judging voltage sag by detecting AC side voltage eliminates the influence of large capacitor in traditional rectifier circuit, and can detect voltage sag earlier.

4.3 LOW COST IMPLEMENTATION IN ISOLATION WITH MCU

The following functions can be achieved at low cost when the 90E21/22/23/24 is isolated from the MCU:

SPI: MCU can perform read and write operations through low speed optocoupler (e.g. NEC2501) when the 90E21/22/23/24 is isolated from the MCU. The SPI interface can be of 3-wire or 4-wire.

Energy Pulses CFx: Energy can be accumulated by reading values in corresponding energy registers. CFx can also connect to the optocoupler and the energy pulse light can be turned on by CFx.

Fatal Error WarnOut: Fatal error can be acquired by reading the CalErr[1:0] bits (SysStatus, 01H).

IRQ: IRQ interrupt can be acquired by reading the SysStatus register (01H).

Reset: The 90E21/22/23/24 is reset when '789AH' is written to the software reset register (SoftReset, 00H).

5 REGISTER

5.1 REGISTER LIST

Table-11 Register List

Register Address	Register Name	Read/Write Type	Functional Description	Comment[note 1]	Page
Status and Special Register					
00H	SoftReset	W	Software Reset		P 21
01H	SysStatus	R/C	System Status	different for various chips[note 2, note 3]	P 22
02H	FuncEn	R/W	Function Enable	different for various chips[note 2]	P 23
03H	SagTh	R/W	Voltage Sag Threshold		P 23
04H	SmallPMod	R/W	Small-Power Mode		P 24
06H	LastSPIData	R	Last Read/Write SPI Value		P 24
Metering Calibration and Configuration Register					
20H	CalStart	R/W	Calibration Start Command		P 25
21H	PLconstH	R/W	High Word of PL_Constant		P 25
22H	PLconstL	R/W	Low Word of PL_Constant		P 26
23H	Lgain	R/W	L Line Calibration Gain		P 26
24H	Lphi	R/W	L Line Calibration Angle		P 26
25H	Ngain	R/W	N Line Calibration Gain	Not applicable to the 90E21/22[note 3]	P 27
26H	Nphi	R/W	N Line Calibration Angle	Not applicable to the 90E21/22[note 3]	P 27
27H	PStartTh	R/W	Active Startup Power Threshold		P 27
28H	PNolTh	R/W	Active No-Load Power Threshold		P 28
29H	QStartTh	R/W	Reactive Startup Power Threshold	Not applicable to the 90E21/23[note 2]	P 28
2AH	QNolTh	R/W	Reactive No-Load Power Threshold	Not applicable to the 90E21/23[note 2]	P 28
2BH	MMode	R/W	Metering Mode Configuration	different for various chips[note 2, note 3]	P 29
2CH	CS1	R/W	Checksum 1		P 31
Measurement Calibration Register					
30H	AdjStart	R/W	Measurement Calibration Start Command		P 32
31H	Ugain	R/W	Voltage rms Gain		P 32
32H	IgainL	R/W	L Line Current rms Gain		P 33
33H	IgainN	R/W	N Line Current rms Gain	Not applicable to the 90E21/22[note 3]	P 33
34H	Uoffset	R/W	Voltage Offset		P 33
35H	IoffsetL	R/W	L Line Current Offset		P 34
36H	IoffsetN	R/W	N Line Current Offset	Not applicable to the 90E21/22[note 3]	P 34
37H	PoffsetL	R/W	L Line Active Power Offset		P 34
38H	QoffsetL	R/W	L Line Reactive Power Offset	Not applicable to the 90E21/23[note 2]	P 35
39H	PoffsetN	R/W	N Line Active Power Offset	Not applicable to the 90E21/22[note 3]	P 35
3AH	QoffsetN	R/W	N Line Reactive Power Offset	Not applicable to the 90E21/22/23[note 2, note 3]	P 35
3BH	CS2	R/W	Checksum 2		P 36
Energy Register					
40H	APenergy	R/C	Forward Active Energy		P 37

Table-11 Register List (Continued)

Register Address	Register Name	Read/Write Type	Functional Description	Comment[note 1]	Page
41H	ANenergy	R/C	Reverse Active Energy		P 37
42H	ATenergy	R/C	Absolute Active Energy		P 38
43H	RPenergy	R/C	Forward (Inductive) Reactive Energy	Not applicable to the 90E21/23[note 2]	P 38
44H	RNenergy	R/C	Reverse (Capacitive) Reactive Energy	Not applicable to the 90E21/23[note 2]	P 39
45H	RTenergy	R/C	Absolute Reactive Energy	Not applicable to the 90E21/23[note 2]	P 39
46H	EnStatus	R	Metering Status	different for various chips[note 2, note 3]	P 40
Measurement Register					
48H	Irms	R	L Line Current rms		P 41
49H	Urms	R	Voltage rms		P 41
4AH	Pmean	R	L Line Mean Active Power		P 42
4BH	Qmean	R	L Line Mean Reactive Power	Not applicable to the 90E21/23[note 2]	P 42
4CH	Freq	R	Voltage Frequency		P 43
4DH	PowerF	R	L Line Power Factor		P 43
4EH	Pangle	R	Phase Angle between Voltage and L Line Current		P 43
4FH	Smean	R	L Line Mean Apparent Power		P 44
68H	Irms2	R	N Line Current rms	Not applicable to the 90E21/22[note 3]	P 44
6AH	Pmean2	R	N Line Mean Active Power	Not applicable to the 90E21/22[note 3]	P 45
6BH	Qmean2	R	N Line Mean Reactive Power	Not applicable to the 90E21/22/23[note 2, note 3]	P 45
6DH	PowerF2	R	N Line Power Factor	Not applicable to the 90E21/22[note 3]	P 46
6EH	Pangle2	R	Phase Angle between Voltage and N Line Current	Not applicable to the 90E21/22[note 3]	P 46
6FH	Smean2	R	N Line Mean Apparent Power	Not applicable to the 90E21/22[note 3]	P 47

Note:
1. This register list shows all registers for the 90E24.
2. This register is related to reactive energy metering. Part of this register is invalid for the 90E21/23 which does not have reactive metering. Reading these registers always return 0000H and writing these registers always take no effect.
3. This register is related to N line metering. Part of this register is invalid for the 90E21/22 which does not have N line metering. Reading these registers always return 0000H and writing these registers always have no effect.

5.2 STATUS AND SPECIAL REGISTER

SoftReset
Software Reset

Address: 00H
Type: Write
Default Value: 0000H

15	14	13	12	11	10	9	8
SoftReset15	SoftReset14	SoftReset13	SoftReset12	SoftReset11	SoftReset10	SoftReset9	SoftReset8
7	6	5	4	3	2	1	0
SoftReset7	SoftReset6	SoftReset5	SoftReset4	SoftReset3	SoftReset2	SoftReset1	SoftReset0

Bit	Name	Description
15 - 0	SoftReset[15:0]	Software reset register. The 90E21/22/23/24 resets if only 789AH is written to this register.

SysStatus
System Status

Address: 01H
Type: Read/Clear
Default Value: 0000H

15	14	13	12	11	10	9	8
CalErr1	CalErr0	AdjErr1	AdjErr0	-	-	-	-
7	6	5	4	3	2	1	0
LNchange	RevQchg	RevPchg	-	-	-	SagWarn	-

Bit	Name	Description
15 - 14	CalErr[1:0]	These bits indicate CS1 checksum status. 00: CS1 checksum correct (default) 11: CS1 checksum error. At the same time, the WarnOut pin is asserted.
13 - 12	AdjErr[1:0]	These bits indicate CS2 checksum status. 00: CS2 checksum correct (default) 11: CS2 checksum error.
11 - 8	-	Reserved.
7	LNchange	This bit indicates whether there is any change of the metering line (L line and N line). 0: metering line no change (default) 1: metering line changed
6	RevQchq	This bit indicates whether there is any change with the direction of reactive energy. 0: direction of reactive energy no change (default) 1: direction of reactive energy changed This status is enabled by the RevQEn bit(FuncEn, 02H).
5	RevPchg	This bit indicates whether there is any change with the direction of active energy. 0: direction of active energy no change (default) 1: direction of active energy changed This status is enabled by the RevPEn bit (FuncEn, 02H).
4 - 2	-	Reserved.
1	SagWarn	This bit indicates the voltage sag status. 0: no voltage sag (default) 1: voltage sag Voltage sag is enabled by the SagEn bit (FuncEn, 02H). Voltage sag status can also be reported by the WarnOut pin. It is enabled by the SagWo bit(FuncEn, 02H).
0	-	Reserved.

Note: Any of the above events will prompt the IRQ pin to be asserted, which can be supplied to external MCU as an interrupt.

FuncEn
Function Enable

Address: 02H
Type: Read/Write
Default Value: 000CH

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	SagEn	SagWo	RevQEn	RevPEn	-	-

Bit	Name	Description
15 - 6	-	Reserved.
5	SagEn	This bit determines whether to enable the voltage sag interrupt. 0: disable (default) 1: enable
4	SagWo	This bit determines whether to enable voltage sag to be reported by the WarnOut pin. 0: disable (default) 1: enable
3	RevQEn	This bit determines whether to enable the direction change interrupt of reactive energy. 0: disable 1: enable (default)
2	RevPEn	This bit determines whether to enable the direction change interrupt of active energy. 0: disable 1: enable (default)
1 - 0	-	Reserved.

SagTh
Voltage Sag Threshold

Address: 03H
Type: Read/Write
Default Value: 1D6AH

15	14	13	12	11	10	9	8
SagTh15	SagTh14	SagTh13	SagTh12	SagTh11	SagTh10	SagTh9	SagTh8
7	6	5	4	3	2	1	0
SagTh7	SagTh6	SagTh5	SagTh4	SagTh3	SagTh2	SagTh1	SagTh0

Bit	Name	Description
15 - 0	SagTh[15:0]	Voltage sag threshold configuration. Data format is XXX.XX. Unit is V. The power-on value of SagTh is 1D6AH, which is calculated by 22000*sqrt(2)*0.78/(4*Ugain/32768) For details, please refer to application note AN-641.

SmallPMod
Small-Power Mode

Address: 04H
Type: Read/Write
Default Value: 0000H

15	14	13	12	11	10	9	8
SmallPMod15	SmallPMod14	SmallPMod13	SmallPMod12	SmallPMod11	SmallPMod10	SmallPMod9	SmallPMod8
7	6	5	4	3	2	1	0
SmallPMod7	SmallPMod6	SmallPMod5	SmallPMod4	SmallPMod3	SmallPMod2	SmallPMod1	SmallPMod0

Bit	Name	Description
15 - 0	SmallPMod[15:0]	Small-power mode command. A987H: small-power mode. The relationship between the register value of L line and N line active/reactive power in small-power mode and normal mode is: power in normal mode = power in small-power mode *10*Igain*Ugain /2^42 Others: Normal mode. Small-power mode is mainly used in the power offset calibration.

LastSPIData
Last Read/Write SPI Value

Address: 06H
Type: Read
Default Value: 0000H

15	14	13	12	11	10	9	8
LastSPIData15	LastSPIData14	LastSPIData13	LastSPIData12	LastSPIData11	LastSPIData10	LastSPIData9	LastSPIData8
7	6	5	4	3	2	1	0
LastSPIData7	LastSPIData6	LastSPIData5	LastSPIData4	LastSPIData3	LastSPIData2	LastSPIData1	LastSPIData0

Bit	Name	Description
15 - 0	LastSPI-Data[15:0]	This register stores the data that is just read or written through the SPI interface. Refer to Table-9 and Table-10.

5.3 METERING/ MEASUREMENT CALIBRATION AND CONFIGURATION

5.3.1 METERING CALIBRATION AND CONFIGURATION REGISTER

CalStart
Calibration Start Command

Address: 20H
Type: Read/Write
Default Value: 6886H

15	14	13	12	11	10	9	8
CalStart15	CalStart14	CalStart13	CalStart12	CalStart11	CalStart10	CalStart9	CalStart8
7	6	5	4	3	2	1	0
CalStart7	CalStart6	CalStart5	CalStart4	CalStart3	CalStart2	CalStart1	CalStart0

Bit	Name	Description
15 - 0	CalStart[15:0]	Metering calibration start command: 6886H: Power-on value. Metering function is disabled. 5678H: Metering calibration startup command. After 5678H is written to this register, registers 21H-2BH resume to their power-on values. The 90E21/22/23/24 starts to meter and output energy pulses regardless of the correctness of diagnosis. The CalErr[1:0] bits (SysStatus, 01H) are not set and the WarnOut/IRQ pins do not report any warning/interrupt. 8765H: Check the correctness of the 21H-2BH registers. If correct, normal metering. If not correct, metering function is disabled, the CalErr[1:0] bits (SysStatus, 01H) are set and the WarnOut/IRQ pins report warning/interrupt. Others: Metering function is disabled. The CalErr[1:0] bits (SysStatus, 01H) are set and the WarnOut/IRQ pins report warning/interrupt.

PLconstH
High Word of PL_Constant

Address: 21H
Type: Read/Write
Default Value: 0015H

15	14	13	12	11	10	9	8
PLconstH15	PLconstH14	PLconstH13	PLconstH12	PLconstH11	PLconstH10	PLconstH9	PLconstH8
7	6	5	4	3	2	1	0
PLconstH7	PLconstH6	PLconstH5	PLconstH4	PLconstH3	PLconstH2	PLconstH1	PLconstH0

Bit	Name	Description
15 - 0	PLconstH[15:0]	The PLconstH[15:0] and PLconstL[15:0] bits are high word and low word of PL_Constant respectively. PL_Constant is a constant which is proportional to the sampling ratios of voltage and current, and inversely proportional to the Meter Constant. PL_Constant is a threshold for energy calculated inside the chip, i.e., energy larger than PL_Constant will be accumulated in the corresponding energy registers and then output on CFx. It is suggested to set PL_constant as a multiple of 4 so as to double or redouble Meter Constant in low current state to save verification time. Note: PLconstH takes effect after PLconstL are configured. For details, please refer to application note AN-641.