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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Poly-Phase High-Performance Wide-Span Energy Metering IC

90E32A

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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FEATURES

Metering Features

- Metering features fully in compliance with the requirements of IEC62052-11, IEC62053-22 and IEC62053-23, ANSI C12.1 and ANSI C12.20; applicable in class 0.5S or class 1 poly-phase watt-hour meter or class 2 poly-phase var-hour meter.
- Accuracy of ±0.1% for active energy and ±0.2% for reactive energy over the dynamic range of 5000:1.
- Temperature coefficient is 6 ppm/ ℃ (typical) for on-chip reference voltage.
- Single-point calibration on each phase over the whole dynamic range for active energy; no calibration needed for reactive/ apparent energy.
- ±1 ℃ (typical) temperature sensor accuracy.
- Electrical parameters measurement: less than ±0.5% fiducial error for Vrms, Irms, mean active/ reactive/ apparent power, frequency, power factor and phase angle.
- Active (forward/reverse), reactive (forward/reverse), apparent energy with independent energy registers. Active/ reactive/ apparent energy can be output by pulse or read through energy registers to adapt to different applications.
- Programmable startup and no-load power threshold, special designed of startup and no-load circuits to eliminate crosstalk among phases achieving better accuracy especially at low power conditions.
- Dedicated ADC and different gains for phase A/B/C current sampling circuits. Current sampled over current transformer (CT) or Rogowski coil (di/dt coil); phase A/B/C voltage sampled over resistor divider network or potential transformer (PT).
- Programmable power modes: Normal mode (N mode), Idle mode (I mode), Detection mode (D mode) and Partial Measurement mode (M mode).
- Fundamental (CF3, 0.2%) and harmonic (CF4, 1%) active energy with dedicated energy and power registers.
- Event detection: sag, phase loss, reverse voltage/ current phase sequence, reverse flow, calculated neutral line current I_{NC} over-current and THD+N over-threshold.

Other Features

- 3.3V single power supply. Operating voltage range: 2.8V~3.6V. Metering accuracy guaranteed within 3.0V~3.6V.
- Four-wire SPI interface.
- Parameter diagnosis function and programmable interrupt output of the IRQ interrupt signals and the WarnOut signal.
- Programmable voltage sag detection and zero-crossing output.
- CF1/CF2/CF3/CF4 output active/ reactive/ apparent energy pulses and fundamental/ harmonic energy pulses respectively.
- Crystal oscillator frequency: 16.384 MHz. On-chip two capacitors and no need of external capacitors.
- TQFP48 package.
- Operating temperature: -40 ℃ ~ +85 ℃ .

APPLICATION

- Poly-phase energy meters of class 0.5S and class 1 which are used in three-phase four-wire (3P4W, Y0) or three-phase three-wire (3P3W, Y or Δ) systems.
- Power monitoring instruments which need to measure voltage, current, mean power, etc.

GENERAL DESCRIPTION

The 90E32A is a poly-phase high performance wide-dynamic range metering IC. The 90E32A incorporates 6 independent 2nd order sigma-delta ADCs, which could be employed in three voltage channels (phase A, B and C) and three current channels (phase A, B, C) in a typical three-phase four-wire system.

The 90E32A has an embedded DSP which executes calculation of active energy, reactive energy, apparent energy, fundamental and harmonic active energy over ADC signal and on-chip reference voltage. The DSP also calculates measurement parameters such as voltage and current RMS value as well as mean active/reactive/apparent power.

A four-wire SPI interface is provided between the 90E32A and the external microcontroller.

The 90E32A is suitable for poly-phase multi-function meters which could measure active/reactive/apparent energy and fundamental/harmonic energy either through four independent energy pulse outputs CF1/CF2/CF3/CF4 or through the corresponding registers.

The ADC and auto-temperature compensation technology for reference voltage ensure the 90E32A's long-term stability over variations in grid and ambient environment conditions.

*Notice: The information in this document is subject to change without notice

BLOCK DIAGRAM

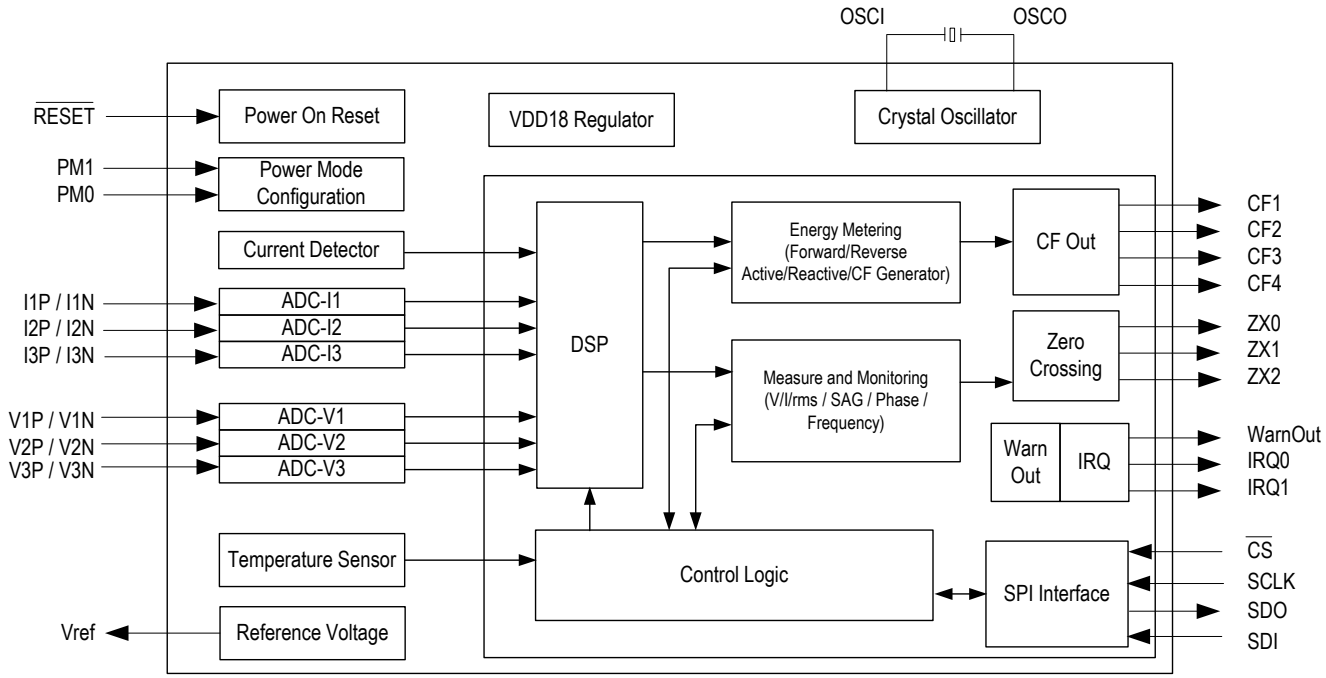

Figure-1 90E32A Block Diagram

1 PIN ASSIGNMENT

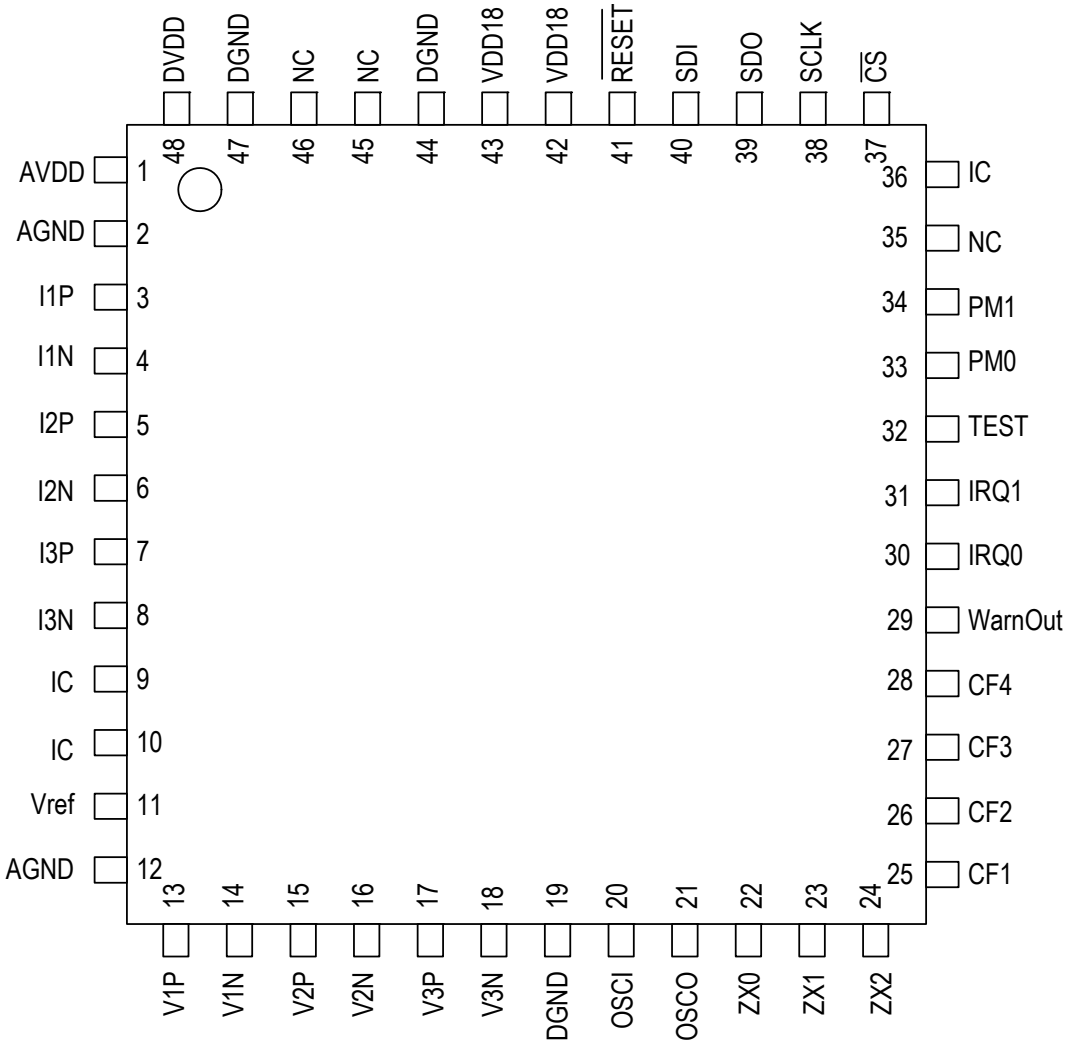

Figure-2 Pin Assignment (Top View)

2 PIN DESCRIPTION

Table-1 Pin Description

Name	Pin No.	I/O	Type	Description
$\overline{\text{Reset}}$	41	I	LVTTL	**$\overline{\text{Reset}}$: Reset Pin (active low)** This pin should connect to ground through a 0.1 μF filter capacitor and a 10kΩ resistor to VDD. In application it can also directly connect to one output pin from microcontroller (MCU).
AVDD	1	I	Power	**AVDD: Analog Power Supply** This pin provides power supply to the analog part. This pin should connect to DVDD and be decoupled with a 0.1μF capacitor.
DVDD	48	I	Power	**DVDD: Digital Power Supply** This pin provides power supply to the digital part. It should be decoupled with a 10μF capacitor and a 0.1μF capacitor.
VDD18	42, 43	P	Power	**VDD18: Digital Power Supply (1.8 V)** These two pins should be connected together and connected to ground through a 10μF capacitor.
DGND	19, 44, 47	I	Power	**DGND: Digital Ground**
AGND	2, 12	I	Power	**AGND: Analog Ground**
I1P I1N	3 4	I	Analog	**I1P: Positive Input for Phase A Current** **I1N: Negative Input for Phase A Current** These pins are differential inputs for phase A current. Note: I1 to phase A and I3 to phase C mapping can be swapped by configuring the I1I3Swap bit (b13, MMode0).
I2P I2N	5 6	I	Analog	**I2P: Positive Input for Phase B Current** **I2N: Negative Input for Phase B Current** These pins are differential inputs for phase B current.
I3P I3N	7 8	I	Analog	**I3P: Positive Input for Phase C Current** **I3N: Negative Input for Phase C Current** These pins are differential inputs for phase C current. Note: I1 to phase A and I3 to phase C mapping can be swapped by configuring the I1I3Swap bit (b13, MMode0).
Vref	11	O	Analog	**Vref: Output Pin for Reference Voltage** This pin should be decoupled with a 10μF capacitor, possibly a 0.1μF ceramic capacitor and a 1nF ceramic capacitor.
V1P V1N	13 14	I	Analog	**V1P: Positive Input for Phase A Voltage** **V1N: Negative Input for Phase A Voltage** These pins are differential inputs for phase A voltage.
V2P V2N	15 16	I	Analog	**V2P: Positive Input for Phase B Voltage** **V2N: Negative Input for Phase B Voltage** These pins are differential inputs for phase B voltage.
V3P V3N	17 18	I	Analog	**V3P: Positive Input for Phase C Voltage** **V3N: Negative Input for Phase C Voltage** These pins are differential inputs for phase C voltage.
OSCI	20	I	OSC	**OSCI: External Crystal Input**
OSCO	21	O	OSC	**OSCO: External Crystal Output** A 16.384 MHz crystal is connected between OSCI and OSCO. There are two on-chip capacitor, therefore no need of external capacitors.
ZX0 ZX1 ZX2	22 23 24	O	LVTTL	**ZX2/ZX1/ZX0:Zero-Crossing Output** These pins are asserted when voltage or current crosses zero. Zero-crossing mode can be configured by the ZXConfig register (07H).
CF1	25	O	LVTTL	**CF1: (all-phase-sum total) Active Energy Pulse Output**
CF2	26	O	LVTTL	**CF2: (all-phase-sum total) Reactive/ Apparent Energy Pulse Output** The output of this pin is determined by the CF2varh bit (b7, MMode0) and the CF2ESV bit (b8, MMode0).

Table-1 Pin Description (Continued)

Name	Pin No.	I/O	Type	Description
CF3	27	O	LVTTL	**CF3: (all-phase-sum total) Active Fundamental Energy Pulse Output**
CF4	28	O	LVTTL	**CF4: (all-phase-sum total) Active Harmonic Energy Pulse Output**
WarnOut	29	O	LVTTL	**WarnOut: Fatal Error Warning** This pin is asserted high when there is metering related parameter checksum error. Otherwise this pin stays low. Refer to 6.2.2 IRQ and WarnOut Signal Generation.
IRQ0	30	O	LVTTL	**IRQ0: Interrupt Output 0** This pin is asserted when one or more events in the SysStatus0 register (01H) occur. It is deasserted when there is no bit set in the SysStatus0 register (01H). In Detection mode, the IRQ0 is used to indicate the output of current detector. The IRQ0 state is cleared when entering or exiting Detection mode.
IRQ1	31	O	LVTTL	**IRQ1: Interrupt Output 1** This pin is asserted when one or more events in the SysStatus1 register (02H) occur. It is deasserted when there is no bit set in the SysStatus1 register (02H). In Detection mode, the IRQ1 is used to indicate the output of current detector. The IRQ1 state is cleared when entering or exiting Detection mode.
PM0 PM1	33 34	I	LVTTL	**PM1/0: Power Mode Configuration** These two pins define the power mode of 90E32A. Refer to Table-2.
$\overline{CS}$	37	I	LVTTL	**$\overline{CS}$: Chip Select (Active Low)** In SPI mode, this pin must be driven from high to low for each read/ write operation, and maintain low for the entire operation.
SCLK	38	I	LVTTL	**SCLK: Serial Clock** This pin is used as the clock for the SPI interface. Refer to 4 SPI Interface.
SDO	39	O	LVTTL	**SDO: Serial Data Output** This pin is used as the data output for the SPI mode. Refer to 4 SPI Interface.
SDI	40	I	LVTTL	**SDI: Serial Data Input** This pin is used as the data input for the SPI mode. Refer to 4 SPI Interface.
TEST	32	I	LVTTL	This pin should be always connected to DGND in system application.
IC	9, 10, 36		LVTTL	These pins should be always connected to DGND in system application.
NC	35, 45, 46			**NC: These pins should be left open.**

3 FUNCTION DESCRIPTION

3.1 POWER SUPPLY

The 90E32A works with single power rail 3.3V. An on-chip voltage regulator regulates the 1.8V voltage for the digital logic.

The regulated 1.8V power is connected to the VDD18 pin. It needs to be bypassed by an external capacitor.

The 90E32A has multiple power modes, in Idle and Detection modes the 1.8V power regulator is not turned on and the digital logic is not powered. When the logic is not powered, all the configured register values are not kept (all context lost) except for Detection mode related registers (10H~13H) for Detection mode configuration.

User has to re-configure the registers in Partial Measurement mode or Normal mode when transiting from Idle or Detection mode. Refer to 3.6 Power Mode for power mode details.

3.2 CLOCK

The 90E32A has an on-chip oscillator and can directly connect to an external crystal.

The OSCI pin can also be driven with a clock source.

The oscillator will be powered down in Idle and Detection power modes, as described in 3.6 Power Mode.

3.3 RESET

There are three reset sources for the 90E32A:

- $\overline{\text{RESET}}$ pin
- On-chip Power On Reset circuit
- Software Reset generated by the Software Reset register

3.3.1 $\overline{\text{RESET}}$ PIN

The $\overline{\text{RESET}}$ pin can be asserted to reset the 90E32A. The $\overline{\text{RESET}}$ pin has RC filter with typical time constant of 2μs in the I/O, as well as a 2μs (typical) de-glitch filter.

Any reset pulse that is shorter than 2μs can not reset the 90E32A.

3.3.2 POWER ON RESET (POR)

The POR circuit resets the 90E32A at power up.

POR circuit triggers reset when:

- DVDD power up, crossing the power-up threshold. Refer to Figure-19.
- VDD18 regulator changing from disable to enable, i.e. from Idle or Detection mode to Partial Measurement mode or Normal mode. Refer to Figure-18.

3.3.3 SOFTWARE RESET

Chip reset can be triggered by writing to the SoftReset register in Normal mode. The software reset is the same as the reset scope generated from the $\overline{\text{RESET}}$ pin or POR.

These three reset sources have the same reset scope.

All digital logics and registers, except for the Harmonic Ratio registers will be subject to reset.

- Interface logic: clock dividers
- Digital core/ logic: All registers except for some other special registers, refer to 6.3.1 Detection Mode Registers.

3.4 METERING FUNCTION

The accumulated energy is converted to pulse frequency on the CF pins and stored in the corresponding energy registers. The 90E32A provides energy accumulation registers with 0.1 or 0.01 CF resolution. 0.01CF / 0.1CF setting is defined by the 001LSB bit (b9, MMode0).

3.4.1 THEORY OF ENERGY REGISTERS

The energy accumulation runs at 1 MHz clock rate, by accumulating the power value calculated by the DSP processor.

The power accumulation process is equivalent to digitally integrating the instantaneous power with a delta-time of about 1us. The accumulated energy is used to calculate the CF pulses and the corresponding internal energy registers.

The accumulated energy is converted to frequency of the CF pulses. One CF usually corresponds to 1KWh / MC (MC is Meter Constant, e.g. 3200 imp/kWh), and is usually referenced as an energy unit in this datasheet. The internal energy resolution for accumulation and conversion is 0.01 CF.

The 0.01 CF pulse energy constant is referenced as 'PL_constant'.

Within 0.01 CF, forward and reverse energy are counteracted. When energy exceeds 0.01 pulse, the respective forward/ reverse energy is increased.

Take the example of active energy, suppose:

T0: Forward energy register is 12.34 pulses and reverse energy register is 1.23 pulses.

From t0 to t1: 0.005 forward pulses appeared.

From t1 to t2: 0.004 reverse pulses appeared.

From t2 to t3: 0.005 reverse pulses appeared.

From t3 to t4: 0.007 reverse pulses appeared.

The following table illustrates the process of energy accumulation process:

	t0	t1	t2	t3	t4
Input energy	+ 0.005	-0.004	-0.005	-0.007	
Bidirectional energy accumulator	0.005	0.001	-0.004	-0.001	
Forward 0.01 CF	0	0	0	0	
Reverse 0.01CF	0	0	0	1	
Forward energy register	12.34	12.34	12.34	12.34	12.34
Reverse energy register	1.23	1.23	1.23	1.23	1.24

When forward/reverse energy reaches 0.1/0.01 pulse, the respective register is updated. When forward or reverse energy reaches 1 pulse, CFx pins output pulse and the REVP/REVQ bits (b7~0, SysStatus1) are updated. Refer to Figure-3.

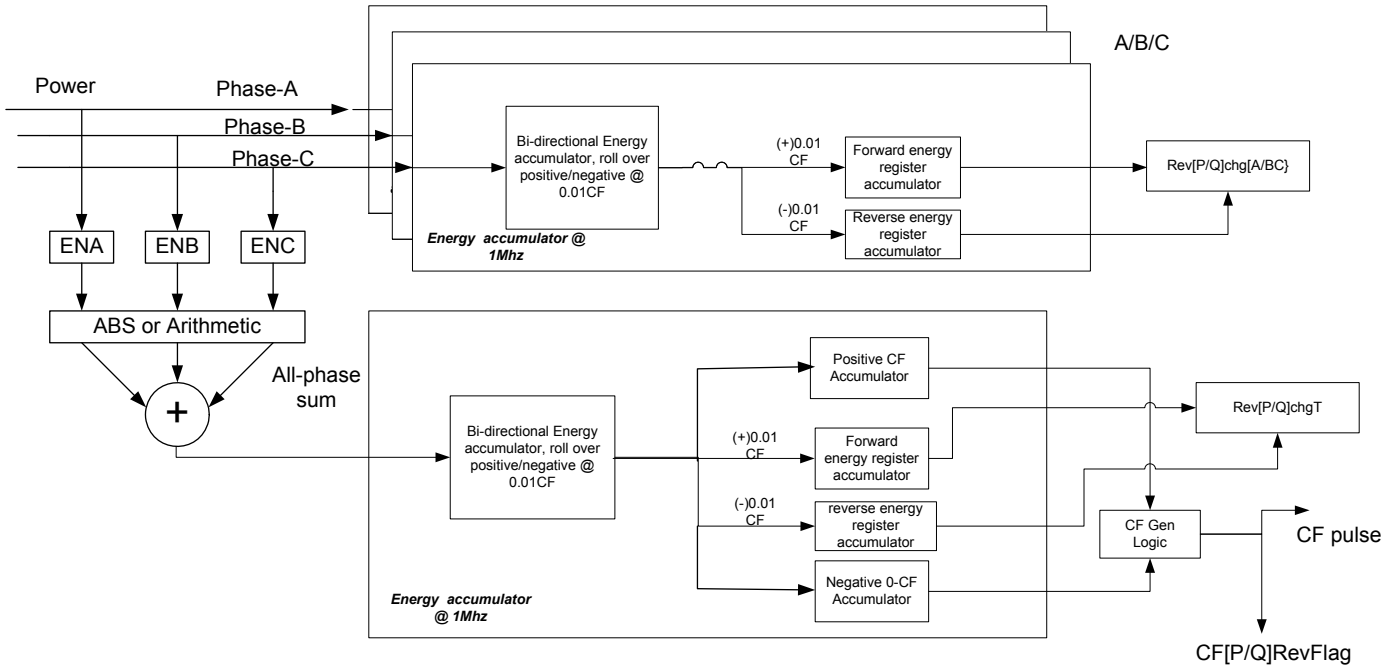

Figure-3 Energy Register Operation Diagram

For all-phase-sum total of active, reactive and (arithmetic sum) apparent energy, the associated power is obtained by summing the power of the three phases. The accumulation method of all-phase-sum energy is determined by the EnPC/EnPB/EnPA/ABSEnP/ABSEnQ bits (b0~b4, MMode0).

Note that the direction of all-phase-sum power and single-phase power might be different.

3.4.2 ENERGY REGISTERS

The 90E32A meters non-decomposed total active, reactive and apparent energy, as well as decomposed active fundamental and harmonic energy. The registers are listed as below.

3.4.2.1 Total Energy Registers

Each phase and all-phase-sum has the following registers:

- Active forward/ reverse
- Reactive forward/ reverse
- Apparent energy

Altogether there are 20 energy registers. Those registers are defined in 6.5.1 Regular Energy Registers.

3.4.2.2 Fundamental and Harmonic Energy Registers

The 90E32A counts decomposed active fundamental and harmonic energy. Reactive energy is not decomposed to fundamental and harmonic.

The fundamental/harmonic energy is accumulated in the same way as active energy accumulation method described above.

Registers:

- Fundamental / harmonic
- all-phase-sum / phase A / phase B / phase C
- Forward / reverse

Altogether there are 16 energy registers. Refer to 3.4.2.2 Fundamental and Harmonic Energy Registers.

3.4.3 ENERGY PULSE OUTPUT

CF1 is fixed to be total active energy output (all-phase-sum). Both forward and reverse energy registers can generate the CF pulse (change of forward/ reverse direction can generate an interrupt if enabled).

CF2 is reactive energy output (all-phase-sum) by default. It can also be configured to be arithmetic sum apparent energy output (all-phase-sum).

CF3 is fixed to be active fundamental energy output (all-phase-sum).

CF4 is fixed to be active harmonic energy output (all-phase-sum).

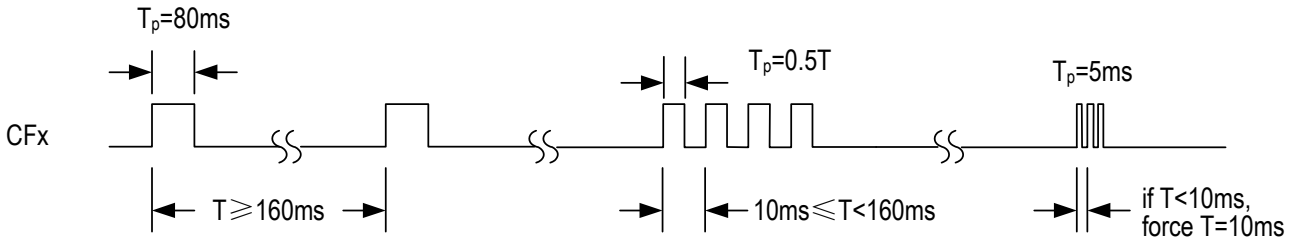

Figure-4 CFx Pulse Output Regulation

For CFx pulse width regulation, refer to Figure-4.

Case1 T>=160ms, Tp=80ms

Case 2 10ms<=T<160ms, Tp=T/2

Case 3 If Calculated T < 10ms, force T=10ms, Tp=5ms

3.4.4 STARTUP AND NO-LOAD POWER

There are startup power threshold registers (e.g. PStartTh(35H)). Refer to 6.4 Configuration and Calibration Registers. The power threshold registers are defined for all-phase-sum active, reactive and apparent power. The 90E32A starts metering when the corresponding all-phase-sum power is greater than the startup threshold. When the power value is lower than the startup threshold, energy is not accumulated and it is assumed as in no-load status. Refer to Figure-5.

There are also no-load Current Threshold registers for Active, Reactive and Apparent energy metering participation for each of the 3 phases. If |P|+|Q| is lower than the corresponding power threshold, that particular phase will not be accumulated. Refer to the PStartTh register and other threshold registers.

There are also no-load status bits (the TPnoload/TQnoload bits (b14~15, EnStatus0)) defined to reflect the no-load status. The 90E32A does not output any pulse in no-load status. The power-on state is of no-load status.

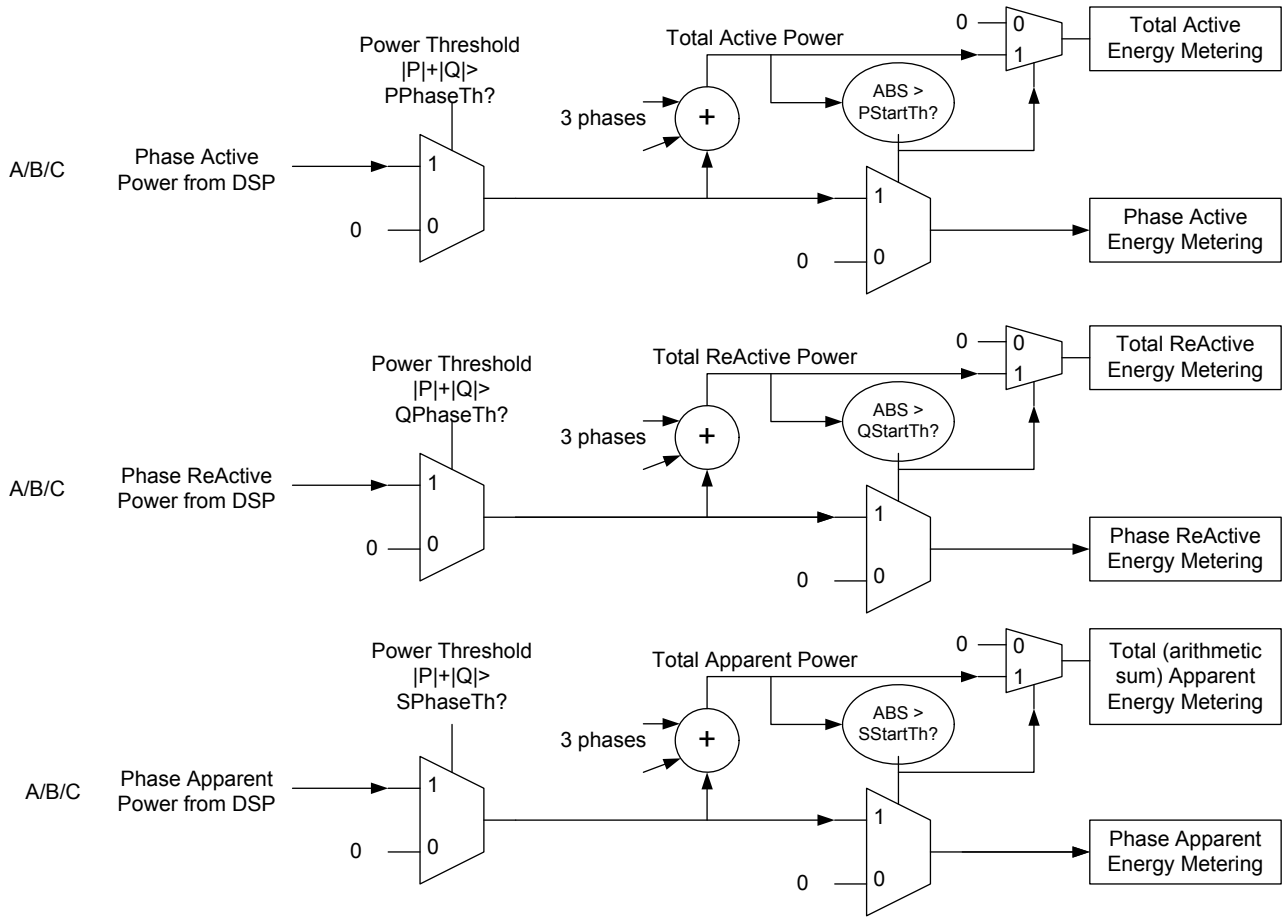

Figure-5 Metering Startup Handling

3.5 MEASUREMENT FUNCTION

Measured parameters can be divided to 7 types as follows:

- Active/ Reactive/ Apparent Power
- Fundamental/ Harmonic Power
- RMS for Voltage and Current
- Power Factor
- Phase Angle
- Frequency
- Temperature

Measured parameters are average values that are averaged among 16 phase-voltage cycles (about 320ms at 50Hz) except for the temperature. The measured parameter update frequency is approximately 3Hz. Refer to Table-15.

3.5.1 ACTIVE/ REACTIVE/ APPARENT POWER

Active/ Reactive/ Apparent Power measurement registers can be divided as below:

- active, reactive, apparent power
- all-phase-sum / phase A / phase B / phase C

Altogether there are 12 power registers. Refer to 6.6.1 Power and Power Factor Registers and the SVmeanT register (98H).

Per-phase apparent power is defined as the product of measured Vrms and Irms of that phase.

All-phase-sum power is measured by arithmetically summing the per-phase measured power. The summing of phases can be configured by the MMode0 register.

3.5.2 FUNDAMENTAL / HARMONIC ACTIVE POWER

Fundamental / harmonic active power measurement registers can be divided as below:

- fundamental and harmonic power
- all-phase-sum / phase A / phase B / phase C

Altogether there are 8 power registers. Refer to 6.6.2 Fundamental/ Harmonic Power and Voltage/ Current RMS Registers.

3.5.3 MEAN POWER FACTOR (PF)

Power Factor is defined for those cases: all-phase-sum / phase A / phase B / phase C.

Altogether there are 4 power factor registers. Refer to 6.6.1 Power and Power Factor Registers.

For all-phase:

$$PF\_all = \frac{All\_phase\_\ sum\ active\_pow\ er}{All\_phase\_\ sum\ apparent\_p\ ower}$$

For each of the phase::

$$PF\_phase = \frac{active\_pow\ er}{apparent\_p\ ower}$$

3.5.4 VOLTAGE / CURRENT RMS

Voltage/current RMS registers can be divided as follows:

Per-phase: Phase A / Phase B / Phase C

Voltage / Current

Altogether there are 6 RMS registers.

Neutral Line Current RMS:

Neutral line current can be calculated by instantaneous value $i_N = i_A + i_B + i_C$.

Refer to 6.6.2 Fundamental/ Harmonic Power and Voltage/ Current RMS Registers.

3.5.5 PHASE ANGLE

Phase Angle measurement registers can be divided as below:

- phase A / phase B / phase C
- voltage / current

Altogether there are 6 phase angle registers. Refer to 6.6.3 THD+N, Frequency, Angle and Temperature Registers.

Note: Calculation of phase angle is based on zero-crossing interval and frequency. There might be big error when voltage/current at low value.

3.5.6 FREQUENCY

Frequency is measured using phase A voltage by default. When phase A has voltage sag, phase C is used, and phase B is used when both phase A and C have voltage sag.

Refer to 6.6.3 THD+N, Frequency, Angle and Temperature Registers.

3.5.7 TEMPERATURE

Chip Junction-Temperature is measured roughly every 100 ms by on-chip temperature sensor.

Refer to 6.6.3 THD+N, Frequency, Angle and Temperature Registers.

3.5.8 THD+N FOR VOLTAGE AND CURRENT

Voltage THD+N is defined as:

$$\frac{\sqrt{(V_{rms\_total}^{\ 2} - V_{rms\_fundamental}^{\ 2})}}{V_{rms\_fundamental}}$$

Current THD+N's definition is similar to that of voltage.

Registers:

- voltage and current
- phase A / phase B / phase C

Altogether there are 6 THD+N registers. Refer to 6.6.3 THD+N, Frequency, Angle and Temperature Registers.

The THD+N measurement is mainly used to monitor the percentage of harmonics in the system. Accuracy is not guaranteed when THD+N is lower than 10%.

3.6 POWER MODE

The 90E32A has four power modes. The power mode is solely defined by the PM1 and PM0 pins.

Table-2 Power Mode Mapping

PM1:PM0 Value	Power Mode
11	Normal (N mode)
10	Partial Measurement (M mode)
01	Detection (D mode)
00	Idle (I mode)

3.6.1 NORMAL MODE (N MODE)

In Normal mode, all function blocks are active except for current detector block. Refer to Figure-6.

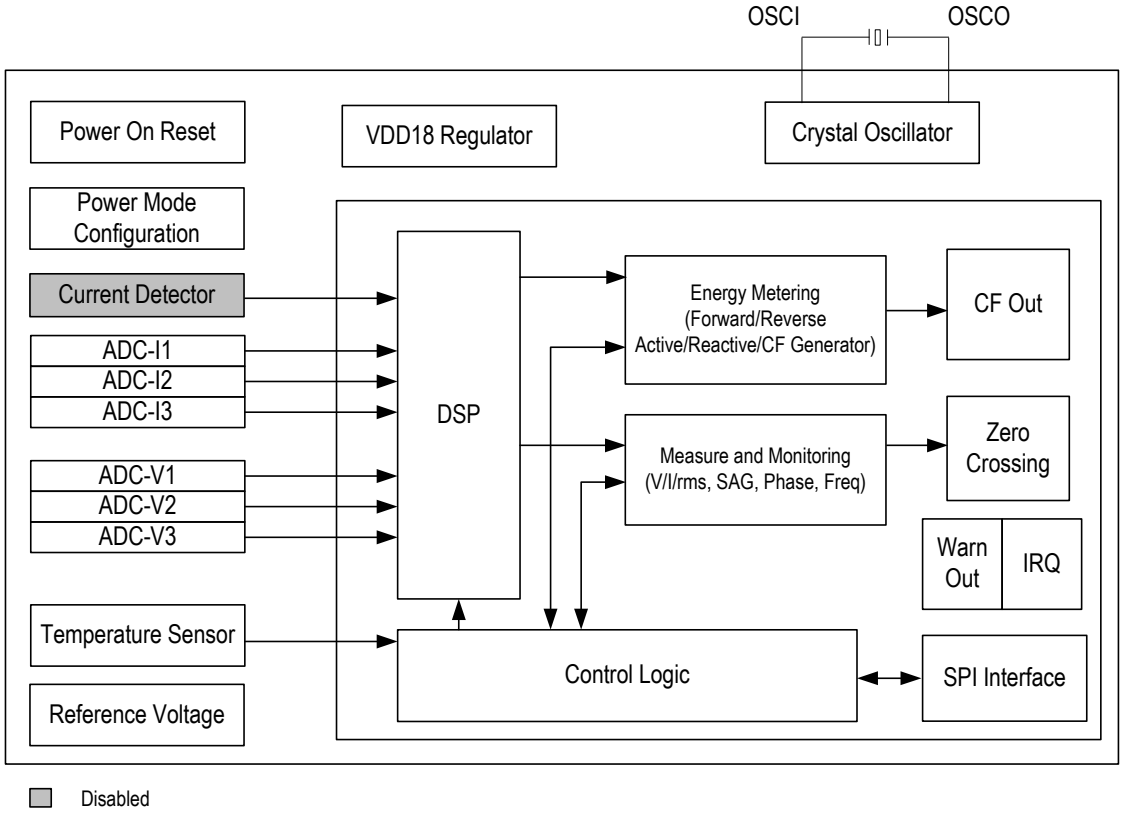

Figure-6 Block Diagram in Normal Mode

3.6.2 IDLE MODE (I MODE)

In Idle mode, all functions are shut off.

The analog blocks' power supply is powered but circuits are set into power-down mode, i.e, power supply applied but all current paths are shut off. There is very low current since only very low device leakage could exist in this mode.

The digital I/Os' supply is powered.

In I/O and analog interface, the input signals from digital core (which is not powered) will be set to known state as described in Table-3. The PM1 and PM0 pins which are controlled by external MCU are active and can configure the 90E32A to other modes.

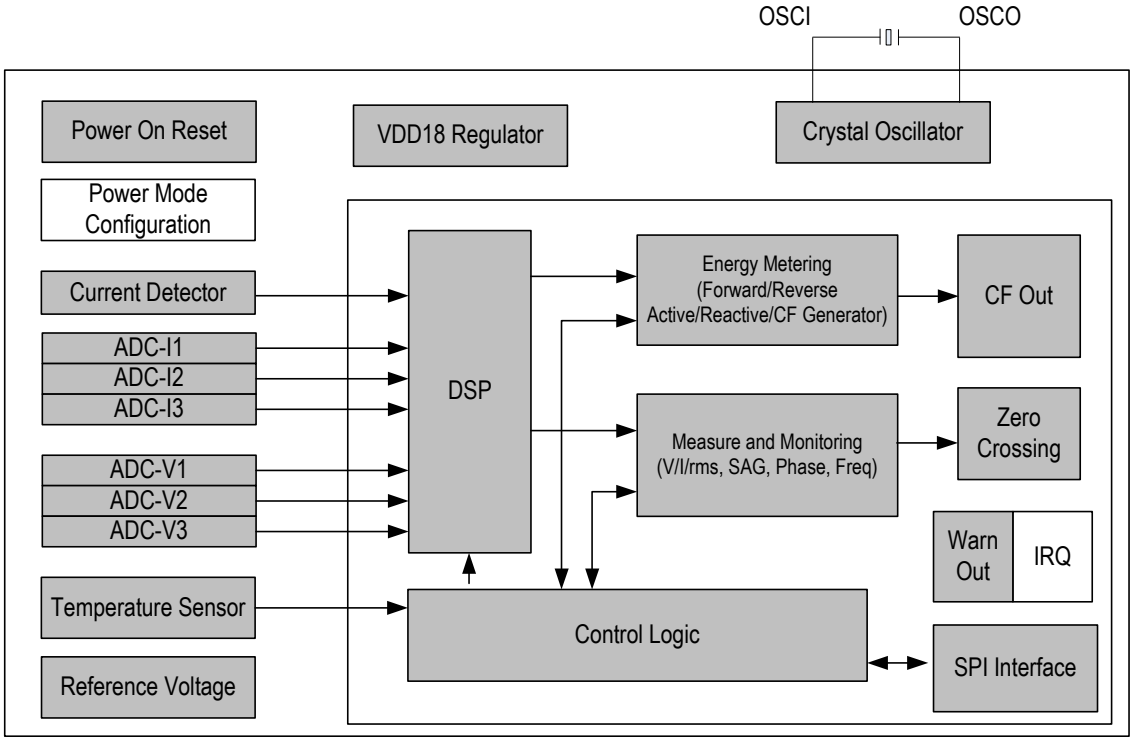

Figure-7 Block Diagram in Idle Mode

Please note that since the digital I/O is not shut off, the I/O circuit is active in the Idle mode. The application shall make sure that valid logic levels are applied to the I/O.

Table-3 lists digital I/O and power pins' states in Idle mode. It lists the requirements for inputs and the output level for output.

Table-3 Digital I/O and Power Pin States in Idle Mode

Name	I/O type	Type	Pin State in Idle Mode
$\overline{\text{Reset}}$	I	LVTTL	Input level shall be VDD33.
$\overline{\text{CS}}$	I	LVTTL	I/O set in input mode. Input level shall be VDD33 or VSS.
SCLK	I	LVTTL	I/O set in input mode. Input level shall be VDD33 or VSS.
SDO	O	LVTTL	I/O set in input mode. Input level shall be VDD33 or VSS.
SDI	I	LVTTL	I/O set in input mode. Input level shall be VDD33 or VSS.
PM1 PM0	I	LVTTL	As defined in Table-2
OSCI OSCO	I O	OSC	Oscillator powered down. OSCO stays at fixed (low) level.

Table-3 Digital I/O and Power Pin States in Idle Mode

Name	I/O type	Type	Pin State in Idle Mode
ZX0 ZX1 ZX2	O	LVTTL	0
CF1 CF2 CF3 CF4	O	LVTTL	0
WarnOut	O	LVTTL	0
IRQ0 IRQ1	O	LVTTL	0
VDD18	I	Power	Regulated 1.8V: high impedance
DVDD	I	Power	Digital Power Supply: powered by system
AVDD	I	Power	Analog Power Supply: powered by system
Test	I	Input	Always tie to ground in system application

3.6.3 DETECTION MODE (D MODE)

In Detection mode, the current detector is active. The current detector compares whether any phase current exceeds the configured threshold using low-power comparators.

When the current of one phase or multiple phases exceeds the configured threshold, the 90E32A asserts the IRQ0 pin to high and hold it until power mode change. The IRQ0 state is cleared when entering or exiting Detection mode.

When the current of all three current channels exceed the configured threshold, the 90E32A asserts the IRQ1 pin to high and hold it until power mode change. The IRQ1 state is cleared when entering or exiting Detection mode.

The threshold registers need to be programmed in Normal mode before entering Detection mode.

The digital I/O state is the same as that in Idle state (except for IRQ0/IRQ1 and PM1/PM0).

The 90E32A has two comparators for detecting each phase's positive and negative current. Each comparator's threshold can be set individually. The two comparators are both active by default, which called 'double-side detection'. User also can enable one comparator only to save power consumption, which called 'single-side detection'.

Double-side detection has faster response and can detect 'half-wave' current. But it consumes nearly twice as much power as single-side detection.

Comparators can be power-down by configuring the DetectCtrl register.

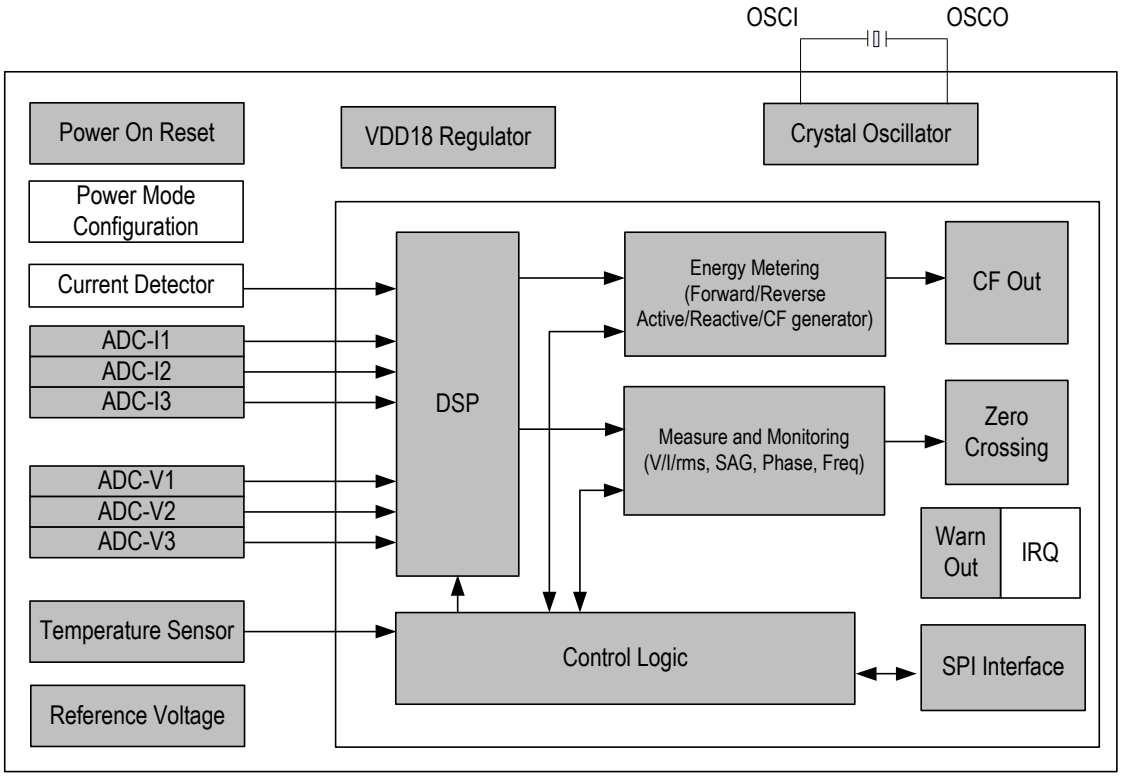

Figure-8 Block Diagram in Detection Mode

3.6.4 PARTIAL MEASUREMENT MODE (M MODE)

In this mode, Voltage ADCs and digital circuits are inactive.

The 90E32A measures the current RMS of one line cycle.

When the measurement is done, the 90E32A asserts the IRQ0 pin high until the Partial Measurement mode exits.

In this mode, the user needs to program the related registers (including PGA gain, channel gain, offset, etc.) to make the current RMS measurement accurate. Refer to 5.2 Partial Measurement mode Calibration. Please note that not all registers in this mode is accessible. Only the Partial Measurement related registers (14H~1DH) and some special registers (00H, 01H, 03H, 07H,0EH, 0FH) can be accessed.

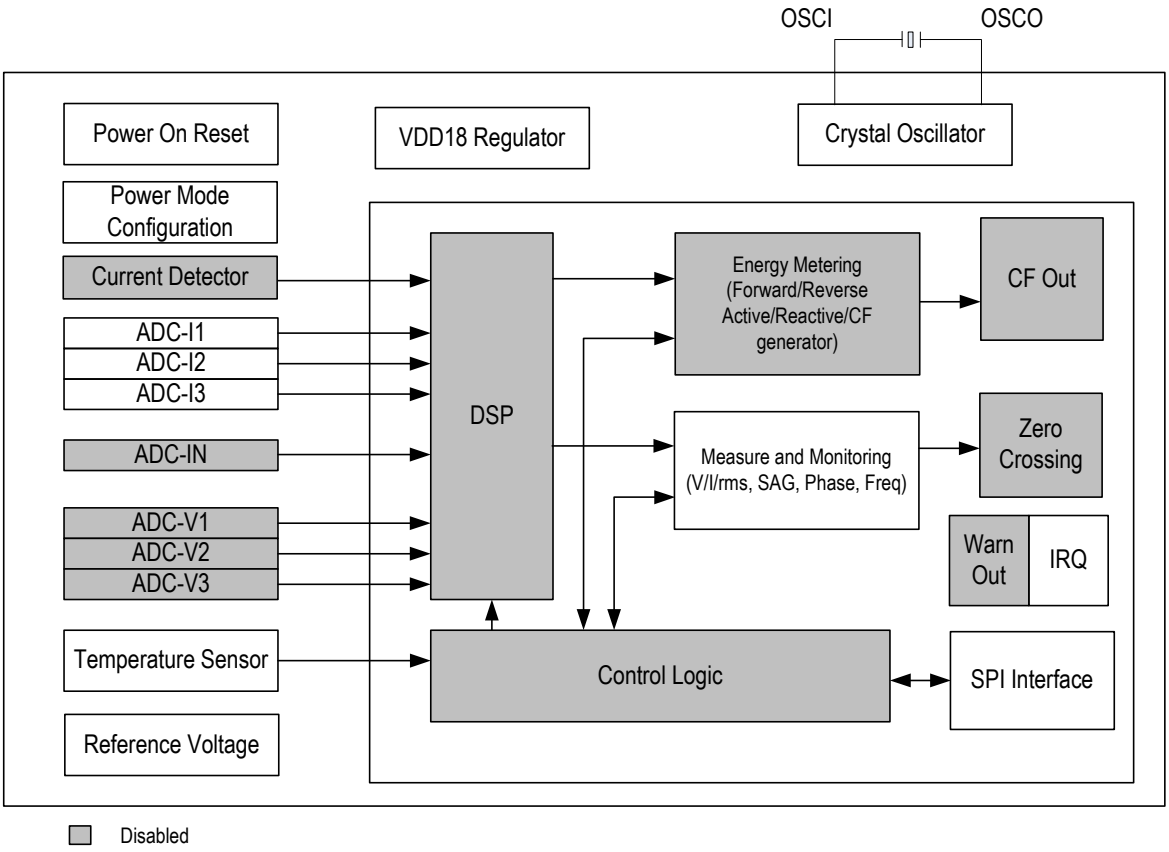

Figure-9 Block Diagram in Partial Measurement mode

3.6.5 TRANSITION OF POWER MODES

The above power modes are controlled by the PM0 and PM1 pins. In application, the PM0 and PM1 pins are connected to external MCU. The PM0 and PM1 pins have internal RC- filters.

Generally, the 90E32A stays in Idle mode most of the time while outage. It enters Detection mode at a certain interval (for example 5s) as controlled by the MCU. It informs the MCU if the current exceeds the configured threshold. The MCU then commands the 90E32A to enter Partial Measurement mode at a certain interval (e.g. 60s) to read related current. After current reading, the 90E32A gets back to the Idle mode.

The measured current may be used to count energy according to some metering model (like current RMS multiplying the rated voltage to compute the power).

Any power mode transition goes through the Idle mode, as shown in Figure-10.

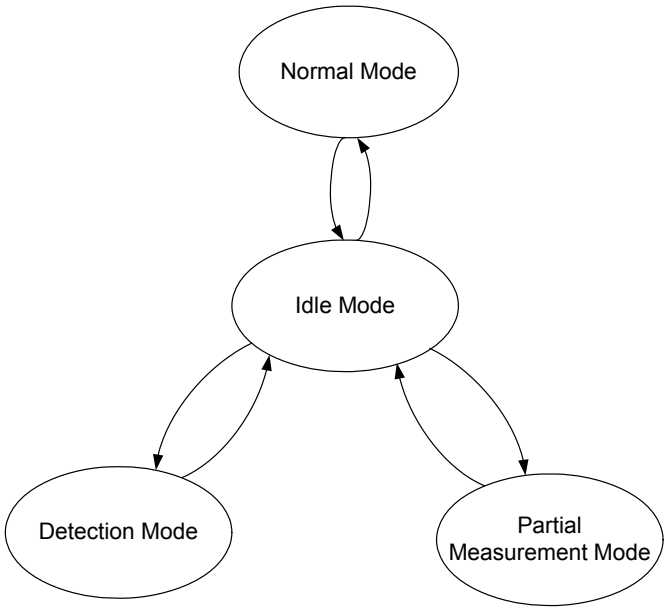

Figure-10 Power Mode Transition

3.7 EVENT DETECTION

3.7.1 ZERO-CROSSING DETECTION

Zero-crossing detector detects the zero-crossing point of the fundamental component of voltage and current for each of the 3 phases.

Zero-crossing signal can be independently configured and output. Refer to the definition of the ZXConfig register.

3.7.2 SAG DETECTION

Usually in the application the Sag threshold is set to be 78% of the reference voltage. The 90E32A generates Sag event when there are less than three 8KHz samples (absolute value) greater than the sag threshold during two continuous 11ms time-window.

For the computation of Sag threshold register value, refer to AN-644.

The Sag event is captured by the SagWarn bit (b3, SysStatus0). If the corresponding IRQ enable bit the SagWnEn bit (b3, FuncEn0) is set, IRQ can be generated. Refer to Figure-21.

3.7.3 PHASE LOSS DETECTION

The phase loss detection detects if there is one or more phases' voltage is less than the phase-loss threshold voltage.

The processing and handling is similar to sag detection, only the threshold is different. The threshold computation flow is also similar. The typical threshold setting could be 10% Un or less.

If any phase line is detected as in phase-loss mode, that phase's zero-crossing detection function (both voltage and current) is disabled.

3.7.4 COMPUTED NEUTRAL LINE OVERCURRENT DETECTION

The neutral line computed current (calculated) RMS is checked with the threshold defined in the INWarnTh0 register. If the N Line current is greater than the threshold, the INOv0 bit (b14, SysStatus1) bit is set. IRQ1 is generated if the corresponding Enable bit the INOv0En bit (b14, FuncEn1) is set.

3.7.5 PHASE SEQUENCE ERROR DETECTION

The phase sequence is detected in two cases: 3P4W and 3P3W, which is defined by the 3P3W bit (b8, MMode0).

3P4W case:

Correct sequence: Voltage/current zero-crossing sequence: phase-A, phase-B and phase-C.

3P3W case:

Correct sequence: Voltage/current zero-crossing between phase-A and phase-C is greater than 180 degree.

If the above mentioned criteria are violated, it is assumed as a phase sequence error.

3.8 DC AND CURRENT RMS ESTIMATION

The 90E32A has a module named 'PMS' which can estimate current channel RMS or current channel arithmetic average (DC component). The measurement type is defined in the PMConfig register. It can be used to estimate current RMS in Partial Measurement mode. Since the PMS block only consume very small power, it can be also used to estimate current RMS in Normal mode. The PMS module is turned on in both Partial Measurement mode and Normal mode.

The result is in different format and different scale for the RMS and average respectively. The RMS result is unsigned; while current average is signed.

Refer to 6.3.2 Partial Measurement mode Registers for associated register definition.