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## Low Skew Buffers

### General Description

The **ICS9179B-01** generates SDRAM clock buffers required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro or Pentium II. An output enable is provided for testability.

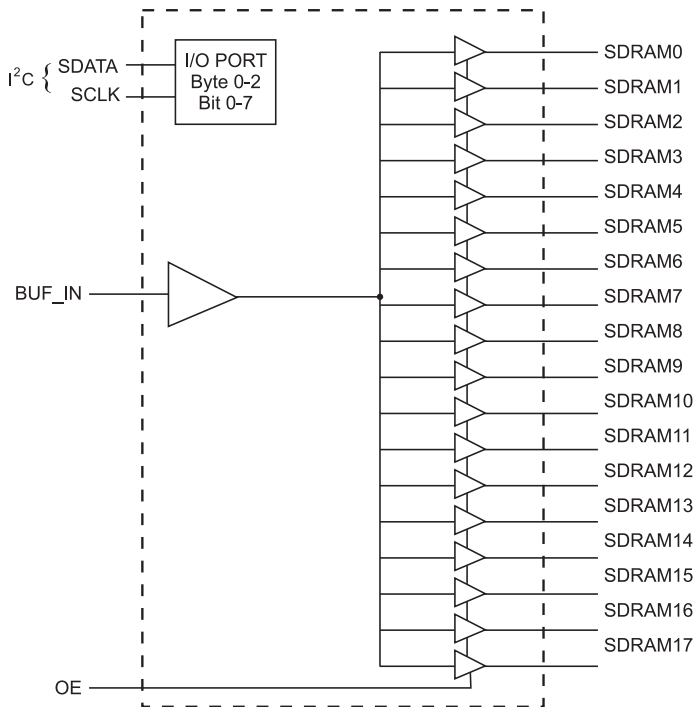
The device is a buffer with low output to output skew. This is a Fanout buffer device, not using an internal PLL. This buffer can also be a feedback to an external PLL stage for phase synchronization to a master clock.

The individual clock outputs are addressable through I<sup>2</sup>C to be enabled, or stopped in a low state for reduced EMI when the lines are not needed.

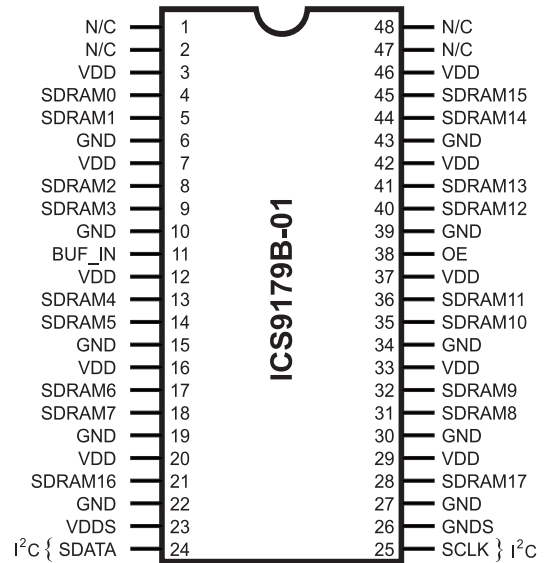
### Features

- High speed, low noise non-inverting (0:17) buffer for SDRAM clock buffer applications.
- Supports up to four SDRAM DIMMS
- Synchronous clocks skew matched to 250 ps window on SDRAM.
- I<sup>2</sup>C Serial Configuration interface to allow individual clocks to be stopped.
- Multiple VDD, VSS pins for noise reduction
- Tri-state pin for testing
- Custom configurations available
- 3.0V – 3.7V supply range
- 48-pin SSOP package

### Block Diagram



### Pin Configuration



**48-Pin SSOP**



## Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
4, 5, 8, 9	SDRAM (0:3)	OUT	SDRAM Byte 0 clock outputs <sup>1</sup>
13, 14, 17, 18	SDRAM (4:7)	OUT	SDRAM Byte 1 clock outputs <sup>1</sup>
31, 32, 35, 36	SDRAM (8:11)	OUT	SDRAM Byte 2 clock outputs <sup>1</sup>
40, 41, 44, 45	SDRAM (12:15)	OUT	SDRAM Byte 3 clock outputs <sup>1</sup>
21, 28	SDRAM (16:17)	OUT	SDRAM clock outputs useable for feedback. <sup>1</sup>
11	BUF_IN	IN	Input for buffers
38	OE	IN	Tri-states all outputs when held LOW. Has internal pull-up. <sup>2</sup>
24	SDATA	I/O	Data pin for I <sup>2</sup> C circuitry <sup>3</sup>
25	SCLK	I/O	Clock pin for I <sup>2</sup> C circuitry <sup>3</sup>
3, 7, 12, 16, 20, 29, 33, 37, 42, 46	VDD	PWR	3.3V Power supply for SDRAM buffer
6, 10, 15, 19, 22, 27, 30, 34, 39, 43	GND	PWR	Ground for SDRAM buffer
23	VDDS	PWR	3.3V Power supply for I <sup>2</sup> C circuitry
26	GNDS	PWR	Ground for I <sup>2</sup> C circuitry
1, 2, 47, 48	N/C	-	Pins are not internally connected

### Notes:

- At power up all eighteen SDRAM outputs are enabled and active.
- OE has a 100K Ohm internal pull-up resistor to keep all outputs active.
- The SDATA and SCLK inputs both also have internal pull-up resistors with values above 100K Ohms as well for complete platform flexibility.

## Power Groups

VDD = Power supply for SDRAM buffer

VDDS = Power supply for I<sup>2</sup>C circuitry

## Ground Groups

GND = Ground for SDRAM buffer

GNDS = Ground for I<sup>2</sup>C circuitry





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## Technical Pin Function Descriptions

### VDD

This is the power supply to the internal core logic of the device as well as the clock output buffers for SDRAM(0:17).

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

### GND

This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

### SDRAM(0:17)

These Output Clocks are used to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the SDRAM's output is controlled by the supply voltage that is applied to VDD of the device, operates at 3.3 volts.

### I<sup>2</sup>C

The SDATA and SCLOCK Inputs are used to program the device. The clock generator is a slave-receiver device in the I<sup>2</sup>C protocol. It will allow read-back of the registers. See configuration map for register functions. The I<sup>2</sup>C specification in Philips I<sup>2</sup>C Peripherals Data Handbook (1996) should be followed.

### BUF\_IN

Input for Fanout buffers (SDRAM 0:17).

### OE

OE tristates all outputs when held low.

### VDDS

This is the power supply to I<sup>2</sup>C circuitry.

### GNDS

This is the ground to I<sup>2</sup>C circuitry.



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## General I<sup>2</sup>C serial interface information

- A. For the clock generator to be addressed by an I<sup>2</sup>C controller, the following address must be sent as a start sequence, with an acknowledge bit between each byte.

Then Byte 0, 1, 2, etc in sequence until STOP.

- B. The clock generator is a slave/receiver I<sup>2</sup>C component. It can "read back" (in Philips I<sup>2</sup>C protocol) the data stored in the latches for verification. (set R/W# to 1 above). There is no BYTE count supported, so it does not meet the Intel SMB PIIX4 protocol.

Byte 0, 1, 2, etc in sequence until STOP.

- C. The data transfer rate supported by this clock generator is 100K bits/sec (standard mode)
- D. The input is operating at 3.3V logic levels.
- E. The data byte format is 8 bit bytes.
- F. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
- G. In the power down mode (PWR\_DWN# Low), the SDATA and SCLK pins are tristated and the internal data latches maintain all prior programming information.
- H. At power-on, all registers are set to a default condition. Bytes 0 through 2 default to a 1 (Enabled output state).

## Serial Configuration Command Bitmaps

### Byte 0: SDRAM Clock Register

**Notes:** 1 = Enabled; 0 = Disabled, outputs held low

**Note:** PWD = Power-Up Default



Functionality

Byte 1: SDRAM Clock Register

Byte 2: PCICLK Clock Register

BIT #	PIN#	IN#	WD#	DESCRIPTION	SDRAM (8:11)	SDRAM (12:15)	SDRAM (16:17)
Bit 7	OE#	1	1	SDRAM (14:7) Max discrete cap loads	SDRAM (8:11)	SDRAM (12:15)	SDRAM (16:17)
Bit 6	2	2	2	Condition (Act/Inact) VDD = 3.465V			
Bits 6:0	41:21			Notes: (Act/Inact) SDRAM (14:7) All static Hi-Zs = VDD or GNDZ 0 = Disabled, outputs held low		Notes: Hi-Z	Hi-Z
Bit 5	Lock	MO	SDRAM#2	SDRAM#2			
Bit 4	BUF_IN	1	1	Notes: (Act/Inact) Power Up Default	1 X BUF_IN	1 X BUF_IN	1 X BUF_IN
Bit 3	3			Notes: (Act/Inact) Reserved			
Bit 2	2			Notes: (Act/Inact) Reserved			
Bit 1	1			Notes: (Act/Inact) Reserved			
Bit 0	0			Notes: (Act/Inact) Reserved			
<p><b>IC9179B-01 Power Management</b></p> <p>Active 100MHz (BUF_IN = 100.00MHz) 15mA 180mA</p> <p>The values below are estimates of target specifications.</p>							



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## Absolute Maximum Ratings

Supply Voltage	7.0 V
Logic Inputs	GND -0.5 V to $V_{DD} + 0.5$ V
Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.



### Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 20 - 30 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	$R_{DSP}$	$V_O = V_{DD} * (0.5)$	10		24	W
Output Impedance	$R_{DSN}$	$V_O = V_{DD} * (0.5)$	10		24	W
Output High Voltage	$V_{OH}$	$I_{OH} = -36 \text{ mA}$	2.4	3		V
Output Low Voltage	$V_{OL}$	$I_{OL} = 23 \text{ mA}$		0.27	0.4	V
Output High Current	$I_{OH}$	$V_{OH} = 2.0 \text{ V}$		-115	-54	mA
Output Low Current	$I_{OL}$	$V_{OL} = 0.8 \text{ V}$	40	57		mA
Rise Time <sup>1</sup>	$T_r$	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$	0.5	0.95	1.33	ns
Fall Time <sup>1</sup>	$T_f$	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$	0.5	0.95	1.33	ns
Duty Cycle <sup>1</sup>	$D_t$	$V_T = 1.5 \text{ V}$	45	51	55	%
Skew <sup>1</sup>	$T_{sk}$	$V_T = 1.5 \text{ V}$		110	250	ps
Propagation <sup>1</sup>	$T_{PROP}$	$V_T = 1.5 \text{ V}$	1	5	6	ns
	$T_{PROPEN}$	$V_T = 1.5 \text{ V}$	1		8	ns
	$T_{PROPDIS}$	$V_T = 1.5 \text{ V}$	1		8	ns

<sup>1</sup>Guaranteed by design, not 100% tested in production.



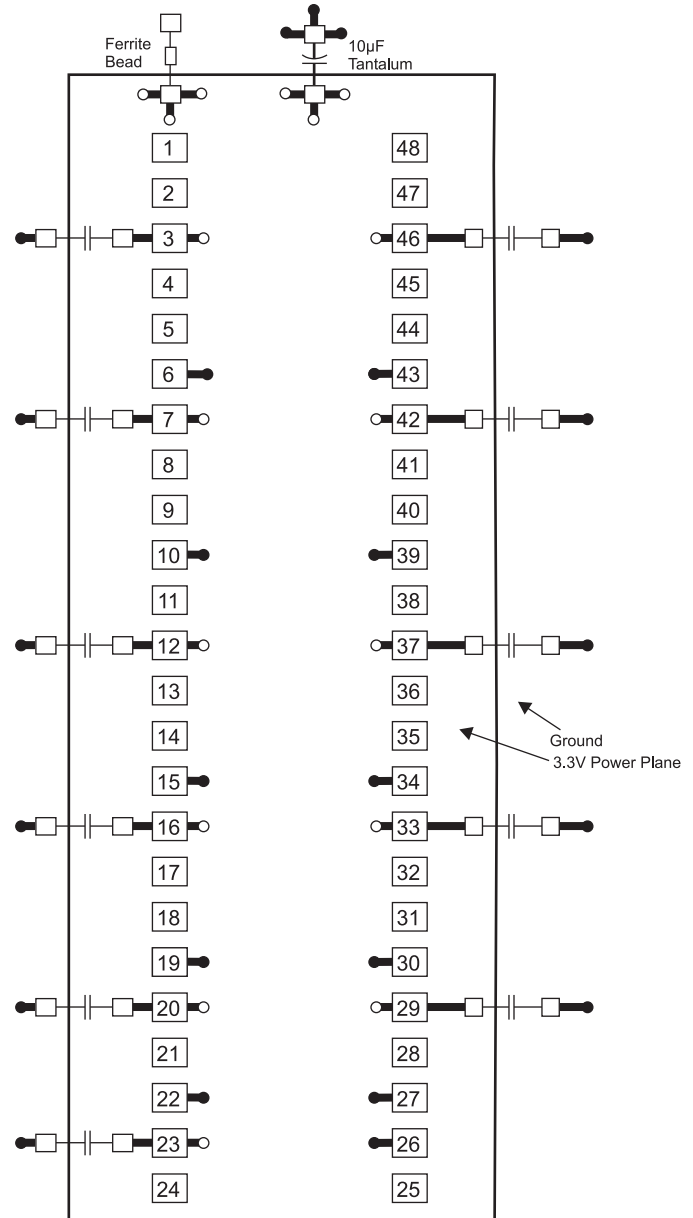


### General Layout Precautions:

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and vias as wide as possible to lower inductance.

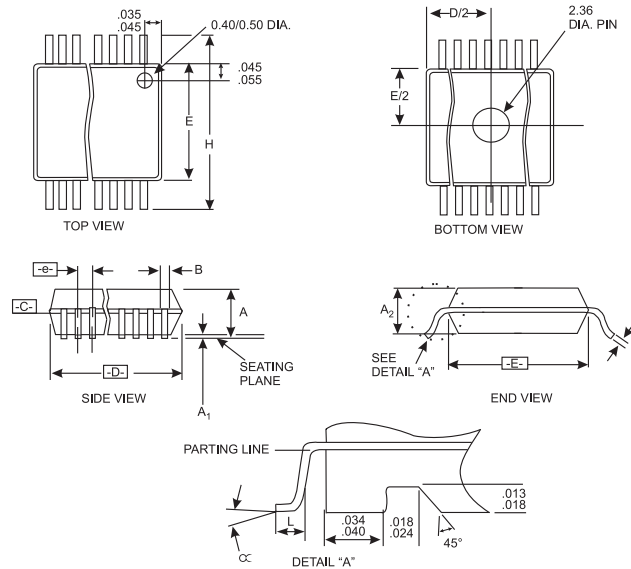
### Notes:

- 1 All clock outputs should have series terminating resistor. Not shown in all places to improve readability of diagram
- 2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.



### Capacitor Values:

All unmarked capacitors are 0.01µF ceramic



**SSOP Package**

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
μ	0°	5°	8°					
X	.085	.093	.100					

**Ordering Information**

**9179BF-01LF**

Example:

