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DATASHEET

TEN CHANNEL HD AUDIO CODEC

Low Power Optimized for ECR15b and EuP

92HD68E

Description

The 92HD68E is a low power optimized, high fidelity, 10-channel audio codec compatible with Intel's High Definition (HD) Audio Interface.

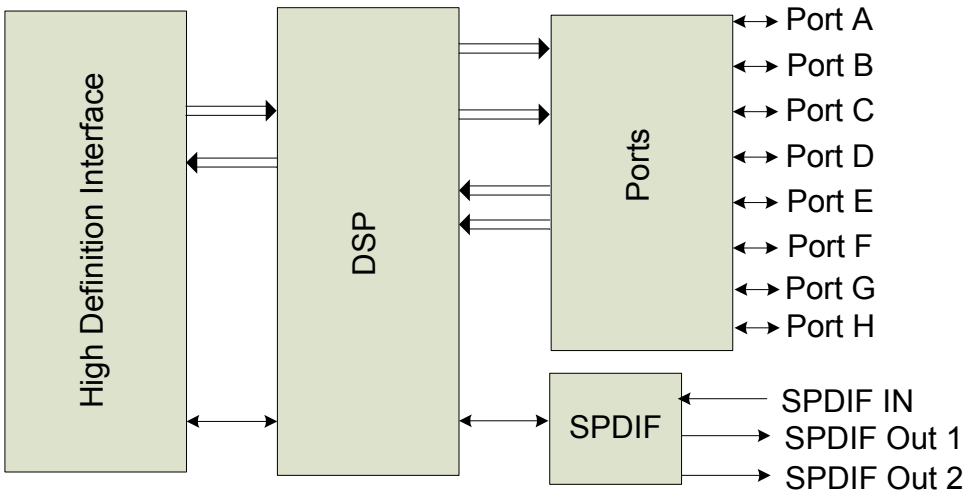
The 92HD68E provides stereo 24-bit resolution with sample rates up to 192kHz.

The 92HD68E provides high quality, HD Audio capability to notebook and desktop PC applications.

Features

- **10 Channels (5 stereo DACs and 2 stereo ADCs) with 24-bit resolution**
  - Supports full-duplex 7.1 audio and simultaneous VoIP
- **ECR 15b and EuP low power support**
- **Microsoft WLP premium logo compliant, per Logo Point**
- **8 analog ports with port presence detect + CD In**
- **3 integrated headphone amps**
- **4 adjustable VREF Out pins for microphone bias**
- **Dual SPDIF for WLP compliant support of simultaneous HDMI and SPDIF output**
- **SPDIF Input**
- **Digital microphone input (mono or stereo or quad)**
- **High performance analog mixer**
- **Support for 1.5V and 3.3V HDA signaling**
- **Digital and Analog PC Beep to all outputs**
- **48-pin QFP and 40-pad QFN RoHS packages**

Block Diagram



Software Support

- Intuitive IDT HD Sound graphical user interface that allows configurability and preference settings
- 12 band fully parametric equalizer
  - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
  - System-level effects automatically disabled when external audio connections made
- Dynamics Processing
  - Enables improved voice articulation
  - Compressor/limiter allows higher average volume level without resonances or damage to speakers.
- IDT Vista APO wrapper
  - Enables multiple APOs to be used with the IDT Driver
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression
- Dynamic Stream Switching
  - Improved multi-streaming user experience with less support calls
- Broad 3rd party branded software including Creative, Dolby, DTS, and SRS
- Smart Configuration Suite (SCS) improves time to market and software quality
  - Online pin and feature configuration tool generates BIOS verb table for Windows and Linux.
  - Downloadable WHQL compliant, self configurable driver for XP, Vista and Win7 based on verb table and test files generated.
  - BIOS verb tables can be tested with the self configurable driver prior to flashing into BIOS.

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1. DESCRIPTION

1.1. Overview

The 92HD68E is a high fidelity, 10-channel audio codec compatible with the Intel High Definition (HD) Audio Interface. The 92HD68E codec provides high quality, HD Audio capability notebooks and desktops.

The 92HD68E is designed to meet or exceed premium logo requirements for Microsoft's Windows Logo Program (WLP) per Logo Point.

The 92HD68E provides stereo 24-bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. 92HD68E SPDIF outputs support sample rates of 192kHz, 176.4kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz.

The 92HD68E supports a wide range of notebook and desktop 10-channel configurations. The 2 independent SPDIF output interfaces provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. Simultaneous HDMI and SPDIF output is possible.

MIC inputs can be programmed with 0/10/20/30dB boost. For more advanced configurations, the 92HD68E has up to 7 General Purpose I/O (GPIO).

The port presence detect capabilities allow the codecs to detect when audio devices are connected to the codec. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The 92HD68E operates with a 3.3V digital supply and a 5V analog supply. It can also work with 1.5V and 3.3V HDA signaling.

The 92HD68E is available in a 48-pin QFP or 40-pad QFN Environmental (ROHS) package.

1.2. Orderable Part Numbers

92HD68E1X5NDGXyyX	5V Analog, 40QFN, 1.5V HDA Signaling
92HD68E2X5NDGXyyX	5V Analog, 40QFN, 3.3V HDA Signaling
92HD68E3X5PRGXyyX	5V Analog, 48QFP, switchable 1.5V or 3.3V HDA Signaling

yy = silicon stepping/revision, contact sales for current data.
Add an "8" to the end for tape and reel delivery.

1.3. Block Diagram

Figure 1. 92HD68E Block Diagram

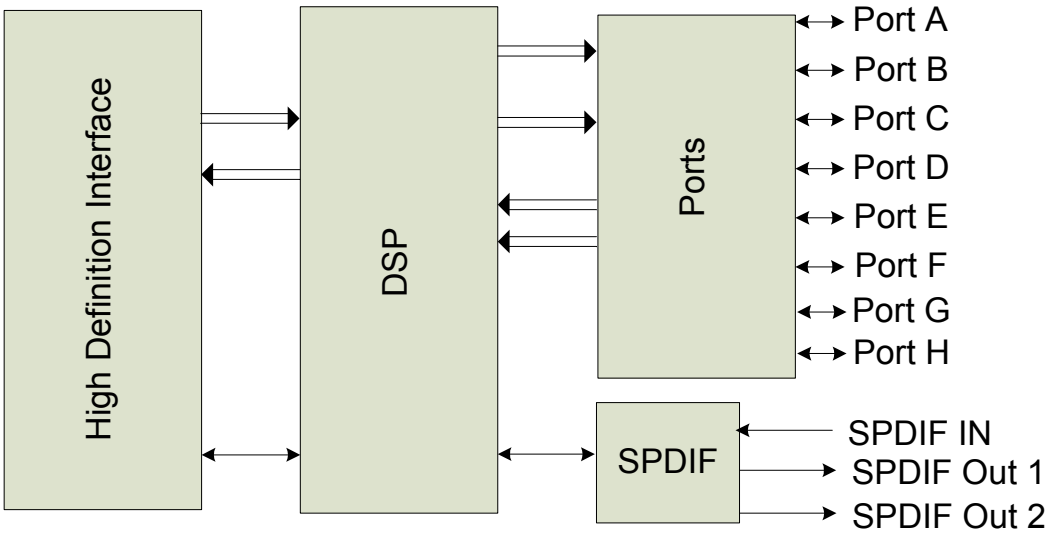
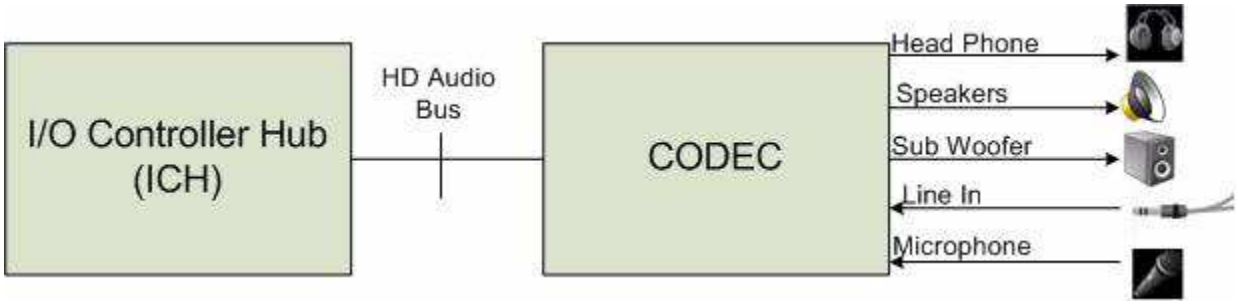


Figure 2. System Diagram



2. DETAILED DESCRIPTION

2.1. Port Functionality

Multi-function (Input / output) ports allow for the highest possible flexibility. 8 bi-directional ports, 3 are headphone capable, support a wide variety of consumer desktop and mobile system use models.

Pins	Port	Input	Output	Headphone	Mic Bias (Vref pin)	Input boost amp
39/41	A	Yes	Yes	Yes	Yes	Yes
21/22	B	Yes	Yes	Yes	Yes	Yes
23/24	C	Yes	Yes		Yes	Yes
35/36	D	Yes	Yes	Yes		Yes
14/15	E	Yes	Yes		Yes	Yes
16/17	F	Yes	Yes			Yes
43/44	G	Yes	Yes			Yes
45/46	H	Yes	Yes			Yes
48	SPDIF_OUT0		Yes			
40	SPDIF_OUT1		Yes			
47	SPDIF_IN/OUT1	Yes	Yes			
4 (CLK=2)	DMIC0	Yes				Yes
30 (CLK=2)	DMIC1	Yes				Yes

Table 1. 48QFP Port Characteristics

Pins	Port	Input	Output	Headphone	Mic Bias (Vref pin)	Input boost amp
33/34	A	Yes	Yes	Yes	Yes	Yes
18/19	B	Yes	Yes	Yes	Yes	Yes
20/21	C	Yes	Yes			Yes
29/30	D	Yes	Yes	Yes		Yes
11/12	E	Yes	Yes		Yes	Yes
13/14	F	Yes	Yes			Yes
36/37	G	Yes	Yes			Yes
38/39	H	Yes	Yes			Yes
1	SPDIF_OUT0		Yes			
40	SPDIF_OUT1		Yes			

Table 2. 40QFN Port Characteristics

2.1.1. Port Characteristics

Universal (Bi-directional) jacks are supported on ports A, B, C, D, E, F, G and H for all family members. Ports A, B, and D are designed to drive 32 ohm (nominal) headphones or a 10K (nominal) load. Line Level outputs are intended to drive an external 10K load (nominal) and an on board shunt resistor of 20-47K (nominal). However, applications may support load impedances of 2.8K ohms and above when implementing ports capable of operating as microphone inputs or line outputs. Input ports are 75K (nominal) at the pin.

DAC full scale outputs and intended full scale input levels are greater than 1V rms at 5V (+5%/ -10%) to meet WLP requirements. Line output ports and Headphone output ports on the Yangtze Series codec may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports are always on to prevent pops/clicks associated with charging and discharging output coupling capacitors. This maintains proper bias on output coupling caps even in power state D3 as long as AVDD is available. Unused ports should be left unconnected. When updating existing designs, ensure that there are no conflicts between the output ports on the codec and existing circuitry.

AFG Power State	Input Enable	Output Enable	Port Behavior
D0-D1	1	1	Not allowed. Port is active as Input.
	1	0	Active - Port enabled as input
	0	1	Active - Port enabled as output
	0	0	Inactive -port is powered on (low output impedance) but drives silence only.
D2	1	1	Not allowed. Port is active as Input.
	1	0	Inactive - Port enabled as input but powered down
	0	1	Active - Port enabled as output
	0	0	Inactive -port is powered on (low output impedance) but drives silence only.
D3	1	1	Not allowed. Port is active as Input.
	1	0	Inactive (lower power) - Port keeps output coupling caps charged.
	0	1	Low power state. If enabled, Beep will output from the port
	0	0	Inactive (lower power) - Port keeps output coupling caps charged.
D3cold	-	-	Inactive (lower power) - Port keeps output coupling caps charged.
D4	-	-	Inactive (lower power) - Port keeps output coupling caps charged.
D5	-	-	Off - Charge on coupling caps will not be maintained.

Table 3. Analog Output Port Behavior

2.1.2. Vref_Out

Ports A, B, C (48-pin package only), & E support Vref_Out pins for biasing electret cartridge microphones. Settings of 80% AVDD, 50% AVDD, GND, and Hi-Z are supported. Attempting to program a pin widget control with a reserved or unsupported value will cause the associated Vref_Out pin to assume a Hi-Z state and the pin widget control Vref_En field will return a value of '000' (Hi-Z) when read.

2.1.3. Jack Detect

Plugs inserted to a jack are detected using SENSE inputs as described in the tables below. Per ECR15-B, the detection circuit operates when the CODEC is in D0 - D3 and can also operate if both the CODEC and Controller are in D3 (no bus clock.) Jack detection requires that all supplies (analog and digital) are active and stable. When AVDD is not present, the value reported in the pin widget is invalid.

When the HD Audio bus is in a low power state (reset asserted and clock stopped) the CODEC will generate a Power State Change Request when a change in port connectivity is sensed and then generate an unsolicited response after the HD Audio link has been brought out of a low power state and the device has been enumerated. Per ECR015-B, this will take less than 10mS.

The following table summarizes the proper resistor tolerances for different analog supply voltages.

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance Pull-Up	Resistor Tolerance SENSE_A/B/C
4.75 or 5VV	1%	1%

Resistor	SENSE_A	SENSE_B	SENSE_C
39.2K	PORT A	PORT E	SPDIFOUT0
20.0K	PORT B	PORT F	SPDIFOUT1(pin40)
10.0K	PORT C	PORT G	DMIC0
5.11K	PORT D	Port H	DMIC1
2.49K	Pull-up to AVDD	Pull-up to AVDD	Pull-up to AVDD

Table 4. 48pin Jack Detect

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20.0K	PORT B	PORT F
10.0K	PORT C	PORT G
5.11K	PORT D	PORT H
2.49K	Pull-up to AVDD	Pull-up to AVDD

Table 5. 40pin Jack Detect

See reference design for more information on Jack Detect implementation.

2.1.4. SPDIF Output

Both SPDIF Outputs can operate at 44.1kHz, 48kHz, 88.2kHz, 96kHz and 192KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with

all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

The two SPDIF output converters can not be aligned in phase with the DACs. Even when attached to the same stream, the two SPDIF output converters may be misaligned with respect to their frame boundaries.

Per the HDA015-B ECR, the SPDIF outputs support the ability to provide clocking information even when no stream is selected for the converter, or when in a low power state. Also, as stated in the ECR, the SPDIF output ports support port presence detect.

SPDIF Outputs are outlined in tables below.

AFG Power State	RESET#	Output Enable	Keep Alive Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	-	Hi-Z[1] immediately after power on, otherwise the previous state is retained.
D0	De-Asserted (High)	Disabled	-	-	-	Hi-Z
		Enabled	Disabled	Disabled	-	Active - Pin drives 0
				Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes
					1-15	Active - Pin drives SPDIFOut0 data
			Enabled	Disabled	-	Active - Pin drives SPDIF-format, but data is zeroes
				Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes
					1-15	Active - Pin drives SPDIFOut0 data
D1-D2		Disabled	-	-	-	Hi-Z
		Enabled	Disabled	Disabled	-	Active - Pin drives 0
				Enabled	-	Active - Pin drives 0
			Enabled	Disabled	-	Active - Pin drives SPDIF-format, but data is zeroes
				Enabled	-	Active - Pin drives SPDIF-format, but data is zeroes
D3		Disabled	-	-	-	Hi-Z
		Enabled	Disabled	Disabled	-	Hi-Z
				Enabled	-	Hi-Z
			Enabled	Disabled	-	Active - Pin drives SPDIF-format, but data is zeroes
				Enabled	-	Active - Pin drives SPDIF-format, but data is zeroes
D3cold	-	-	-	-	-	Hi-Z
D4	-	-	-	-	-	Hi-Z
D5	-	-	-	-	-	Hi-Z

Table 6. SPDIF OUT 0 Behavior

1.Internal Pull-Down always enabled

AFG Power State	RESET#	GPIO0 Enable	Input Enable	Output Enable	Keep Alive En	Converter Dig En	Strm ID	Pin Mode	Pin Behavior
D0-D4	Asserted (Low)	-	-	-	-	-	-		EAPD (internal pull-up enabled) immediately after power on, otherwise the previous state is retained.
D0-D4	De-Asserted (High)	0	0	0	-	-	-	EAPD	Pin functions as EAPD
D0-D4	De-Asserted (High)	1	-	-	-	-	-	GPIO	Active - Pin reflects GPIO0 configuration (internal pull-down enabled)
D0-D4	De-Asserted (High)	0	1	0	-	-	-	SPDIF IN	Pin functions as SPDIF input (internal bias enabled)
D0	De-Asserted (High)	0	0	1	0	0	-	SPDIF OUT	Active - Pin drives 0
						1	0		Active - Pin drives SPDIF-format, but data is zeroes
							1-15		Active - Pin drives SPDIFOut1 data
					1	0	-		Active - Pin drives SPDIF-format, but data is zeroes
						1	0		Active - Pin drives SPDIF-format, but data is zeroes
							1-15		Active - Pin drives SPDIFOut1 data
D1-D2	De-Asserted (High)	0	0	1	0	0	-		Active - Pin drives 0
					0	1	-		Active - Pin drives 0
					1	0	-		Active - Pin drives SPDIF-format, but data is zeroes
					1	1	-		Active - Pin drives SPDIF-format, but data is zeroes
D3	De-Asserted (High)	0	0	1	0	0	-		Hi-Z
					0	1	-		Hi-Z
					1	0	-		Active - Pin drives SPDIF-format, but data is zeroes
					1	1	-		Active - Pin drives SPDIF-format, but data is zeroes
D3cold	De-Asserted (High)	0	0	1	-	-	-		Hi-Z
D4	De-Asserted (High)	0	0	1	-	-	-		Hi-Z
D5	-	-	-	-	-	-	-		Hi-Z

Table 7. SPDIF OUT 1 Behavior

2.2. SPDIF Input

SPDIF IN can operate at 44.1 KHz, 48 KHz, or 96 KHz, and implements internal Jack Sensing (Port presence Detect).

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs.

Status flags from the input stream are updated only after the entire valid block has been received (or at least when all bits of a particular status flag have been received) to ensure that software does not read an invalid mixture of old and new data.

In general, the SPDIF input block does not alter the data received. However, it is sometimes necessary to alter the data when the converter widget settings do not match the stream format. The following table outlines a few cases and the expected behavior.

Port presence detect for SPDIF_IN operates differently from other ports. Once the PLL has locked and valid framing (no errors) has been detected, then the port presence detect bit is set. In D3, and D3 without a clock, it is not possible to check for proper framing. Monitoring of activity (rising and falling edges) is sufficient to verify a change in connectivity in D3. If no clock is present, then the internal oscillator is used until a clock is restored. When the HD Audio bus is in a low power state (reset asserted and clock stopped) the CODEC will generate a Power State Change Request when a change in SPDIF_IN port connectivity is sensed and then generate an unsolicited response after the HD Audio link has been brought out of a low power state and the device has been enumerated. Per ECR015-B, this will take less than 10mS.

Conflict	Behavior	Resolution
Converter widget rate does not equal the stream rate	Although the SPDIF input block is designed to handle inputs slightly above or below the programmed rate, samples may be lost if the input rate is much higher than the rate programmed into the converter widget.	Program the converter widget with the same rate as indicated by the input stream.
Converter widget programmed for a word length less than the word length provided by the input stream	If the input stream indicates non PCM data, the data will be truncated to the requested word length. If LPCM data is indicated in the input stream, the CODEC will round the received data to the requested length.[1]	Program the converter widget with the word length indicated in the input stream.
Converter widget programmed with a word length greater than the word length provided by the input stream.	Regardless of content, 24 bits per channel of data will be transferred from the SPDIF input stream to the HD Audio bus interface. Truncation or rounding to the requested word length will be handled as described as above. Any non-zero data in the incoming stream will cause problems.	Program the converter widget with the word length indicated in the input stream. Although not recommended, application or driver software may program the converter widget with a word length of 24 bits, truncate the input to the word length indicated by the input stream, then right extend the data using 0s to the desired word length.

Table 8. SPDIF Behavior

1.Rounding may be disabled by setting the disable bit (AFG vendor specific verb -see widget list) or setting the SPDIF_IN converter widget Frmt StrmType field to 1 (non-PCM)

2.3. Analog Mixer

The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input. The following inputs are available: The output of the mixer may be sent to the ADC where the ADC record gain can adjust the volume. If the output of the mixer is sent to an analog port, then a separate volume control is provided to adjust the output volume. This mixer output volume control supports a gain range of -46.5dB to 0dB in 1.5dB steps. (Selecting -46.5dB will automatically mute the output.)

- inMux0
- inMux1
- inMux2
- inMux3
- CD In

2.4. Input Multiplexers

The codec implements 4 port input multiplexers. These multiplexers allow a preselection of one of four possible inputs:

Inport0_Mux	Inport1_Mux	Inport2_Mux	Inport3_mux
Port A	Port A	Port B	DAC 0
Port B	Port E	Port C	DAC 1
Port D	Port G	Port G	DAC 2
Port F	Port H	Port H	DAC 3

Table 9. Input Multiplexers

2.5. ADC Multiplexers

The codec implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function (0 to +22.5dB gain in 1.5dB steps) as an output amp and allow a preselection of one of these possible inputs:

- Port A
- Port B
- Port C
- Port D
- Port E
- Port F
- Port G
- Port H
- CD In
- Mixer Output
- DMIC 0 (only available in 48 pin package)
- DMIC1 (only available in 48 pin package)

2.6. Power Management

The HD Audio specification defines power states, power state widgets, and power state verbs. Power management is implemented at several levels. The Audio Function Group (AFG) , all converter widgets, and all pin complexes support the power state verb F05/705. Converter widgets are active in D0 and inactive in D1-D3.

The following table describes what functionality is active in each power state.

Function	D0	D1[1]	D2	D3	D3cold	Vendor Specific D4[2]	Vendor SpecificD5[2]
SPDIF Outputs	On	On	On (idle)	On (idle)[6]	Off	Off	Off
SPDIF Input	On	Off	Off	Off	Off	Off	Off
Digital Microphone inputs	On	Off	Off	Off	Off	Off	Off
DAC	On	Off	Off	Off	Off	Off	Off
D2S	On	Off	Off	Off	Off	Off	Off
ADC	On	Off	Off	Off	Off	Off	Off

Function	D0	D1[1]	D2	D3	D3cold	Vendor Specific D4[2]	Vendor SpecificD5[2]
ADC Volume Control	On	Off	Off	Off	Off	Off	Off
Ref ADC	On	Off	Off	Off	Off	Off	Off
Analog Clocks	On	Off	Off	Off	Off	Off	Off
GPIO pins	On	On	On	On[6]	On	On	Off
VrefOut Pins	On	On	Off	Off	Off	Off	Off
Input Boost	On	On	Off	Off	Off	Off	Off
Analog mixer	On	On	Off	Off	Off	Off	Off
Mixer Volumes	On	On	Off	Off	Off	Off	Off
Analog PC_Beep	On	On	On	On	Off	Off	Off
Digital PC_Beep	On	On	On	On[6]	Off	Off	Off
Lo/HP Amps	On	On	On	Low Drive[3]	Low Drive[3]	Low Drive[3]	Off
VAG amp	On	On	On	Low Drive[4]	Low Drive	Low Drive	Off
Port Sense	On	On	On	On[5]	Off	Off	Off
Reference Bias generator	On	On	On	On	On	On	Off
Reference Bandgap core	On	On	On	On	On	On	Off
HD Audio-Link	On	On	On	On[6]	Limited[7]	Off	Off
PLL	On	On	On	Off[8]	Off[9]	Off	Off

1.No DAC or ADC streams are active. Analog mixing and loop thru are supported.
2.D4 and D5 power states are entered only when D3cold is requested. D4 and D5 may be viewed as D3cold behavioral options.
3.VAG is kept active when ports are disabled or in D3/D3cold/D4. PC_Beep is supported in D3 but may be attenuated and distorted depending on load impedance.
4.VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
5. Both AVDD and DVDD must be available for Port Sense to operate.
6.Not active if BITCLK is not running (Controller in D3), but can signal power state change request (PME)
7.Only double function group reset verbs and link reset supported per ECR15b
8.PLL remains on if SPDIF_Out Keep Alive is enabled. PLL disabled only after DAC fading is complete and SDM has settled.
9.PLL disabled only after DAC fading is complete and SDM has settled.

The D3-default state is available for HD Audio compliance. The programmable values, exposed via vendor-specific settings, are under IDT Device Driver control for further power reduction. The analog mixer, line and headphone amps, port presence detect, and internal references may be disabled using vendor specific verbs. Use of these vendor specific verbs will cause pops.

The default power state for the Audio Function Group after reset is D3.

2.7. AFG D0

The AFG D0 state is the active state for the device. All functions are active if their power state (if they support power management at their node level) has been set to D0.

2.8. AFG D1

D1 is a lower power mode where all converter widgets are disabled. Analog mixer and port functions are active. The part will resume from theD1 to theD0 state within 1 mS.

2.9. AFG D2

The D2 state further reduces power by disabling the mixer and port functions. The port amplifiers and internal references remain active to keep port coupling caps charged and the system ready for a quick resume to either the D1 or D0 state. The part will resume from the D2 state to the D0 state within 2mS.

2.10. AFG D3

The D3-default state is available for HD Audio compliance. All converters are shut down. Port amplifiers and references are active but in a low power state to prevent pops. Resume times may be longer than those from D2, but still less than 10mS to meet Intel low power goals. The default power state for the Audio Function Group after power is applied is D3.

The traditional use for D3 was as a transitional state before power was removed (D3 cold) before the system entered into standby, hibernate, or shut-down. To conserve power, Intel now promotes using D3 whenever there are no active streams or other activity that requires the part to consume full power. The system remains in S0 during this time. When a stream request or user activity requires the CODEC to become active, the driver will immediately transition the CODEC from D3 to D0. To enable this use model, the CODEC must resume within 10mS and not pop. Intel HDA ECR-15b / Low Power White paper power goals are < 30mW when analog PC_Beep is not enabled, and < 60mW when analog PC_Beep is enabled.

While in AFG D3, the HD Audio controller may be in a D0 state (HD Audio bus active) or in a D3 state (HD Audio bus held in reset with no Bit_Clk, SData_Out, or Sync activity.) The expected behavior is as follows (see the ECR15b section for more information):

Function	HDA Bus active	HDA Bus stopped
Port Presence Detect state change	Unsolicited Response	Wake Event followed by an unsolicited response
GPIO state change	Unsolicited Response	Wake Event followed by an unsolicited response

2.10.1. AFG D3cold

The D3cold power state is the lowest power state available that does not use vendor specific verbs. While in D3cold, the CODEC will still respond to bus requests to revert to a higher power state (double AFG reset, link reset). However, audio processing, port presence detect, and other functions are disabled. Per the HD Audio bus ECR 015b, the D3cold state is intended to be used just prior to removing power to the CODEC. Typically, power will be removed within 200mS. However, the codec may exit from the D3cold state by generating 2, back-to-back, AFG reset events. Resume time from D3cold is less than 200mS.

2.11. Vendor Specific Function Group Power States D4/D5

The codec introduces vendor specific power states. A vendor defined verb is added to the Audio Function Group that combines multiple vendor specific power control bits into logical power states for use by the audio driver. The 2 states defined offer lower power than the 5 existing states defined in the HD Audio specification and ECR15b. The Vendor Specific D4 state provides lower digital power consumption relative to D3cold by disabling HD Audio link responses. Vendor specific D5 further reduces power consumption on the digital supply by turning off GPIO drivers, and reduces analog power consumption by turning off all analog circuitry except for reset circuits.

States D4/D5 are not entered until D3cold has been requested so are actually D3cold options rather than true, independent, power states. Software can pre-program the D4 or D5 state as a re-definition of how the part will behave when the D3cold power state is requested or software may enter D3cold, then set the D4 or D5 before performing the power state get command. The preferred method is to request D3cold, then select D4 or D5 as desired.This will reduce the severity of pops encountered when entering D4 or D5.

Both power states require a link reset or removal of DVDD to exit.

The CODEC may pop when using these verbs and transition times to an active state (D1 or D0 for example) may take several seconds.

2.12. Low-voltage HDA Signaling

The codec is compatible with either 1.5V or 3.3V HDA bus signaling; in the 48QFP package the voltage selection is done dynamically based on the input voltage of DVDD_IO. For the 40-QFN package, seperate orderable part numbers to use 1.5V or 3.3V HDA bus signaling.

DVDD_IO is currently not a logic configuration pin, but rather provides the digital power supply to be used for the HDA bus signals.

When in 1.5V mode, the codec can correctly decode BITCLK, SYNC, RESET# and SDO as they operate at 1.5V; additionally it will drive SDI and SDO at 1.5V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

2.13. Multi-channel capture

The capability to assign multiple “ADC Converters” to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported this is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) may be used to create a multi-channel input stream. There are no restrictions regarding digital microphones.

The ADC Converters can be associated with a single stream as long the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

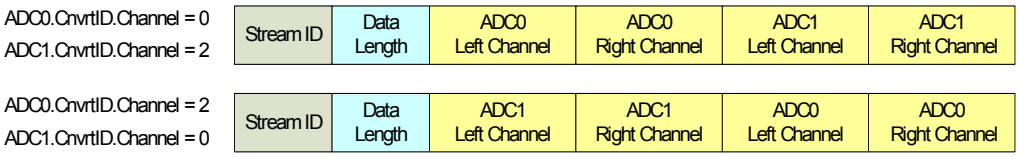
The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the “Multi-Converter Stream Critical Entries.” table.

An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2 & 3 is shown below. A 4 Channel stream can be created by assigning the same non-zero stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NmbrChan = 0011”.

ADC1 CnvtrID	**(NID = 0x08)**	
	[3:0]	Ch = 2
ADC0 CnvtrID	**(NID = 0x07)**	
	[3:0]	Ch=0

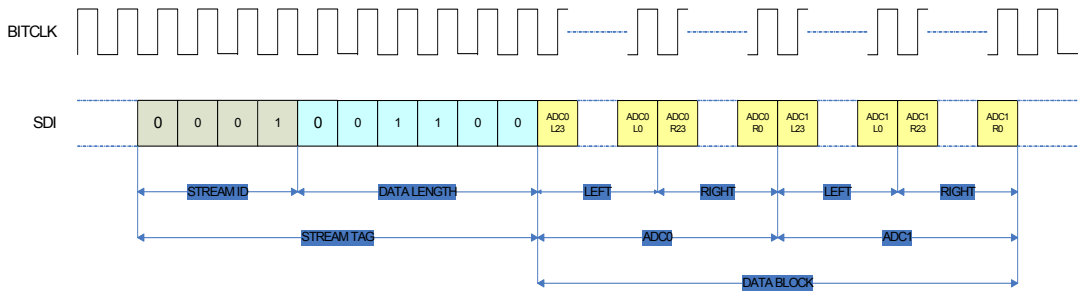
Table 10. Example channel mapping

Figure 3. Multi-channel capture



The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

Figure 4. Multi-channel timing diagram



ADC[1:0] Cnvtr	Bit Number	Sub Field Name	Description
	[15]	StrmType	Stream Type (TYPE): 0: PCM 1: Non-PCM (not supported)
	[14]	FrmtSmplRate	Sample Base Rate 0= 48kHz 1=44.1KHz
	[13:11]	SmplRateMultp	Sample Base Rate Multiple 000=48kHz/44.1kHz or less 001= x2 010= x3 (not supported) 011= x4 192kHz only, 176.4 not supported 100-111= Reserved
	[10:8]	SmplRateDiv	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 (not supported) 010= Divide by 3 (not supported) 011= Divide by 4 (not supported) 100= Divide by 5 (not supported) 101= Divide by 6 (not supported) 110= Divide by 7 (not supported) 111= Divide by 8 (not supported)

Table 11: Mult-channel

	[6:4]	BitsPerSmpl	Bits per Sample 000= 8 bits (not supported) 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
	[3:0]	NmbrChan	Number of Channels Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link. 0000=1 channel (not supported) 0001 = 2 channels … 1111= 16 channels.
	[7:4]	Strm	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
	[3:0]	Ch	Integer representing lowest channel used by converter. 0 and 2 are valid Entries If assigned to the same stream, one ADC must be assigned a value of 0 and the other ADC assigned a value of 2.

Table 11: Mult-channel

2.14. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0 and DMIC_CLK 2-pin interface. The DMIC0 signal is an input that carries individual channels of digital microphone data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels. This mode is selected using a vendor specific verb and the left time slot is copied to the ADC left and right inputs.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the internal master clock. The default frequency is 2.352Mhz.

The DMIC data input is reported as a stereo input pin widget that incorporates a boost amplifier. The pin widget is shown connected to the ADCs through the same multiplexors as the analog ports. Although the internal implementation is different between the analog ports and the digital microphones, the functionality is the same. In most cases, the default values for the DMIC clock rate and data sample phase will be appropriate and an audio driver will be able to configure and use the digital microphones exactly like an analog microphone.

To conserve power, the analog portion of the ADC will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input. This should take less than 10mS.

DMIC pin widgets support port presence detect directly using SENSE-C input on 4/5 DAC parts in a 48-pin package.