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SIX CHANNEL HD AUDIO CODEC

92HD73C

PREMIUM WLP 3/4 COMPLIANT

Description

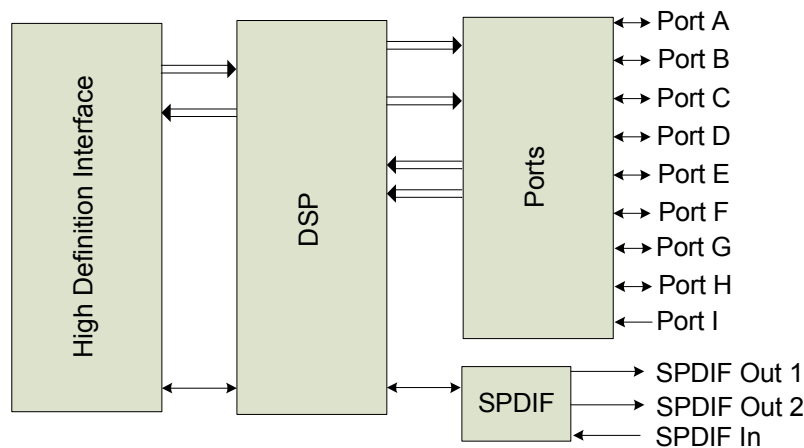
The 92HD73C codec is a low power optimized, high fidelity, 6-channel audio codec compatible with Intel's High Definition (HD) Audio Interface. The 92HD73C codec provides stereo 24-bit resolution with sample rates up to 192kHz. Dual SPDIF provides connectivity to consumer electronic equipment that is WLP compliant. The 92HD73C provides high quality, HD Audio capability to multimedia notebook and desktop PC applications.

Features

- **6 Channels (3 stereo DACs and 2 stereo ADCs) with 24-bit resolution**
 - Supports 5.1 audio
- **Microsoft WLP 3/4 premium logo compliant, as defined in WLP 3.09**
- **Optimized and flexible power management with pop/click mitigation**
- **2 independent S/PDIF Output converters for WLP compliant HDMI/SPDIF support.**

- **Support for 1.5V and 3.3V HDA signaling with runtime selection**
- **Digital microphone input (mono, stereo, or quad array)**
- **4 adjustable VREF Out pins for microphone bias**
- **High performance analog mixer**
- **9 stereo analog ports with presence detect capability**
- **Two-pin volume up/down control**
- **Digital and Analog PC BEEP to all outputs**
- **Integrated headphone amps (3)**
- **Sample rates up to 192kHz**
- **+3.3 V, +4 V, +4.75 V and +5 V analog power supply options**
- **Package Options**
 - 48-pin QFP RoHS package
 - 48-pin QFP RoHS package INDUSTRIAL TEMP

Block Diagram



Software Support

- Intuitive graphical user interface that allows configurability and preference settings
- SKPI (Kernel Processing Interface)
 - Enables plug-ins that can operate globally on all audio streams of the system
- 12 band fully parametric equalizer (SKPI plug-in)
 - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
 - System-level effects automatically disabled when external audio connections made
- Dynamics Processing (SKPI plug-in)
 - Enables improved voice articulation
 - Compressor/limiter allows higher average noise level without resonances or damage to speakers.
- IDT Vista APO wrapper
 - Enables multiple APOs to be used with the IDT Driver
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression
- Dynamic Stream Switching
 - Improved multi-streaming user experience with less support calls
- Dolby PC Entertainment Experience Logo Program
 - Dolby Master Studio™ (MS)
 - Dolby Home Theater™ (HT)
 - Dolby Sound Room™ (SR)
- Dolby Technologies
 - Dolby Headphone™, Dolby Virtual Speaker™
 - Dolby ProLogic II™, Dolby ProLogic IIx™
 - Dolby Digital Live™ (DDL)
- Maxx Player™ from Waves
- WOW™ and Tru Surround™ from SRS

TABLE OF CONTENTS

1. DESCRIPTION	11
1.1. Overview	11
1.2. Orderable Part Numbers	11
1.3. Block Diagram	12
1.4. Detailed Description	13
1.4.1. Port Functionality	13
1.4.2. Port Characteristics	13
1.4.3. Jack Detect	14
1.4.4. SPDIF Output	14
1.4.5. SPDIF Input	16
1.4.6. Analog Mixer	16
1.4.7. Input Multiplexers	17
1.4.8. ADC Multiplexers	17
1.4.9. Power Management	17
1.4.10. Low-voltage HDA Signaling	19
1.4.11. Multi-channel capture	19
1.4.12. EAPD	21
1.4.13. Digital Microphone Support	23
1.4.14. PC-Beep	28
1.4.15. Headphone Drivers	28
1.4.16. GPIO	29
1.4.17. External Volume Control	30
2. CHARACTERISTICS	32
2.1. Electrical Specifications	32
2.1.1. Absolute Maximum Ratings	32
2.1.2. Recommended Operating Conditions	32
2.2. 92HD73C 5V, 4.75V, and 3.3V Analog Performance Characteristics	33
3. PORT CONFIGURATIONS	39
4. FUNCTIONAL BLOCK DIAGRAMS	40
5. WIDGET INFORMATION AND SUPPORTED COMMAND VERBS	41
5.1. Widget List	42
5.2. Pin Configuration Default Register Settings	43
6. WIDGET INFORMATION	44
6.1. Root Node (NID = 00)	44
6.1.1. Root VendorID	44
6.1.2. Root RevID	45
6.2. AFG Node (NID = 01)	46
6.2.1. AFG Reset	46
6.2.2. AFG NodeInfo	46
6.2.3. AFG FGType	46
6.2.4. AFG AFGCap	47
6.2.5. AFG PCMCap	48
6.2.6. AFG StreamCap	49
6.2.7. AFG InAmpCap	49
6.2.8. AFG PwrStateCap	50
6.2.9. AFG GPIOCnt	50
6.2.10. AFG OutAmpCap	51
6.2.12. AFG UnsolResp	52
6.2.11. AFG PwrState	52
6.2.13. AFG GPIO	53
6.2.14. AFG GPIOEn	54
6.2.15. AFG GPIODir	55
6.2.16. AFG GPIOWakeEn	56

6.2.17. AFG GPIOUnsol	58
6.2.18. AFG GPIOSticky	59
6.2.19. AFG SubID	60
6.2.20. AFG GPIOIrty	61
6.2.21. AFG GPIODrive	62
6.2.22. AFG DMic	63
6.2.23. AFG AnaBeep	64
6.3. Port A Node (NID = 0A)	64
6.3.1. PortA WCap	64
6.3.2. PortA PinCap	65
6.3.3. PortA ConLst	66
6.3.4. PortA ConLstEntry0	67
6.3.5. PortA ConSelectCtrl	67
6.3.6. PortA PinWCntrl	68
6.3.7. PortA UnsolResp	68
6.3.8. PortA ChSense	69
6.3.9. PortA InAmpLeft	70
6.3.10. PortA InAmpRight	70
6.3.11. PortA ConfigDefault	70
6.4. PortB Node (NID = 0B)	72
6.4.1. PortB WCap	72
6.4.2. PortB PinCap	73
6.4.3. PortB ConLstEntry0	74
6.4.4. PortB ConLstEntry0	74
6.4.5. PortB ConSelectCtrl	75
6.4.6. PortB PinWCntrl	75
6.4.7. PortB UnsolResp	76
6.4.8. PortB ChSense	77
6.4.9. PortB InAmpLeft	77
6.4.10. PortD InAmpRight	78
6.4.11. PortB ConfigDefault	78
6.5. Port C Node (NID = 0C)	79
6.5.1. PortC WCap	79
6.5.2. PortC PinCap	81
6.5.3. PortC ConLst	82
6.5.4. PortC ConLstEntry0	82
6.5.5. PortC ConSelectCtrl	83
6.5.6. PortC PinWCntrl	83
6.5.7. PortC UnsolResp	84
6.5.8. PortC ChSense	84
6.5.9. PortC InAmpLeft	85
6.5.10. PortC InAmpRight	85
6.5.11. PortC ConfigDefault	86
6.6. Port D Node (NID = 0D)	87
6.6.1. PortD WCap	87
6.6.2. PortD PinCap	89
6.6.3. PortD ConLst	90
6.6.4. PortD ConLstEntry0	90
6.6.5. PortD ConSelectCtrl	91
6.6.6. PortD PinWCntrl	91
6.6.7. PortD UnsolResp	92
6.6.8. PortD ChSense	92
6.6.9. PortD InAmpLeft	93
6.6.10. PortD InAmpRight	93
6.6.11. PortD ConfigDefault	94

6.7. PortE Node (NID = 0E)	95
6.7.1. PortE WCap	95
6.7.2. PortE PinCap	96
6.7.3. PortE ConLst	97
6.7.4. PortE ConLstEntry0	98
6.7.5. PortE ConSelectCtrl	98
6.7.6. PortE PinWCntrl	99
6.7.7. PortE UnsolResp	99
6.7.8. PortE ChSense	100
6.7.9. PortE InAmpLeft	101
6.7.10. PortE InAmpRight	101
6.7.11. PortE ConfigDefault	101
6.8. PortF Node (NID = 0F)	103
6.8.1. PortF WCap	103
6.8.2. PortF PinCap	104
6.8.3. PortF ConLst	105
6.8.4. PortF ConLstEntry0	105
6.8.5. PortF ConSelectCtrl	106
6.8.6. PortF PinWCntrl	106
6.8.7. PortF UnsolResp	107
6.8.8. PortF ChSense	107
6.8.9. PortF InAmpLeft	108
6.8.10. PortF InAmpRight	108
6.9. PortG Node (NID = 10)	109
6.9.1. PortG WCap	109
6.9.2. PortG PinCap	110
6.9.3. PortG ConLst	111
6.9.4. PortG ConLstEntry0	112
6.9.5. PortG ConSelectCtrl	112
6.9.6. PortG PinWCntrl	113
6.9.7. PortG UnsolResp	113
6.9.8. PortG ChSense	114
6.9.9. PortG InAmpLeft	114
6.9.10. PortG InAmpRight	115
6.9.11. PortG ConfigDefault	116
6.10. PortH Node (NID = 11)	117
6.10.1. PortH WCap	117
6.10.2. PortH PinCap	118
6.10.3. PortH ConLst	119
6.10.4. PortH ConLstEntry0	120
6.10.5. PortH ConSelectCtrl	120
6.10.6. PortH PinWCntrl	121
6.10.7. PortH UnsolResp	121
6.10.8. PortH ChSense	122
6.10.9. PortH InAmpLeft	122
6.10.10. PortH InAmpRight	123
6.10.11. PortH ConfigDefault	124
6.11. PortI Node (NID = 12)	125
6.11.1. PortI WCap	125
6.11.2. PortI PinCap	126
6.11.3. PortI PinWCntrl	127
6.11.4. PortI UnsolResp	127
6.11.5. PortI ChSense	128
6.11.6. PortI ConfigDefault	128
6.12. DMic0 Node (NID = 13)	130

6.12.1. DMic0 WCap	130
6.12.2. DMic0 PinCap	131
6.12.3. DMic0 PinWCntrl	132
6.12.4. DMic0 InAmpLeft	132
6.12.5. DMic0 InAmpRight	133
6.12.6. DMic0 ConfigDefault	133
6.13. DMic1 Node (NID = 14)	134
6.13.1. DMic1 WCap	134
6.13.2. DMic1 PinCap	136
6.13.3. DMic1 PinWCntrl	137
6.13.4. DMic1 InAmpLeft	137
6.13.5. DMic1 InAmpRight	137
6.13.6. DMic1 ConfigDefault	138
6.14. DAC0 Node (NID = 15)	139
6.14.1. DAC0 WCap	139
6.14.2. DAC0 Cnvtr	140
6.14.3. DAC0 OutAmpLeft	141
6.14.4. DAC0 OutAmpRight	142
6.14.5. DAC0 PwrState	142
6.14.6. DAC0 CnvtrID	143
6.14.7. DAC0 LR	143
6.15. DAC1 Node (NID = 16)	144
6.15.1. DAC1 WCap	144
6.15.2. DAC1 Cnvtr	145
6.15.3. DAC1 OutAmpLeft	146
6.15.4. DAC1 OutAmpRight	147
6.15.5. DAC1 PwrState	147
6.15.6. DAC1 CnvtrID	148
6.15.7. DAC1 LR	148
6.16. DAC2 Node (NID = 17)	149
6.16.1. DAC2 WCap	149
6.16.2. DAC2 Cnvtr	150
6.16.3. DAC2 OutAmpLeft	151
6.16.4. DAC2 OutAmpRight	152
6.16.5. DAC2 PwrState	152
6.16.6. DAC2 CnvtrID	153
6.16.7. DAC2 LR	153
6.17. Reserved (NID = 18)	154
6.18. Reserved (NID = 19)	154
6.19. ADC0 Node (NID = 1A)	154
6.19.1. ADC0 WCap	154
6.19.2. ADC0 ConLst	155
6.19.3. ADC0 ConLstEntry0	156
6.19.4. ADC0 Cnvtr	156
6.19.5. ADC0 ProcState	157
6.19.6. ADC0 PwrState	158
6.19.7. ADC0 CnvtrID	158
6.20. ADC1 Node (NID = 1B)	159
6.20.1. ADC1 WCap	159
6.20.2. ADC1 ConLst	160
6.20.3. ADC1 ConLstEntry0	161
6.20.4. ADC1 Cnvtr	161
6.20.5. ADC1 ProcState	162
6.20.6. ADC1 PwrState	163
6.20.7. ADC1 CnvtrID	163

6.21. DigBeep Node (NID = 1C)	164
6.21.1. DigBeep WCap	164
6.21.2. DigBeep OutAmpCap	164
6.21.3. DigBeep OutAmpLeft	165
6.21.4. DigBeep Gen	166
6.22. Mixer Node (NID = 1D)	166
6.22.1. Mixer WCap	166
6.22.2. Mixer ConLst	168
6.22.3. Mixer ConLstEntry0	168
6.22.4. Mixer InAmpCap	169
6.22.5. Mixer InAmpLeft0	169
6.22.6. Mixer InAmpRight0	170
6.22.7. Mixer InAmpLeft1	170
6.22.8. Mixer InAmpRight1	171
6.22.9. Mixer InAmpLeft2	171
6.22.10. Mixer InAmpRight2	172
6.22.11. Mixer InAmpLeft3	172
6.22.12. Mixer InAmpRight3	173
6.22.13. Mixer InAmpLeft4	173
6.22.14. Mixer InAmpRight4	174
6.23. MixerOutVol Node (NID = 1E)	174
6.23.1. MixerOutVol WCap	174
6.23.2. MixerOutVol ConLst	176
6.23.3. MixerOutVol ConLstEntry0	176
6.23.4. MixerOutVol OutAmpCap	177
6.23.5. MixerOutVol OutAmpLeft	177
6.23.6. MixerOutVol OutAmpRight0	178
6.24. VolumeKnob Node (NID = 1F)	178
6.24.1. VolumeKnob WCap	178
6.24.2. VolumeKnob VolKnobCap	179
6.24.3. VolumeKnob ConLst	179
6.24.4. VolumeKnob ConLstEntry0	180
6.24.5. VolumeKnob UnsolResp	180
6.24.6. VolumeKnob Cntrl	181
6.24.7. VolumeKnob VS	181
6.25. ADC0Mux Node (NID = 20)	182
6.25.1. ADC0Mux WCap	182
6.25.2. ADC0Mux ConLst	183
6.25.3. ADC0Mux ConLstEntry0	184
6.25.4. ADC0Mux ConSelectCtrl	184
6.25.5. ADC0Mux LR	185
6.25.6. ADC0Mux OutAmpCap	185
6.25.7. ADC0Mux OutAmpLeft	186
6.25.8. ADC0Mux OutAmpRight	187
6.26. ADC1Mux Node (NID = 21)	187
6.26.1. ADC1Mux WCap	187
6.26.2. ADC1Mux ConLst	188
6.26.3. ADC1Mux ConLstEntry0	189
6.26.4. ADC1Mux ConSelectCtrl	189
6.26.5. ADC1Mux LR	190
6.26.6. ADC1Mux OutAmpCap	190
6.26.7. ADC1Mux OutAmpLeft	191
6.26.8. ADC1Mux OutAmpRight	192
6.27. Dig0Pin Node (NID = 22)	192
6.27.1. Dig0Pin WCap	192

6.27.2. Dig0Pin PinCap	193
6.27.3. Dig0Pin ConLst	194
6.27.4. Dig0Pin ConLstEntry0	195
6.27.5. Dig0Pin ConSelectCtrl	195
6.27.6. Dig0Pin PinWCntrl	196
6.27.7. Dig0Pin ConfigDefault	196
6.28. Dig1Pin Node (NID = 23)	198
6.28.1. Dig1Pin WCap	198
6.28.2. Dig1Pin PinCap	199
6.28.3. Dig1Pin ConLst	200
6.28.4. Dig1Pin ConLstEntry0	200
6.28.5. Dig1Pin ConSelectCtrl	201
6.28.6. Dig1Pin PinWCntrl	201
6.28.7. Dig1Pin ConfigDefault	202
6.29. Dig2Pin Node (NID = 24)	203
6.29.1. Dig2Pin WCap	203
6.29.2. Dig2Pin PinCap	205
6.29.3. Dig2Pin PinWCntrl	206
6.29.4. Dig2Pin UnsolResp	206
6.29.5. Dig2Pin ChSense	207
6.29.6. Dig2Pin PwrState	207
6.29.7. Dig2Pin EAPD	208
6.29.8. Dig2Pin ConfigDefault	208
6.30. SPDIFOut0 Node (NID = 25)	210
6.30.1. SPDIFOut0 WCap	210
6.30.2. SPDIFOut0 PCMCap	211
6.30.3. SPDIFOut0 StreamCap	212
6.30.4. SPDIFOut0 Cnvtr	213
6.30.5. SPDIFOut0 CnvtrID	214
6.30.6. SPDIFOut0 DigCnvtr	214
6.30.7. SPDIFOut0 OutAmpCap	215
6.30.8. SPDIFOut0 OutAmpLeft	216
6.30.9. SPDIFOut0 OutAmpRight	216
6.31. SPDIFOut1 Node (NID = 26)	216
6.31.1. SPDIFOut1 WCap	216
6.31.2. SPDIFOut1 PCMCap	218
6.31.3. SPDIFOut1 StreamCap	219
6.31.4. SPDIFOut1 Cnvtr	219
6.31.5. SPDIFOut1 CnvtrID	220
6.31.6. SPDIFOut1 DigCnvtr	221
6.31.7. SPDIFOut1 OutAmpCap	222
6.31.8. SPDIFOut1 OutAmpLeft	222
6.31.9. SPDIFOut1 OutAmpRight	223
6.32. SPDIFIn Node (NID = 27)	223
6.32.1. SPDIFOut1 WCap	223
6.32.2. SPDIFInCnvtr	225
6.32.3. SPDIFIn PCMCap	226
6.32.4. SPDIFIn StreamCap	227
6.32.5. SPDIFIn ConLst	227
6.32.6. SPDIFIn ConLstEntry0	228
6.32.7. SPDIFIn CnvtrID	228
6.32.8. SPDIFIn DigCnvtr	229
6.32.9. SPDIFIn OutAmpCap	230
6.32.10. SPDIFIn InAmpLeft	230
6.32.11. SPDIFIn InAmpRight	231

6.32.12. SPDIFIn VS	231
6.32.13. SPDIFIn Status	232
6.33. InPort0Mux Node (NID = 28)	235
6.33.1. InPort0Mux WCap	235
6.33.2. InPort0Mux ConLst	236
6.33.3. InPort0Mux ConLstEntry0	236
6.33.4. InPort0Mux ConSelectCtrl	237
6.34. InPort1Mux Node (NID = 29)	237
6.34.1. InPort1Mux WCap	237
6.34.2. InPort1Mux ConLst	239
6.34.3. InPort1Mux ConLstEntry0	239
6.34.4. InPort1Mux ConSelectCtrl	240
6.35. InPort2Mux Node (NID = 2A)	240
6.35.1. InPort2Mux WCap	240
6.35.2. InPort2Mux ConLst	241
6.35.3. InPort2Mux ConLstEntry0	242
6.35.4. InPort1Mux ConSelectCtrl	242
6.36. InPort3Mux Node (NID = 2B)	243
6.36.1. InPort3Mux WCap	243
6.36.2. InPort3Mux ConLst	244
6.36.3. InPort3Mux ConLstEntry0	245
6.36.4. InPort3Mux ConSelectCtrl	245
7. DISCLAIMER	246
8. PINOUTS	247
8.1. Pin Assignment	247
8.2. Pin Tables for 48-pin QFP	248
9. PACKAGE OUTLINE AND PACKAGE DIMENSIONS	251
9.1. 48-Pin QFP Package	251
10. SOLDER REFLOW PROFILE	252
10.1. Standard Reflow Profile Data	252
10.2. Pb Free Process - Package Classification Reflow Temperatures	253
11. REVISION HISTORY	253

LIST OF FIGURES

Figure 1. 92HD73D Block Diagram	12
Figure 2. System Diagram	12
Figure 3. Multi-channel capture	20
Figure 4. Multi-channel timing diagram	20
Figure 5. EAPD	23
Figure 6: Mono Digital Microphone (data is ported to both left and right channels)	25
Figure 7: Stereo Digital Microphone Configuration	26
Figure 8: Quad Digital Microphone Configuration	27
Figure 9: External Volume Control Circuit	31
Figure 10. Port Configuration	39
Figure 11. Functional Block Diagram	40
Figure 12. Widget Diagram	41
Figure 13. Pin Assignment	253
Figure 14. 48-pin QFP Package Drawing	257
Figure 15. Solder Reflow Profile	258

LIST OF TABLES

Table 1. Port Functionality	13
Table 2. Analog I/O Port Behavior	14
Table 4. SPDIF OUT 0 (Pin 48) Behavior	15
Table 5. SPDIF OUT 1 (Pin 40) Behavior	15
Table 6. Input Multiplexers	17
Table 7. Function state vs. AFG power state	17
Table 10. EAPD Behavior	22
Table 11. Valid Digital Mic Configurations	24
Table 12. DMIC_CLK and DMIC_0,1 Operation During Power States	24
Table 13. GPIO Pin mapping	29
Table 14. Electrical Specification: Maximum Ratings	32
Table 15. Recommended Operating Conditions	32
Table 16. 92HD73D 5V, 4.75V, and 3.3V Analog Performance Characteristics	33
Table 17. High Definition Audio Widget	42
Table 18. Pin Configuration Default Settings	43
Table 19. Command Format for Verb with 4-bit Identifier	45
Table 20. Command Format for Verb with 12-bit Identifier	45
Table 21. Solicited Response Format	45
Table 22. Unsolicited Response Format	45
Table 23. Digital Pins	254
Table 24. Analog Pins	254
Table 25. Power Pins	255
Table 26. Standard Reflow Profile	258
Table 27. Pb-Free Process Reflow	259

1. DESCRIPTION

1.1. Overview

The 92HD73C is a high fidelity, 6-channel audio codec compatible with the Intel High Definition (HD) Audio Interface. The 92HD73C codec provides high quality, HD Audio capability to desktop and multi-media notebook.

The 92HD73C is designed to meet or exceed premium logo requirements for Microsoft's Windows Logo Program (WLP) 3.09 and revisions 4 as indicated in WLP 3.09.

The 92HD73C provides stereo 24-bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. 92HD73C SPDIF outputs support sample rates of 192kHz, 176.4kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz. 92HD73C SPDIF input supports sample rates of 96kHz, 88.2kHz, 48kHz, and 44.1kHz. Additional sample rates are supported by the driver software.

The 92HD73C supports a wide range of desktop and consumer 8 channel configurations. The 2 independent SPDIF output interfaces provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. Simultaneous HDMI and SPDIF output is possible.

MIC inputs can be programmed with 0/10/20/30dB boost. For more advanced configurations, the 92HD73C has 8 General Purpose I/O (GPIO).

The port presence detect capabilities allow the codecs to detect when audio devices are connected to the codec. Load impedance sensing helps identify attached peripherals for easy set-up and a better user experience. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The 92HD73C operates with a 3.3V digital supply and either 3.3V, or 5V analog supply. It can also work with 1.5V and 3.3V HDA signaling; the correct signalling level is selected dynamically based on the power supply voltage on the DVDD-IO pin.

The 92HD73C1X is available in a 48-pin LQFP Environmental (ROHS) package.

The 92HD73C1T is available in a 48-pin LQFP Environmental (ROHS) INDUSTRIAL Temperature package.

Additional products with the same features as the 92HD73C are the 10-channel 92HD73E and the 8-channel 92HD73D.

1.2. Orderable Part Numbers

92HD73C1X5PRGXyyX	6 channel, 5V, 48QFP
92HD73C1T5PRGIyyX	6 channel, 5V, 48QFP i-temp

yy = silicon stepping/revision, contact sales for current data.

Add an "8" to the end for tape and reel delivery. Min/Mult order quantity 2ku.

Contact IDT if interested in 3.3V Analog version.

1.3. Block Diagram

Figure 1. 92HD73C Block Diagram

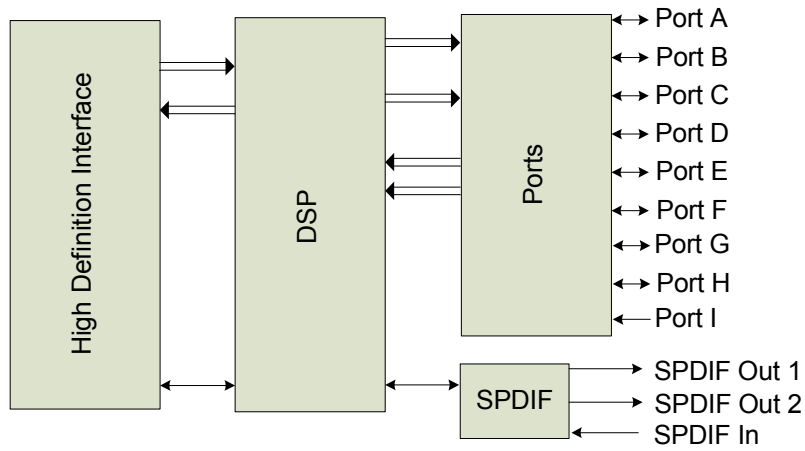
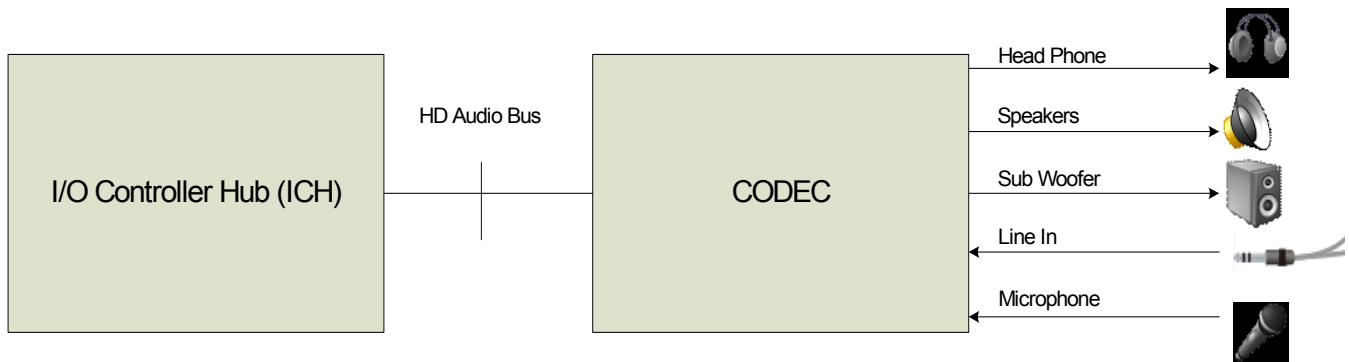


Figure 2. System Diagram



1.4. Detailed Description

1.4.1. Port Functionality

Multi-function (Input / output) ports allow for the highest possible flexibility. 8 bi-directional ports (3 headphone capable) support a wide variety of consumer desktop and mobile system use models.

Pins	Port	Input	Output	Headphone	Mic Bias (Vref pin)	Input boost amp ¹	CD (pseudo differential)
39/41	A	Yes	Yes	Yes	Yes	Yes	
21/22	B	Yes	Yes	Yes	Yes	Yes	
23/24	C	Yes	Yes		Yes	Yes	
35/36	D	Yes	Yes	Yes		Yes	
14/15	E	Yes	Yes		Yes	Yes	
16/17	F	Yes	Yes			Yes	
43/44	G	Yes	Yes			Yes	
45/46	H	Yes	Yes			Yes	
18/19/20	CD (Port I)	Yes					Yes
48	SPDIF_OUT0		Yes				
40	SPDIF_OUT1		Yes				
47	SPDIF_IN	Yes					
4 (CLK=2)	DMIC0	Yes				Yes	
30 (CLK=2)	DMIC1	Yes				Yes	

Table 1. Port Functionality

Note¹: 40dB boost requires using the IDT driver. When the 40dB mic boost feature is enabled, additional gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB MIC boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.

1.4.2. Port Characteristics

Universal (Bi-directional) jacks are supported on all ports except the CD input. Ports A, B, and D are designed to drive a set of 32 ohm (nominal) headphones or a 10K (nominal) load with on board shunt resistance as low as 20K ohms (typical - used to maintain coupling CAP bias.) Line Level outputs are intended to drive an external 10K speaker load (nominal) and an on board shunt resistor of 20K-47K (nominal). However, applications may support load impedances of 5K ohms and above. Input ports are 47K (nominal) at the pin.

DAC full scale output and intended full scale input levels are 1V rms. Line output ports and Headphone output ports on 92HD73C may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports are always on to prevent pops/clicks associated with charging and discharging output coupling capacitors. This maintains proper bias on output coupling caps even in D3 as long as AVDD is available. Unused ports should be left unconnected. When updating existing designs to use the 92HD73C, ensure that there are no conflicts between the output ports on 92HD73C and existing circuitry.

AFG Power State	Input Enable	Output Enable	Mute	Port Behavior
D0-D2	1	1	-	Not allowed. Port becomes input.
	1	0	-	Active - port enabled as input
	0	1	0	Active - port enabled as output
	0	1	1	Mute - port enabled as output but drives silence
	0	0	-	Inactive - Port keeps coupling caps charged (same as mute.)
D3		-	-	Inactive (lower power) - Port keeps output coupling caps charged but consumes less power.

Table 2. Analog I/O Port Behavior

1.4.3. Jack Detect

Plugs inserted to a jack on Ports A, B, C, & D are detected using SENSE_A. Plugs inserted to a jack on Ports E, F, G, and H are detected using SENSE_B. The following table summarizes the proper resistor tolerances for different analog supply voltages.

SENSE_C, is different from SENSE_A and SENSE_B. Because SENSE_C only determines the presence of a plug for the CD port (port I), SENSE_C is a simple digital input pin referenced to the analog supply. An internal pull-up resistor is provided. No external resistors are needed (jack switch shorts to ground when a plug is inserted.) If external components are added, or if the pin is driven by a logic gate, care should be taken to ensure that the pin voltage is above 70% of AVDD when no plug is in the jack and less than 30% AVDD when a plug is inserted

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance SENSE_A (If port D used)	Resistor Tolerance SENSE_A (If port D is not used)	Resistor Tolerance SENSE_B (If port H used)	Resistor Tolerance SENSE_B (If port H is not used)
5V	1%	1%	1%	1%
4.75V	1%	1%	1%	1%
4V	0.50%	1%	0.50%	1%
3.3V	0.10%	1%	0.10%	1%

Table 3: SENSE Resistor Tolerance

See reference design for more information on Jack Detect implementation.

1.4.4. SPDIF Output

All SPDIF Outputs can operate at 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4KHz, and 192KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

A second independant SPDIF Output is provided as an option for WLP compliant HDMI and SPDIF outputs. Its function is identical to the primary SPDIF output.

Note: Peak to peak jitter is currently limited to less than 4.5nS (half of the internal master clock cycle) which does not meet the IEC-60958-3 0.05UI requirement at 192KHz.

The two SPDIF output converters can not be aligned in phase with the DACs. Even when attached to the same stream, the two SPDIF output converters may be misaligned with respect to their frame boundaries.

SPDIF Outputs on pins 48 and 40 are outlined in tables below. Pin 47 behavior table resides in the EAPD section

AFG Power State	RESET#	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
D0	De-Asserted (High)	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Enabled	Disabled	-	Active - Pin drives 0 (internal pull-down NA)
	De-Asserted (High)	Enabled	Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA)
	De-Asserted (High)	Enabled	Enabled	1-15	Active - Pin drives SPDIFOut0 data (internal pull-down NA)
D1-D2	De-Asserted (High)	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Enabled	-	-	Active - Pin drives 0 (internal pull-down NA)
D3	De-Asserted (High)	-	-	-	Hi-Z (internal pull-down enabled)

Table 4. SPDIF OUT 0 (Pin 48) Behavior

AFG Power State	RESET#	GPIO 3 Enable	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
D0-D3	De-Asserted (High)	Enabled	-	-	-	Active - Pin reflects GPIO7 configuration (internal pull-up enabled)

Table 5. SPDIF OUT 1 (Pin 40) Behavior

AFG Power State	RESET#	GPIO 3 Enable	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0	De-Asserted (High)	Disabled	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Disabled	-	Active - Pin drives 0 (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Enabled	1-15	Active - Pin drives SPDIFOut1 data (internal pull-down enabled)
D1-D2	De-Asserted (High)	Disabled	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	-	-	Active - Pin drives 0 (internal pull-down NA)
D3	De-Asserted (High)	Disabled	-	-	-	Hi-Z (internal pull-down enabled)

Table 5. SPDIF OUT 1 (Pin 40) Behavior

1.4.5. SPDIF Input

SPDIF IN can operate at 44.1 KHz, 48 KHz, 88.2 KHz or 96 KHz, and implements internal Jack Sensing.

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs. Advanced features such as record-slot-select and SPDIF_IN routing to the DAC allow for simultaneous record and play.

1.4.6. Analog Mixer

An analog mixer is available on the 92HD73C. The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input. A master volume follows mixing and provides gain from -46.5dB to 0dB in 1.5dB steps.

The following inputs are available:

- CD
- Analog PC_Beep
- Inport0_Mux
- Inport1_Mux
- Inport2_Mux
- Inport3_mux

1.4.7. Input Multiplexers

92HD73C implements 4 port input multiplexers. These multiplexers allow a preselection of one of four possible inputs:

Inport0_Mux	Inport1_Mux	Inport2_Mux	Inport3_mux
Port A	Port A	Port B	DAC 0
Port B	Port E	Port C	DAC 1
Port D	Port G	Port G	DAC 2
Port F	Port H	Port H	DAC 3

Table 6. Input Multiplexers

1.4.8. ADC Multiplexers

92HD73C implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function (0 to +22.5dB gain in 1.5dB steps) as an output amp and allow a preselection of one of 12 possible inputs:

- DMIC 0
- DMIC 1
- Mixer output
- CD input
- Ports A - H

1.4.9. Power Management

The HD Audio specification defines power states, power state widgets, and power state verbs. Power management is implemented at several levels. The Audio Function Group (AFG) and all converter widgets support the power state verb F05/705 (as well as the pin widget associated with pin 47.) Converter widgets are active in D0 and inactive in D1-D3.

The following table describes what functionality is active in each power state supported by the AFG.

Function	D0	D1 ¹	D2	D3	vendor specific
SPDIF Outputs	On	Off	Off	Off	-
SPDIF Inputs	On	Off	Off	Off	-
Digital Microphone inputs	On	Off	Off	Off	-
DAC	On	Off	Off	Off	-
D2S	On	Off	Off	Off	-
ADC	On	Off	Off	Off	-
ADC Volume Control	On	Off	Off	Off	-
Ref ADC	On	Off	Off	Off	-
Analog Clocks	On	Off	Off	Off	-
GPIO pins	On	On	On	On	-
VrefOut Pins	On	On	Off	Off	-

Table 7. Function state vs. AFG power state

Function	D0	D1 ¹	D2	D3	vendor specific
Input Boost	On	On	Off	Off	-
Analog mixer	On	On	Off	Off	-
Mixer Volumes	On	On	Off	Off	
Analog PC_Beep	On	On	Off	Off	
Digital PC_Beep	On	On	On	On	-
Lo Amp	On	On	On	Low Drive ²	Programmable
HP Amps	On	On	On	Low Drive ²	Programmable
VAG amp	On	On	On	Low Drive ³	Programmable
Port Sense	On	On	On	On ⁴	Programmable
Reference Bias generator	On	On	On	On	Programmable ⁵
Reference Bandgap core	On	On	On	On	Programmable ⁵
HD Audio-Link	On	On	On	On ⁶	-

Table 7. Function state vs. AFG power state

- 1.No DAC or ADC streams are active. Analog mixing and loop thru are supported.
- 2.VAG is kept active when ports are disabled or in D2/D3. Ports may be powered down using vendor specific verbs.
- 3.VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
4. BITCLK must be active and both AVDD and DVDD must be available for Port Sense to operate.
- 5.Vendor specific bit for Ref Top controls VAG generator, Bandgap Reference, and Reference bias generator. Place part into D3 and power down all ports (using vendor specific verbs) before powering down Ref Top.
- 6.Obviously not active if BITCLK is not running (Controller in D3).

1.4.9.1. AFG D0

The AFG D0 state is the active state for the device. All functions are active if their power state (if they support power management at their node level) has been set to D0.

1.4.9.2. AFG D1

D1 is a lower power mode where all converter widgets are disabled. Analog mixer and port functions are active.

1.4.9.3. AFG D2

The D2 state further reduces power by disabling the mixer and port functions. The port amplifiers and internal references remain active to keep port coupling caps charged and the system ready for a quick resume to either the D1 or D0 state.

1.4.9.4. AFG D3

The D3-default state is available for HD Audio compliance. All converters are shut down. Port amplifiers and references are active but in a low power state to prevent pops. Resume times may be longer than those from D2, but still very fast to meet Intel low power goals.

The traditional use for D3 was as a transitional state before power was removed (D3 cold) before the system entered into standby, hibernate, or shut-down. To conserve power, Intel now promotes using D3 whenever there are no active streams or other activity that requires the part to consume full power. The system remains in S0 during this time. When a stream request or user activity requires

the CODEC to become active, the driver will immediately transition the CODEC from D3 to D0. To enable this use model, the CODEC must resume within 10mS and not pop.

The default power state for the Audio Function Group after reset is D3-default

1.4.9.5. AFG D3 and vendor specific verbs

The programmable values, exposed via vendor-specific settings, are under the IDT Device Driver control for further power reduction.

1.4.10. Low-voltage HDA Signaling

The 92HD73C is compatible with either 1.5V or 3.3V HDA bus signaling; the voltage selection is done dynamically based on the input voltage of DVDD_IO.

When in 1.5V mode, the 92HD73C can correctly decode BITCLK, SYNC, RESET# and SDO as they operate at 1.5V; additionally it will drive SDI and SDO at 1.5V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

1.4.11. Multi-channel capture

The capability to assign multiple ADC “Input Converters” to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported and is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) may be used to create a multi-channel input stream. There are no restrictions regarding digital microphones. However, the SPDIF input can not be used with an ADC to create a 4-channel stream. SPDIF_In only supports stereo capture.

The ADC Converters can be associated with a single stream as long as the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NnbrChan field. These are listed the “Multi-Converter Stream Critical Entries” table.

An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2&3 is shown below. A 4 Channel stream can be created by assigning the same non-zero stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NnbrChan = 0011”.

ADC1 CnvtrID	(NID = 0x08)	
	[3:0]	Ch = 2
ADC0 CnvtrID	(NID = 0x07)	
	[3:0]	Ch = 0

Table 8: Example channel mapping

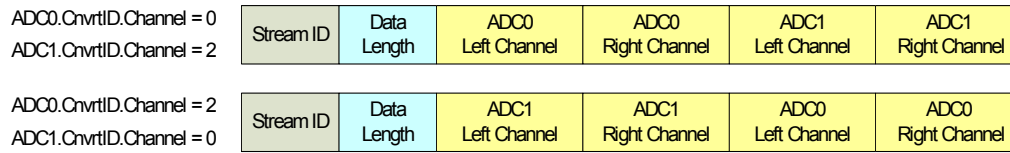


Figure 3. Multi-channel capture

The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

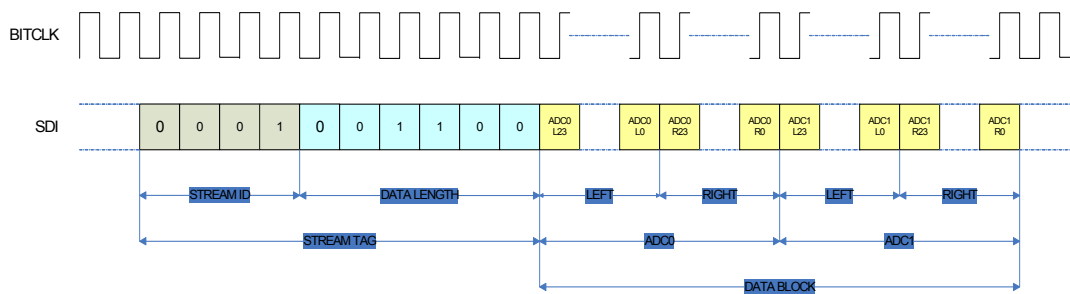


Figure 4. Multi-channel timing diagram

ADC[1:0] Cnvr	Bit Number	Sub Field Name	Description
	[15]	StrmType	Stream Type (TYPE): 0: PCM 1: Non-PCM (not supported)
	[14]	FrmtSmplRate	Sample Base Rate 0= 48kHz 1=44.1KHz
	[13:11]	SmplRateMultp	Sample Base Rate Multiple 000=48kHz/44.1kHz or less 001= x2 010= x3 (not supported) 011= x4 100-111= Reserved

Table 9: Multi-Converter Stream Critical Entries.

	[10:8]	SmplRateDiv	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 (not supported) 010= Divide by 3 (not supported) 011= Divide by 4 (not supported) 100= Divide by 5 (not supported) 101= Divide by 6 (not supported) 110= Divide by 7 (not supported) 111= Divide by 8 (not supported)
	[6:4]	BitsPerSmpl	Bits per Sample 000= 8 bits (not supported) 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
	[3:0]	NmbrChan	Number of Channels Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link. 0000=1 channel (not supported) 0001 = 2 channels ... 1111= 16 channels.
ADC[1:0] CnvtrID	Bit Number	Sub Field Name	Description
	[7:4]	Strm	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
	[3:0]	Ch	Integer representing lowest channel used by converter. 0 and 2 are valid Entries If assigned to the same stream, one ADC must be assigned a value of 0 and the other ADC assigned a value of 2.

Table 9: Multi-Converter Stream Critical Entries.

1.4.12. EAPD

The EAPD pin (pin 47) also supports SPDIF_In and GPIO functions. The pin defaults to EAPD after power on reset and will remain in EAPD mode until either GPIO is enabled for pin 47 or the port I/O is enabled to support SPDIF. Although named External Amplifier Power Down (EAPD) by the HD Audio specification, this pin operates as an external amplifier power up signal. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up, and a 0 causes it to power down. When the EAPD value = 1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value may remain 1. The default state of this pin is 0 (driving low) and a Pull-down prevents the line from floating high when the part is in reset.

AFG Power State	RESET#	GPIO Enable	Input Enable	EAPD Power State	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
D0	De-Asserted (High)	Enabled	-	-	Active - Pin reflects GPIO0 configuration (internal pull-up enabled)
	De-Asserted (High)	Disabled	Enabled	-	Active - Pin is SPDIF_In
	De-Asserted (High)	Disabled	Disabled	D0-D1	Active - Pin drives the value of the EAPD bit (internal pull-down enabled)
	De-Asserted (High)	Disabled	Disabled	D2-D3	Hi-Z (internal pull-down enabled)
D1	De-Asserted (High)	Disabled	Enabled	-	Inactive - Pin configured as input, but SPDIF_In idle.
	De-Asserted (High)	Disabled	Disabled	D0-D1	Active - Pin drives the value of the EAPD bit (internal pull-down enabled)
	De-Asserted (High)	Disabled	Disabled	D2-D3	Hi-Z (internal pull-down enabled)
D2	De-Asserted (High)	Disabled	-	D0-D3	Hi-Z (internal pull-down enabled)
D3	De-Asserted (High)	Disabled	-	D0-D3	Hi-Z (internal pull-down enabled)

Table 10. EAPD Behavior

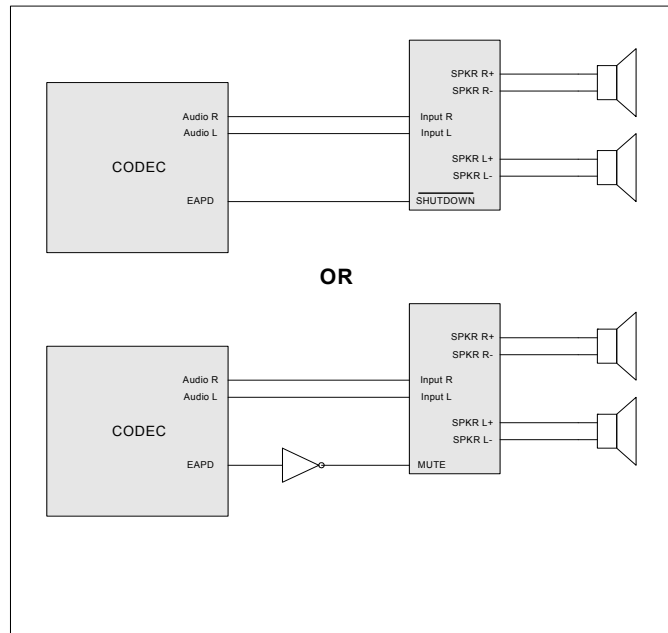


Figure 5. EAPD

1.4.13. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0, DMIC1, and DMIC_CLK 3-pin interface. The DMIC0 and DMIC1 signals are inputs that carry individual channels of digital Mic data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the 24Mhz internal clock. The default frequency is 2.352Mhz.

The two DMIC data inputs are reported as two stereo input pin widgets that incorporate a boost amplifier. The pin widgets are shown connected to the ADCs through the same multiplexors as the analog ports. Although the internal implementation is different between the analog ports and the digital microphones, the functionality is the same. In most cases, the default values for the DMIC clock rate and data sample phase will be appropriate and an audio driver will be able to configure and use the digital microphones exactly like an analog microphone.

92HD73C supports the following digital microphone configurations:

Digital Mics	Data Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones
1	Single Edge	0, or 1	Available on either DMIC_0 or DMIC_1 Both ADC Channels produce data, may be in phase or out by 1/2 DMIC_CLK period depending upon external configuration and timing
2	Double Edge on either DMIC_0 or 1 OR Single Edge on DMIC_0 and 1	0, or 1	Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. If both DMIC_0 and DMIC_1 are used to support 2 digital microphones, 2 separate ADC units will be used, however, this configuration is not recommended since it consumes two stereo ADC resources.
3	Double Edge on one DMIC pin and Single Edge on the second DMIC pin.	0, or 1	Requires both DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration
4	Double Edge	0, or 1	Connected to DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration

Table 11. Valid Digital Mic Configurations

Power State	DMIC Widget Enabled	DMIC_CLK Output	DMIC_0,1	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D1-D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down

Table 12. DMIC_CLK and DMIC_0,1 Operation During Power States

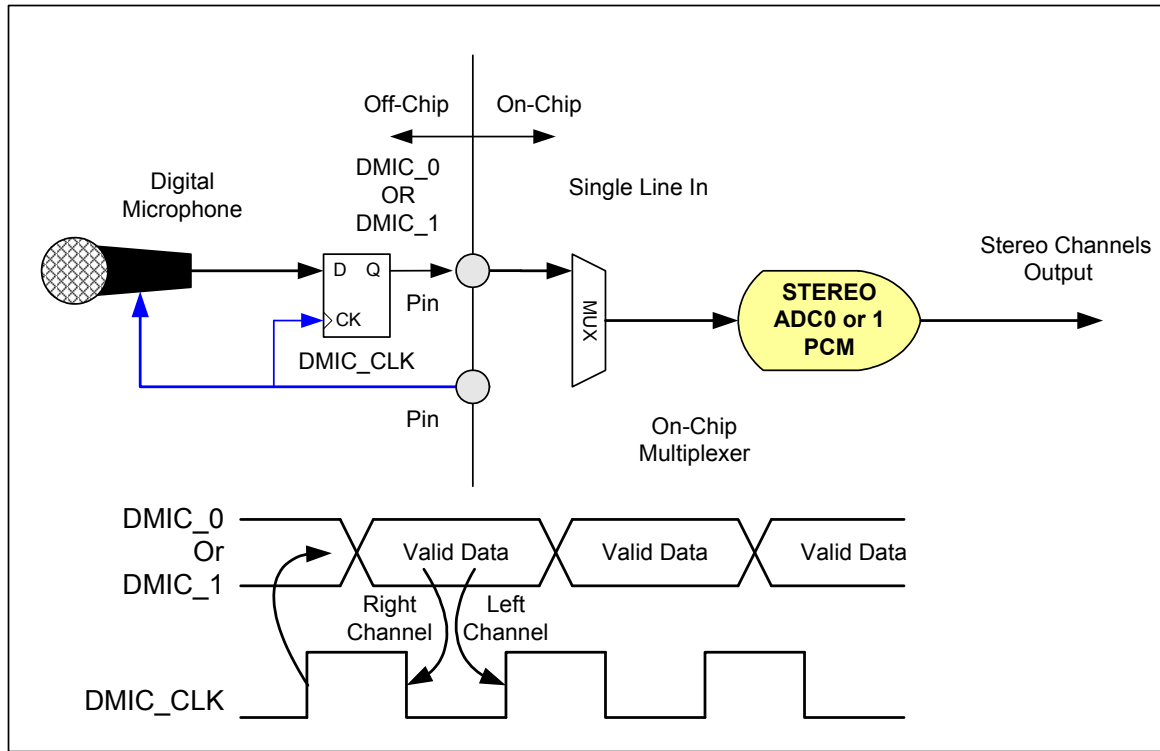


Figure 6: Mono Digital Microphone (data is ported to both left and right channels)