Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

DATASHEET

TEN CHANNEL HD AUDIO CODEC

92HD73E

Description

The 92HD73E codec is a low power optimized, high fidelity, 10-channel audio codec compatible with Intel's High Definition (HD) Audio Interface. The 92HD73E codec provides stereo 24-bit resolution with sample rates up to 192kHz. Dual SPDIF provides connectivity to consumer electronic equipment that is WLP compliant. The 92HD73E provides high quality, HD Audio capability to multimedia notebook and desktop PC applications.

Features

- **10 Channels (5 stereo DACs and 2 stereo ADCs) with 24-bit resolution**
  - Supports full-duplex 7.1 audio and simultaneous VoIP
- **Microsoft WLP premium logo compliant**
- **Optimized and flexible power management with pop/click mitigation**
- **SPDIF**
  - 48QFP package supports 2 independent S/PDIF Output converters for WLP compliant HDMI/SPDIF support
  - 40QFN package supports a single SPDIF Out
  - Both packages support SPDIF Input
- **HDA signaling**
  - 48QFP package support for 1.5V and 3.3V with runtime selection
  - 40QFN package supports 3.3V only
- **3 adjustable VREF Out pins for microphone bias**
- **High performance analog mixer**
- **9 stereo analog ports with presence detect capability**
- **Digital and Analog PC Beep to all outputs**
- **3 Integrated headphone amps**
- **Sample rates up to 192kHz**
- **Additional Features on 48QFP package**
  - Two-pin volume up/down control
  - Digital microphone input (mono, stereo, or quad array)
  - 4th adjustable VREF Out
  - Additional 5 GPIOs
- **Package Options**
  - 48-pin QFP RoHS package
  - 48-pin QFP RoHS package, Industrial Temp
  - 40-pin QFN RoHS package

Software Support

- **Intuitive IDT HD Sound graphical user interface that allows configurability and preference settings**
- **12 band fully parametric equalizer**
- **Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode "presets" tailored for specific acoustical environments and applications**
- **System-level effects automatically disabled when external audio connections made**
- **Dynamics Processing**
- **Enables improved voice articulation**
- **Compressor/limiter allows higher average volume level without resonances or damage to speakers.**
- **IDT Vista APO wrapper**
- **Enables multiple APOs to be used with the IDT Driver**
- **Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression**
- **Dynamic Stream Switching**
- **Improved multi-streaming user experience with less support calls**
- **Broad 3rd party branded software including Creative, Dolby, DTS, and SRS**

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. DESCRIPTION

1.1. Overview

The 92HD73E is a high fidelity, 10-channel audio codec compatible with the Intel High Definition (HD) Audio Interface. The 92HD73E codec provides high quality, HD Audio capability to desktop and multi-media notebook.

The 92HD73E is designed to meet or exceed premium logo requirements for Microsoft's Windows Logo Program (WLP) 3.09 and revisions 4 as indicated in WLP 3.09.

The 92HD73E provides stereo 24-bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. 92HD73E SPDIF outputs support sample rates of 192kHz, 176.4kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz. 92HD73E SPDIF input supports sample rates of 96kHz, 88.2kHz, 48kHz, and 44.1kHz. Additional sample rates are supported by the driver software.

The 92HD73E supports a wide range of desktop and consumer 8/10 channel configurations. The 2 independent SPDIF output interfaces provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. Simultaneous HDMI and SPDIF output is possible.

MIC inputs can be programmed with 0/10/20/30dB boost. For more advanced configurations, the 92HD73E has 8 General Purpose I/O (GPIO) in the 48QFP package.

The port presence detect capabilities allow the codecs to detect when audio devices are connected to the codec. Load impedance sensing helps identify attached peripherals for easy set-up and a better user experience. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The 92HD73E operates with a 3.3V digital supply and a 5V analog supply. It can also work with 1.5V and 3.3V HDA signaling; the correct signalling level is selected dynamically based on the power supply voltage on the DVDD-IO pin in the 48QFP package. The 40QFN package allows for 3.3V HDA signalling.

1.2. Orderable Part Numbers

92HD73E1X5PRGXB2X* 92HD73E1X5PRGXC1X	48QFP
92HD73E1T5PRGIC1X	48QFP, Industrial Temp
92HD73E2X5NDGXC1X	40QFN

* limited quantities of the B2 available, contact IDT sales.
Add an "8" to the end for tape and reel delivery.

1.3. Detailed Description

1.3.1. Port Functionality

Multi-function (Input / output) ports allow for the highest possible flexibility. 8 bi-directional ports (3 headphone capable) support a wide variety of consumer desktop and mobile system use models.

Port	Input	Output	Headphone	Mic Bias (Vref pin)	Input boost amp[1]	CD (pseudo differential)
A	Yes	Yes	Yes	Yes	Yes	
B	Yes	Yes	Yes	Yes	Yes	
C	Yes	Yes		Yes	Yes	
D	Yes	Yes	Yes		Yes	
E	Yes	Yes		Yes	Yes	
F	Yes	Yes			Yes	
G	Yes	Yes			Yes	
H	Yes	Yes			Yes	
CD (Port I)	Yes					Yes
SPDIF_OUT0		Yes				
SPDIF_OUT1		Yes				
SPDIF_IN	Yes					
DMIC0	Yes				Yes	
DMIC1	Yes				Yes	

Table 1. Port Functionality

Note[1]: 40dB boost requires using the IDT driver. When the 40dB mic boost feature is enabled, additional gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB MIC boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.

1.3.2. Port Characteristics

Universal (Bi-directional) jacks are supported on all ports except the CD input. Ports A, B, and D are designed to drive a set of 32 ohm (nominal) headphones or a 10K (nominal) load with on board shunt resistance as low as 20K ohms (typical - used to maintain coupling CAP bias.) Line Level outputs are intended to drive an external 10K speaker load (nominal) and an on board shunt resistor of 20K-47K (nominal). However, applications may support load impedances of 5K ohms and above. Input ports are 47K (nominal) at the pin.

DAC full scale output and intended full scale input levels are 1V rms. Line output ports and Headphone output ports on 92HD73E may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports are always on to prevent pops/clicks associated with charging and discharging output coupling capacitors. This maintains proper bias on output coupling caps even in D3 as long as AVDD is available. Unused ports should be left unconnected. When updating existing designs to use the 92HD73E, ensure that there are no conflicts between the output ports on 92HD73E and existing circuitry.

AFG Power State	Input Enable	Output Enable	Mute	Port Behavior
D0-D2	1	1	-	Not allowed. Port becomes input.
	1	0	-	Active - port enabled as input
	0	1	0	Active - port enabled as output
	0	1	1	Mute - port enabled as output but drives silence
	0	0	-	Inactive - Port keeps coupling caps charged (same as mute.)
D3		-	-	Inactive (lower power) - Port keeps output coupling caps charged but consumes less power.

Table 2. Analog I/O Port Behavior

1.3.3. Jack Detect

Plugs inserted to a jack on Ports A, B, C, & D are detected using SENSE_A. Plugs inserted to a jack on Ports E, F, G, and H are detected using SENSE_B. The following table summarizes the proper resistor tolerances for different analog supply voltages.

SENSE_C, is different from SENSE_A and SENSE_B. Because SENSE_C only determines the presence of a plug for the CD port (port I), SENSE_C is a simple digital input pin referenced to the analog supply. An internal pull-up resistor is provided. No external resistors are needed (jack switch shorts to ground when a plug is inserted.) If external components are added, or if the pin is driven by a logic gate, care should be taken to ensure that the pin voltage is above 70% of AVDD when no plug is in the jack and less than 30% AVDD when a plug is inserted.

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance SENSE_A (If port D used)	Resistor Tolerance SENSE_A (If port D is not used)	Resistor Tolerance SENSE_B (If port H used)	Resistor Tolerance SENSE_B (If port H is not used)
5V	1%	1%	1%	1%
4.75V	1%	1%	1%	1%
4V	0.50%	1%	0.50%	1%
3.3V	0.10%	1%	0.10%	1%

Table 3: SENSE Resistor Tolerance

See reference design for more information on Jack Detect implementation.

1.3.4. SPDIF Output

All SPDIF Outputs can operate at 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4KHz, and 192KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

A second independent SPDIF Output is provided as an option for WLP compliant HDMI and SPDIF outputs, available only of 48QFP package. Its function is identical to the primary SPDIF output.

Note: Peak to peak jitter is currently limited to less than 4.5nS (half of the internal master clock cycle) which does not meet the IEC-60958-3 0.05UI requirement at 192KHz.

The two SPDIF output converters can not be aligned in phase with the DACs. Even when attached to the same stream, the two SPDIF output converters may be misaligned with respect to their frame boundaries.

SPDIF Outputs on pins 48 and 40 are outlined in tables below. Pin 47 behavior table resides in the EAPD section

AFG Power State	RESET#	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
D0	De-Asserted (High)	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Enabled	Disabled	-	Active - Pin drives 0 (internal pull-down NA)
	De-Asserted (High)	Enabled	Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA)
	De-Asserted (High)	Enabled	Enabled	1-15	Active - Pin drives SPDIFOut0 data (internal pull-down NA)
D1-D2	De-Asserted (High)	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Enabled	-	-	Active - Pin drives 0 (internal pull-down NA)
D3	De-Asserted (High)	-	-	-	Hi-Z (internal pull-down enabled)

Table 4. SPDIF OUT 0 (Pin 48) Behavior

AFG Power State	RESET#	GPIO 3 Enable	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
D0-D3	De-Asserted (High)	Enabled	-	-	-	Active - Pin reflects GPIO7 configuration (internal pull-up enabled)
D0	De-Asserted (High)	Disabled	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Disabled	-	Active - Pin drives 0 (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Enabled	1-15	Active - Pin drives SPDIFOut1 data (internal pull-down enabled)

Table 5. SPDIF OUT 1 (Pin 40) Behavior

AFG Power State	RESET#	GPIO 3 Enable	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D1-D2	De-Asserted (High)	Disabled	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	-	-	Active - Pin drives 0 (internal pull-down NA)
D3	De-Asserted (High)	Disabled	-	-	-	Hi-Z (internal pull-down enabled)

Table 5. SPDIF OUT 1 (Pin 40) Behavior

1.3.5. SPDIF Input

SPDIF IN can operate at 44.1 KHz, 48 KHz, 88.2 KHz or 96 KHz, and implements internal Jack Sensing.

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs. Advanced features such as record-slot-select and SPDIF_IN routing to the DAC allow for simultaneous record and play.

1.3.6. Analog Mixer

An analog mixer is available on the 92HD73E. The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input. A master volume follows mixing and provides gain from -46.5dB to 0dB in 1.5dB steps.

The following inputs are available:

- CD
- Analog PC_Beep
- Inport0_Mux
- Inport1_Mux
- Inport2_Mux
- Inport3_mux

1.3.7. Input Multiplexers

92HD73E implements 4 port input multiplexers. These multiplexers allow a preselection of one of four possible inputs:

Inport0_Mux	Inport1_Mux	Inport2_Mux	Inport3_mux
Port A	Port A	Port B	DAC 0
Port B	Port E	Port C	DAC 1
Port D	Port G	Port G	DAC 2
Port F	Port H	Port H	DAC 3

Table 6. Input Multiplexers

1.3.8. ADC Multiplexers

92HD73E implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function (0 to +22.5dB gain in 1.5dB steps) as an output amp and allow a preselection of one of 12 possible inputs:

- DMIC 0 (not on 40QFN)
- DMIC 1 (not on 40QFN)
- Mixer output
- CD input
- Ports A - H

1.3.9. Power Management

The HD Audio specification defines power states, power state widgets, and power state verbs. Power management is implemented at several levels. The Audio Function Group (AFG) and all converter widgets support the power state verb F05/705 (as well as the pin widget associated with pin 47.) Converter widgets are active in D0 and inactive in D1-D3.

The following table describes what functionality is active in each power state supported by the AFG.

Function	D0	D1[1]	D2	D3	vendor specific
SPDIF Outputs	On	Off	Off	Off	-
SPDIF Inputs	On	Off	Off	Off	-
Digital Microphone inputs	On	Off	Off	Off	-
DAC	On	Off	Off	Off	-
D2S	On	Off	Off	Off	-
ADC	On	Off	Off	Off	-
ADC Volume Control	On	Off	Off	Off	-
Ref ADC	On	Off	Off	Off	-
Analog Clocks	On	Off	Off	Off	-
GPIO pins	On	On	On	On	-
VrefOut Pins	On	On	Off	Off	-
Input Boost	On	On	Off	Off	-
Analog mixer	On	On	Off	Off	-
Mixer Volumes	On	On	Off	Off	
Analog PC_Beep	On	On	Off	Off	
Digital PC_Beep	On	On	On	On	-
Lo Amp	On	On	On	Low Drive[2]	Programmable
HP Amps	On	On	On	Low Drive[2]	Programmable
VAG amp	On	On	On	Low Drive[3]	Programmable
Port Sense	On	On	On	On[4]	Programmable
Reference Bias generator	On	On	On	On	Programmable[5]
Reference Bandgap core	On	On	On	On	Programmable[5]
HD Audio-Link	On	On	On	On[6]	-

Table 7. Function state vs. AFG power state

1.No DAC or ADC streams are active. Analog mixing and loop thru are supported.
2.VAG is kept active when ports are disabled or in D2/D3. Ports may be powered down using vendor specific verbs.

3.VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
4. BITCLK must be active and both AVDD and DVDD must be available for Port Sense to operate.
5.Vendor specific bit for Ref Top controls VAG generator, Bandgap Reference, and Reference bias generator. Place part into D3 and power down all ports (using vendor specific verbs) before powering down Ref Top.
6.Obviously not active if BITCLK is not running (Controller in D3).

1.3.9.1. AFG D0

The AFG D0 state is the active state for the device. All functions are active if their power state (if they support power management at their node level) has been set to D0.

1.3.9.2. AFG D1

D1 is a lower power mode where all converter widgets are disabled. Analog mixer and port functions are active.

1.3.9.3. AFG D2

The D2 state further reduces power by disabling the mixer and port functions. The port amplifiers and internal references remain active to keep port coupling caps charged and the system ready for a quick resume to either the D1 or D0 state.

1.3.9.4. AFG D3

The D3-default state is available for HD Audio compliance. All converters are shut down. Port amplifiers and references are active but in a low power state to prevent pops. Resume times may be longer than those from D2, but still very fast to meet Intel low power goals.

The traditional use for D3 was as a transitional state before power was removed (D3 cold) before the system entered into standby, hibernate, or shut-down. To conserve power, Intel now promotes using D3 whenever there are no active streams or other activity that requires the part to consume full power. The system remains in S0 during this time. When a stream request or user activity requires the CODEC to become active, the driver will immediately transition the CODEC from D3 to D0. To enable this use model, the CODEC must resume within 10mS and not pop.

The default power state for the Audio Function Group after reset is D3-default

1.3.9.5. AFG D3 and vendor specific verbs

The programmable values, exposed via vendor-specific settings, are under the IDT Device Driver control for further power reduction.

1.3.10. Low-voltage HDA Signaling

The 92HD73E is compatible with either 1.5V or 3.3V HDA bus signaling; the voltage selection is done dynamically based on the input voltage of DVDD_IO on the 48QFP package. The 40QFN allows for 3.3V only.

When in 1.5V mode, the 92HD73E can correctly decode BITCLK, SYNC, RESET# and SDO as they operate at 1.5V; additionally it will drive SDI and SDO at 1.5V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

1.3.11. Multi-channel capture

The capability to assign multiple ADC “Input Converters” to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported and is done by assigning unique non zero Stream IDs to each converter. All cap-

ture devices (ADCs 0 and 1) may be used to create a multi-channel input stream. There are no restrictions regarding digital microphones. However, the SPDIF input can not be used with an ADC to create a 4-channel stream. SPDIF_In only supports stereo capture.

The ADC Converters can be associated with a single stream as long as the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the “Multi-Converter Stream Critical Entries” table.

An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2&3 is shown below. A 4 Channel stream can be created by assigning the same non-zero stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NmbrChan = 0011”.

ADC1 CnvtrID	(NID = 0x08)	
	[3:0]	Ch = 2
ADC0 CnvtrID	(NID = 0x07)	
	[3:0]	Ch = 0

Table 8: Example channel mapping

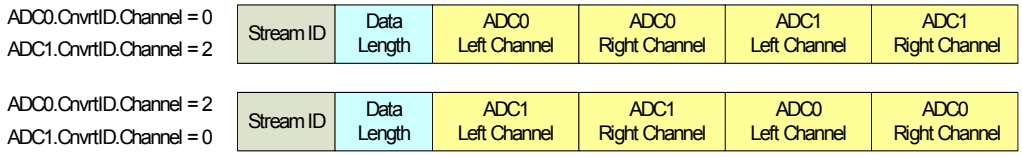

Figure 1. Multi-channel capture

The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

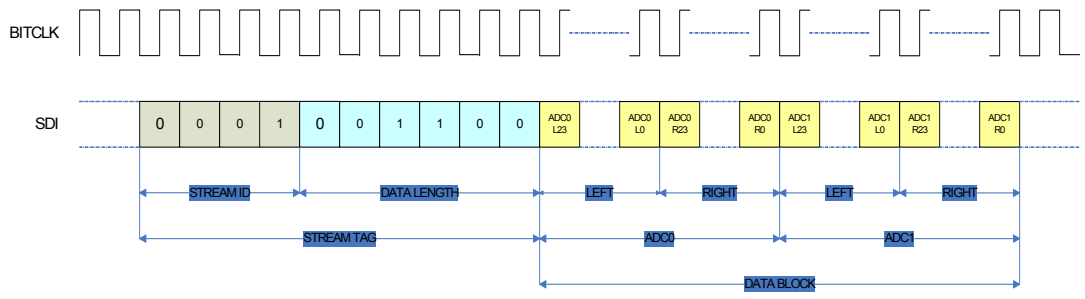

Figure 2. Multi-channel timing diagram

ADC[1:0] Cnvtr	Bit Number	Sub Field Name	Description
	[15]	StrmType	Stream Type (TYPE): 0: PCM 1: Non-PCM (not supported)
	[14]	FrmtSmplRate	Sample Base Rate 0= 48kHz 1=44.1KHz
	[13:11]	SmplRateMultp	Sample Base Rate Multiple 000=48kHz/44.1kHz or less 001= x2 010= x3 (not supported) 011= x4 100-111= Reserved
	[10:8]	SmplRateDiv	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 (not supported) 010= Divide by 3 (not supported) 011= Divide by 4 (not supported) 100= Divide by 5 (not supported) 101= Divide by 6 (not supported) 110= Divide by 7 (not supported) 111= Divide by 8 (not supported)
	[6:4]	BitsPerSmpl	Bits per Sample 000= 8 bits (not supported) 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
	[3:0]	NmbrChan	Number of Channels Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link. 0000=1 channel (not supported) 0001 = 2 channels … 1111= 16 channels.
ADC[1:0] CnvtrID	**Bit Number**	**Sub Field Name**	**Description**
	[7:4]	Strm	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
	[3:0]	Ch	Integer representing lowest channel used by converter. 0 and 2 are valid Entries If assigned to the same stream, one ADC must be assigned a value of 0 and the other ADC assigned a value of 2.

Table 9: Multi-Converter Stream Critical Entries.

1.3.12. EAPD

The EAPD pin also supports SPDIF_In and GPIO functions. The pin defaults to EAPD after power on reset and will remain in EAPD mode until either GPIO is enabled for pin 47 or the port I/O is enabled to support SPDIF. Although named External Amplifier Power Down (EAPD) by the HD Audio specification, this pin operates as an external amplifier power up signal. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up, and a 0 causes it to power down. When the EAPD value = 1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value may remain 1. The default state of this pin is 0 (driving low) and a Pull-down prevents the line from floating high when the part is in reset.

AFG Power State	RESET#	GPIO Enable	Input Enable	EAPD Power State	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
D0	De-Asserted (High)	Enabled	-	-	Active - Pin reflects GPIO0 configuration (internal pull-up enabled)
	De-Asserted (High)	Disabled	Enabled	-	Active - Pin is SPDIF_In
	De-Asserted (High)	Disabled	Disabled	D0-D1	Active - Pin drives the value of the EAPD bit (internal pull-down enabled)
	De-Asserted (High)	Disabled	Disabled	D2-D3	Hi-Z (internal pull-down enabled)
D1	De-Asserted (High)	Disabled	Enabled	-	Inactive - Pin configured as input, but SPDIF_In idle.
	De-Asserted (High)	Disabled	Disabled	D0-D1	Active - Pin drives the value of the EAPD bit (internal pull-down enabled)
	De-Asserted (High)	Disabled	Disabled	D2-D3	Hi-Z (internal pull-down enabled)
D2	De-Asserted (High)	Disabled	-	D0-D3	Hi-Z (internal pull-down enabled)
D3	De-Asserted (High)	Disabled	-	D0-D3	Hi-Z (internal pull-down enabled)

Table 10. EAPD Behavior

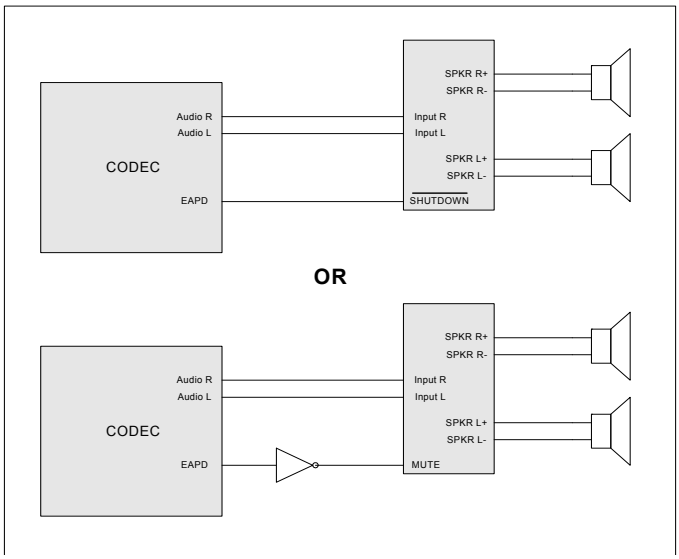

Figure 3. EAPD

1.3.13. Digital Microphone Support (on 48QFP package)

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0, DMIC1, and DMIC_CLK 3-pin interface. The DMIC0 and DMIC1 signals are inputs that carry individual channels of digital Mic data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the 24Mhz internal clock. The default frequency is 2.352Mhz.

The two DMIC data inputs are reported as two stereo input pin widgets that incorporate a boost amplifier. The pin widgets are shown connected to the ADCs through the same multiplexors as the analog ports. Although the internal implementation is different between the analog ports and the digital microphones, the functionality is the same. In most cases, the default values for the DMIC clock rate and data sample phase will be appropriate and an audio driver will be able to configure and use the digital microphones exactly like an analog microphone.

92HD73E supports the following digital microphone configurations:

Digital Mics	Data Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones
1	Single Edge	0, or 1	Available on either DMIC_0 or DMIC_1 Both ADC Channels produce data, may be in phase or out by 1/2 DMIC_CLK period depending upon external configuration and timing
2	Double Edge on either DMIC_0 or 1 OR Single Edge on DMIC_0 and 1	0, or 1	Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. If both DMIC_0 and DMIC_1 are used to support 2 digital microphones, 2 separate ADC units will be used, however, this configuration is not recommended since it consumes two stereo ADC resources.
3	Double Edge on one DMIC pin and Single Edge on the second DMIC pin.	0, or 1	Requires both DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration
4	Double Edge	0, or 1	Connected to DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration

Table 11. Valid Digital Mic Configurations

Power State	DMIC Widget Enabled	DMIC_CLK Output	DMIC_0,1	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D1-D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down

Table 12. DMIC_CLK and DMIC_0,1 Operation During Power States

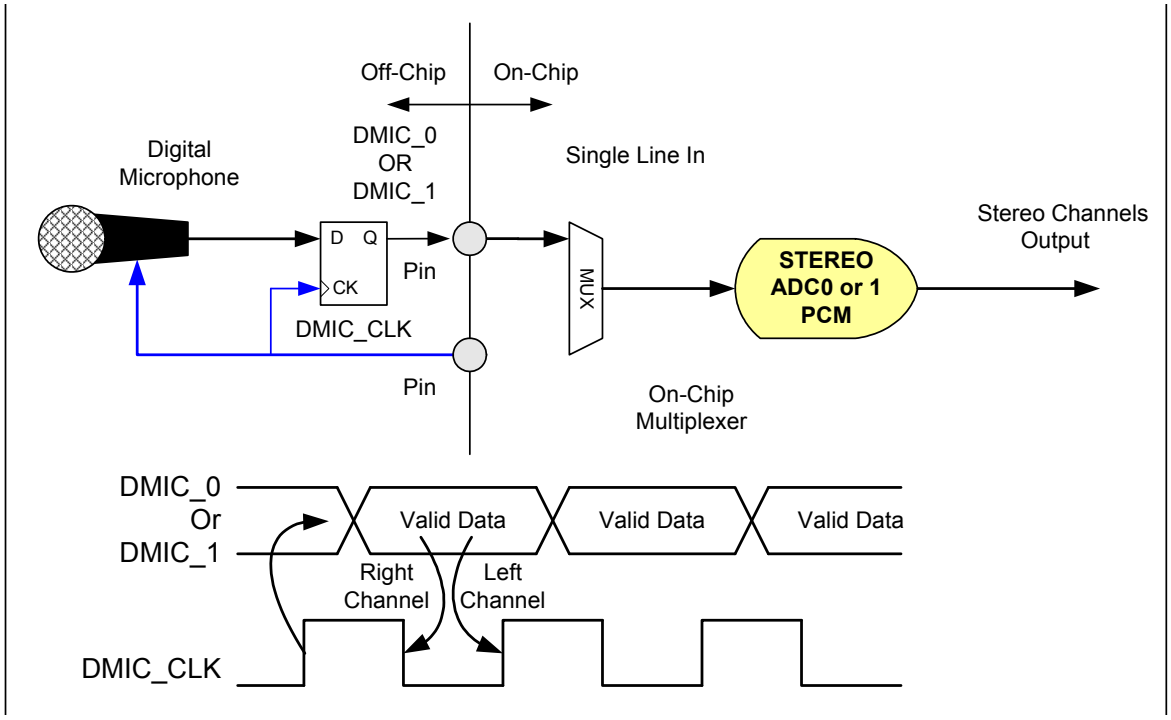

Figure 4: Mono Digital Microphone (data is ported to both left and right channels)

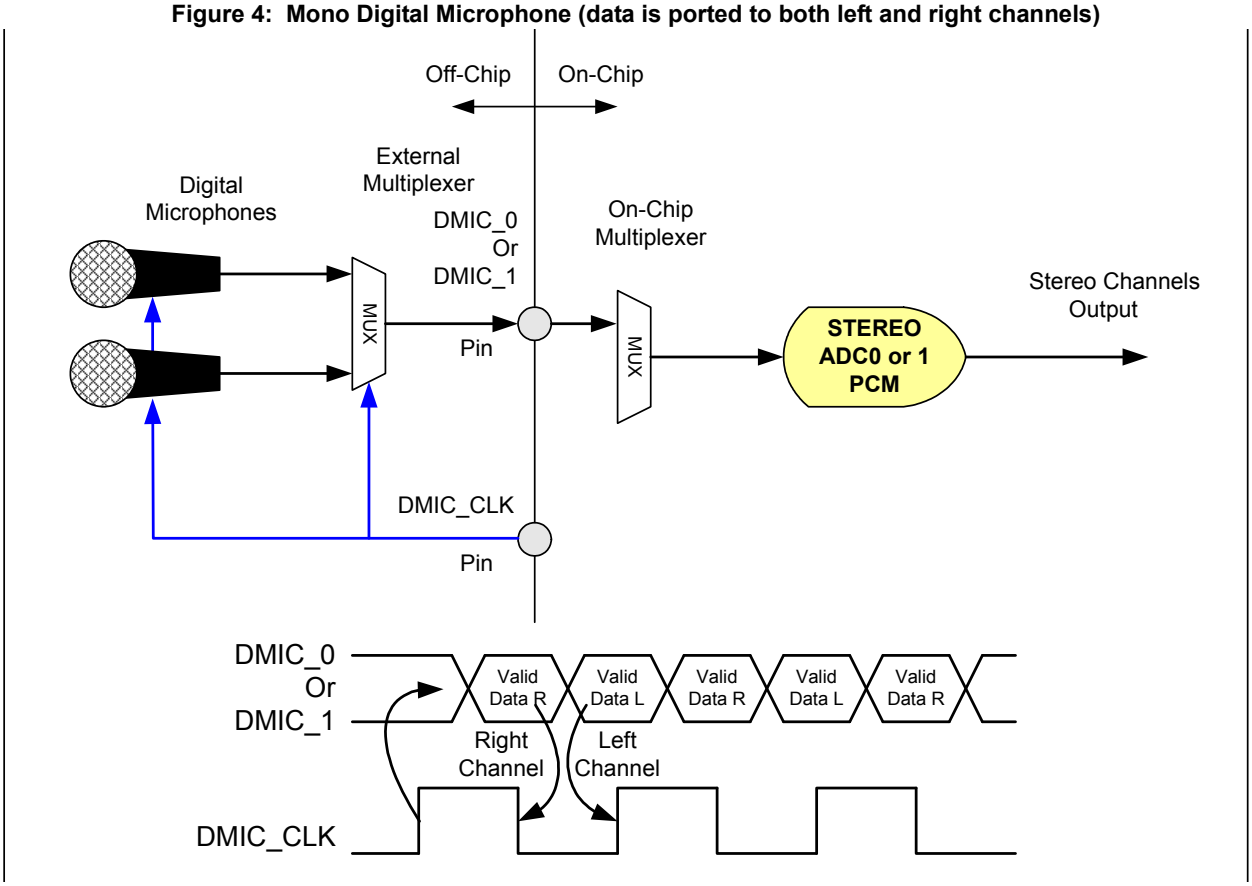

Figure 5: Stereo Digital Microphone Configuration

Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

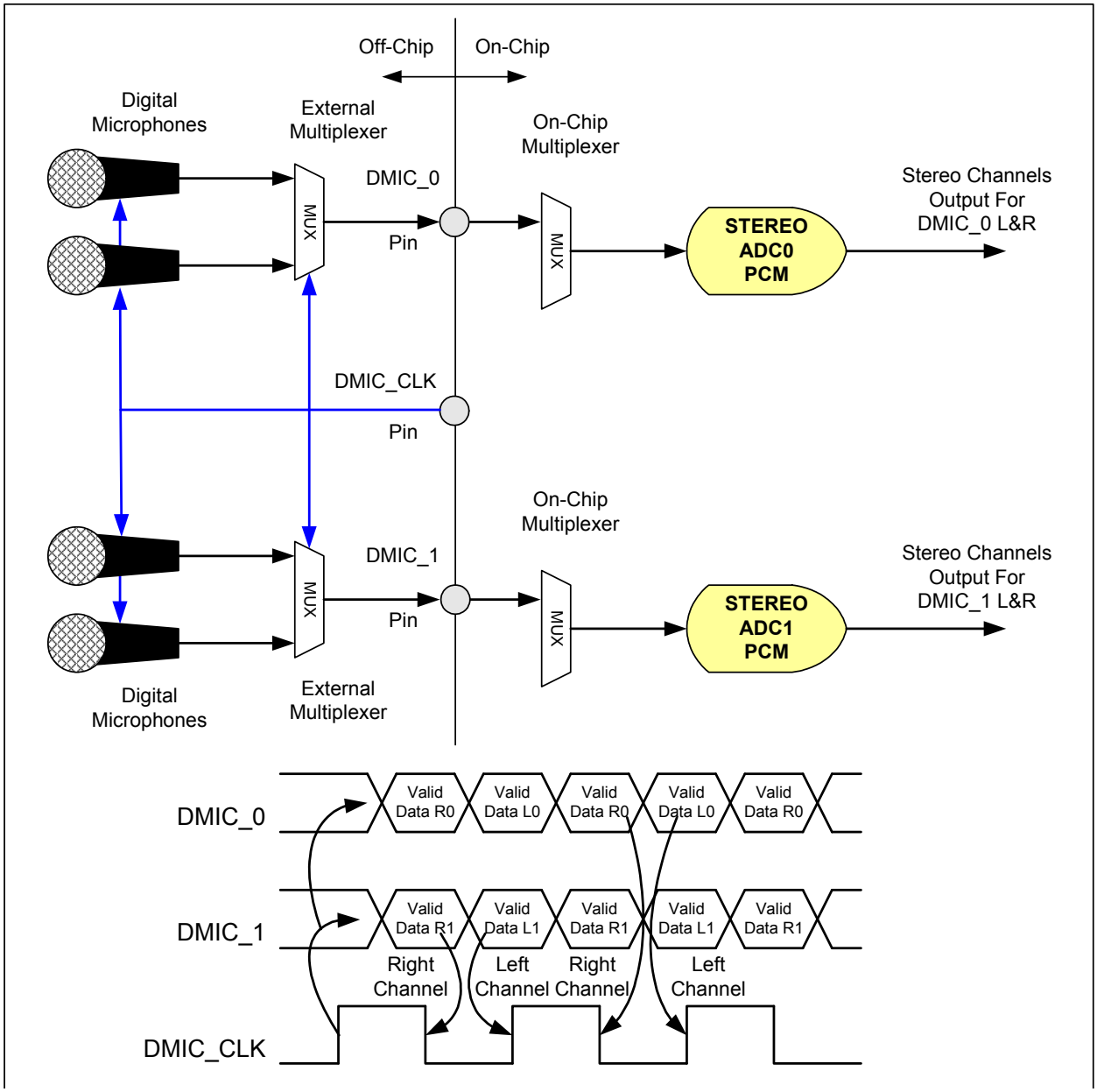

Figure 6: Quad Digital Microphone Configuration

Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

1.3.14. PC-Beep

92HD73E supports both analog and digital PC_Beep functions.

1.3.14.1. Analog PC-Beep

92HD73E does not support automatic routing of the PC_Beep pin to all outputs when the link is in reset. Analog PC-Beep may be supported during Link Reset if the mixer is manually configured for pass-thru. Otherwise, Reset# must be high and Bit_Clk active.

The default values for the vendor specific verb (7EE/FEE in AFG) associated with Analog PC-Beep are:

- Enable = 0h (Analog PC-Beep disabled - mute)
- volume = 3h (0dB)

Analog PC-Beep is supported in D3, but may be attenuated or distorted depending on the load-impedance on the port. Line outputs can drive 10K ohm loads in D3 at 1Vrms, but will be current limited when driving lower impedance loads. Enabling or disabling analog PC-Beep may cause a click or pop sound.

1.3.14.2. Digital PC-Beep

This block uses an 8-bit divider value to generate the PC beep from the 48kHz Azalia sync pulse. The digital PC_Beep block generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). Other audio sources are disabled when digital PC_Beep is active.

It should be noted that digital PC Beep is disabled if the divider = 00h.

1.3.15. Headphone Drivers

This product implements a +3dBV output option on headphone capable ports. (HP output and line output levels are defined as 1Vrms at this time with an option to enable +3dBV FSOV using a vendor specific verb.) The Microsoft Windows Logo Program allows up to the equivalent of 100ohms in series. However, an output level of +3dBV at the pin is required to support 300mV at the jack with a 32ohm load and 1V with a 320 ohm load. Microsoft allows device and system manufactures to limit output voltages to address EU safety requirements. (WLP 3.09 - please refer to the latest Windows Logo Program requirements from Microsoft.) 92HD73E, however, requires external components (series resistors) to limit the output voltage to 150mV with a 32 ohm load or secure software limiting by restricting DAC and mixer gain ranges.

Although 3 Headphone amplifiers are present, only two may be used simultaneously.

Performance will degrade when driving more than one set of headphones. Only one set of headphones (32 ohm nominal) may be connected to a headphone capable port.

1.3.16. GPIO

1.3.16.1. GPIO Pin mapping and shared functions.

GPIO #	Supply	SPDIF In	SPDIF Out	GPI/O	GPI	GPO	VrefOut	DMIC	VOL	Pull Up	Pull Down
0	DVDD	YES		YES						50K (GPIO)	50K[1] (SPDIF/EAPD)
1	DVDD			YES				CLK	YES	50K (GPIO/VOL)	50K (DMIC)
2	DVDD			YES				IN	YES	50K (GPIO/VOL)	50K (DMIC)
3	AVDD		YES	YES						50K (GPIO)	50K[1] (SPDIF)
4	AVDD			YES			YES				
5	AVDD			YES				IN		50K[1]	50K (DMIC)
6	AVDD			YES			YES				
7	AVDD			YES			YES				

Table 13. GPIO Pin mapping

1.Default condition.

1.3.16.2. Volume/Digital Microphone/GPIO Selection

There are 3 functions available on pins 2 and 4. To determine which function is actually enabled on the 2 pins, the order of precedence is followed:

1. If the GPIOs are enabled, they override both Volume Control and Digital Mics
2. If the GPIOs are not enabled through the AFG, then at reset, the Volume control is enabled with the weak pull-up.
3. If BIOS or other software application enables either Digital Microphones inputs through the Configuration Default Register, the Volume is disconnected and the pull-ups are disconnected with the weak pull-downs enabled.

1.3.16.3. VRefOut/GPIO Selection

Two functions are available on pins 29, 31, and 37. To determine which function is actually enabled, the order of precedence is followed:

1. If the GPIOx function is enabled, it overrides VRefOut-X
2. If the GPIO function is not enabled through the AFG, then the VrefOut function is enabled and in its default state.
3. If using a VrefOut pin as GPIO, make sure to incorporate a 10K ohm external pull-up to AVDD to prevent the pin from floating in GPI mode and to allow proper operation in open-drain GPO mode.

1.3.17. External Volume Control (on 48QFP package)

92HD73E incorporates a 2-pin volume control interface. Volume up, down, and mute functions are easily implemented using 2 push-button switches. The CODEC provides internal pull-up resistors simplifying external CODEC circuitry. Also, repeat and direct modes of operation add flexibility to the

interface. The typical usage model is for front panel master volume buttons on an entertainment PC, or case mounted hardware volume control for mobile platforms.

1.3.17.1. Theory of Operation

The codec monitors the volume up/down inputs for a change of state from high to low, and waits for the inputs to settle. If the inputs have not settled by the end of the de-bounce period, then the value at the end of the period is used. A 0 (low voltage) on the Down pin will decrement the volume register, while a 0 on the Up pin will increment the volume register. If both inputs are 0 at the same time, then the volume register will be set to its lowest value (mute). Pressing Up, Down, or both buttons at the same time when the volume control interface is in mute mode, will cause the part to un-mute.

The de-bounce / repeat rate is selectable from 2.5Hz to 20Hz in 2.5Hz increments using the Volume Knob VCSR0 verb (FE0) Rate bits (bits 2:0). This value is used for both de-bounce and repeat rates. The de-bounce period is the time that the CODEC waits for the inputs to settle, and the repeat rate is the rate at which the CODEC will increment/decrement the volume if a volume button is pushed and held. When a falling edge is detected on either one of the volume control pins, the codec will wait for (1/Rate) seconds for the input to settle. If the Continuous bit is set in the Volume Knob VCSR0 verb (bit 3), then the codec will wait for the de-bounce period to expire then repeatedly increment or decrement the volume register at the rate specified in the Rate bits until the button is released.

1.3.17.2. Modes of Operation

- DIRECT MODE

In Direct mode, the Volume Knob widget directly controls the volume of all of the DACs in the part. The volume in the Volume Knob widget acts as the master volume and limits the maximum volume for each of the DAC amplifiers. The amp gain for each of the DACs can also be adjusted using the DAC amplifiers. However, the actual gain for an individual DAC will be the sum of the Volume Knob volume and the DAC amplifier volume. For example, if the DAC amplifier gain is set to 0x7F (0dB) and the Volume Knob volume is set to 0x3F (-48dB) the resulting gain would be -48dB. If the combination of gains is less than -95.25dB (the equivalent to a value of 0x0 for the DAC or Volume Knob volume settings) then the actual gain will be -95.25dB. For example, if the Volume Knob is set to 0x3F (-48dB) and the DAC amplifier volume is set to 0x1F (-72dB) then the DAC volume will be set to -95.25dB.

Direct mode is enabled by setting bit 7 in the Volume Knob Cntrl verb (F0F). The volume is reflected in the Volume Knob Cntrl bits 6:0 and the step size is 0.75dB. In direct mode, software can read or write the volume in the Volume Knob widget.

- INDIRECT MODE

In indirect mode, the Volume Knob widget does not directly control the DAC amplifier gains. An event on the volume Up/Down pins will increment/decrement the value in the Volume Knob Cntrl verb (F0F) volume bits (bits 6:0) just as in Direct mode. However, instead of adjusting the DAC amplifier gain, an unsolicited response is generated (if enabled) and the control software must read the volume in the Volume Knob widget and take appropriate action. Indirect mode is particularly useful when it is undesirable to control all of the DAC amplifier volumes at the same time, or when implementing ADC volume control.

In indirect mode, there are only 128 volume levels in the Volume Knob Cntrl volume bits, the value will not go beyond the lower and upper limits (0x0 or 0x7F), and an unsolicited response will be gen-

erated if an input event tries to go beyond these limits. Therefore, it is the responsibility of the controlling software to monitor the volume in the Volume Knob Widget and take appropriate action.

Indirect mode is enabled by clearing bit 7 in the Volume Knob Cntrl verb (F0F). The volume is reflected in the Volume Knob Cntrl bits 6:0 and the step size is 0.75dB. In direct mode, software can read or write the volume in the Volume Knob widget.

1.3.17.3. Hardware Implementation

The Volume Knob interface is comprised of two input pins, CODEC pins 2 and 4. Both pins have internal pull-up resistors, so only two push button switches are required for most implementations. Typically, a series resistor and shunt capacitor are used to help reduce noise and prevent damage from ESD and other potential faults. An example circuit is shown below in below.

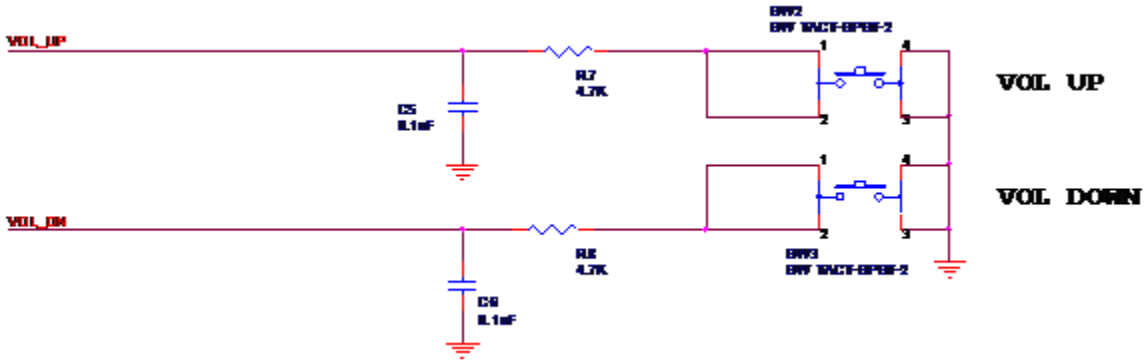

Figure 7: External Volume Control Circuit

2. CHARACTERISTICS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 92HD73E. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0 ^{O}C to +70 ^{O}C -40 ^{O}C to +85^{O}C (INDUSTRIAL TEMP for 92HD73E1T only)
Storage temperature		-55 ^{O}C to +125 ^{O}C
Soldering temperature		Soldering temperature information for all available in the package section of this datasheet.

Table 14. Electrical Specification: Maximum Ratings

2.1.2. Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-QFP)			+90	°C
	T_{case} (40-QFN)			+95	°C
	T_{case} Industrial			+110	°C

Table 15. Recommended Operating Conditions

ESD: The 92HD73E is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the 92HD73E implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.2. 92HD73E Analog Performance Characteristics

(Tambient = 25 ºC, AVdd = Supply ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 20Hz to 20KHz swept sinusoidal input; Sample Frequency = 48 kHz; 0 dB = 1 VRMS, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Digital to Analog Converters						
Resolution		All		24		Bits
Dynamic Range[1]: PCM to All Analog Outputs	-60dB FS signal level	5V	90	94		dB
SNR[2] - DAC to All Line-Out Ports	Analog Mixer Disabled, PCM data	5V	90	97		dB
THD+N[3] - DAC to All Line-Out Ports	Analog Mixer Disabled, 0dB FS Signal, PCM data	5V	80	83		dBr
THD+N[3] - DAC to All Line-Out Ports	Analog Mixer Disabled,-1dB FS Signal, PCM data	5V	80	83		dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Disabled, 10KΩ load, PCM data	5V	90	97		dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, 0dB FS Signal, 10KΩ load, PCM data	5V	80	83		dBr
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, -1dB FS Signal, 10KΩ load, PCM data	5V	80	83		dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Disabled, 32Ω load, PCM data	5V	90	97		dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, 0dB FS Signal, 32Ω load, PCM data	5V	65	70		dBr
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, -1dB FS Signal, 32Ω load, PCM data	5V	65	70		dBr
Any Analog Input (ADC) to DAC Crosstalk	10KHz Signal Frequency. 0dBV signal applied to ADC, DACs idle, ports enabled as output.	All	-	-80	-	dB
Any Analog Input (ADC) to DAC Crosstalk	1KHz Signal Frequency see above	All	-	-85	-	dB
DAC L/R crosstalk	DAC to LO or HP 20-15KHz into 10KΩ load	All	65	70		dB
DAC L/R crosstalk	DAC to HP 20-15KHz into 32Ω load	All	65	70		dB
Gain Error	Analog Mixer Disabled	All			0.5	dB
Interchannel Gain Mismatch	Analog Mixer Disabled	All			0.5	dB
D/A Digital Filter Pass Band[4]		All	20	-	21,000	Hz
D/A Digital Filter Transition Band		All	21,000	-	31,000	Hz
D/A Digital Filter Stop Band		All	31,000	-	-	Hz
D/A Digital Filter Stop Band Rejection[5]		All	-100	-	-	dB
D/A Out-of-Band Rejection[6]		All	-55	-	-	dB
Group Delay (48KHz sample rate)		All	-	-	1	ms

Table 16. 92HD73E Analog Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Attenuation, Gain Step Size DIGITAL		All	-	0.75	-	dB
DAC Offset Voltage		All	-	10	20	mV
Deviation from Linear Phase		All	-	1	10	deg.
Analog Outputs						
Full Scale All Line-Outs	DAC PCM Data	5V	1.00	1.07	-	Vrms
Full Scale All Line-Outs	DAC PCM Data	5V	2.83	3.03	-	Vp-p
All Headphone Capable Outputs	32Ω load	5V	40	60	-	mW (peak)
Amplifier output impedance	Line Outputs Headphone Outputs	All		150 0.1		Ohms
Analog inputs						
Full Scale Input Voltage	0dB Boost @4.75V (input voltage required for 0dB FS output)	5V	1.05	1.10	-	Vrms
All Analog Inputs with boost	10dB Boost	5V	0.31	-	-	Vrms
All Analog Inputs with boost	20dB Boost	5V	0.10	-	-	Vrms
All Analog Inputs with boost	30dB Boost	5V	0.03	-	-	Vrms
Input Impedance		All	-	50	-	KΩ
Input Capacitance		All	-	15	-	pF
Analog Mixer						
SNR[2] - All Line-Inputs or DACs to A, B, and D headphone capable outputs	Analog Mixer Enabled, 10KΩ load. DAC playing silence, line inputs driven by ATE. Gain set to 0dB	5V	85	90		dB
THD+N[3] - All Line-Inputs or DACs to A, B, and D headphone capable outputs	Analog Mixer Enabled, 0dB FS Signal, 10KΩ load	5V	70	75		dBr
SNR[2] - All Line-Inputs or DACs to A, B, and D headphone capable outputs	Analog Mixer Enabled, 32Ω load. DAC playing silence, Line inputs driven by ATE.	5V	85	90		dB
THD+N[3] - All Line-Inputs or DACs to A, B, and D headphone capable outputs	Analog Mixer Enabled, 0dB FS Signal, 32Ω load	5V	60	70		dBr
SNR[2] - DAC to All Line-Out Ports (C, E, F, G, and H)	Analog Mixer Enabled, DACs playing silence, line inputs driven by ATE. Gain set to 0dB	5V	85	90		dB
THD+N[3] - DAC to All Line-Out Ports (C, E, F, G, and H)	Analog Mixer Enabled, 0dB FS Signal, , 10KΩ load	5V	70	75		dBr
Attenuation, Gain Step Size ANALOG		All	-	1.5	-	dB
Gain Drift[7]		All	-	100	-	ppm/ºC
Analog to Digital Converter						
Resolution		All		24		Bits
Dynamic Range[1], All Analog Inputs to A/D	High Pass Filer Enabled, -60dB FS, No boost	5V	86	90		dB
SNR[2]- All Analog Inputs to A/D	High Pass Filter enabled	5V	86	90		dB

Table 16. 92HD73E Analog Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
THD+N[3] All Analog Inputs to A/D	High Pass Filter enabled, -1dB FS signal level	5V	75	85		dBr
THD+N[3] All Analog Inputs to A/D	High Pass Filter enabled, -3dB FS signal level	5V	75	85		dBr
Analog Frequency Response[8]		All	10	-	30,000	Hz
A/D Digital Filter Pass Band[4]		All	20	-	21,000	Hz
A/D Digital Filter Transition Band		All	21,000	-	31,000	Hz
A/D Digital Filter Stop Band		All	31,000	-	-	Hz
A/D Digital Filter Stop Band Rejection[5]		All	-100	-90	-	dB
Group Delay	48 KHz sample rate	All	-	-	1	ms
Any unselected analog Input to ADC Crosstalk	10KHz Signal Frequency	All	-65	-80	-	dB
Any unselected analog Input to ADC Crosstalk	1KHz Signal Frequency	All	-65	-85	-	dB
ADC L/R crosstalk	Any selected input to ADC 20-15Khz	All	-65			dB
DAC to ADC crosstalk	DAC output 0dBFS. All outputs loaded. Input to ADC open. 20-15Khz	All	-55			dB
Spurious Tone Rejection[9]		All	-	-100	-	dB
Attenuation, Gain Step Size (analog)		All	-	1.5	-	dB
Gain Drift		All	-	100	-	ppm/ºC
Interchannel Gain Mismatch ADC		All	-	-	0.5	dB
Power Supply						
Power Supply Rejection Ratio	10kHz	All	-	-60	-	dB
Power Supply Rejection Ratio	1kHz	All	-	-70	-	dB
D0 (7.1 Playback)[10]	Single 7.1 stream. No ADC or SPDIF					
Didd	3.3V			68		mA
Aidd	5.0V			50		mA
D0 (Stereo Playback)[10]	Single 2 channel stream. No ADC or SPDIF					
Didd	3.3V			38		mA
Aidd	5.0V			37		mA
D0 (idle)[10]	All converters enabled but no streams playing					
Didd	3.3V			55		mA
Aidd	5.0V			72		mA
D1[10]	Analog mixer active, all converters and ports off					
D1 Didd	3.3V			14		mA
D1 Aidd	5.0V			35		mA
D2[10]	All converters, ports and mixer off					

Table 16. 92HD73E Analog Performance Characteristics