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DATASHEET

SINGLE CHIP PC AUDIO SYSTEM

CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

92HD99

Description

The 92HD99 single-chip audio system is a low power optimized, high fidelity, 4-channel audio codec with stereo integrated speaker amplifier, capless headphone amplifier, and low drop out voltage regulator.

The high integration of the 92HD99 enables the smallest PCB footprint with the lowest system BOM count and cost. 92HD99 provides high quality HD Audio capability to notebook and business desktop PC applications.

Features

- **4 Channels (2 stereo DACs and 2 stereo ADCs) with 24-bit resolution**
  - Supports full-duplex stereo audio and simultaneous VoIP
- **2W Class-D stereo BTL speaker amplifier @ 4 ohms and 5V**
  - 10 band hardware parametric equalizer
  - Hardware compressor limiter
  - Dedicated BTL high pass filter for speaker protection
- **Capless headphone amplifier with charge pump/LDO**
- **Combo Jack Support allowing for dual-function headphone and headset detection**
- **Full HDA015-B low power support**
- **Internal digital core LDO voltage regulator**
- **Microsoft WLP desktop premium logo compliant**
- **Support for 1.5V and 3.3V HDA signaling**
- **Digital microphone inputs (mono or stereo mics)**
- **Microphone Mute Input (on WB revisions and beyond)**
- **High performance analog mixer**
- **2 adjustable VREF Out pins for analog microphone bias**
- **5 analog ports with port presence detect (4 single ended, 1 BTL)**
- **Analog and digital PC Beep support**
- **AUX Audio mode for playback**
- **40-pad QFN RoHS packages in Commercial and Industrial Temperature Ranges**

Full HDA015-B low power support

- Audio inactivity transitions codec from D0 to D3 low power mode
- Resume from D3 to D0 with audio activity in < 10 msec
- D3 to D0 transition with < -65dB pop/click
- Port presence detect in D3 with or without bit clock
- PC beep wake up in D3
- Additional vendor specific modes for even lower power

Software Support

- Intuitive IDT HD Sound graphical user interface that allows configurability and preference settings
- 12 band fully parametric equalizer
  - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
  - System-level effects automatically disabled when external audio connections made
- Dynamics Processing
  - Enables improved voice articulation
  - Compressor/limiter allows higher average volume level without resonances or damage to speakers.
- IDT Vista APO wrapper
  - Enables multiple APOs to be used with the IDT Driver
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression
- Dynamic Stream Switching
  - Improved multi-streaming user experience with less support calls
- Broad 3rd party branded software including Creative, Dolby, DTS, and SRS

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1. DESCRIPTION

1.1. Overview

The 92HD99 audio CODEC provides stereo 24- bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC.

An integrated BTL stereo amplifier is ideal for driving 4ohm or 8ohm integrated speakers in mobile and ultra-mobile computers. For desktop computers or mobile computers using only one speaker, the BTL output stage may be configured to support a single mono speaker.

Port presence detect capabilities allow the CODEC to detect when audio devices are connected to the CODEC. The fully parametric Internal EQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The 92HD99 audio CODEC operates with a 3.3V digital supply and a 5V (4.75V allowed when using external voltage regulator) analog supply. It allows for 1.5V and 3.3V HDA signaling; the correct signalling level is selected dynamically based on the power supply voltage on the DVDD-IO pin.

The 92HD99 audio CODEC is offered in a 40-pin QFN Environmental (ROHS) package.

1.2. Orderable Part Numbers

92HD99B1X5NDGXyyX	HDA 3.3V, Aux mode
92HD99B2X5NDGXyyX	HDA 3.3V, No Aux mode
92HD99B3X5NDGXyyX	HDA 1.5V, Aux mode
92HD99B4X5NDGXyyX	HDA 1.5V, No Aux mode
92HD99B1X5NDGIyyX	HDA 3.3V, Aux mode. Industrial Temp
92HD99B2X5NDGIyyX	HDA 3.3V, No Aux mode. Industrial Temp
92HD99B3X5NDGIyyX	HDA 1.5V, Aux mode. Industrial Temp
92HD99B4X5NDGIyyX	HDA 1.5V, No Aux mode. Industrial Temp

yy = silicon stepping/revision, contact sales for current data.
Add an “8” to the end for tape and reel delivery.

Please note that Industrial Temp is only available on revision WC and forward.

2. DETAILED DESCRIPTION

2.1. Port Functionality

Multi-function (Input/Output) ports allow for the highest possible flexibility. 7 bi-directional ports, 2 are headphone capable, support a wide variety of consumer desktop and mobile system use models.

- Port A supports
  - Headphone Out
  - Line Out
  - Line Input
  - Mic with 0/10/20/30 dB Boost
- Port B supports
  - Capless Headphone Out
  - Capless Line Out
- Port C
  - Line In
  - Line Out
  - Mic with 0/10/20/30 dB Boost
- Port D supports
  - BTL stereo out
- Port F supports
  - Line In
  - Line Out
  - Mic with 0/10/20/30 dB Boost

Pins 40-QFN	Port	Input	Output	Headphone	BTL	Mic Bias (Vref pin)	Input boost amp
22/23	A	Yes	Yes	Yes		Yes	Yes
25/26	B		Yes	Yes			
15/16	C	Yes	Yes			Yes	Yes
34/35/37/38	D		Yes		Yes		
13/14	F	Yes	Yes				Yes
3 (CLK=2)	DMIC0	Yes					Yes

Table 1. Port Functionality

2.1.1. Port Characteristics

Universal (Bi-directional) jacks are supported on ports A,C, and F. Ports A and B are designed to drive 32 ohm (nominal) headphones or a 10K (nominal) load. Line Level outputs are intended to drive an external 10K load (nominal) and an on board shunt resistor of 20-47K (nominal). However, applications may support load impedances of 5K ohms and above. Input ports are 50K (nominal) at the pin.

DAC full scale outputs and intended full scale input levels are 1V rms at 5V. Line output ports and Headphone output ports on the 92HD99 codec may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports are always on to prevent pops/clicks associated with charging and discharging output coupling capacitors. This maintains proper bias on output coupling caps even in power state D3 as long as AVDD is available. Unused ports should be left unconnected. When updating existing

designs to use the 92HD99 codec, ensure that there are no conflicts between the output ports on the codec and existing circuitry.

AFG Power State	Input Enable	Output Enable	Used as output for DAC/Mixer	Used as output for analog PC_Beep	Used as input for ADC, mixer	Port Behavior
D0-D2	1	1	Don't care	Don't care	Yes	Not allowed. Port is active as input.
					No	Not allowed. Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
	1	0	NA	NA	Yes	Active - Port enabled as input
	1	0	NA	NA	No	Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
	0	1	currently used by DAC, mixer, beep, or is traditional line or headphone output		NA	Active - Port enabled as output
	0	1	not currently used by DAC, mixer, beep and is capless HP/BTL port			Inactive (Power Down)
	0	0	NA	NA	NA	Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
D3	1	1	NA	NA	Don't care	Not allowed. Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
	1	0	NA	NA	Don't care	Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
	0	1	currently used by DAC, mixer, beep, or is traditional line or headphone output		Don't care	Low power state. If enabled, Beep will output from the port
	0	1	not currently used by DAC, mixer, beep and is capless HP/BTL port		Don't care	Inactive (Power Down)
	0	0	NA	NA	Don't care	Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps.
D3cold	-	-				Inactive (lower power) - Port keeps output coupling caps charged if port uses caps.
D4	-	-				Inactive (lower power) - Port keeps output coupling caps charged if port uses caps.
D5	-	-				Off - Charge on coupling caps (if used) will not be maintained.

Table 2. Analog Output Port Behavior

2.1.2. Vref_Out

Ports C, & A support Vref_Out pins for biasing electret cartridge microphones. Settings of 80% AVDD, 50% AVDD, GND, and Hi-Z are supported. Attempting to program a pin widget control with a reserved or unsupported value will cause the associated Vref_Out pin to assume a Hi-Z state and the pin widget control Vref_En field will return a value of '000' (Hi-Z) when read.

2.1.3. Jack Detect

Plugs inserted to a jack on Ports A, B, C are detected using SENSE_A. Plugs inserted to a jack on Port F, DMIC0, are detected using SENSE_B. Per HDA015-B, the detection circuit operates when the CODEC is in D0 - D3 and can also operate if both the CODEC and Controller are in D3 (no bus clock.) Jack detection requires that all supplies (analog and digital) are active and stable. When AVDD is not present, the value reported in the pin widget is invalid.

When the HD Audio bus is in a low power state (reset asserted and clock stopped) the CODEC will generate a Power State Change Request when a change in port connectivity is sensed and then generate an unsolicited response after the HD Audio link has been brought out of a low power state and the device has been enumerated. Per HDA015-B, this will take less than 10mS.

The following table summarizes the proper resistor tolerances for different analog supply voltages..

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance Pull-Up	Resistor Tolerance SENSE_A/B
4.75V	1%	1%

Resistor	SENSE_A	SENSE_B
39.2K	PORT A (HP0)	
20.0K	PORT B (HP1)	PORT F
10.0K	PORT C	DMIC0
5.11K		
2.49K	Pull-up to AVDD	Pull-up to AVDD

Table 3. 48pin Jack Detect

See reference design for more information on Jack Detect implementation.

2.2. Mixer

The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input. The following inputs are available:

- Port A
- Port C
- Port F
- DAC 0
- DAC 1

2.3. ADC Multiplexers

The codec implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function :(-16 to +30dB gain in 1dB steps) as an output amp and allow a preselection of one of below possible inputs:

- Port A
- Port C
- Port F
- Mixer Output
- DMIC 0

2.4. Power Management

The HD Audio specification defines power states, power state widgets, and power state verbs. Power management is implemented at several levels. The Audio Function Group (AFG) , all converter widgets, and all pin complexes support the power state verb F05/705. Converter widgets are active in D0 and inactive in D1-D3.

The following table describes what functionality is active in each power state.

Function	D0	D1[1]	D2	D3	D3cold	Vendor Specific D4	Vendor SpecificD5
Digital Microphone inputs	On	Off	Off	Off	Off	Off	Off
DAC	On	Off	Off	Off	Off	Off	Off
D2S	On	Off	Off	Off	Off	Off	Off
ADC	On	Off	Off	Off	Off	Off	Off
ADC Volume Control	On	Off	Off	Off	Off	Off	Off
Ref ADC	On	Off	Off	Off	Off	Off	Off
Analog Clocks	On	Off	Off	Off	Off	Off	Off
GPIO pins	On	On	On	On[5]	On	On	Off
VrefOut Pins	On	On	Off	Off	Off	Off	Off
Input Boost	On	On	Off	Off	Off	Off	Off
Analog mixer	On	On	Off	Off	Off	Off	Off
Mixer Volumes	On	On	Off	Off	Off	Off	Off
Analog PC_Beep	On	On	On	On	Off	Off	Off
Digital PC_Beep	On	On	On	On[5]	Off	Off	Off
Lo/HP Amps	On	On	On	Low Drive[2]	Low Drive[2]	Low Drive[2]	Off
Cap-less HP Amps	On	On	On	Low Drive[2]	Low Drive[2]	Low Drive[2]	Off
BTL Amp	On	On	On	Low Drive[2]	Off	Off	Off
VAG amp	On	On	On	Low Drive[3]	Low Drive	Low Drive	Off
Port Sense	On	On	On	On[4]	Off	Off	Off
Reference Bias generator	On	On	On	On	On	On	Off
Reference Bandgap core	On	On	On	On	On	On	Off
HD Audio-Link	On	On	On	On[5]	Limited	Off	Off

Table 4. Power Management

1. No DAC or ADC streams are active. Analog mixing and loop thru are supported.

2. VAG is kept active when ports are disabled or in D3/D3cold/D4. PC_Beep is supported in D3 but may be attenuated and distorted depending on load impedance. The codec will shut down the capless headphone amplifiers and BTL amplifier in D3 and below. In D3, Hendrix/Kaveri will turn on the BTL and Capless amplifiers if activity is detected on the PC_BEEP input and analog PC_Beep is enabled.
3. VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
4. Both AVDD and DVDD must be available for Port Sense to operate.
5. Not active if BITCLK is not running (Controller in D3), but can signal power state change request (PME)

The D3-default state is available for HD Audio compliance. The programmable values, exposed via vendor-specific settings, are under IDT Device Driver control for further power reduction. The analog mixer, line and headphone amps, port presence detect, and internal references may be disabled using vendor specific verbs. Use of these vendor specific verbs will cause pops.

The default power state for the Audio Function Group after reset is D3.

2.5. AFG D0

The AFG D0 state is the active state for the device. All functions are active if their power state (if they support power management at their node level) has been set to D0.

2.6. AFG D1

D1 is a lower power mode where all converter widgets are disabled. Analog mixer and port functions are active. The part will resume from theD1 to theD0 state within 1 mS.

2.7. AFG D2

The D2 state further reduces power by disabling the mixer and port functions. The port amplifiers and internal references remain active to keep port coupling caps charged and the system ready for a quick resume to either the D1 or D0 state. The part will resume from the D2 state to the D0 state within 2mS.

2.8. AFG D3

The D3-default state is available for HD Audio compliance. All converters are shut down. Port amplifiers and references are active but in a low power state to prevent pops. Resume times may be longer than those from D2, but still less than 10mS to meet Intel low power goals. The default power state for the Audio Function Group after power is applied is D3.

While in AFG D3, the HD Audio controller may be in a D0 state (HD Audio bus active) or in a D3 state (HD Audio bus held in reset with no Bit_Clk, SData_Out, or Sync activity.) The expected behavior is as follows (see the HDA015-B section for more information):

Function	HDA Bus active	HDA Bus stopped
Port Presence Detect state change	Unsolicited Response	Wake Event followed by an unsolicited response
GPIO state change	Unsolicited Response	Wake Event followed by an unsolicited response

2.8.1. AFG D3cold

The D3cold power state is the lowest power state available that does not use vendor specific verbs. While in D3cold, the CODEC will still respond to bus requests to revert to a higher power state (dou-

ble AFG reset, link reset). However, audio processing, port presence detect, and other functions are disabled. Per the HD Audio bus HDA015-B, the D3cold state is intended to be used just prior to removing power to the CODEC. Typically, power will be removed within 200mS. However, the codec may exit from the D3cold state by generating 2, back-to-back, AFG reset events. Resume time from D3cold is less than 200mS.

2.9. Vendor Specific Function Group Power States D4/D5

The codec introduces vendor specific power states. A vendor defined verb is added to the Audio Function Group that combines multiple vendor specific power control bits into logical power states for use by the audio driver. The 2 states defined offer lower power than the 5 existing states defined in the HD Audio specification and HDA015-B. The Vendor Specific D4 state provides lower digital power consumption relative to D3cold by disabling HD Audio link responses. Vendor specific D5 further reduces power consumption on the digital supply by turning off GPIO drivers, and reduces analog power consumption by turning off all analog circuitry except for reset circuits.

States D4/D5 are not entered until D3cold has been requested so are actually D3cold options rather than true, independent, power states. Software can pre-program the D4 or D5 state as a re-definition of how the part will behave when the D3cold power state is requested or software may enter D3cold, then set the D4 or D5 before performing the power state get command. The preferred method is to request D3cold, then select D4 or D5 as desired.This will reduce the severity of pops encountered when entering D4 or D5.

Both power states require a link reset or removal of DVDD to exit.

The CODEC may pop when using these verbs and transition times to an active state (D1 or D0 for example) may take several seconds.

2.10. Low-voltage HDA Signaling

The codec is compatible with either 1.5V or 3.3V HDA bus signaling; in the 48QFN package the voltage selection is done dynamically based on the input voltage of DVDD_IO.

DVDD_IO is currently not a logic configuration pin, but rather provides the digital power supply to be used for the HDA bus signals.

When in 1.5V mode, the codec can correctly decode BITCLK, SYNC, RESET# and SDO as they operate at 1.5V; additionally it will drive SDI and SDO at 1.5V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

2.11. Multi-channel capture

The capability to assign multiple “ADC Converters” to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported this is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) may be used to create a multi-channel input stream. There are no restrictions regarding digital microphones.

The ADC Converters can be associated with a single stream as long the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

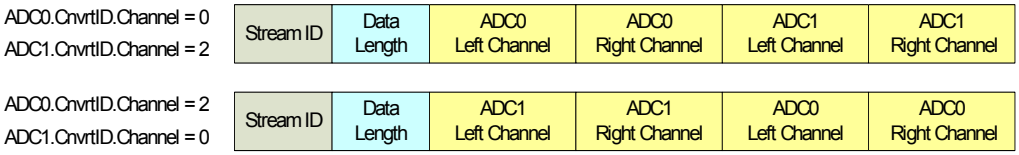
The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the “Multi-Converter Stream Critical Entries.” table.

An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2 & 3 is shown below. A 4 Channel stream can be created by assigning the same non-zero stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NmbrChan = 0011”.

ADC1 CnvtrID	**(NID = 0x08)**	
	[3:0]	Ch = 2
ADC0 CnvtrID	**(NID = 0x07)**	
	[3:0]	Ch=0

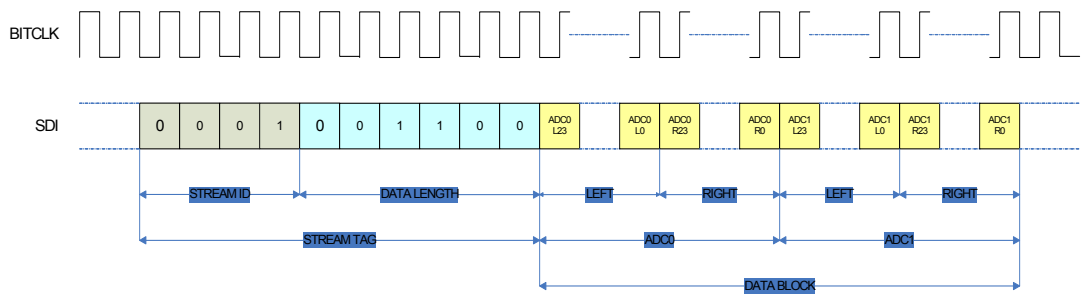
Table 5. Example channel mapping

Figure 1. Multi-channel capture



The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

Figure 2. Multi-channel timing diagram



ADC[1:0] Cnvtr	Bit Number	Sub Field Name	Description
	[15]	StrmType	Stream Type (TYPE): 0: PCM 1: Non-PCM (not supported)
	[14]	FrmtSmplRate	Sample Base Rate 0= 48kHz 1=44.1KHz

Table 6: Mult-channel

	[13:11]	SmplRateMultp	Sample Base Rate Multiple 000=48kHz/44.1kHz or less 001= x2 010= x3 (not supported) 011= x4 192kHz only, 176.4 not supported 100-111= Reserved
	[10:8]	SmplRateDiv	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 (not supported) 010= Divide by 3 (not supported) 011= Divide by 4 (not supported) 100= Divide by 5 (not supported) 101= Divide by 6 (not supported) 110= Divide by 7 (not supported) 111= Divide by 8 (not supported)
	[6:4]	BitsPerSmpl	Bits per Sample 000= 8 bits (not supported) 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
	[3:0]	NmbrChan	Number of Channels Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link. 0000=1 channel (not supported) 0001 = 2 channels … 1111= 16 channels.
	[7:4]	Strm	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
	[3:0]	Ch	Integer representing lowest channel used by converter. 0 and 2 are valid Entries If assigned to the same stream, one ADC must be assigned a value of 0 and the other ADC assigned a value of 2.

Table 6: Mult-channel

2.12. EAPD

The EAPD pin (pin 47) is a dedicated, bi-directional control pin. Although named External Amplifier Power Down (EAPD) by the HD Audio specification, this pin operates as an external amplifier power up signal. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up (equivalent to D0), and a 0 causes it to power down (equivalent to D3.) When the EAPD value = 1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value (in the register) may remain 1. The default state of this pin is 0 (driving low.) The pin defaults to an open-drain configuration (an external pull-up is recommended.)

Per the HD Audio specification and HDA015-B, multiple ports may control EAPD. The EAPD pin assumes the highest power state of all the the EAPD bits in all of the pin complexes. The default value of EAPD is 1 (powered on), but the FG power state will override and the pin will be low. A port will request External Amp Power Up when its power state is active (FG and pin widget power state is

D1 or D0) or (Analog PC_Beep is enabled and port is enabled as an output) and the port's EAPD bit is set to 1. The state of the EAPD pin (unless configured as an input or held low by an external circuit when configured as an open drain output) will be the logical OR of the external amp power up requests from all ports.

By default, the EAPD pin also functions as the Mute#/ShutDown# input for the internal BTL amplifier. In this mode, a low value at the pin (either due to internal EAPD being 0, or to an external entity forcing the pin low) will cause the internal BTL amplifier to mute or enter a low power state depending on the amplifier configuration. (See below)

Vendor specific verbs are available to configure this pin. These verbs retain their values across link and single function group resets but are set to their default values by a power on reset:

MODE1	MODE0	EAPD Pin Function	Description
0	0	Open Drain I/O	Value at pin is wired-AND of EAPD bit and external signal.(default)
0	1	CMOS Output	Value of EAPD bit in pin widget is forced at pin
1	0	CMOS Input	External signal controls internal amps. EAPD bit in pin widget ignored
1	1	CMOS Input	External signal controls internal amps. EAPD bit in pin widget ignored

Table 7. EAPD Pin Mode Select

Control Flag	Description
EAPD PIN MODE 1:0	Defines if EAPD pin is used as input, output, or bi-directional port (Open Drain)
BTL/HP SD	0 = Amp controlled by EAPD pin only (default) / 1 = Amp controlled by power state (pin and FG) only
BTL/HP SD MODE	0 = Amp will mute when disabled. / 1 = Amp will shut down (enter a low power state) when disabled (default for YA forward)
BTL/HP SD INV	0 = AMP will power down (or mute) when EAPD pin is low (default) / 1 = Amp will power down (or mute) when EAPD pin is high.

Table 8. Control bit descriptions for BTL amplifier and Headphone amplifier enable configurations

BTL SD	BTL SD MODE	BTL SD INV	EAPD Pin State	BTL Amp State
0	0	0	0	Amplifier is mute (default[1])
0	0	0	1	Amplifier is active
0	0	1	0	Amplifier is active
0	0	1	1	Amplifier is mute
0	1	0	0	Amplifier is in a low power state
0	1	0	1	Amplifier is active
0	1	1	0	Amplifier is active
0	1	1	1	Amplifier is in a low power state
1	0	NA	NA	Amplifier follows pin/function group power state and will mute when disabled
1	1	NA	NA	Amplifier follows pin/function group power state and will enter a low power state when disabled

Table 9. BTL Amp Enable Configuration

1. EAPD bit is set to one by default but the EAPD state is 0 after power-on reset because the function group is not in D0. The state after a single or double function group reset will be compliant with HDA015-B.

HP SD	HP SD MODE	HP SD INV	EAPD Pin State	Headphone Amp State
0	0	0	0	Amplifier is mute (default[1])
0	0	0	1	Amplifier is active
0	0	1	0	Amplifier is active
0	0	1	1	Amplifier is mute
0	1	0	0	Amplifier is in a low power state
0	1	0	1	Amplifier is active
0	1	1	0	Amplifier is active
0	1	1	1	Amplifier is in a low power state
1	0	NA	NA	Amplifier follows pin/function group power state and will mute when disabled
1	1	NA	NA	Amplifier follows pin/function group power state and will enter a low power state when disabled

Table 10. Headphone Amp Enable Configuration

1. EAPD bit is set to one by default but the EAPD state is 0 after power-on reset because the function group is not in D0. The state after a single or double function group reset will be compliant with HDA015-B.

Analog BEEP enabled	EAPD Pin value[1]	Description
0	Forced to low when in D2 or D3	Follows description in HD Audio spec. External amplifier is shut down when pin or function group power state is D2 or D3 independent of value in EAPD bit.
1	Forced low in D2 or D3 unless port is enabled as output	Power state is ignored if port is enabled as output and port EAPD=1 to allow PC_Beep support in D2 and D3

Table 11. EAPD Analog PC_Beep behavior

1. When pin is enabled as Open Drain or CMOS output.

AFG Power State	RESET#	Analog PC_BEEP	Port Power State	Pin Behavior
D0-D3	Asserted (Low)	-	-	Active low immediately after power on, otherwise the previous state is retained across FG and link reset events
D0	De-Asserted (High)	-	-	Active - Pin reflects EAPD bit unless held low by external source.
D1	De-Asserted (High)	-	D0-D1	Active - Pin reflects EAPD bit unless held low by external source.
D2	De-Asserted (High)	Disabled	D0-D2	Pin forced low to disable external amp
D2	De-Asserted (High)	Enabled	D0-D2	Active - EAPD Pin high if any port EAPD bit =1 and that port also enabled as output.
D3	De-Asserted (High)	Disabled	D0-D3	Pin forced low to disable external amp
D3	De-Asserted (High)	Enabled	D0-D3	Active - EAPD Pin high if any port EAPD bit=1 and that port also enabled as output.
D3cold	De-Asserted (High)	-	-	Pin forced low to disable external amp
D4	De-Asserted (High)	-	-	Pin forced low to disable external amp
D5	De-Asserted (High)	-	-	Pin Hi-Z (off)

Table 12. EAPD Behavior

Figure 3. HP EAPD Example to be replaced by single pin for internal amp

HP AUDIO CONTROL BLOCK DIAGRAM

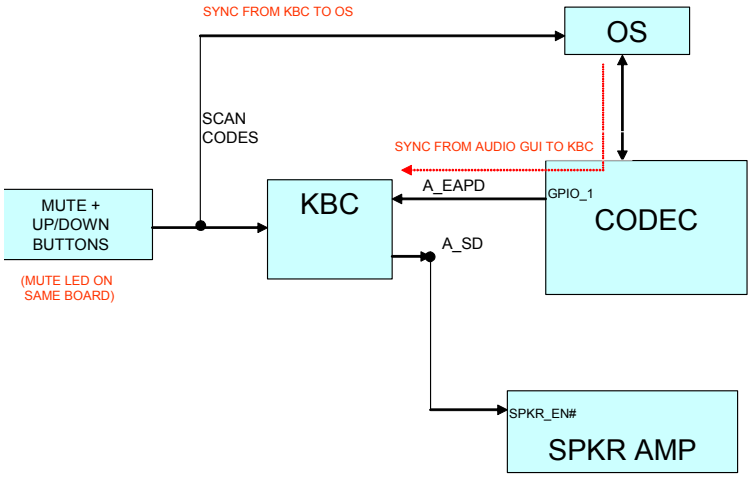
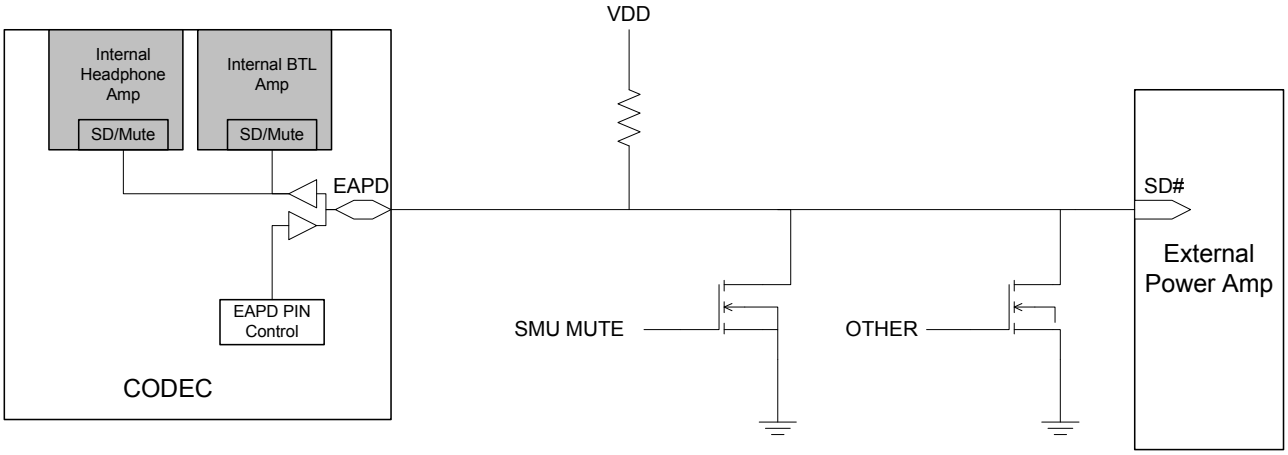


Figure 4. EAPD implementation



2.13. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0 and DMIC_CLK 3-pin interface. The DMIC0 signals are inputs that carry individual channels of digital microphone data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels. This mode is selected using a vendor specific verb and the left time slot is copied to the ADC left and right inputs.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the internal master clock. The default frequency is 2.352Mhz.

The DMIC data input is reported as a stereo input pin widgets that incorporate a boost amplifier. The pin widgets are shown connected to the ADCs through the same multiplexors as the analog ports.

Although the internal implementation is different between the analog ports and the digital microphones, the functionality is the same. In most cases, the default values for the DMIC clock rate and data sample phase will be appropriate and an audio driver will be able to configure and use the digital microphones exactly like an analog microphone.

To conserve power, the analog portion of the ADC will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input. This should take less than 10mS.

DMIC pin widgets support port presence detect directly using SENSE-B input.

The codec supports the following digital microphone configurations:

Digital Mics	Data Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones
1	Single Edge	0, or 1	Available on either DMIC_0 or DMIC_1 When using a microphone that supports multiplexed operation (2-mics can share a common data line), configure the microphone for “Left” and select mono operation using the vendor specific verb. “Left” D-mic data is used for ADC left and right channels.
2	Double Edge on either DMIC_0 or 1	0, or 1	Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge (multiplexed output) capability.

Table 13. Valid Digital Mic Configurations

Power State	DMIC Widget Enabled?	DMIC_CLK Output	DMIC_0	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when DMIC_0 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D1-D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D4	-	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D5	-	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down

Table 14. DMIC_CLK and DMIC_0 Operation During Power States

Figure 5. Single Digital Microphone (data is ported to both left and right channels

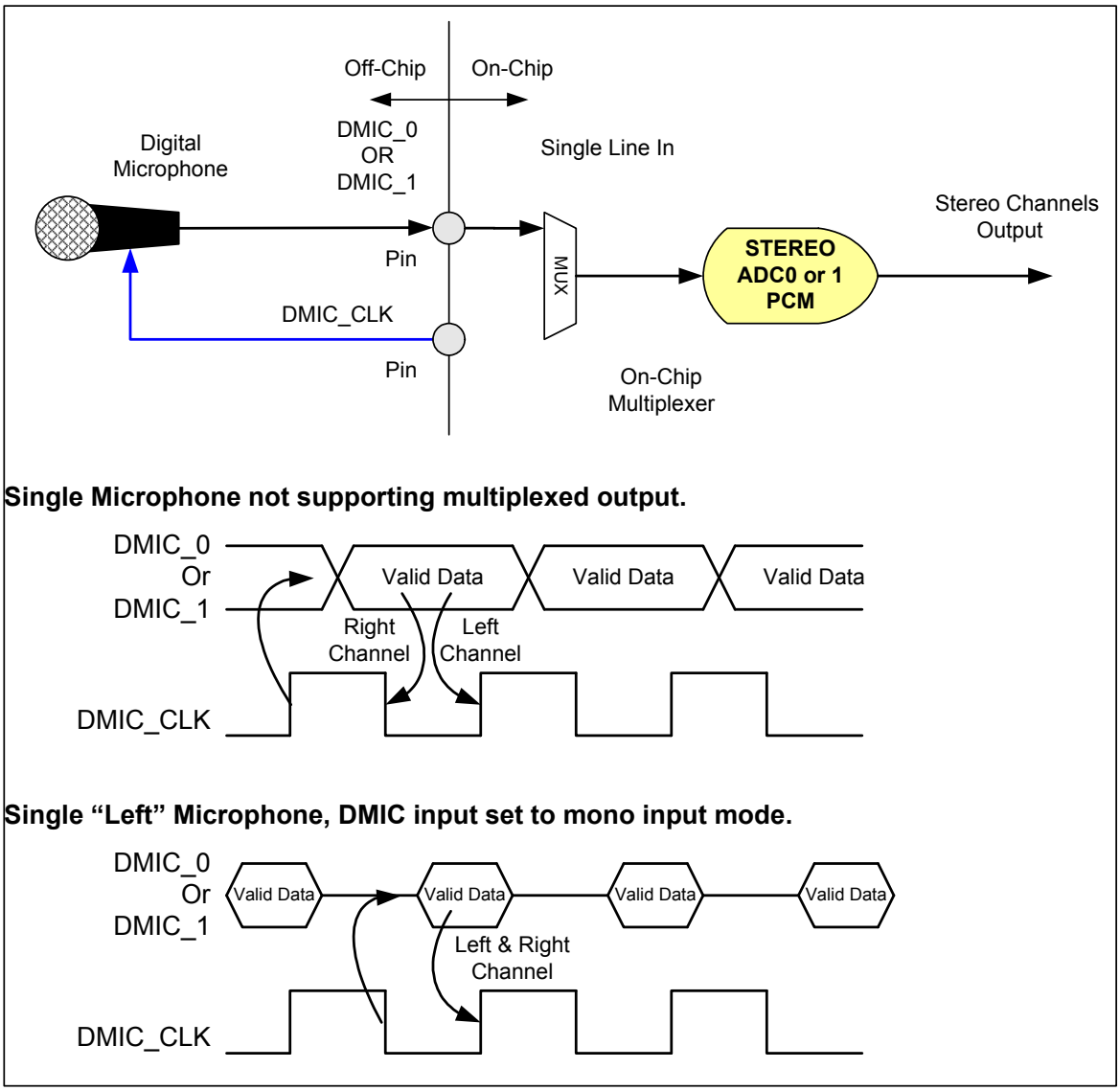
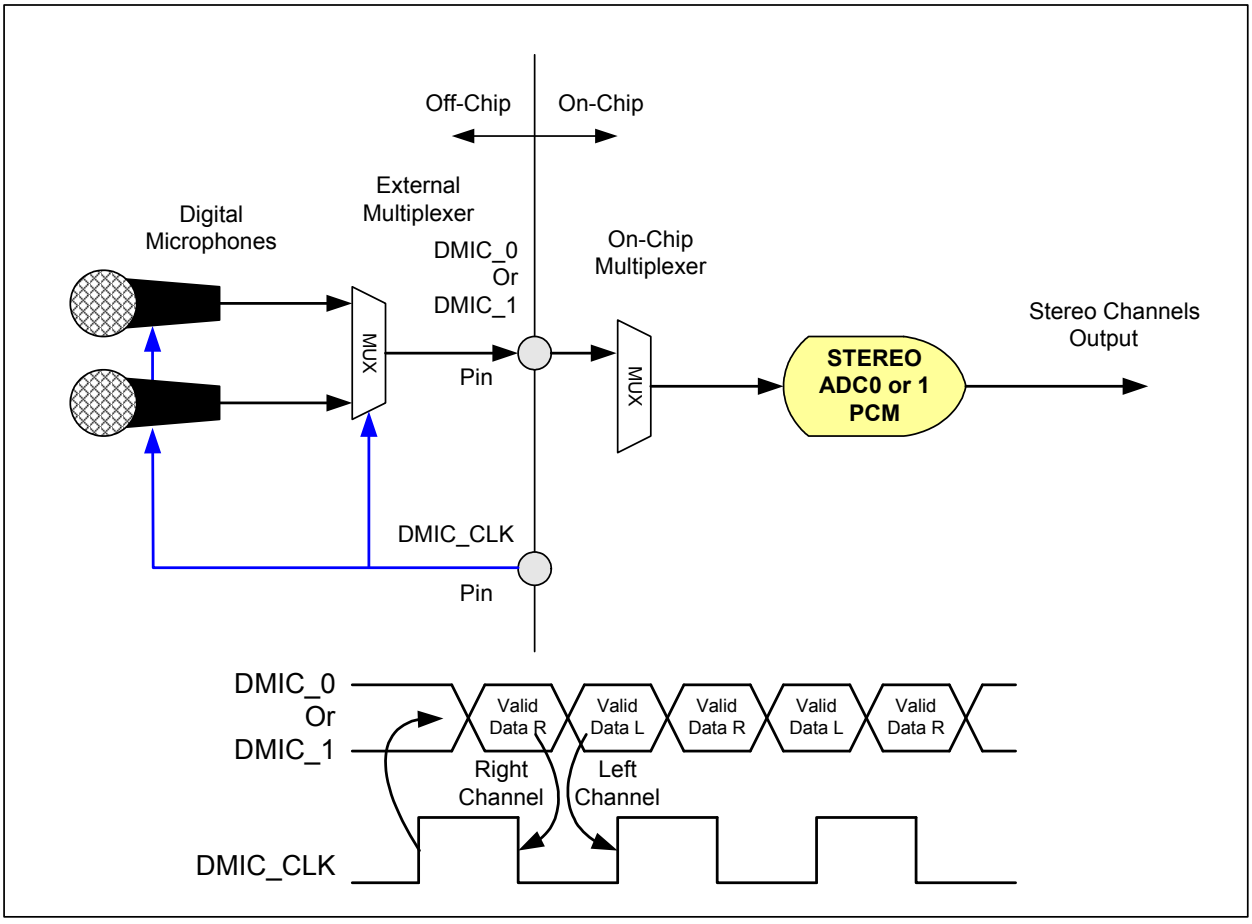


Figure 6. Stereo Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

2.14. Analog PC-Beep

The codec supports automatic routing of the PC_Beep pin to Port A, Port B, and Port D outputs when the HD-Link is in reset.

When the link is active (not held in reset) Analog PC-Beep may be enabled manually. Analog PC_Beep is mixed at the port and only ports enabled as outputs will pass PC_Beep.

Beep activity monitoring is provided when the analog beep path is enabled and the CODEC or amplifier is in a low power state (D3).

The Analog PC Beep input is sampled for 500us every 1ms. If the beep input is high or low (>200mVpp) for at least 37% of that time, it is considered active. If it is active for less than 7.5% of

that time, it is possibly inactive. If no activity is detected for 64ms (128ms, 256ms and 512ms also selectable for the idle threshold), then beep is considered inactive.

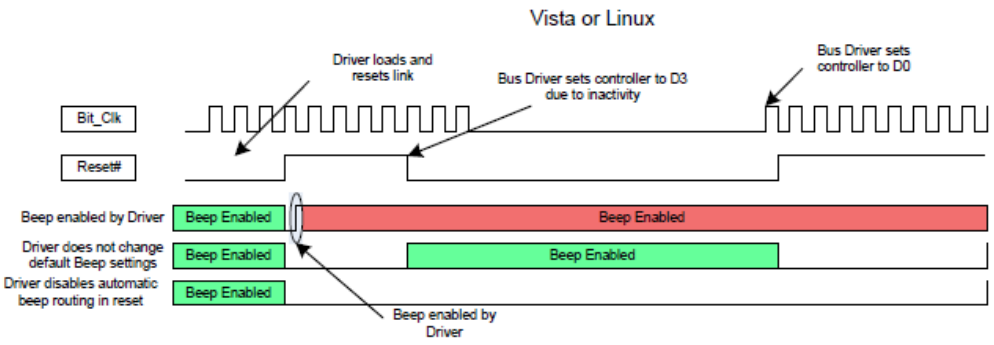


Figure 7. Analog PC Beep Active

Phase 1: analog beep auto-routing phase in the period after application of DVDD, before the first rising edge of link reset.

Once Analog PCbeep is detected(BEEP_PRESENCE=1) after 64ms delays (after POR (power on reset)), the Amplifier will be turned on(port_pwd=0, port_output_en=1, there is a timing between these two signals) and analog_beep_en=1. If BEEP_PRESENCE=0 for longer than the threshold time, the amplifiers will be turned off to save power and prevent unwanted system noise from being heard.

Phase 2: When not in phase 1

A. If analog beep function is disabled by driver.

Analog beep auto-detect will also be disabled.

B. If analog beep function is enabled by driver.

Once analog PCbeep is detected(BEEP_PRESENCE=1), analog pc_beep will be enabled

If in D0-D2, enabled simply means muting or un-muting beep to avoid hearing system noise on the beep input pin but it is acceptable to turn off port amplifiers if not currently used by DACs, mixer, or beep to save power.

If in D3, enabled means that the necessary amplifiers are turned on so that the beep signal may be heard on all ports configured as outputs (see analog pc-beep description section above)

All needed amplifiers are enabled until BEEP_PRESENCE=0 for longer than the idle threshold

A flow chart of Analog PC Beep is below.