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Integrated Circuit Systems, Inc.

ICS93732

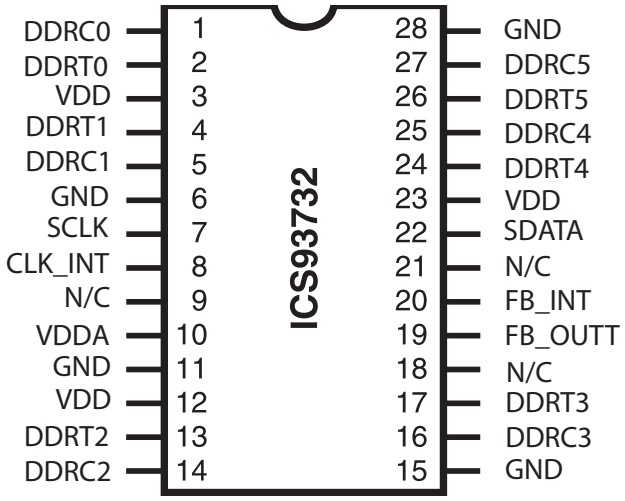
Low Cost DDR Phase Lock Loop Zero Delay Buffer

Recommended Application:
DDR Zero Delay Clock Buffer

Product Description/Features:
- Low skew, low jitter PLL clock driver
- Max frequency supported = 266MHz (DDR 533)
- I^2C for functional and output control
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- 3.3V tolerant CLK_INT input

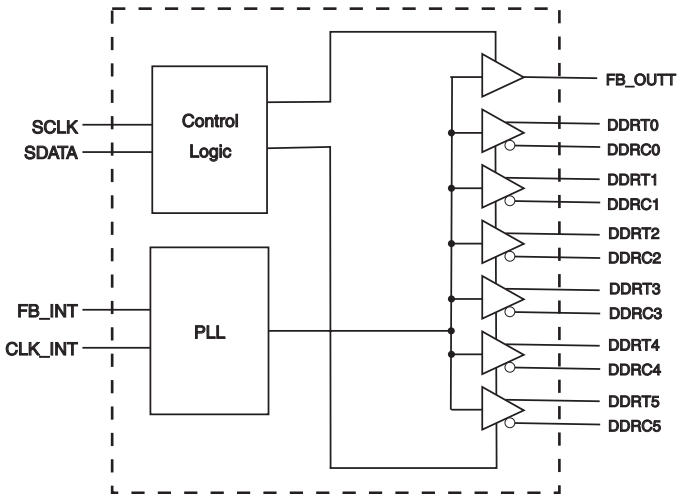
Switching Characteristics:
- CYCLE - CYCLE jitter (66MHz): <120ps
- CYCLE - CYCLE jitter (>100MHz): <65ps
- CYCLE - CYCLE jitter (>200MHz): <75ps
- OUTPUT - OUTPUT skew: <100ps
- DUTY CYCLE: 49.5% - 50.5%

Pin Configuration



28-pin 209mil SSOP

Block Diagram



Functionality

INPUTS		OUTPUTS			PLL State
AVDD	CLK_INT	CLKT	CLKC	FB_OUTT	
2.5V (nom)	L	L	H	L	on
2.5V (nom)	H	H	L	H	on

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	DDRC0	OUT	"Complimentary" Clock of differential pair output.
2	DDRT0	OUT	"True" Clock of differential pair output.
3	VDD	PWR	Power supply, nominal 2.5V
4	DDRT1	OUT	"True" Clock of differential pair output.
5	DDRC1	OUT	"Complimentary" Clock of differential pair output.
6	GND	PWR	Ground pin.
7	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
8	CLK_INT	IN	"True" reference clock input.
9	N/C	N/C	No Connection.
10	VDDA	PWR	2.5V power for the PLL core.
11	GND	PWR	Ground pin.
12	VDD	PWR	Power supply, nominal 2.5V
13	DDRT2	OUT	"True" Clock of differential pair output.
14	DDRC2	OUT	"Complimentary" Clock of differential pair output.
15	GND	PWR	Ground pin.
16	DDRC3	OUT	"Complimentary" Clock of differential pair output.
17	DDRT3	OUT	"True" Clock of differential pair output.
18	N/C	N/C	No Connection.
19	FB_OUT	OUT	Feedback output, dedicated for external feedback.
20	FB_INT	IN	True single-ended feedback input, provides feedback signal to internal PLL for synchronization with CLK_INT to eliminate phase error.
21	N/C	N/C	No Connection.
22	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
23	VDD	PWR	Power supply, nominal 2.5V
24	DDRT4	OUT	"True" Clock of differential pair output.
25	DDRC4	OUT	"Complimentary" Clock of differential pair output.
26	DDRT5	OUT	"True" Clock of differential pair output.
27	DDRC5	OUT	"Complimentary" Clock of differential pair output.
28	GND	PWR	Ground pin.

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operation Conditions

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.50V ± 0.20V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog / Core Supply Volta	AV_{DD}		2.3	2.5	2.7	V
Input Voltage Level	V_{IN}		2	2.5	3	V
Output Differential Pair Crossing Voltage	V_{OC}	66/100/133/166MHz, V_{DD}=2.50V	1.23	1.25	1.32	V

Electrical Characteristics - Input / Supply / Common Output parameters

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.50V ± 0.20V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5}$	R_T = 120W, C_L = 12 pF at 100MHz		236	300	mA
		R_T = 120W, C_L = 12 pF at 133MHz		263	300	
	I_{DDPD}	CL=0 pF			100	mA
Output High Current	I_{OH}	V_{DD} = 2.5V, V_{OUT} = 1V	-48	-33	-29	mA
Output Low Current	I_{OL}	V_{DD} = 2.5V, V_{OUT} = 1.2V	29	33	37	mA
High Impedance Ouptut Current	I_{OZ}	V_{DD} = 2.7V, V_{OUT} = V_{DD} or GND			10	mA
High-level Output Voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1mA	2	2.25		V
		V_{DD} = 2.3V, I_{OH} = -12mA		1.95		
Low-level Output Voltage	V_{OL}	V_{DD} = min to max, I_{OH} = 1mA		0.05	0.1	V
		V_{DD} = 2.3V, I_{OH} = 12mA		0.3	0.4	
Output Capacitance[1]	C_{OUT}	V_I = V_{DD} or GND		3		pF

1. Guaranteed by design, not 100% tested in production.

Timing Requirements

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.50V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Clock Frequency	$freq_{op}$	Input Voltage level: 0-2.50V	22		340	MHz
Input Clock Duty Cycle[1]	d_{tin}		40	50	60	%
Clock Stabilization[1]	t_{STAB}	from VDD = 2.5V to 1% target frequency			100	µs

1. Guaranteed by design, not 100% tested in production.

Switching Characteristics

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.50V ± 0.20V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cycle to cycle Jitter[1,2]	t_{c-c}	66 MHz		100	120	ps
		100 / 125/ 133/167MHz		48	65	
		200/267MHz		47	75	
Phase Error[1]	t_{pe}		-150		150	ps
Output to output Skew[1]	T_{skew}			20	100	ps
Duty Cycle (Sign Ended)[1,3]	DC	66 MHz to 100MHz	49.5	50	50.5	%
		101MHz to 267 MHz	49	49.4	51	%
Rise Time, Fall Time[4]	t_R , t_f	Load=120Ω/14pF		579	950	ps

Notes:

1. Refers to transition on noninverting output.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{wH}/t_c, where the cycle (t_c) decreases as the frequency goes up.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D4_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D4_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D5_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D5_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

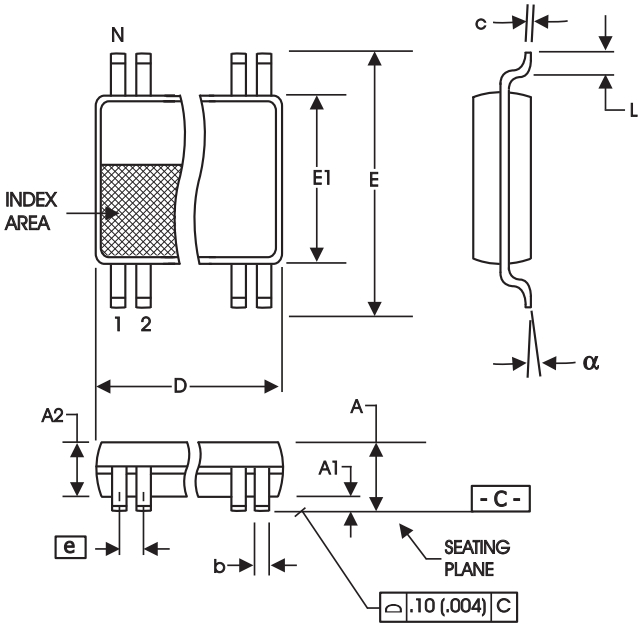
Bytes 0 to 4 are reseved power up default = 1. This allows operation with main clock.

BYTE 5	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	2, 1	DDR0(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 6	4, 5	DDR1(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 5	-	-	Reserved	X	-	-	1
Bit 4	-	-	Reserved	X	-	-	1
Bit 3	13, 14	DDR2(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 2	17, 16	DDR3(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 1	-	-	Reserved	X	-	-	1
Bit 0	-	-	Reserved	X	-	-	1

Note: PWD = Power Up Default

BYTE 6	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	-	Reserved	X	-	-	0
Bit 6	-	-	Reserved	X	-	-	0
Bit 5	-	-	Reserved	X	-	-	0
Bit 4	-	-	Reserved	X	-	-	1
Bit 3	24, 25	DDR4(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 2	-	-	Reserved	X	-	-	1
Bit 1	26, 27	DDR5(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 0	-	-	Reserved	X	-	-	1

Note: PWD = Power Up Default



209 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

Ordering Information

ICS93732yFLFT

Example:

ICS XXXX y F LF T

- **Designation for tape and reel packaging**
- **RoHS Compliant**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0578J—06/20/08

Revision History

Rev.	Issue Date	Description	Page #
I	5/18/2005	Added LF Ordering Information to TSSOP package.	8
J	6/20/2008	Removed TSSOP Ordering Information.	-