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Contact us

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

16K Microwire Compatible Serial EEPROM

Device Selection Table

Part Number	Vcc Range	ORG Pin	PE Pin	Word Size	Temp Ranges	Packages
93AA86A	1.8-5.5	No	No	8-bit	I	P, SN, ST, MS, OT
93AA86B	1.8-5-5	No	No	16-bit	I	P, SN, ST, MS, OT
93LC86A	2.5-5.5	No	No	8-bit	I, E	P, SN, ST, MS, OT
93LC86B	2.5-5.5	No	No	16-bit	I, E	P, SN, ST, MS, OT
93C86A	4.5-5.5	No	No	8-bit	I, E	P, SN, ST, MS, OT
93C86B	4.5-5.5	No	No	16-bit	I, E	P, SN, ST, MS, OT
93AA86C	1.8-5.5	Yes	Yes	8- or 16-bit	I	P, SN, ST, MS, MC, MN
93LC86C	2.5-5.5	Yes	Yes	8- or 16-bit	I, E	P, SN, ST, MS, MC, MN
93C86C	4.5-5.5	Yes	Yes	8- or 16-bit	I, E	P, SN, ST, MS, MC, MN

Features:

- Low-Power CMOS Technology
- ORG Pin to Select Word Size for '86C' Version
- 2048 x 8-bit Organization 'A' Devices (no ORG)
- 1024 x 16-bit Organization 'B' Devices (no ORG)
- Program Enable Pin to Write-Protect the Entire Array ('86C' version only)
- Self-tImed Erase/Write Cycles (including Auto-Erase)
- Automatic Erase All (ERAL) before Write All (WRAL)
- Power-On/Off Data Protection Circuitry
- Industry Standard 3-Wire Serial I/O
- Device Status Signal (Ready/$\overline{Busy}$)
- Sequential Read Function
- 1,000,000 E/W Cycles
- Data Retention > 200 Years
- Pb-free and RoHS Compliant
- Temperature Ranges Supported:
    - Industrial (I)   -40°C to +85°C
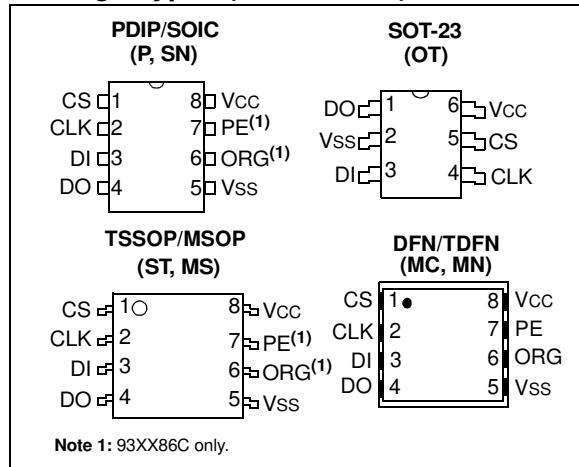   - Automotive (E) -40°C to +125°C

Description:

The Microchip Technology Inc. 93XX86A/B/C devices are 16K bit low-voltage serial Electrically Erasable PROMs (EEPROM). Word-selectable devices such as the 93XX86C are dependent upon external logic levels driving the ORG pin to set word size. The 93XX86A devices provide dedicated 8-bit memory organization, while the 93XX86B devices provide dedicated 16-bit memory organization. A Program Enable (PE) pin allows the user to write-protect the entire memory array. Advanced CMOS technology makes these devices ideal for low-power, nonvolatile memory applications. The entire 93XX Series is available in standard packages including 8-lead PDIP and SOIC, and advanced packaging including 8-lead MSOP, 6-lead SOT-23, 8-lead 2x3 DFN/TDFN and 8-lead TSSOP. All packages are Pb-free (Matte Tin) finish.

Pin Function Table

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
PE	Program Enable – 93XX86C only
ORG	Memory Configuration – 93XX86C only
Vcc	Power Supply

Package Types (not to scale)

PDIP/SOIC (P, SN)

CS	1	8	Vcc
CLK	2	7	PE[1]
DI	3	6	ORG[1]
DO	4	5	Vss

SOT-23 (OT)

DO	1	6	Vcc
Vss	2	5	CS
DI	3	4	CLK

TSSOP/MSOP (ST, MS)

CS	1	8	Vcc
CLK	2	7	PE[1]
DI	3	6	ORG[1]
DO	4	5	Vss

DFN/TDFN (MC, MN)

CS	1	8	Vcc
CLK	2	7	PE
DI	3	6	ORG
DO	4	5	Vss

Note 1: 93XX86C only.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [†]

V_{CC}...7.0V

All inputs and outputs w.r.t. V_{SS} ....-0.6V to V_{CC} +1.0V

Storage temperature ....-65°C to +150°C

Ambient temperature with power applied...-40°C to +125°C

ESD protection on all pins ....$\geq$ 4 kV

Note:	† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			Industrial (I): T_A = -40°C to +85°C, V_{CC} = +1.8V to 5.5V Automotive (E): T_A = -40°C to +125°C, V_{CC} = +2.5V to 5.5V				
Param. No.	Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
D1	V_{IH1} V_{IH2}	High-level input voltage	2.0 0.7 V_{CC}	— —	V_{CC} +1 V_{CC} +1	V V	$V_{CC} \geq$ 2.7V V_{CC} < 2.7V
D2	V_{IL1} V_{IL2}	Low-level input voltage	-0.3 -0.3	— —	0.8 0.2 V_{CC}	V V	$V_{CC} \geq$ 2.7V V_{CC} < 2.7V
D3	V_{OL1} V_{OL2}	Low-level output voltage	— —	— —	0.4 0.2	V V	I_{OL} = 2.1 mA, V_{CC} = 4.5V I_{OL} = 100 μA, V_{CC} = 2.5V
D4	V_{OH1} V_{OH2}	High-level output voltage	2.4 V_{CC} - 0.2	— —	— —	V V	I_{OH} = -400 μA, V_{CC} = 4.5V I_{OH} = -100 μA, V_{CC} = 2.5V
D5	I_{LI}	Input leakage current	—	—	±1	μA	V_{IN} = V_{SS} or V_{CC}
D6	I_{LO}	Output leakage current	—	—	±1	μA	V_{OUT} = V_{SS} or V_{CC}
D7	C_{IN}, C_{OUT}	Pin capacitance (all inputs/outputs)	—	—	7	pF	V_{IN}/V_{OUT} = 0V **(Note 1)** T_A = 25°C, F_{CLK} = 1 MHz
D8	I_{CC} write	Write current	— —	— 500	3 —	mA μA	F_{CLK} = 3 MHz, V_{CC} = 5.5V F_{CLK} = 2 MHz, V_{CC} = 2.5V
D9	I_{CC} read	Read current	— — —	— — 100	1 500 —	mA μA μA	F_{CLK} = 3 MHz, V_{CC} = 5.5V F_{CLK} = 2 MHz, V_{CC} = 3.0V F_{CLK} = 2 MHz, V_{CC} = 2.5V
D10	I_{CCS}	Standby current	— —	— —	1 5	μA μA	I – Temp E – Temp CLK = CS = 0V ORG = DI PE = V_{SS} or V_{CC} **(Note 2) (Note 3)**
D11	V_{POR}	V_{CC} voltage detect	— —	1.5 3.8	— —	V V	**(Note 1)** 93AA86A/B/C, 93LC86A/B/C 93C86A/B/C

Note 1: This parameter is periodically sampled and not 100% tested.

2: ORG and PE pin not available on 'A' or 'B' versions.

3: Ready/$\overline{Busy}$ status must be cleared from DO; see **Section 3.4 "Data Out (DO)"**.

# 93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

TABLE 1-2: AC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.						Industrial (I): T$_A$ = -40°C to +85°C, V$_{CC}$ = +1.8V to 5.5V Automotive (E): T$_A$ = -40°C to +125°C, V$_{CC}$ = +2.5V to 5.5V
Param. No.	Symbol	Parameter	Min.	Max.	Units	Conditions
A1	F$_{CLK}$	Clock frequency	—	3 2 1	MHz MHz MHz	4.5V ≤ V$_{CC}$ < 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
A2	T$_{CKH}$	Clock high time	200 250 450	—	ns ns ns	4.5V ≤ V$_{CC}$ < 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
A3	T$_{CKL}$	Clock low time	100 200 450	—	ns ns ns	4.5V ≤ V$_{CC}$ < 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
A4	T$_{CSS}$	Chip Select setup time	50 100 250	—	ns ns ns	4.5V ≤ V$_{CC}$ < 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
A5	T$_{CSH}$	Chip Select hold time	0	—	ns	1.8V ≤ V$_{CC}$ < 5.5V
A6	T$_{CSL}$	Chip Select low time	250	—	ns	1.8V ≤ V$_{CC}$ < 5.5V
A7	T$_{DIS}$	Data input setup time	50 100 250	—	ns ns ns	4.5V ≤ V$_{CC}$ < 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
A8	T$_{DIH}$	Data input hold time	50 100 250	—	ns ns ns	4.5V ≤ V$_{CC}$ < 5.5V 2.5V ≤ V$_{CC}$ < 4.5V 1.8V ≤ V$_{CC}$ < 2.5V
A9	T$_{PD}$	Data output delay time	—	100 250 400	ns ns ns	4.5V ≤ V$_{CC}$ < 5.5V, CL = 100 pF 2.5V ≤ V$_{CC}$ < 4.5V, CL = 100 pF 1.8V ≤ V$_{CC}$ < 2.5V, CL = 100 pF
A10	T$_{CZ}$	Data output disable time	—	100 200	ns ns	4.5V ≤ V$_{CC}$ < 5.5V, **(Note 1)** 1.8V ≤ V$_{CC}$ < 4.5V, **(Note 1)**
A11	T$_{SV}$	Status valid time	—	200 300 500	ns ns ns	4.5V ≤ V$_{CC}$ < 5.5V, CL = 100 pF 2.5V ≤ V$_{CC}$ < 4.5V, CL = 100 pF 1.8V ≤ V$_{CC}$ < 2.5V, CL = 100 pF
A12	T$_{WC}$	Program cycle time	—	5	ms	Erase/Write mode (AA and LC versions)
A13	T$_{WC}$		—	2	ms	Erase/Write mode (93C versions)
A14	T$_{EC}$		—	6	ms	ERAL mode, 4.5V ≤ V$_{CC}$ ≤ 5.5V
A15	T$_{WL}$		—	15	ms	WRAL mode, 4.5V ≤ V$_{CC}$ ≤ 5.5V
A16	—	Endurance	1M	—	cycles	25°C, V$_{CC}$ = 5.0V, **(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This application is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which may be obtained from Microchip's web site at www.microchip.com.

FIGURE 1-1: **SYNCHRONOUS DATA TIMING**

Note: T_{SV} is relative to CS.
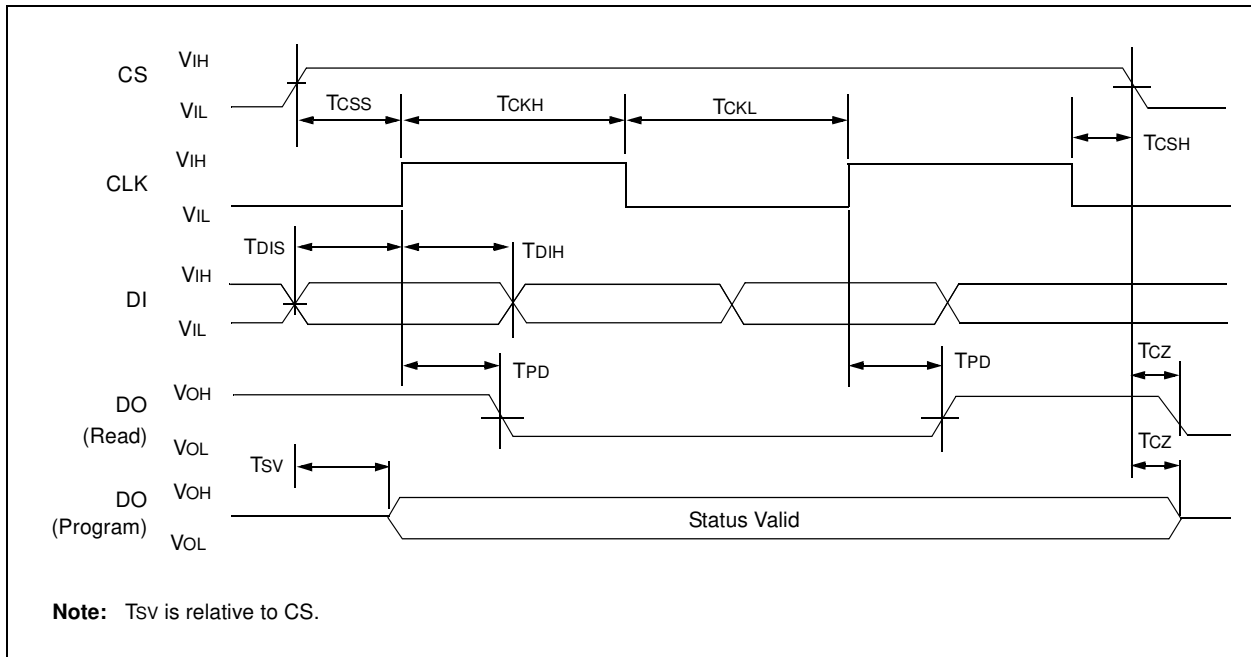
TABLE 1-3: **INSTRUCTION SET FOR X16 ORGANIZATION (93XX86B OR 93XX86C WITH ORG = 1)**

Instruction	SB	Opcode	Address											Data In	Data Out	Req. CLK Cycles
READ	1	10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		—	D15-D0	29
EWEN	1	00	1	1	X	X	X	X	X	X	X	X		—	HighZ	13
ERASE	1	11	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		—	(RDY/$\overline{BSY}$)	13
ERAL	1	00	1	0	X	X	X	X	X	X	X	X		—	(RDY/$\overline{BSY}$)	13
WRITE	1	01	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		D15-D0	(RDY/$\overline{BSY}$)	29
WRAL	1	00	0	1	X	X	X	X	X	X	X	X		D15-D0	(RDY/$\overline{BSY}$)	29
EWDS	1	00	0	0	X	X	X	X	X	X	X	X		—	High-Z	13

TABLE 1-4: **INSTRUCTION SET FOR X8 ORGANIZATION (93XX86A OR 93XX86C WITH ORG = 0)**

Instruction	SB	Opcode	Address											Data In	Data Out	Req. CLK Cycles
READ	1	10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7-D0	22
EWEN	1	00	1	1	X	X	X	X	X	X	X	X	X	—	High-Z	14
ERASE	1	11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	14
ERAL	1	00	1	0	X	X	X	X	X	X	X	X	X	—	(RDY/$\overline{BSY}$)	14
WRITE	1	01	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7-D0	(RDY/$\overline{BSY}$)	22
WRAL	1	00	0	1	X	X	X	X	X	X	X	X	X	D7-D0	(RDY/$\overline{BSY}$)	22
EWDS	1	00	0	0	X	X	X	X	X	X	X	X	X	—	High-Z	14

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

2.0   FUNCTIONAL DESCRIPTION

When the ORG pin (93XX86C) is connected to V_{CC}, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a High-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the High-Z state on the falling edge of CS.

2.1   Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a Start condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

Note:	When preparing to transmit an instruction, either the CLK or DI signal levels must be at a logic low as CS is toggled active high.

2.2   Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of the driver, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

2.3   Data Protection

All modes of operation are inhibited when V_{CC} is below a typical voltage of 1.5V for '93AA' and '93LC' devices or 3.8V for '93C' devices.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

Note:	For added protection, an EWDS command should be performed after every write operation and an external 10 kΩ pull-down protection resistor should be added to the CS pin.

After power-up the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before the initial ERASE or WRITE instruction can be executed.

Note:	To prevent accidental writes to the array in the 93XX86C devices, set the PE pin to a logic low.

Block Diagram

*ORG and PE inputs are not available on A/B devices.
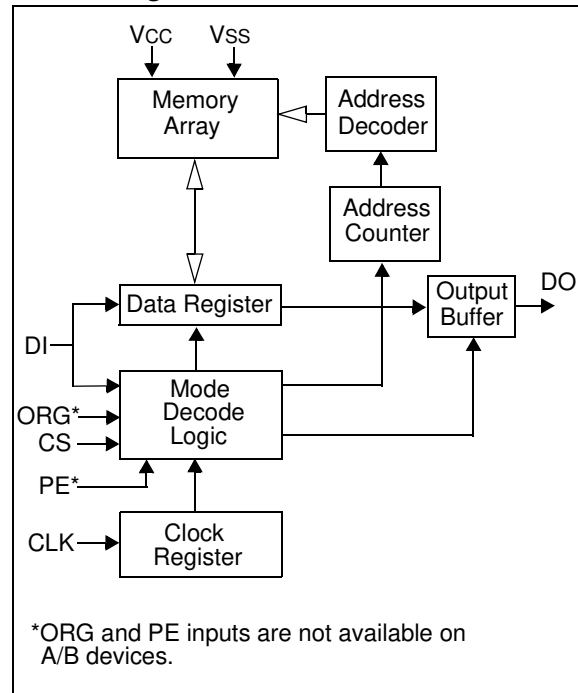
2.4   Erase

The `ERASE` instruction forces all data bits of the specified address to the logical '1' state. The rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (T$_{CSL}$). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been erased and the device is ready for another instruction.

> **Note:** After the Erase cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

FIGURE 2-1:   ERASE TIMING
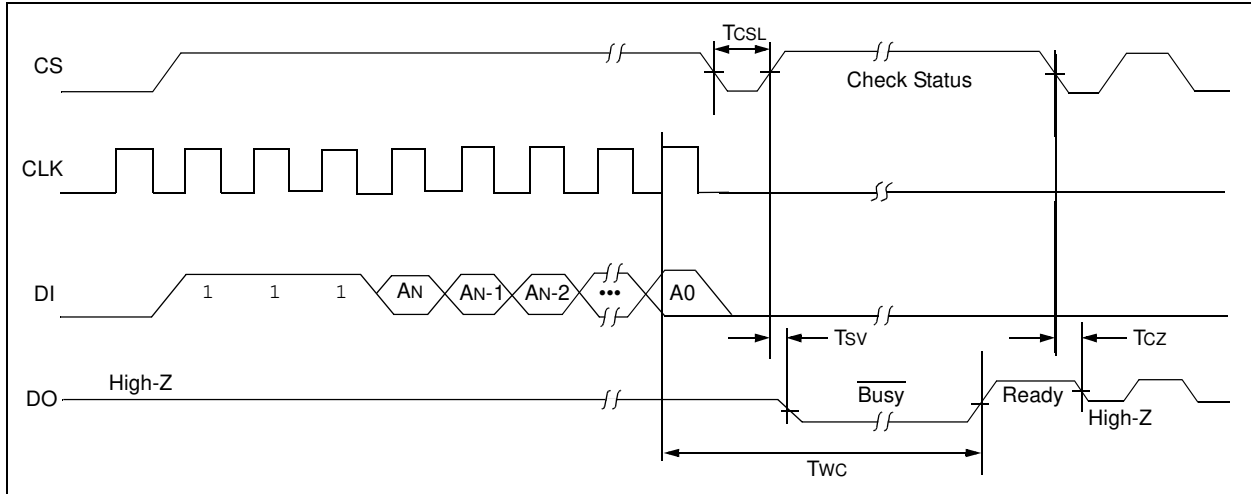
2.5   Erase All (ERAL)

The Erase All (`ERAL`) instruction will erase the entire memory array to the logical '1' state. The ERAL cycle is identical to the erase cycle, except for the different opcode. The ERAL cycle is completely self-timed. The rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device, if CS is brought high after a minimum of 250 ns low (T$_{CSL}$).

> **Note:** After the `ERAL` command is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

V$_{CC}$ must be ≥4.5V for proper operation of ERAL.

FIGURE 2-2:   ERAL TIMING
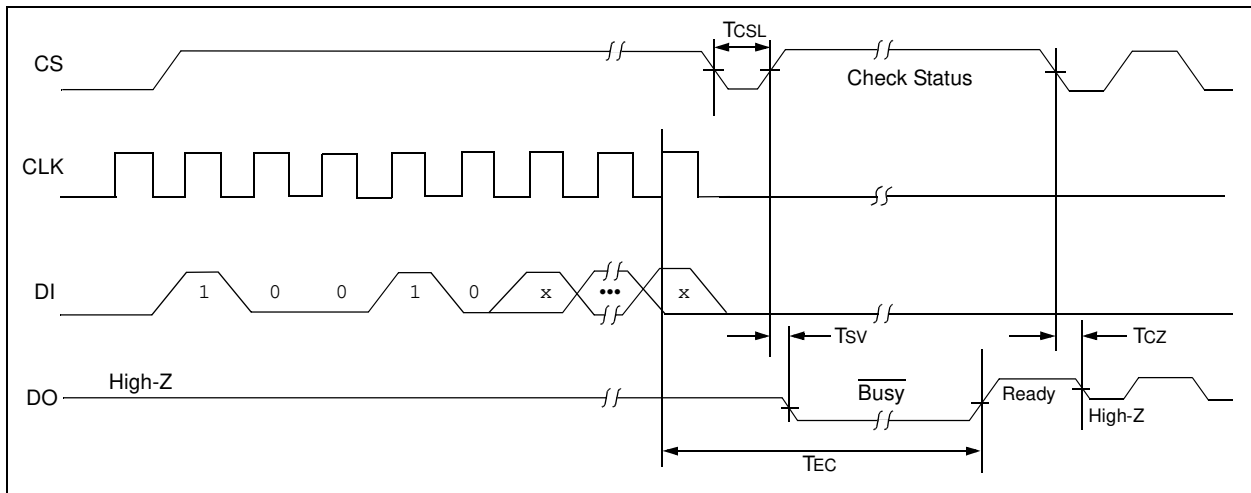
93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

2.6 Erase/Write Disable and Enable (EWDS/EWEN)

The 93XX86A/B/C powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction.

Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

FIGURE 2-3: EWDS TIMING
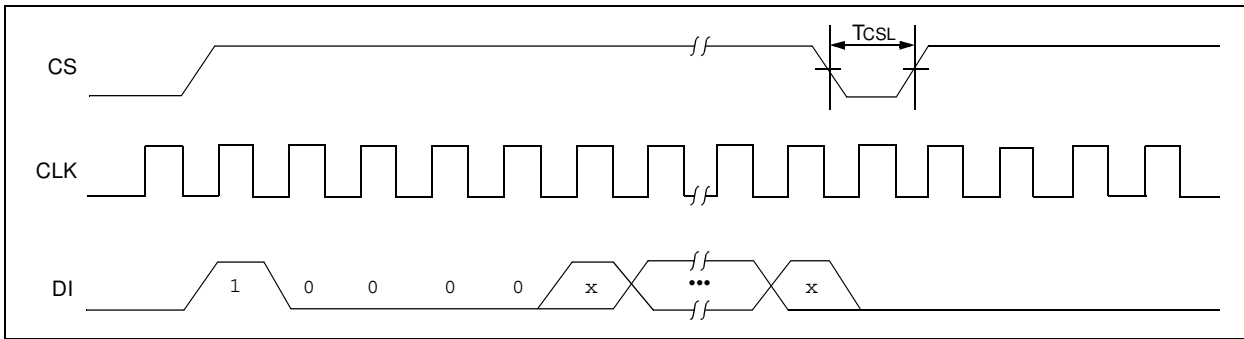
FIGURE 2-4: EWEN TIMING
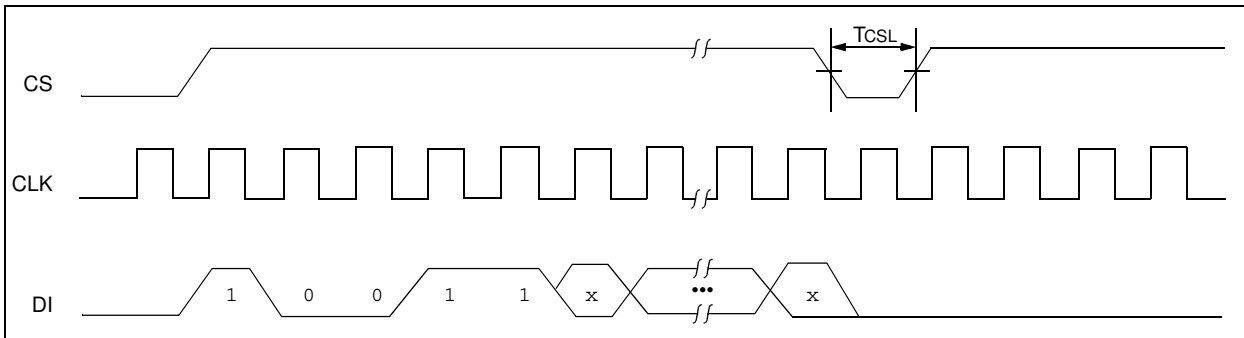
2.7 Read

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (If ORG pin is low or A-Version devices) or 16-bit (If ORG pin is high or B-version devices) output string.

The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 2-5: READ TIMING
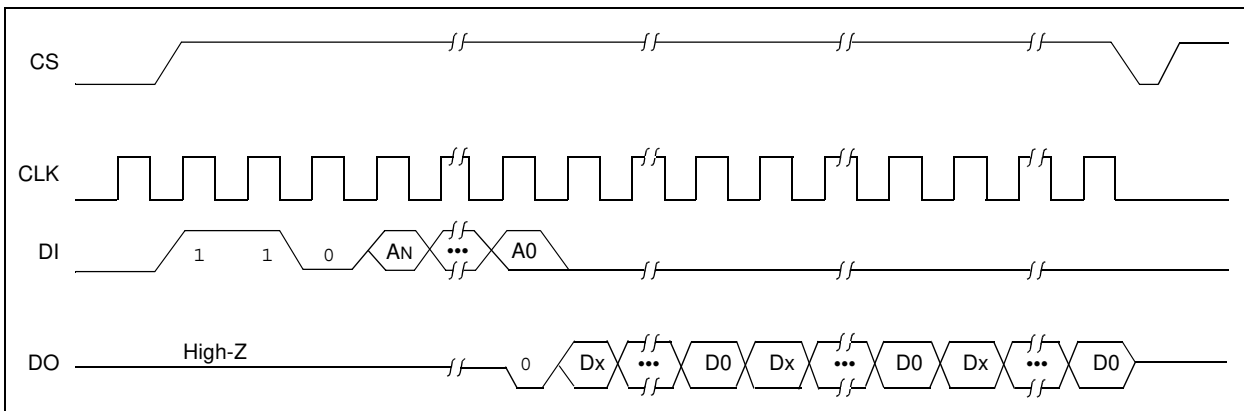
2.8   Write

The `WRITE` instruction is followed by 8 bits (If ORG is low or A-version devices) or 16 bits (If ORG pin is high or B-version devices) of data which are written into the specified address. The self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device, if CS is brought high after a minimum of 250 ns low (T$_{CSL}$). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

> **Note:** The write sequence requires a logic high signal on the PE pin prior to the rising edge of the last data bit.

> **Note:** After the Write cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO

FIGURE 2-6:   WRITE TIMING
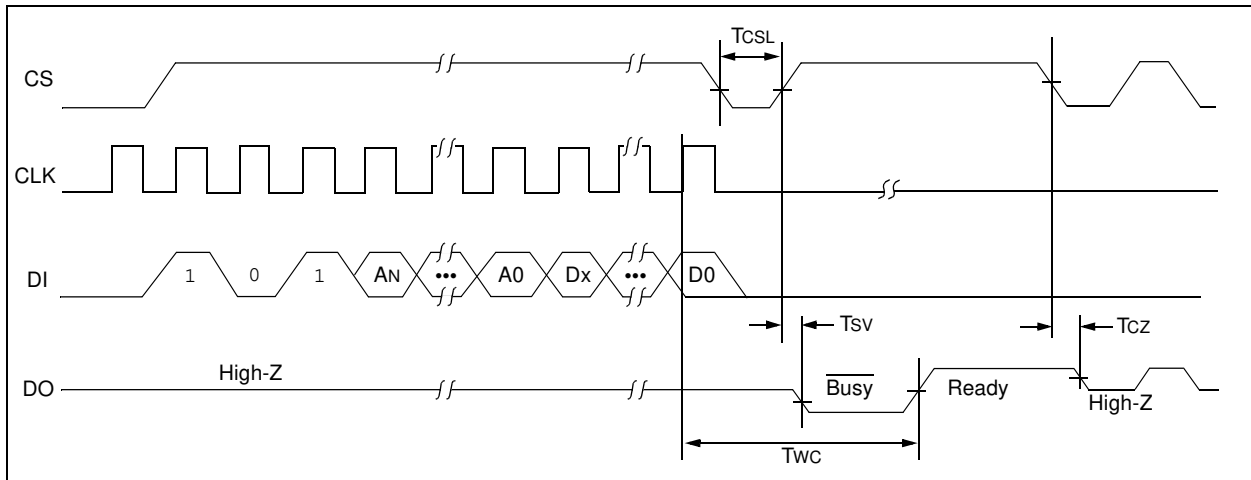
2.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (T$_{CSL}$).

Note:	The write sequence requires a logic high signal on the PE pin prior to the rising edge of the last data bit.

Note:	After the Write All cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{\text{Busy}}$ status from DO.

V$_{CC}$ must be ≥4.5V for proper operation of WRAL.

FIGURE 2-7: WRAL TIMING
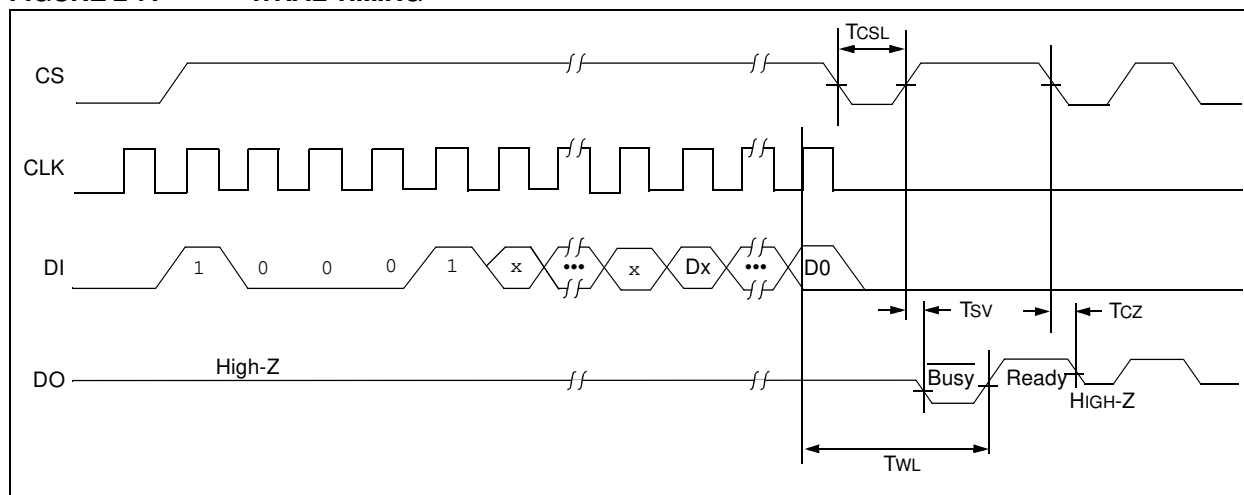
93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN DESCRIPTIONS

Name	PDIP	SOIC	TSSOP	MSOP	DFN[1]	TDFN[1]	SOT-23	Function
CS	1	1	1	1	1	1	5	Chip Select
CLK	2	2	2	2	2	2	4	Serial Clock
DI	3	3	3	3	3	3	3	Data In
DO	4	4	4	4	4	4	1	Data Out
V_{SS}	5	5	5	5	5	5	2	Ground
ORG	6	6	6	6	6	6	—	Organization/93XX86C only
PE	7	7	7	7	7	7	—	Program Enable/93XX86C only
V_{CC}	8	8	8	8	8	8	6	Power Supply

Note 1: The exposed pad on the DFN/TDFN package may be connected to Vss or left floating.

3.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (T_{CSL}) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (T_{CKH}) and clock low time (T_{CKL}). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "don't care" if CS is low (device deselected). If CS is high, but the Start condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed write (i.e., auto erase/write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed. CLK and DI then become "don't care" inputs waiting for a new Start condition to be detected.

3.3 Data In (DI)

Data In (DI) is used to clock in a Start bit, opcode, address and data, synchronously with the CLK input.

3.4 Data Out (DO)

Data Out (DO) is used in the Read mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK).

This pin also provides Ready/$\overline{Busy}$ status information during erase and write cycles. Ready/$\overline{Busy}$ status information is available on the DO pin if CS is brought high after being low for minimum Chip Select low time (T_{CSL}), and an erase or write operation has been initiated.

The Status signal is not available on DO if CS is held low during the entire erase or write cycle. In this case, DO is in the High-Z mode. If status is checked after the erase/write cycle, the data line will be high to indicate the device is ready.

> **Note:** After a programming cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/$\overline{Busy}$ status from DO.

3.5 Organization (ORG)

When the ORG pin is connected to V_{CC} or logic high, the (x16) memory organization is selected. When the ORG pin is tied to V_{SS} or logic low, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

93XX86A devices are always (x8) organization and 93XX86B devices are always (x16) organization.
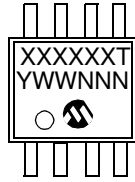
3.6   Program Enable (PE)

This pin allows the user to enable or disable the ability to write data to the memory array. If the PE pin is tied to V_{CC}, the device can be programmed. If the PE pin is tied to V_{SS}, programming will be inhibited. This pin cannot be floated, it must be tied to V_{CC} or V_{SS}. PE is not available on 93XX86A or 93XX86B. On those devices, programming is always enabled.

4.0   PACKAGING INFORMATION

4.1   Package Marking Information

8-Lead MSOP (150 mil)   Example:
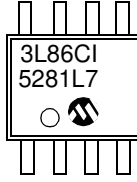
```
XXXXXXT        3L86CI
YWWNNN         5281L7
   ○ Ⓜ            ○ Ⓜ
```

6-Lead SOT-23   Example:

```
XXNN           5EL7
  ○              ○
```

8-Lead PDIP   Example:

```
XXXXXXXX       93LC86C
T/XXXNNN       I/P  (e3) 1L7
  Ⓜ YYWW        Ⓜ 0528
○              ○
```

8-Lead SOIC   Example:

```
XXXXXXXT       93LC86CI
XXXXYYWW       SN (e3) 0528
   Ⓜ NNN        Ⓜ 1L7
○               ○
```

8-Lead TSSOP   Example:

```
  ○ XXXX        ○ L86C
    TYWW          I528
  Ⓜ NNN         Ⓜ 1L7
```
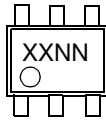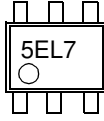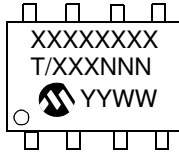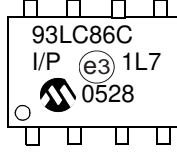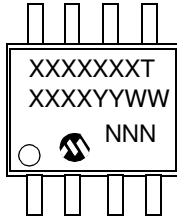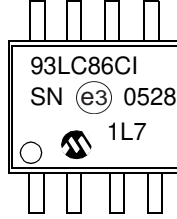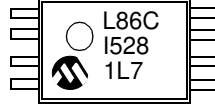
8-Lead 2x3 DFN   Example:

```
XXX            3E4
YWW            528
NN             L7
•              •
```
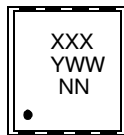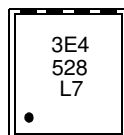
8-Lead 2x3 TDFN   Example:

```
XXX            EE4
YWW            528
NN             L7
•              •
```
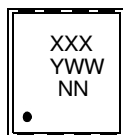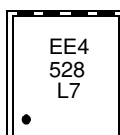
Part Number	1st Line Marking Codes							
	TSSOP	MSOP	SOT-23		DFN		TDFN	
			I Temp.	E Temp.	I Temp.	E Temp.	I Temp.	E Temp.
93AA86A	A86A	3A86AT	5BNN	—	—	—	—	—
93AA86B	A86B	3A86BT	5LNN	—	—	—	—	—
93AA86C	A86C	3A86CT	—	—	3E1	—	EE1	—
93LC86A	L86A	3L86AT	5ENN	5FNN	—	—	—	—
93LC86B	L86B	3L86BT	5PNN	5RNN	—	—	—	—
93LC86C	L86C	3L86CT	—	—	3E4	—	EE4	EE5
93C86A	C86A	3C86AT	5HNN	5JNN	—	—	—	—
93C86B	C86B	3C86BT	5TNN	5UNN	—	—	—	—
93C86C	C86C	3C86CT	—	—	3E7	—	EE7	EE8

Note: T = Temperature grade (I, E)
NN = Alphanumeric traceability code

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator
(e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

TOP VIEW

SIDE VIEW

SEATING PLANE

SEE DETAIL C

END VIEW
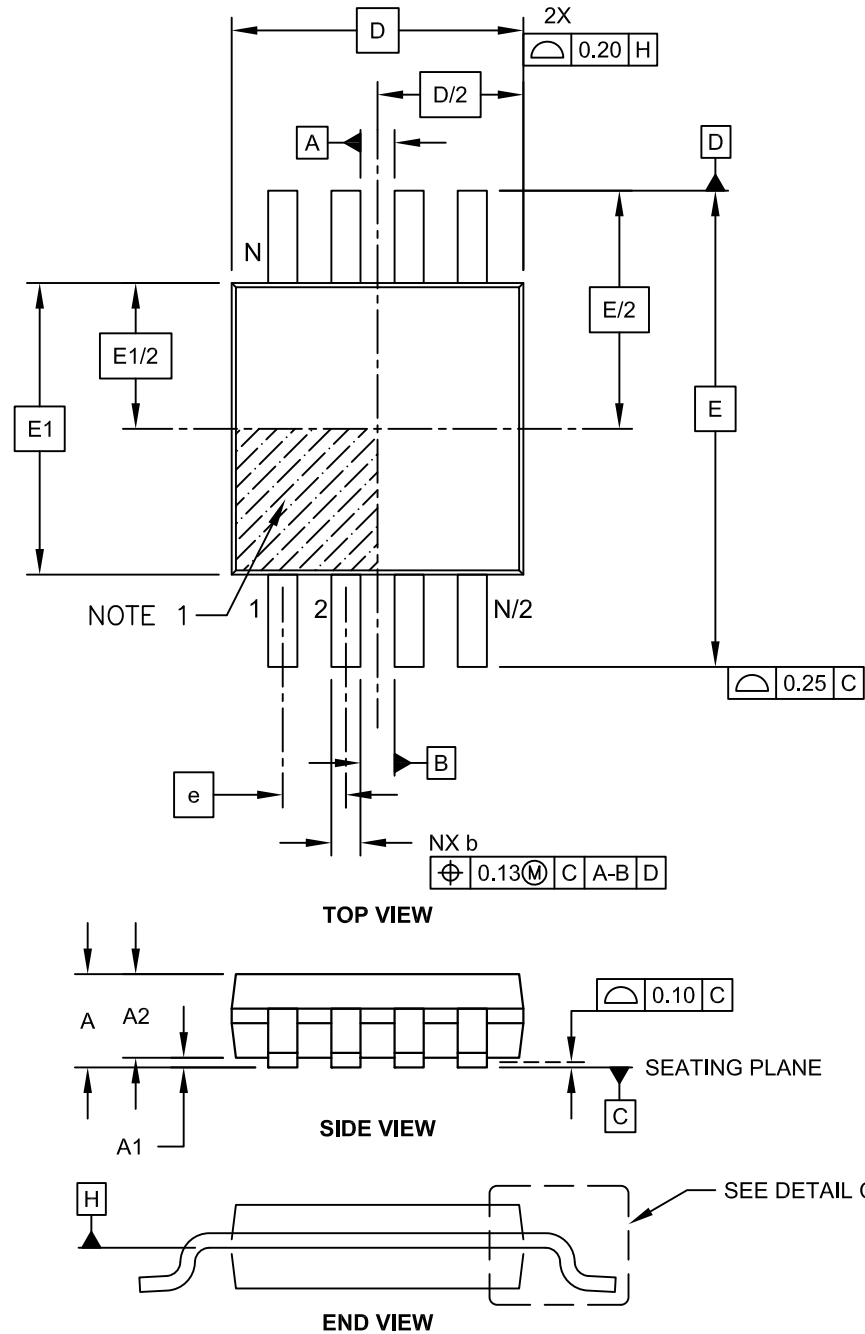
Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

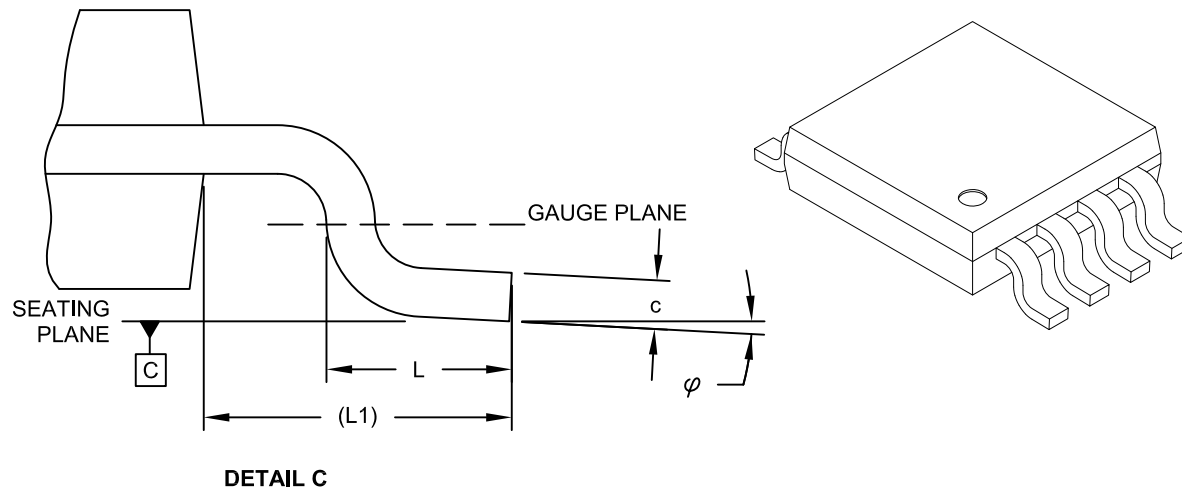| Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

DETAIL C

	Units		MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
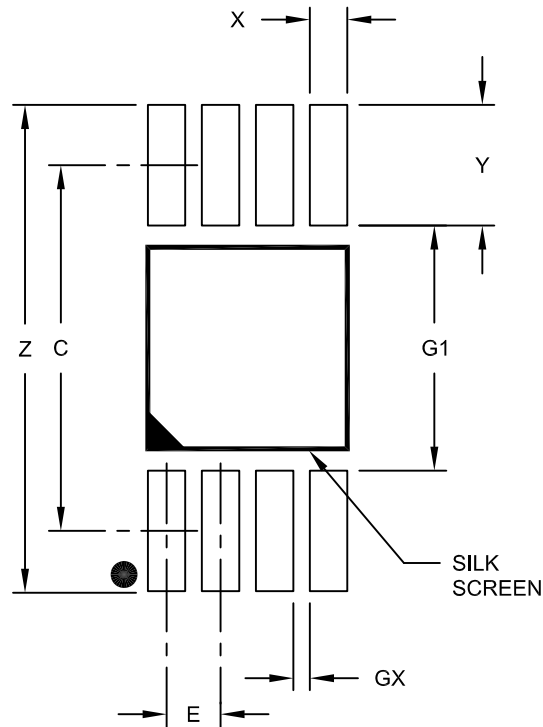   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:
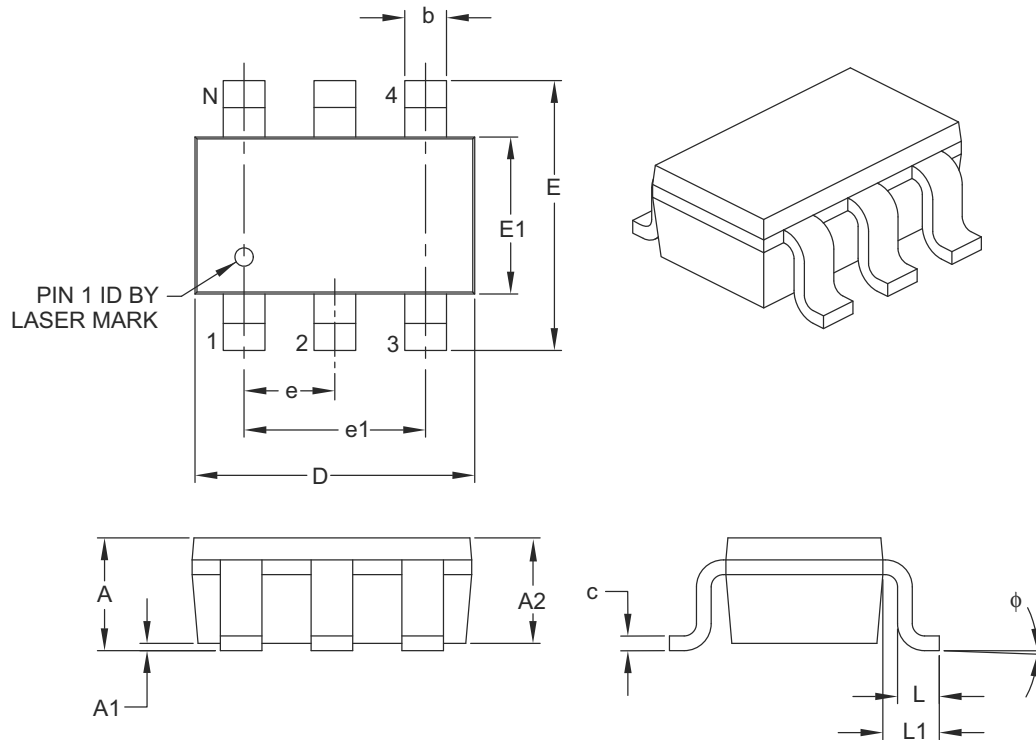1. Dimensioning and tolerancing per ASME Y14.5M
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	φ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
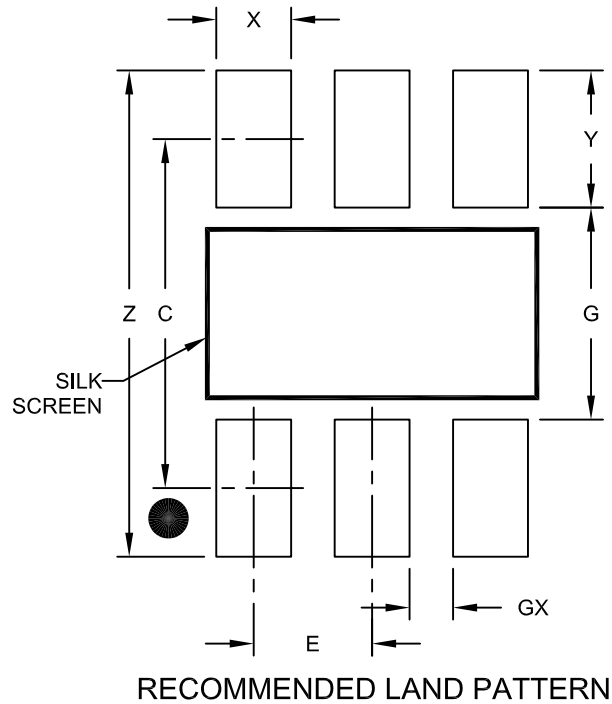2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
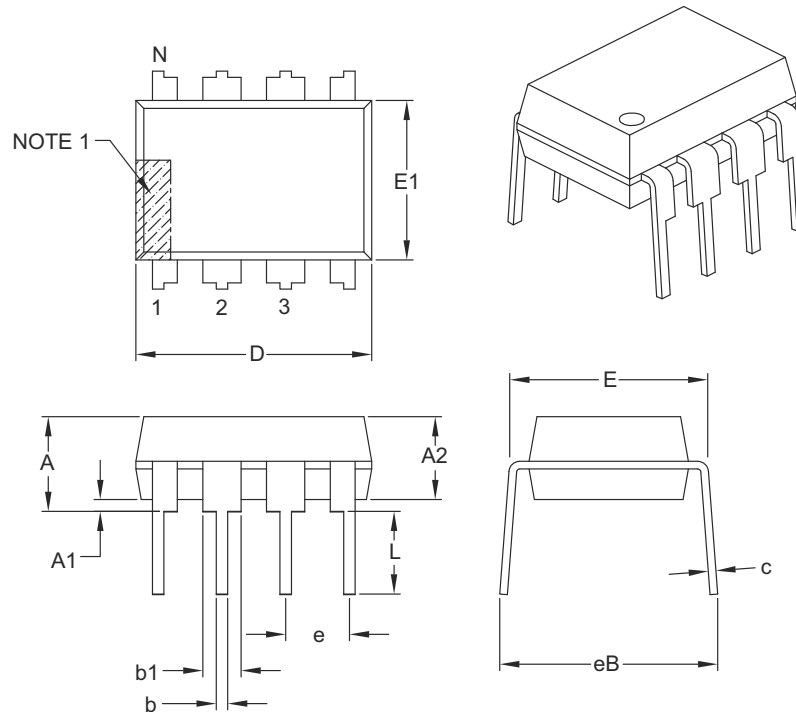
Microchip Technology Drawing No. C04-2028A

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

|	Units		INCHES		
	Dimension Limits		MIN	NOM	MAX
Number of Pins	N			8	
Pitch	e			.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

VIEW A-A
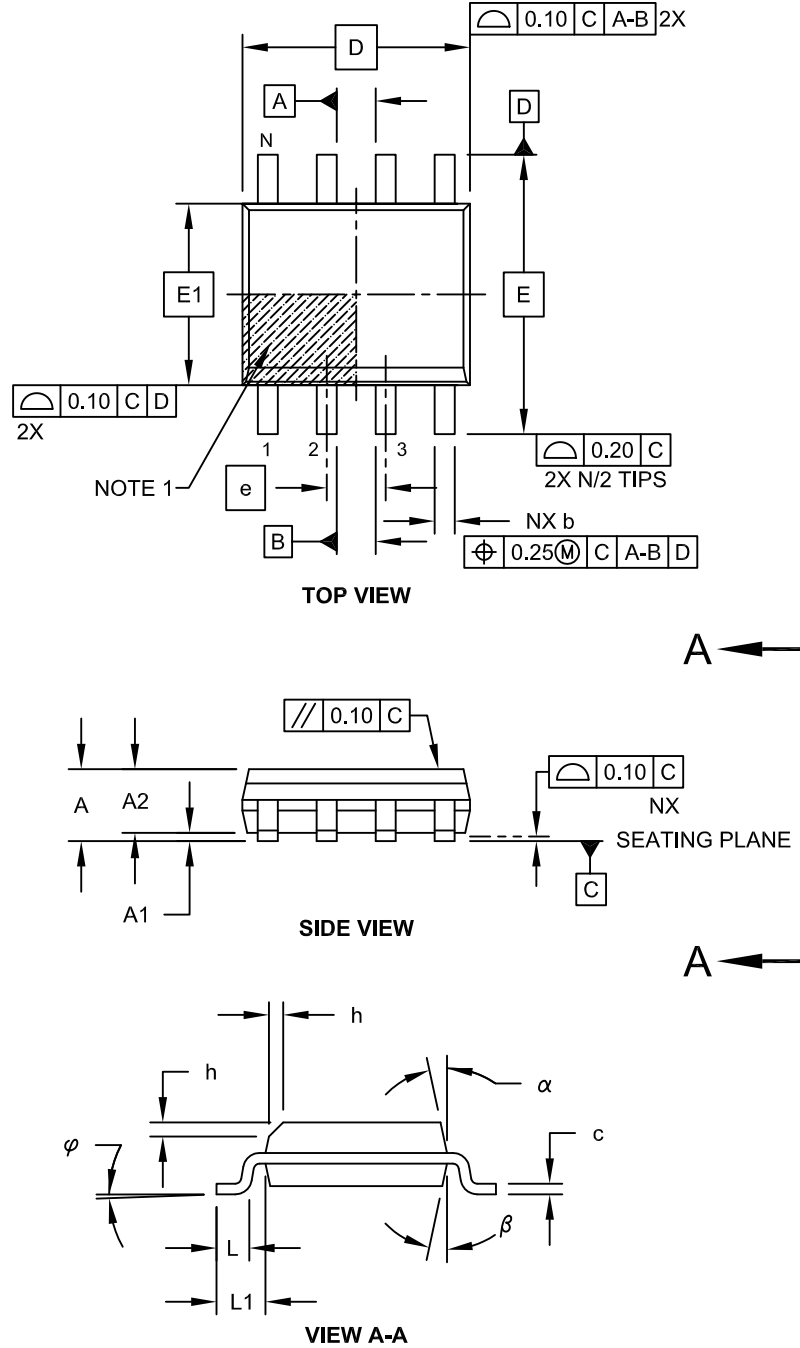
Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

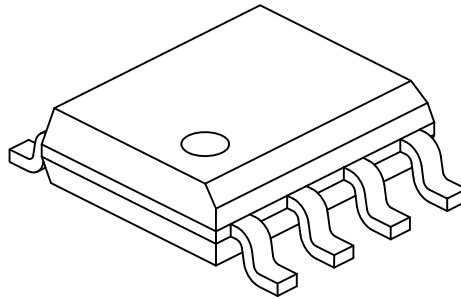| Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

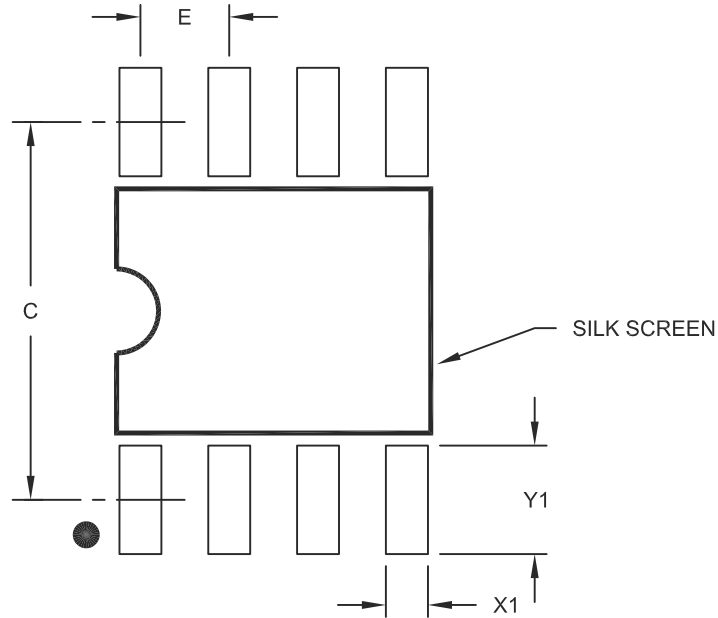BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
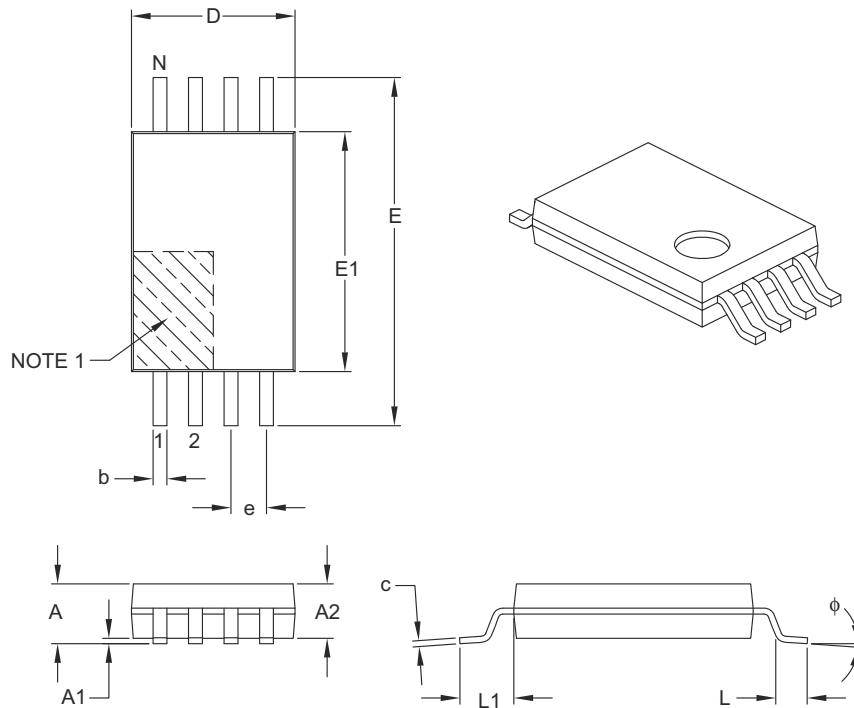
	Units		MILLIMETERS		
	Dimension Limits		MIN	NOM	MAX
Number of Pins	N			8	
Pitch	e			0.65 BSC	
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.80	1.00	1.05
Standoff	A1		0.05	–	0.15
Overall Width	E			6.40 BSC	
Molded Package Width	E1		4.30	4.40	4.50
Molded Package Length	D		2.90	3.00	3.10
Foot Length	L		0.45	0.60	0.75
Footprint	L1			1.00 REF	
Foot Angle	φ		0°	–	8°
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

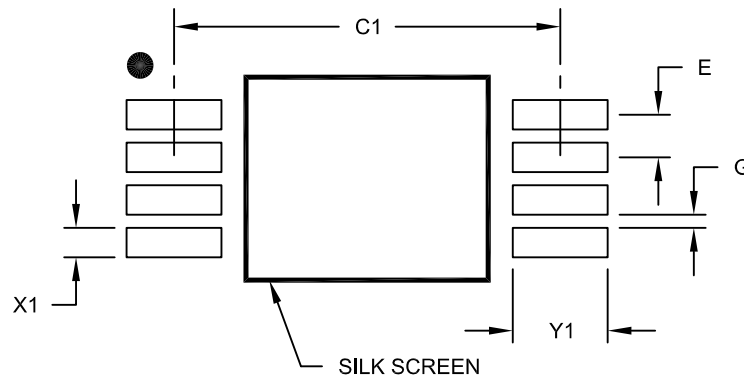   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A