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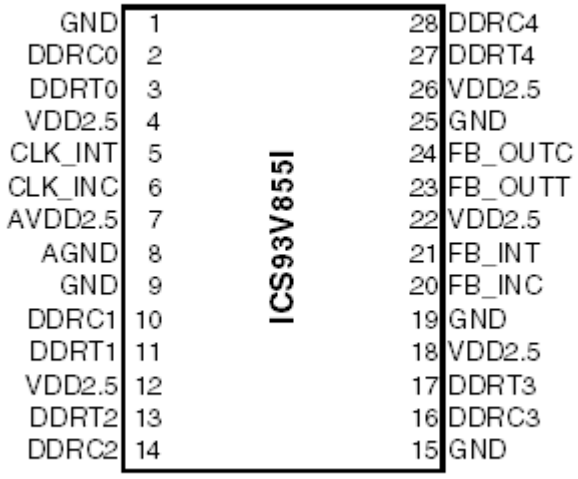
DDR Phase Lock Loop Clock Driver

Recommended Application:
DDR Clock Driver

- Low skew, low jitter PLL clock driver
- External feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- With bypass mode mux
- Operating frequency 60 to 170 MHz
- Operating Temperature –45°C to +85°C

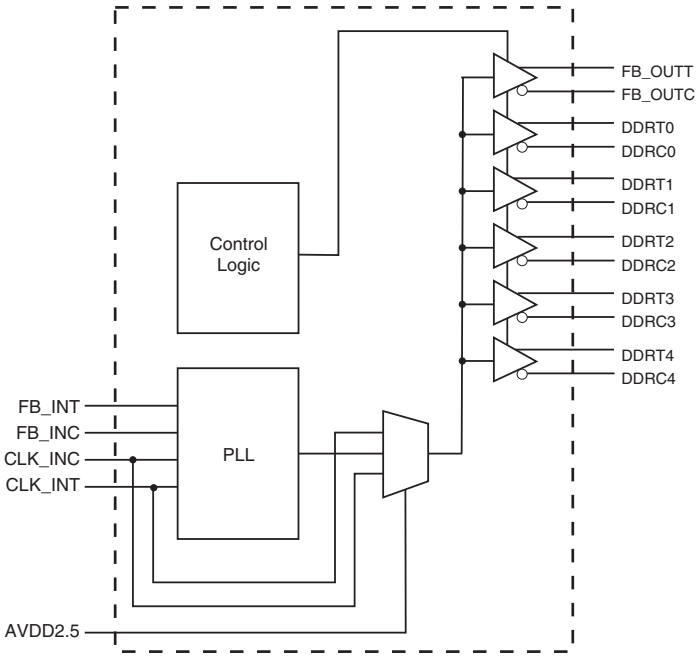
- CYCLE - CYCLE jitter:<75ps
- OUTPUT - OUTPUT skew: <60ps
- Output Rise and Fall Time: 650ps - 950ps

Pin Configuration



28-Pin 4.4mm TSSOP

Block Diagram



Functionality

INPUTS			OUTPUTS				PLL State
AVDD	CLK_INT	CLK_INC	DDRT	DDRC	FB_OUTT	FB_OUTC	
GND	L	H	L	H	L	H	Bypassed/Off
GND	H	L	H	L	H	L	Bypassed/Off
2.5V (nom)	L	H	L	H	L	H	On
2.5V (nom)	H	L	H	L	H	L	On
2.5V (nom)	<20 MHz	<20 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Off

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	GND	PWR	Ground pin.
2	DDRC0	OUT	"Complimentary" Clock of differential pair output.
3	DDRT0	OUT	"True" Clock of differential pair output.
4	VDD2.5	PWR	Power supply, nominal 2.5V
5	CLK_INT	IN	"True" reference clock input.
6	CLK_INC	IN	"Complimentary" reference clock input.
7	AVDD2.5	PWR	2.5V Analog Power pin for Core PLL
8	AGND	PWR	Analog Ground pin for Core PLL
9	GND	PWR	Ground pin.
10	DDRC1	OUT	"Complimentary" Clock of differential pair output.
11	DDRT1	OUT	"True" Clock of differential pair output.
12	VDD2.5	PWR	Power supply, nominal 2.5V
13	DDRT2	OUT	"True" Clock of differential pair output.
14	DDRC2	OUT	"Complimentary" Clock of differential pair output.
15	GND	PWR	Ground pin.
16	DDRC3	OUT	"Complimentary" Clock of differential pair output.
17	DDRT3	OUT	"True" Clock of differential pair output.
18	VDD2.5	PWR	Power supply, nominal 2.5V
19	GND	PWR	Ground pin.
20	FB_INC	IN	Complement single-ended feedback input, provides feedback signal to internal PLL for synchronization with CLK_INT to eliminate phase error.
21	FB_INT	IN	True single-ended feedback input, provides feedback signal to internal PLL for synchronization with CLK_INT to eliminate phase error.
22	VDD2.5	PWR	Power supply, nominal 2.5V
23	FB_OUTT	OUT	True single-ended feedback output, dedicated external feedback. It switches at the same frequency as other DDR outputs, This output must be connect to FB_INT.
24	FB_OUTC	OUT	Complement single-ended feedback output, dedicated external feedback. It switches at the same frequency as other DDR outputs, This output must be connect to FB_INC.
25	GND	PWR	Ground pin.
26	VDD2.5	PWR	Power supply, nominal 2.5V
27	DDRT4	OUT	"True" Clock of differential pair output.
28	DDRC4	OUT	"Complimentary" Clock of differential pair output.

Absolute Maximum Ratings

Supply Voltage: (VDD & AVDD) . . . . . -0.5V to 3.6V

(VDDI) . . . . . -0.5V to 4.6V

Logic Inputs: VI . . . . . V_{SS} –0.5 V to V_{DD} +0.5 V

Logic Outputs: VO . . . . . V_{SS} –0.5 V to V_{DD} +0.5 V

Input clamp current: IIK (VI < 0 or VI > VDD) +/- 50mA

Output clamp current: IOK (VO < 0 or VO > VDD) +/- 50mA

Continuous output current: IO (VO = 0 to VDD) +/- 50mA

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

TA = -45°C to +85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND	5			µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	C_L = 0pf, R_L = 120 ohms			250	mA
	I_{DDPD}	C_L = 0pf, R_L = 120 ohms			100	µA
Output High Current	I_{OH}	V_{DD} = 2.3V, V_{OUT} = 1V	-18			mA
Output Low Current	I_{OL}	V_{DD} = 2.3V, V_{OUT} = 1.2V	26			mA
High Impedance Output Current	I_{OZ}	V_{DD}=2.7V, Vout=V_{DD} or GND			±10	µA
Input Clamp Voltage	V_{IK}	Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1 mA	V_{DD} - 0.1			V
		V_{DD} = 2.3V, I_{OH} = -12 mA	1.7			V
Low-level output voltage	V_{OL}	V_{DD} = min to max I_{OL}=1 mA			0.1	
		V_{DD} = 2.3V I_{OH}=12 mA			0.6	V
Input Capacitance[1]	C_{IN}	VI = V_{DD} or GND		3		pF
Output Capacitance[1]	C_{OUT}	VI = V_{DD} or GND		3		pF

[1]Guaranteed by design and characterization, not 100% tested in production.

DC Electrical Characteristics

T_A = -45°C to +85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DDQ}, A_{VDD}		2.3	2.5	2.7	V
Low level input voltage	V_{IL}	CLK_INT, CLK_INC, FB_INC, FB_INT		0.4	V_{DD}/2 - 0.18	V
High level input voltage	V_{IH}	CLK_INT, CLK_INC, FB_INC, FB_INT	V_{DD}/2 + 0.18	2.1		V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DD} + 0.3	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLK_INT, CLK_INC, FB_INC, FB_INT	0.36		V_{DD} + 0.6	V
		AC - CLK_INT, CLK_INC, FB_INC, FB_INT	0.7		V_{DD} + 0.6	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DD}/2 - 0.15		V_{DD}/2 + 0.15	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DD}/2 - 0.2	V_{DD}/2	V_{DD}/2 + 0.2	V
Operating free-air temperature	T_A		-45		85	°C

Notes:

1 Unused inputs must be held high or low to prevent them from floating.

2 DC input signal voltage specifies the allowable DC excursion of differential input.

3 Differential inputs signal voltages specifies the differential voltage [VT-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.

4 Differential cross-point voltage is expected to track variations of VDD and is the voltage at which the differential signal must be crossing.

Switching Characteristics

T_A = -45°C to +85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Max clock frequency[3]	$freq_{op}$		33		233	MHz
Application Frequency Range[3]	$freq_{App}$		60		170	MHz
Input clock duty cycle	d_{tin}		40		60	%
Output clock slew rate	$t_{sl(o)}$		1		2	v/ns
CLK stabilization	T_{STAB}				100	µs
Low-to high level propagation delay time	t_{PLH}[1]	CLK_IN to any output		5.5		ns
High-to low level propagation delay time	t_{PHL}[1]	CLK_IN to any output		5.5		ns
Output enable time	t_{en}	PD# to any output		5		ns
Output disable time	t_{dis}	PD# to any output		5		ns
Period jitter	$t_{jit(per)}$	Over the application frequency range	-75		75	ps
Half-period jitter	$t_{jit(hper)}$		-100		100	ps
Input clock slew rate	$t_{sl(I)}$		1		2	v/ns
Cycle to Cycle Jitter	t_{cyc}-t_{cyc}		-75		75	ps
Phase error[4]	$t_{(phase\ error)}$		-50		50	ps
Output to Output Skew	t_{skew}			40	60	ps
Rise Time, Fall Time	t_r, t_f	Load = 120ϕ/16pF	650	800	950	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=twH/tc, were the cycle (tc) decreases as the frequency goes up.
3. Switching characteristics are guaranteed for application frequency range. The PLL Locks over the Max Clock Frequency range, but the device doe not necessarily meet other timing parameters.
4. Does not include jitter.

Parameter Measurement Information

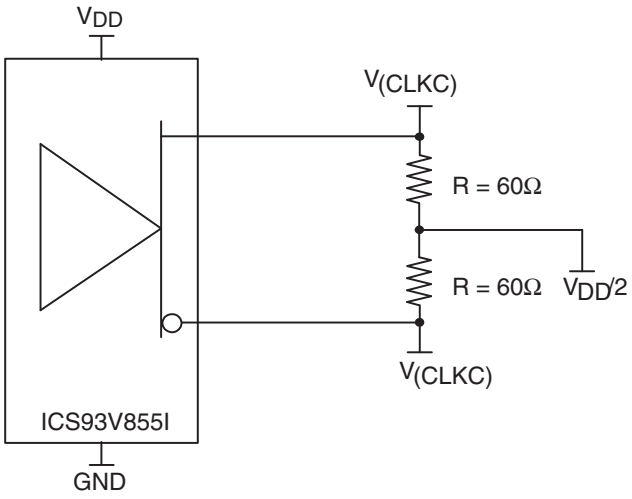
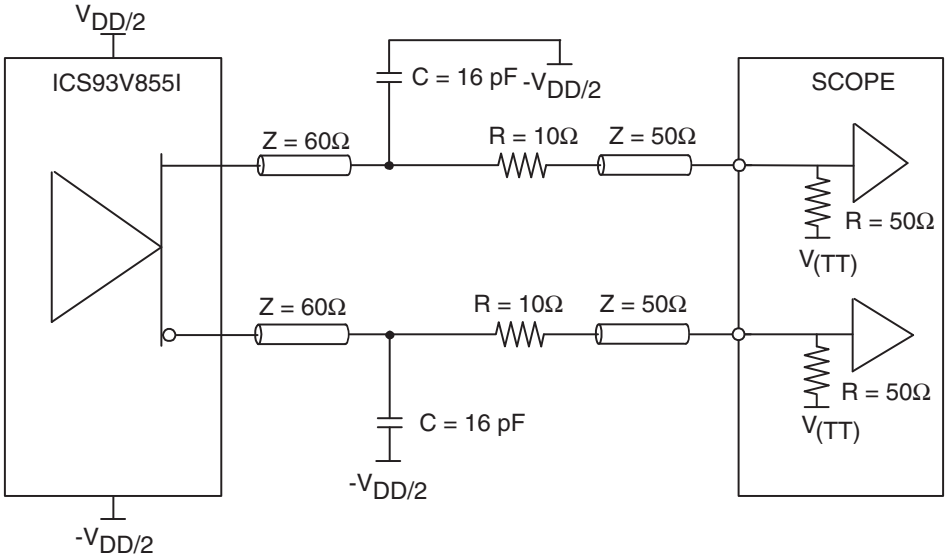
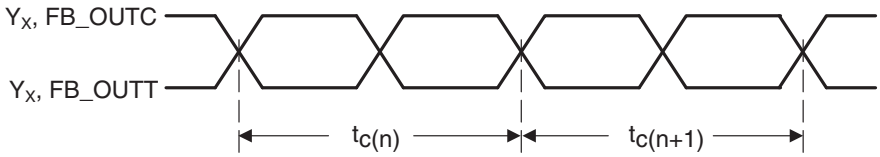


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)} = GND$

Figure 2. Output Load Test Circuit



$$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

Parameter Measurement Information

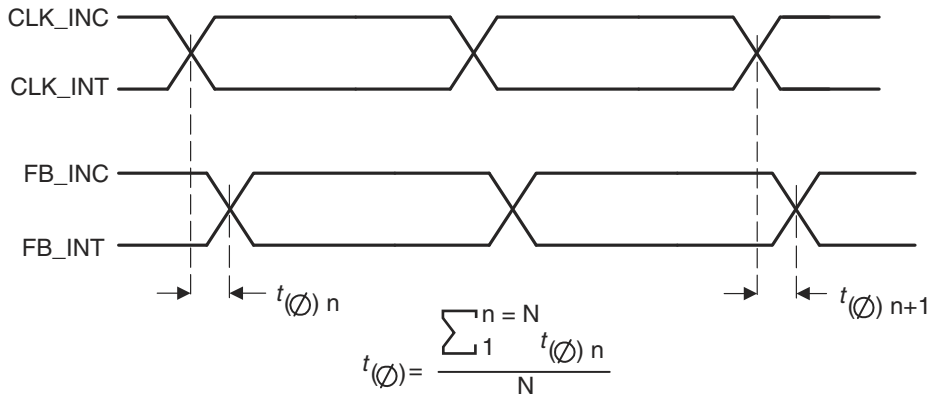


Figure 4. Static Phase Offset

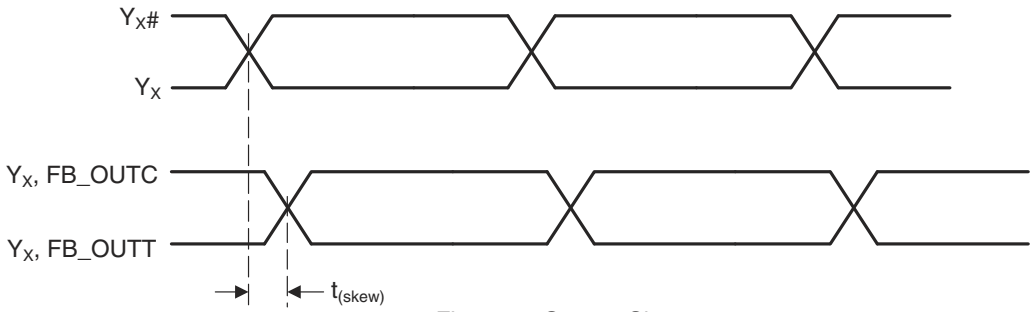


Figure 5. Output Skew

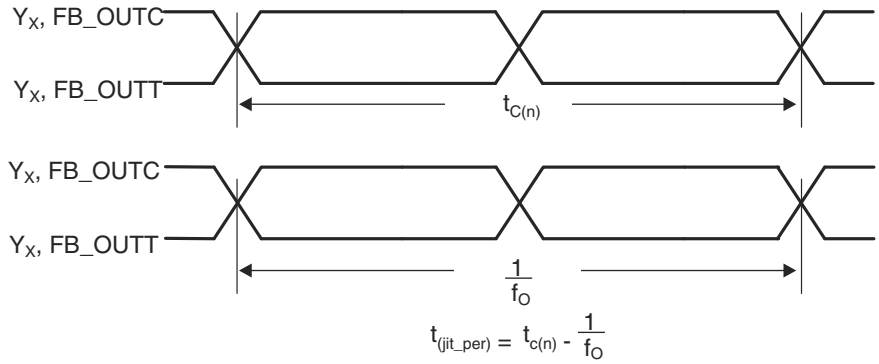


Figure 6. Period Jitter

Parameter Measurement Information

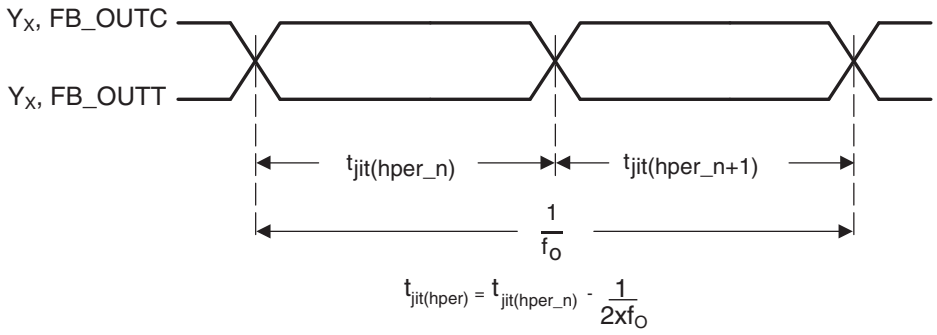


Figure 7. Half-Period Jitter

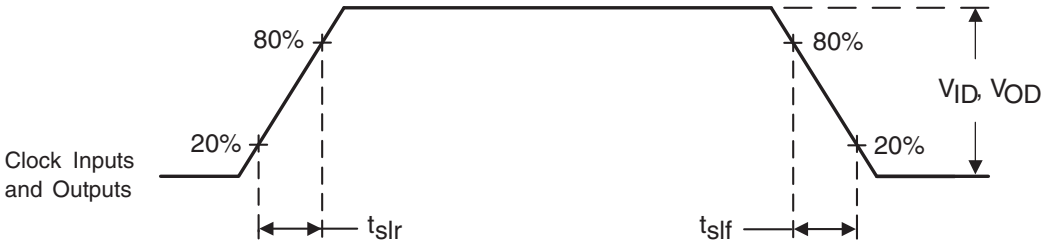
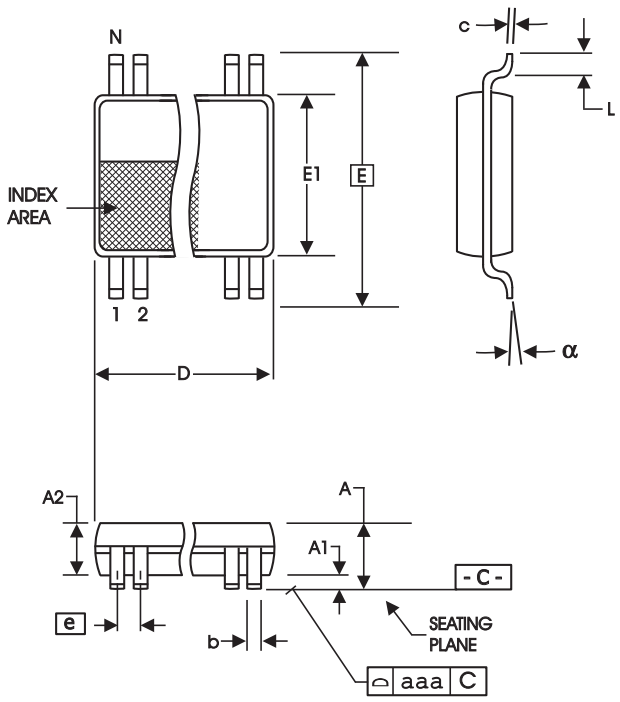


Figure 8. Input and Output Slew Rates



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153
10-0035

4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 Inch)

Ordering Information

93V855yGILF-T

Example:

XXXX y **G** **LF- T**

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

0783C—06/01/04