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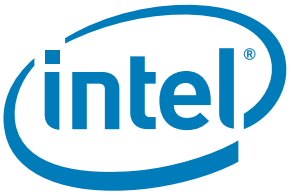
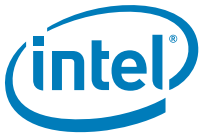


Intel® Xeon® Processor 5600 Series

Datasheet, Volume 1

March 2010

Reference Number: 323369-001



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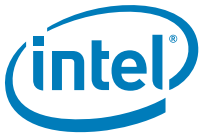
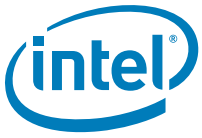


Figures



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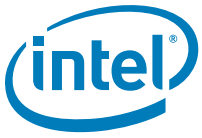

Revision History

Revision Number	Description	Date
-001	• Initial Release	March 2010

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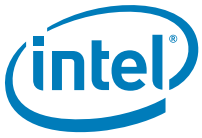


1 Introduction

The Intel® Xeon® processor 5600 series is a server/workstation multi-core processor based on 32 nm process technology. The processors feature two Intel® QuickPath Interconnect point-to-point links capable of up to 6.4 GT/s, up to 12 MB of shared cache, and an Integrated Memory Controller. The processors are optimized for performance with the power efficiencies of a low-power microarchitecture to enable smaller, quieter systems.

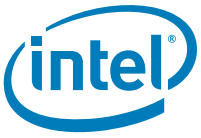
This datasheet provides DC and AC electrical specifications, signal integrity, differential signaling specifications, pinout and signal definitions, package mechanical specifications and thermal requirements, and additional features pertinent to implementation and operation of the processor.

The Intel Xeon processor 5600 series features a range of Thermal Design Power (TDP) envelopes from 40W TDP up to 130W TDP, and is segmented into multiple platforms:

- 2-Socket Frequency Optimized Server/Workstation Platforms support a 130 W Thermal Design Power (TDP) SKU and up to 6 core support. These platforms provide optimal overall performance and reliability, in addition to high-end graphics support.
- 2-Socket Advanced Server/Workstation Platforms support a 95 W Thermal Design Power (TDP) SKU. These platforms provide optimal overall performance featuring up to 6 core support.
- 2-Socket Standard Server/Workstation Platforms support 80 W TDP processor SKUs supporting up to 6 cores. These platforms provide optimal performance per watt for rack-optimized platforms.
- Low Power Platforms implement 60 W TDP (up to 6 cores) and 40 W TDP (up to 4 cores) processor SKU's. These processors are intended for dual-processor server blades and embedded servers.
- 1-Socket Workstation Platforms support Intel® Xeon® Processor W3680. These platforms enable a wide range of options for either the performance, power, or cost sensitive customer.
- Platforms supporting Higher Case Temperature Low-Voltage Processors with 60 W TDP (up to 6 cores) and 40 W TDP (up to 4 cores). The higher case temperatures are intended to meet the short-term thermal profile requirements of NEBS Level 3. These 2-socket processors are ideal for thermally-constrained form factors in embedded servers, communications and storage markets. Specifications denoted as LV-60W apply to the Intel® Xeon® Processor L5638. Specifications denoted as LV-40W apply to the Intel® Xeon® Processor L5618.

Note: All references to "chipset" in this document pertain to the Intel® 5520 chipset and the Intel® 5500 chipset.

Intel is committed to delivering processors for both server and workstation platforms that maximize performance while meeting all Intel Quality and Reliability goals. The product's reliability assessment is based on a datasheet compliant system and reference use condition. Intel utilizes a broad set of use condition assumptions (i.e. percentage of time in active vs. inactive operation, non-operating conditions, and the number of power cycles per year) to ensure proper operation over the life of the



product. The reference use condition differs between workstation and server processor SKU's. Implementing processors outside of reference use conditions may affect reliability performance.

1.1 Processor Features

Table 1-1 provides an overview the Intel Xeon processor 5600 series feature set.

Table 1-1. Intel® Xeon® Processor 5600 Series Feature Set Overview

Feature	Intel® Xeon® Processor 5600 Series
Cache Sizes	Instruction Cache: 32 kB Data Cache: 32 kB 256 kB Mid-Level Cache per core 12 MB Last-Level Cache shared among all cores
Data Transfer Rate (GT/s)	Two full-width Intel® QuickPath Interconnect links; Up to 6.40 GT/s in each direction
Memory Support	Integrated Memory Controller supports up to 3 channels of DDR3 or DDR3L memory, with up to 3 DIMMs per channel
DDR3 Memory Speed (MHz)	800, 1066, 1333
Multi-Core Support	Up to 6 cores per processor (package)
Intel® Hyper-Threading Technology	2 threads per core
Dual Processor Support	Up to 2 processor sockets per platform
Package	1366-land FC-LGA

The Intel Xeon processor 5600 series support all the existing Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Streaming SIMD Extensions 4 (SSE4) instructions. Additionally, Intel Xeon processor 5600 series support Advanced Encryption Standard-New Instructions (AES-NI).

The Intel Xeon processor 5600 series support Direct Cache Access (DCA). DCA enables supported I/O adapter to pre-fetch data from memory to the processor cache, thereby avoiding cache misses and improving application response times.

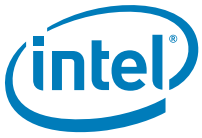
These processors support a maximum physical address size of 40 bits. Also supported is IA-32e paging which adds support for 1 GB (2^{30}) page size in addition to 2 MB and 4 kB page size support for linear to physical address translation.

Finally, these processors support several advanced technologies including Execute Disable Bit, Intel® 64 Technology, Enhanced Intel SpeedStep® Technology, Intel® Virtualization Technology (Intel® VT), Intel® Hyper-Threading Technology, and Intel® Turbo Boost Technology.

1.2 Platform Features

Various new component and platform capabilities are available with the implementation of Intel Xeon processor 5600 series.

New memory subsystem capabilities include Low Voltage DDR3 (DDR3L) DIMM support for power optimization. The Intel Xeon processor 5600 series also add features to provide improved manageability of memory channels. The DDR_THERM2# signal has been added to support high-temperature DIMMs and their 2X refresh requirements.



Intel Xeon processor 5600 series are based on a low-power micro-architecture that supports operation within various C-states. Additionally, six execution cores and power management coordination logic are optimized to manage C-state support at both the execution core and package levels. An Intel Turbo Boost Technology optimization feature is supported on these processors for improved energy efficiency.

Intel® Trusted Execution Technology (Intel® TXT) is also supported and represents a set of enhanced hardware components designed to help protect sensitive information from software-based attacks. Features include capabilities in the microprocessor, chipset, I/O subsystems, and other platform components. When coupled with suitably enabled operating systems and applications, Intel® TXT helps protect the confidentiality and integrity of data in the face of increasingly hostile security environment.

1.3 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low voltage level. For example, when RESET# is low, a reset has been requested.

A '_N' and '_P' after a signal name refers to a differential pair.

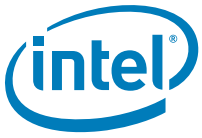
Commonly used terms are explained here for clarification:

- **1366-land FC-LGA package** — The Intel Xeon processor 5600 series is available in a Flip-Chip Land Grid Array (FC-LGA) package, consisting of processor mounted on a land grid array substrate with an integrated heat spreader (IHS).
- **DDR3** — Double Data Rate 3 synchronous dynamic random access memory (SDRAM) is the DDR memory standard, developed as the successor to DDR2 SDRAM.
- **Enhanced Intel SpeedStep® Technology** — Enhanced Intel SpeedStep® Technology allows the operating system to reduce power consumption when performance is not needed.
- **Execute Disable Bit** — Execute Disable allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer over run vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architecture Software Developer's Manuals* for more detailed information.
- **Functional Operation** — Refers to the normal operating conditions in which all processor specifications, including DC, AC, signal quality, mechanical, and thermal, are satisfied.
- **Integrated Memory Controller (IMC)** — This is a memory controller that is integrated in the processor die. Intel Xeon processor 5600 series can support up to 3 channels of DDR3, DDR3L memory, with up to 3 DIMMs per channel. Please refer to Intel Plan of Record for supported DIMM types, densities and configurations.
- **Intel® Turbo Boost Technology** - A way to automatically run the processor core faster than the marked frequency if the part is operating under power, temperature, and current specification limits of the Thermal Design Power (TDP). This results in increased performance of both single and multi-threaded applications.

- **Intel® Trusted Execution Technology** - A highly versatile set of hardware extensions to Intel processors and chipsets that, with appropriate software, enhance the platform security capabilities.
- **Intel® QuickPath Interconnect (Intel® QPI)** — A cache-coherent, links-based interconnect specification for Intel processors, chipsets, and I/O bridge components.
- **Intel® 64 Architecture** — An enhancement to Intel's IA-32 architecture, allowing the processor to execute operating systems and applications written to take advantage of Intel® 64.
- **Intel® Virtualization Technology (Intel® VT)** — A set of hardware enhancements to Intel server and client platforms that can improve virtualization solutions. VT provides a foundation for widely-deployed virtualization solutions and enables more robust hardware assisted virtualization solution.
- **Integrated Heat Spreader (IHS)** — A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Jitter** — Any timing variation of a transition edge or edges from the defined Unit Interval (UI).
- **LGA1366 Socket** — The 1366-land FC-LGA package mates with the system board through this surface mount, 1366-contact socket.
- **Network Equipment Building System (NEBS)** — The most common set of environmental design guidelines applied to telecommunications equipment in the United States.
- **Server SKU** — A processor Stock Keeping Unit (SKU) to be installed in either server or workstation platforms. Electrical, power and thermal specifications for these SKU's are based on specific use condition assumptions. Server processors may be further categorized as Frequency Optimized, Advanced, Standard and Low Power SKUs. For further details on use condition assumptions, please refer to the latest Product Release Qualification (PRQ) Report available via your Customer Quality Engineer (CQE) contact.
- **Storage Conditions** — Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor lands should not be connected to any supply voltages, have any I/Os biased, or receive any clocks.
- **Unit Interval (UI)** — Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,...., t_k then the UI at instance "n" is defined as:

$$UI_n = t_n - t_{n-1}$$

- **Workstation SKU** — A processor SKU to be installed in workstation platforms only. Electrical, power and thermal specifications for these processors have been developed based on Intel's reliability goals at a reference use condition. In addition, the processor validation and production test conditions have been optimized based on these conditions. Operating "Workstation" processors in a server environment or other application, could impact reliability performance, which means Intel's reliability goals may not be met. For further details on use condition assumptions or reliability performance, please refer to the latest Product Release Qualification (PRQ) Report available via your Customer Quality Engineer (CQE) contact.



1.4 References

Platform designers are strongly encouraged to maintain familiarity with the most up-to-date revisions of processor and platform collateral.

Table 1-2. References

Document	Location / Document# [1]	Notes
Advanced Configuration and Power Interface Specification	www.acpi.info.	
Compact Electronics Bay Specification: A Server System Infrastructure (SSI) Specification for Value Servers and Workstations	www.ssiforum.org	
Electronics Bay Specification for 2008 Servers and Workstation		
Entry-Level Electronics-Bay Specifications: A Server System Infrastructure (SSI) Specification for Entry Pedestal Servers and Workstations		
Thin Electronics Bay Specification: A Server System Infrastructure (SSI) Specification for Rack-Optimized Servers		
Intel® 64 and IA-32 Architecture Software Developer's Manual • *Volume 1: Basic Architecture* • *Volume 2A: Instruction Set Reference, A-M* • *Volume 2B: Instruction Set Reference, N-Z* • *Volume 3A: System Programming Guide, Part 1* • *Volume 3B: Systems Programming Guide, Part 2*	 253665 253666 253667 253668 253669	1
Intel® 64 and IA-32 Architectures Optimization Reference Manual	248966	1
Intel® Xeon® Processor 5600 Series Datasheet, Volume 2	323370	1
Intel® Xeon® Processor 5500/5600 Series Thermal/Mechanical Design Guidelines	323371	1

Notes:
1. Document is available publicly at http://www.intel.com.

2 Electrical Specifications

2.1 Processor Signaling

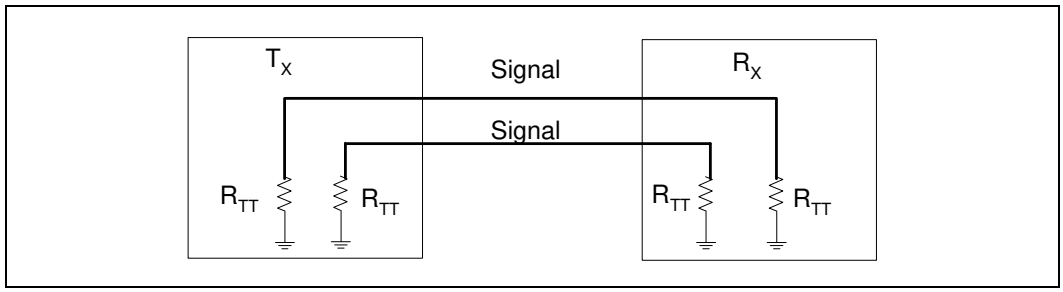
The Intel Xeon processor 5600 series include 1366 lands, which utilize various signaling technologies. Signals are grouped by electrical characteristics and buffer type into various signal groups. These include Intel® QuickPath Interconnect, DDR3 (Reference Clock, Command, Control, and Data), Platform Environmental Control Interface (PECI), Processor Sideband, System Reference Clock, Test Access Port (TAP), and Power/Other signals. Refer to Table 2-5 for details.

2.1.1 Intel® QuickPath Interconnect

The Intel Xeon processor 5600 series provide two Intel® QuickPath Interconnect ports for high speed serial transfer between other enabled components. Each port consists of two uni-directional links (for transmit and receive). A differential signaling scheme is utilized, which consists of opposite-polarity (D_P, D_N) signal pairs.

On-die termination (ODT) is included on the processor silicon and terminated to V_{SS}. Intel chipsets also provide ODT, thus eliminating the need to terminate on the system board. Figure 2-1 illustrates the active ODT.

Figure 2-1. Active ODT for a Differential Link Example



2.1.2 DDR3 Signal Groups

The memory interface utilizes DDR3 technology, which consists of numerous signal groups. These include: Reference Clocks, Command Signals, Control Signals, and Data Signals. Each group consists of numerous signals, which may utilize various signaling technologies. Please refer to Table 2-5 for further details.

2.1.3 Platform Environmental Control Interface (PECI)

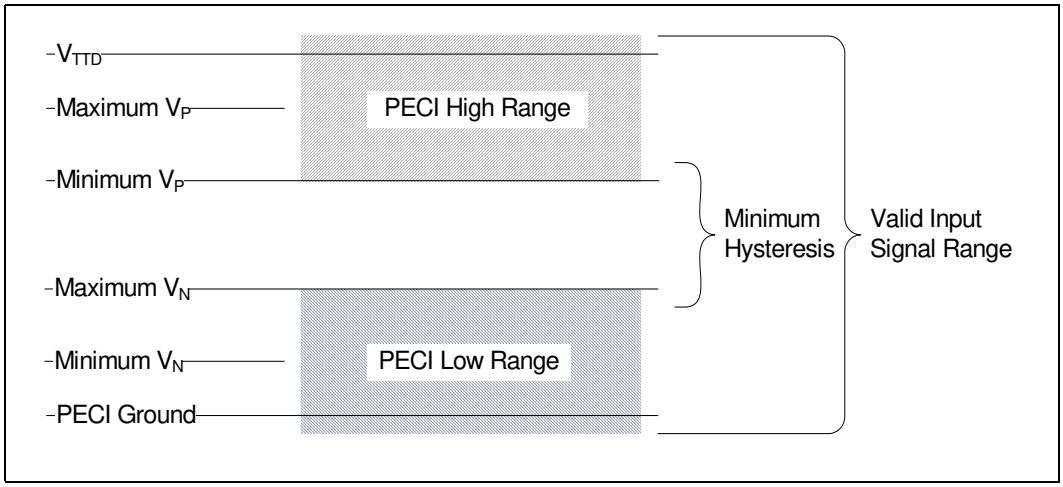
PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external thermal monitoring devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics. Please refer to Section 7.3 for processor specific implementation details for PECI.

The PECI interface operates at a nominal voltage set by V_{TTD}. The set of DC electrical specifications shown in Table 2-13 is used with devices normally operating from a V_{TTD} interface supply.

2.1.3.1 Input Device Hysteresis

The PECI client and host input buffers must use a Schmitt-triggered input design for improved noise immunity. Please refer to Figure 2-2 and Table 2-13.

Figure 2-2. Input Device Hysteresis



2.1.4 Processor Sideband Signals

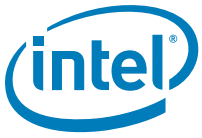
Intel Xeon processor 5600 series include sideband signals that provide a variety of functions. Details can be found in Table 2-5.

All Asynchronous Processor Sideband signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Table 2-18 and Table 2-26 for DC and AC specifications, respectively. Refer to Section 3 for applicable signal integrity specifications.

2.1.5 System Reference Clock

The processor core, processor uncore, Intel QuickPath Interconnect link, and DDR3 memory interface frequencies are generated from BCLK_DP and BCLK_DN signals. There is no direct link between core frequency and Intel QuickPath Interconnect link frequency (e.g., no core frequency to Intel QuickPath Interconnect multiplier). The processor maximum core frequency, Intel QuickPath Interconnect link frequency and DDR memory frequency are set during manufacturing. It is possible to override the processor core frequency setting using software. This permits operation at lower core frequencies than the factory set maximum core frequency.

The processor core frequency is configured during reset by using values stored within the device during manufacturing. The stored value sets the lowest core multiplier at which the particular processor can operate. If higher speeds are desired, the appropriate ratio can be configured via the IA32_PERF_CTL MSR (MSR 199h); Bits [15:0].



Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK_DP, BCLK_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK_DP, BCLK_DN inputs are provided in Table 2-14 and AC specifications in Table 2-22. These specifications must be met while also meeting the associated signal quality specifications outlined in Section 3.

2.1.6 Test Access Port (TAP) Signals

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the processor(s) be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Similar considerations must be made for TCK, TDO, TMS, and TRST# . Two copies of each signal may be required with each driving a different voltage level.

Processor TAP signal DC specifications can be found in Table 2-18. AC specifications are located in Table 2-27.

Note: While TDI, TMS and TRST# do not include On-Die Termination (ODT), these signals are weakly pulled-up via a 1-5 kΩ resistor to V_{TT}.

Note: While TCK does not include ODT, this signal is weakly pulled-down via a 1-5 kΩ resistor to V_{SS}.

2.1.7 Power / Other Signals

Processors also include various other signals including power/ground, sense points, and analog inputs. Details can be found in Table 2-5.

Table 2-1 outlines the required voltage supplies necessary to support Intel Xeon processor 5600 series.

Table 2-1. Processor Power Supply Voltages[1]

Power Rail	Nominal Voltage	Notes
V_{CC}	See Table 2-9; Figure 2-3	Each processor includes a dedicated VR11.1 regulator.
V_{CCPLL}	1.80 V	Each processor includes dedicated V_{CCPLL} and PLL circuits.
V_{DDQ}	1.50 V 1.35 V	Each processor and DDR3 / DDR3L stack shares a dedicated voltage regulator. It is expected that regulators will support both 1.50 and 1.35 V.
V_{TTA}, V_{TTD}	See Table 2-11; Figure 2-10	Each processor includes a dedicated VR11.0 regulator. V_{TT} = V_{TTA} + V_{TTD}; P1V1_Vtt is VID[4:2] controlled, VID range is 1.025-1.2000V; 20 mV offset (see Table 2-4); V_{TT} represents a ***typical*** voltage. V_{TT_MIN} and V_{TT_MAX} loadlines represent a 31.5 mV offset from V_{TT} (typ).

Note:
1. Refer to Table 2-8 for voltage and current specifications.

2.1.7.1 Power and Ground Lands

For clean on-chip power distribution, processors include lands for all required voltage supplies. These include:

- 210 each V_{CC} (271 ea. V_{SS}) lands must be supplied with the voltage determined by the VID[7:0] signals. Table 2-2 defines the voltage level associated with each core VID pattern. Table 2-9 and Figure 2-3 represent V_{CC} static and transient limits.
- 3 each V_{CCPLL} lands, connected to a 1.8 V supply, power the Phase Lock Loop (PLL) clock generation circuitry. An on-die PLL filter solution is implemented within the processor.
- 45 each V_{DDQ} (17 ea. V_{SS}) lands, connected to a 1.50 / 1.35 V supply, provide power to the processor DDR3 interface. This supply also powers the DDR3 memory subsystem.
- 7 each V_{TTA} (5 ea. V_{SS}) and 26 ea. V_{TTD} (17 ea. V_{SS}) lands must be supplied with the voltage determined by the VTT_VID[4:2] signals. Coupled with a 20 mV offset, this corresponds to a VTT_VID pattern of '010xxx10'. Table 2-4 specifies the voltage levels associated with each VTT_VID pattern. Table 2-11 and Figure 2-10 represent V_{TT} static and transient limits.

All V_{CC}, V_{CCPLL}, V_{DDQ}, V_{TTA}, and V_{TTD} lands must be connected to their respective processor power planes, while all V_{SS} lands must be connected to the system ground plane.

2.1.7.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply

current during longer lasting changes in current demand, for example coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the baseboard design to ensure that the voltages provided to the processor remain within the specifications listed in Table 2-8. Failure to do so can result in timing violations or reduced lifetime of the processor.

2.1.7.3 Processor V_{CC} Voltage Identification (VID) Signals

The voltage set by the VID signals is the maximum reference voltage regulator (VR) output to be delivered to the processor V_{CC} lands. VID signals are CMOS push/pull outputs. Please refer to Table 2-18 for the DC specifications for these signals.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same core frequency may have different default VID settings.

The processor uses eight voltage identification signals, VID[7:0], to support automatic selection of power supply voltages. Table 2-2 specifies the voltage level corresponding to the state of VID[7:0]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the processor socket is empty (SKTOCC# pulled high), or the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself.

The processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (V_{CC}). This is represented by a DC shift in the loadline. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the maximum specified VID are not permitted. Table 2-8 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 2-9.

The VRM or EVRD utilized must be capable of regulating its output to the value defined by the new VID. DC specifications for dynamic VID transitions are included in Table 2-18, while AC specifications are included in Table 2-28.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

Table 2-2. Voltage Identification Definition (Sheet 1 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375

Table 2-2. Voltage Identification Definition (Sheet 2 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125

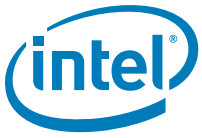


Table 2-2. Voltage Identification Definition (Sheet 3 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875

Table 2-2. Voltage Identification Definition (Sheet 4 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625

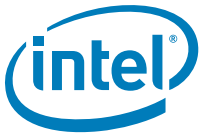


Table 2-2. Voltage Identification Definition (Sheet 5 of 6)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625