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Approval Sheet

Customer	
Product Number	M1SF-1GPCX103-F
Module speed	PC-3200
Pin	200 pin
CAS Latency	CL-3
DRAM Operating Temp.	-20 °C ~ +85 °C
Date	26 th November 2014

Approval by Customer

P/N:

Signature:

Date:

Sales: _____

Sr. Technical Manager: John Hsieh

Rev 1.1

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=2	CL=2.5	3			
PC-3200	F	266	333	400	15	15	55

- JEDEC Standard 200-pin Dual In-Line Memory Module
- Intend for 400 MHz applications
- Inputs and Outputs are SSTL-2 compatible
- VDD=VDDQ= 2.6 Volt ± 0.2 (PC-3200)
- Differential clock input
- DLL aligns DQ and DQS transition with CK transition
- Bi-Directional data strobe with one clock cycle
- Golden Connector (Au: 30µ")
- Built with 512Mb DDR SDRAMs in 60-ball BGA packages
- Self-Refresh Modes support.
- Serial Presence Detect with EEPROM
- Self-refresh 7.8µs (TA ≤ +70°C)
- SDRAM Operation Temperature
 - -20°C ≤ TA ≤ +85°C
- Programmable Device Operation:
 - Burst Type: Sequential or Interleave
 - Device CAS# Latency: 2, 2.5 & 3
 - Burst Length: 2, 4 or 8
- RoHS Compliant (*Section 14*)

2. Environmental Requirements

iDIMM's SDRAM are intended for use in standard industrial environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
ToPR	DRAM Operating Temperature (ambient)	-20 to +85	°C	1
TstG	Storage Temperature	-50 to +100	°C	1

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.

3. Ordering Information

E/T DDR SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M1SF-1GPCX103-F	1GB	PC-3200	128M x64	16	2	N/A

4. Pin Configurations (Front side/Back side)

Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	
1	V _{REF}	26	DM1	51	V _{SS}	76	V _{SS}	101	A9	126	V _{SS}	151	DQ42	176	DQ55
2	V _{REF}	27	V _{SS}	52	V _{SS}	77	DQS8	102	A8	127	DQ32	152	DQ46	177	DQ56
3	V _{SS}	28	V _{SS}	53	DQ19	78	DM8	103	V _{SS}	128	DQ36	153	DQ43	178	DQ60
4	V _{SS}	29	DQ10	54	DQ23	79	CB2	104	V _{SS}	129	DQ33	154	DQ47	179	V _{DD}
5	DQ0	30	DQ14	55	DQ24	80	CB6	105	A7	130	DQ37	155	V _{DD}	180	V _{DD}
6	DQ4	31	DQ11	56	DQ28	81	V _{DD}	106	A6	131	V _{DD}	156	V _{DD}	181	DQ57
7	DQ1	32	DQ15	57	V _{DD}	82	V _{DD}	107	A5	132	V _{DD}	157	V _{DD}	182	DQ61
8	DQ5	33	V _{DD}	58	V _{DD}	83	CB3	108	A4	133	DQS4	158	/CK1	183	DQS7
9	V _{DD}	34	V _{DD}	59	DQ25	84	CB7	109	A3	134	DM4	159	V _{SS}	184	DM7
10	V _{DD}	35	CK0	60	DQ29	85	DU	110	A2	135	DQ34	160	CK1	185	V _{SS}
11	DQS0	36	V _{DD}	61	DQS3	86	DU/Reset	111	A1	136	DQ38	161	V _{SS}	186	V _{SS}
12	DM0	37	/CK0	62	DM3	87	V _{SS}	112	A0	137	V _{SS}	162	V _{SS}	187	DQ58
13	DQ2	38	V _{SS}	63	V _{SS}	88	V _{SS}	113	V _{DD}	138	V _{SS}	163	DQ48	188	DQ62
14	DQ6	39	V _{SS}	64	V _{SS}	89	CK2	114	V _{DD}	139	DQ35	164	DQ52	189	DQ59
15	V _{SS}	40	V _{SS}	65	DQ26	90	V _{SS}	115	A10/AP	140	DQ39	165	DQ49	190	DQ63
16	V _{SS}	41	DQ16	66	DQ30	91	CK2	116	BA1	141	DQ40	166	DQ53	191	V _{DD}
17	DQ3	42	DQ20	67	DQ27	92	V _{DD}	117	BA0	142	DQ44	167	V _{DD}	192	V _{DD}
18	DQ7	43	DQ17	68	DQ31	93	V _{DD}	118	RAS	143	V _{DD}	168	V _{DD}	193	SDA
19	DQ8	44	DQ21	69	V _{DD}	94	V _{DD}	119	WE	144	V _{DD}	169	DQS6	194	SA0
20	DQ12	45	V _{DD}	70	V _{DD}	95	CKE1	120	CAS	145	DQ41	170	DM6	195	SCL
21	V _{DD}	46	V _{DD}	71	CB0	96	CKE0	121	/S0	146	DQ45	171	DQ50	196	SA1
22	V _{DD}	47	DQS2	72	CB4	97	DU	122	/S1	147	DQS5	172	DQ54	197	V _{DD} SPD
23	DQ9	48	DM2	73	CB1	98	DU	123	DU (A13)	148	DM5	173	V _{SS}	198	SA2
24	DQ13	49	DQ18	74	CB5	99	A12	124	DU	149	V _{SS}	174	V _{SS}	199	V _{DD} ID
25	DQS1	50	DQ22	75	V _{SS}	100	A11	125	V _{SS}	150	V _{SS}	175	DQ51	200	DU

Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are reserved for x72 variants of this module and are not used on the x64 versions.
 1. Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version.
 2. Pins 89, 91 are reserved for x72 modules or registered modules.
 3. Pin 123 reserved for higher density memories, requiring A13

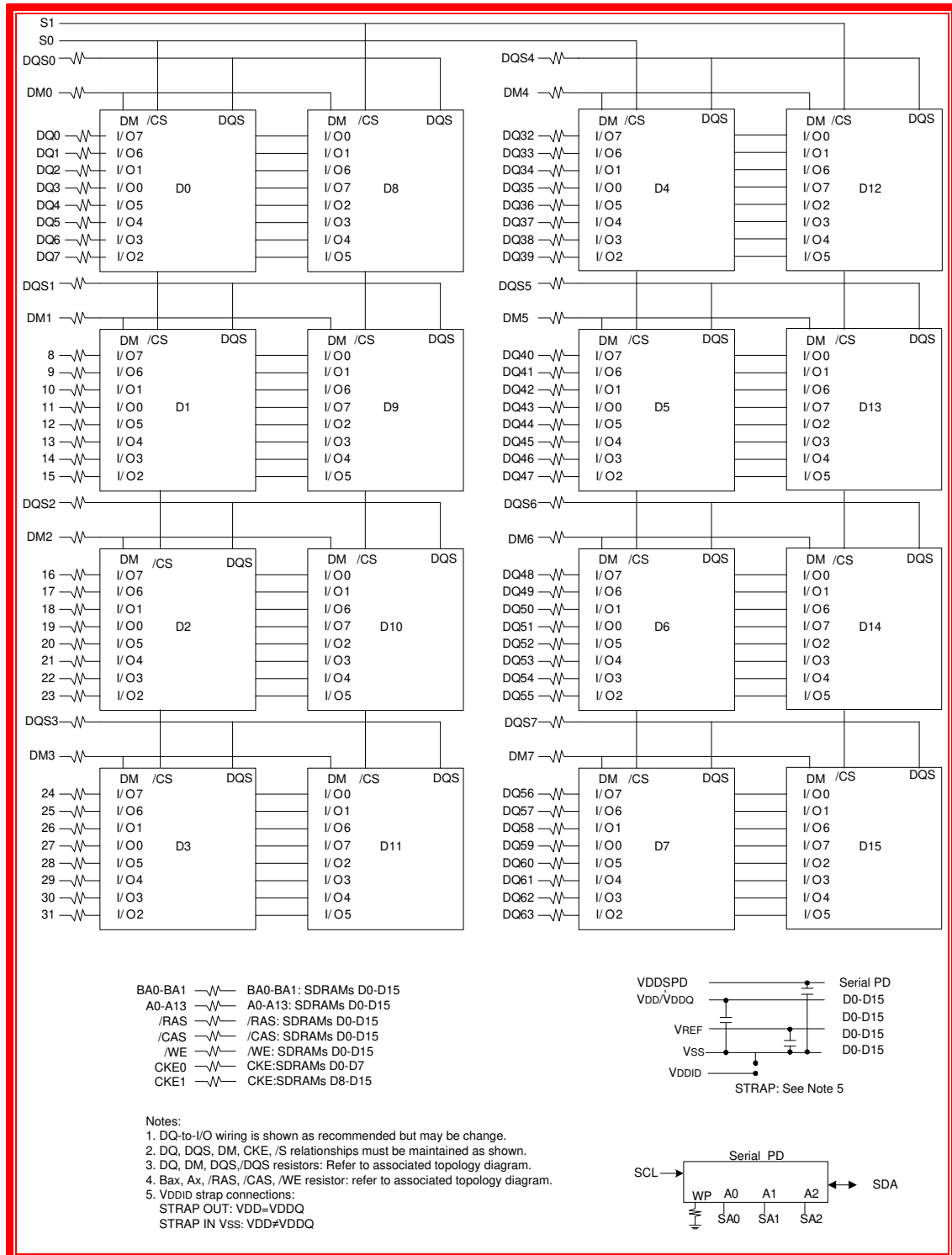
5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	CK0 – CK1 CK0# - CK1#	Differential SDRAM Clocks
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS#	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS#	SDRAM column address strobe	SA0 – SA1	Serial Presence Detect Address Inputs
WE#	SDRAM write enable	V _{DD}	Power Supply
S0# - S1#	DIMM Rank Select Lines	V _{DDID}	V _{DD} Identification Flag
CK0 – CK1	SDRAM clock enable lines	V _{DDQ}	SDRAM I/O Driver power supply
DQ0 – DQ63	DIMM memory data bus	V _{REF}	SDRAM I/O Reference supply
CB0 – CB7	DIMM ECC check bit	V _{SS}	Ground
DQS0 – DQS17	SDRAM data strobes	V _{DDSPD}	Serial EEPROM positive power supply
DM0 – DM7	SDRAM data masks	Reset	Reset enable
NC	Spare Pin		

6. Function Block Diagram:

- (1GB, 2 Ranks 64Mx8 DDR base Unbuffered SODIMM)



7. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
T _A	Operation Temperature	-20 to 85	°C
T _{STG}	Storage Temperature	-55 to 150	°C
V _{INPUT}	Voltage input pins relative to V _{SS}	-1.0 to +3.6	V
V _{IO}	Voltage on I/O pins relative to V _{SS}	-0.5 to +3.6	V
V _{DD}	Voltage on VDD supply relative to V _{SS}	-1.0 to +3.6	V
V _{DDQ}	Voltage on VDDQ supply relative to V _{SS}	-1.0 to +3.6	V
I _{OS}	Output short Circuit Current	50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8. AC & DC Operating Conditions

- AC Operating Conditions

(T_{CASE} = -20 °C ~ 85 °C; V_{SS}=0V)

Symbol	Parameter	Value		Units	Notes
		Min	Max		
V _{IH} (AC)	Input High (Logic1) Voltage	V _{REF} + 0.31	-	V	
V _{IL} (AC)	Input Low (Logic0) Voltage	-	V _{REF} + 0.31	V	
V _{ID} (AC)	Input differential Voltage: CK, /CK	0.7	V _{DDQ} + 0.6	V	1
V _{Ix} (AC)	Input crossing point Voltage: CK, /CK	0.5* V _{DDQ} + 0.2	0.5* V _{DDQ} - 0.2	V	2

Note:

- VID is the magnitude of the difference between the input level on CK and the input on /CK.
- The value of VIX is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

- DC Electrical Characteristics and Operating Conditions

 (T_{CASE} = -20 °C ~ 85 °C; V_{SS} = 0V)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
VDD	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
VDDQ	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
VIH (DC)	Input High (Logic1) Voltage	VREF + 0.15	-	VDDQ + 0.3	V	1
VIL (DC)	Input Low (Logic0) Voltage	-0.3	-	VREF - 0.15	V	1
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	3
VREF	I/O Reference Voltage	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	2
VIN(DC)	Input Voltage Level: CK, /CK	-0.3	-	VDDQ + 0.3	V	
VID(DC)	Input Differential Voltage: CK, /CK	0.36	-	VDDQ + 0.6	V	
VI(RATIO)	V-I Matching	0.71	-	1.4	V	

Note:

- Inputs are not recognized as valid until VREF stabilizes.
- VREF is expected to be equal to 0.5 V DDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
- VTT of transmitting device must track VREF of receiving device.

9. Operating, Standby, and Refresh Currents

- 1GB SODIMM (2 Rank, 128Mx8 DDR SDRAMs $T_{CASE} = -20\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$)

Symbol	Parameter/Condition	PC-3200	Unit
I _{DD0}	One bank; Active - Precharge; t _{RC} =t _{RC} (min); t _{CK} =t _{CK} (min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1520	mA
I _{DD1}	One bank; Active - Read - Precharge; Burst Length=2; t _{RC} =t _{RC} (min); t _{CK} =t _{CK} (min); address and control inputs changing once per clock cycle	1840	mA
I _{DD2P}	All banks idle; Power down mode; CKE=Low, t _{CK} =t _{CK} (min)	160	mA
I _{DD2F}	/CS=High, All banks idle; t _{CK} =t _{CK} (min); CKE= High; address and control inputs changing once per clock cycle.VIN=VREF for DQ, DQS and DM	560	mA
I _{DD3P}	One bank active ; Power down mode; CKE=Low, t _{CK} =t _{CK} (min)	720	mA
I _{DD3N}	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge;t _{RC} =t _{RAS} (max); t _{CK} =t _{CK} (min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	960	mA
I _{DD4R}	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (min); IOUT=0mA	2160	mA
I _{DD4W}	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (min); DQ, DM and DQS inputs changing twice per clock cycle	2320	mA
I _{DD5}	t _{RC} =t _{RFC} (min) - 8*t _{CK} for DDR200 at 100Mhz, 10*t _{CK} for DDR266A & DDR266B at 133Mhz; distributed refresh	2560	mA
I _{DD6}	CKE=<0.2V; External clock on; t _{CK} =t _{CK} (min)	80	mA
I _{DD7}	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	3360	mA

10. AC Timing Specifications

(T_{CASE} = -20 °C ~ +85 °C; V_{DDQ} = V_{DD}, See AC Characteristics)

Symbol	Parameter	PC2-3200		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.7	0.7	ns
tdQSCk	DQS output access time from CK/CK#	-0.55	0.55	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	min (tCL,tCH)	-	ns
tCK	Clock Cycle Time	5	10	ns
tDS	DQ and DM input setup time(differential data strobe)	0.4	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.4	-	ns
tIPW	Input pulse width	2.2	-	ns
tdIPW	DQ and DM input pulse width (each input)	1.75	-	ns
tHZ	Data-out high-impedance time from CK/CK	-0.7	0.7	ns
tLZ(DQS)	DQS low-impedance time from CK/CK	-0.7	0.7	ns
tLZ(DQ)	DQ low-impedance time from CK/CK	-0.7	0.7	ns
tdQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.4	ns
tQHS	Data hold Skew Factor	-	0.5	ns
tQH	Data output hold time from DQS	tHP -tQHS	-	ns
tdQSS	Write command to 1st DQS latching transition	0.72	1.25	tCK
tdQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tdSS	DQS falling edge to CK setup time (write cycle)	0.35	-	tCK
tdSH	DQS falling edge hold time from CK (write cycle)	0.4	-	tCK
tMRD	Mode register set command cycle time	2	-	tCK
tWPST	Write postamble	0.4	0.6	tCK
tWPRE	Write preamble	0.9	1.1	tCK
tIH	Address and control input hold time	0.6	-	ns

tIS	Address and control input setup time	0.7	-	ns
tRPRE	Read preamble	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	tCK
tRRD	Active bank A to Active bank B command	10	-	ns
tREFI	Average Periodic Refresh Interval (85°C < T _{CASE} ≤ 95°C)	-	3.9	μs
	Average Periodic Refresh Interval (0°C ≤ T _{CASE} ≤ 85°C)	-	7.8	μs
tCCD	CAS# to CAS# delay	15	-	tCK
tWR	Write recovery time without Auto-Precharge	15	-	ns
tDAL	Auto precharge write recovery + precharge time	$(tWR/tCK) + (tRP/tCK)$	-	tCK
tWTR	Internal write to read command delay	2	-	ns
tXSNR	Exit self refresh to a Non-read command	75	-	ns
tXSRD	Exit self refresh to a Read command	200	-	tCK
tCKE	CKE minimum pulse width			tCK

11. SPD Serial Presence Detect –(1GB)

128Mx64 2 RANKs UNBUFFERED DDR SDRAM SODIMM based on 64Mx8, 4Banks, 8K Refresh, 2.6V DDR SDRAMs with SPD

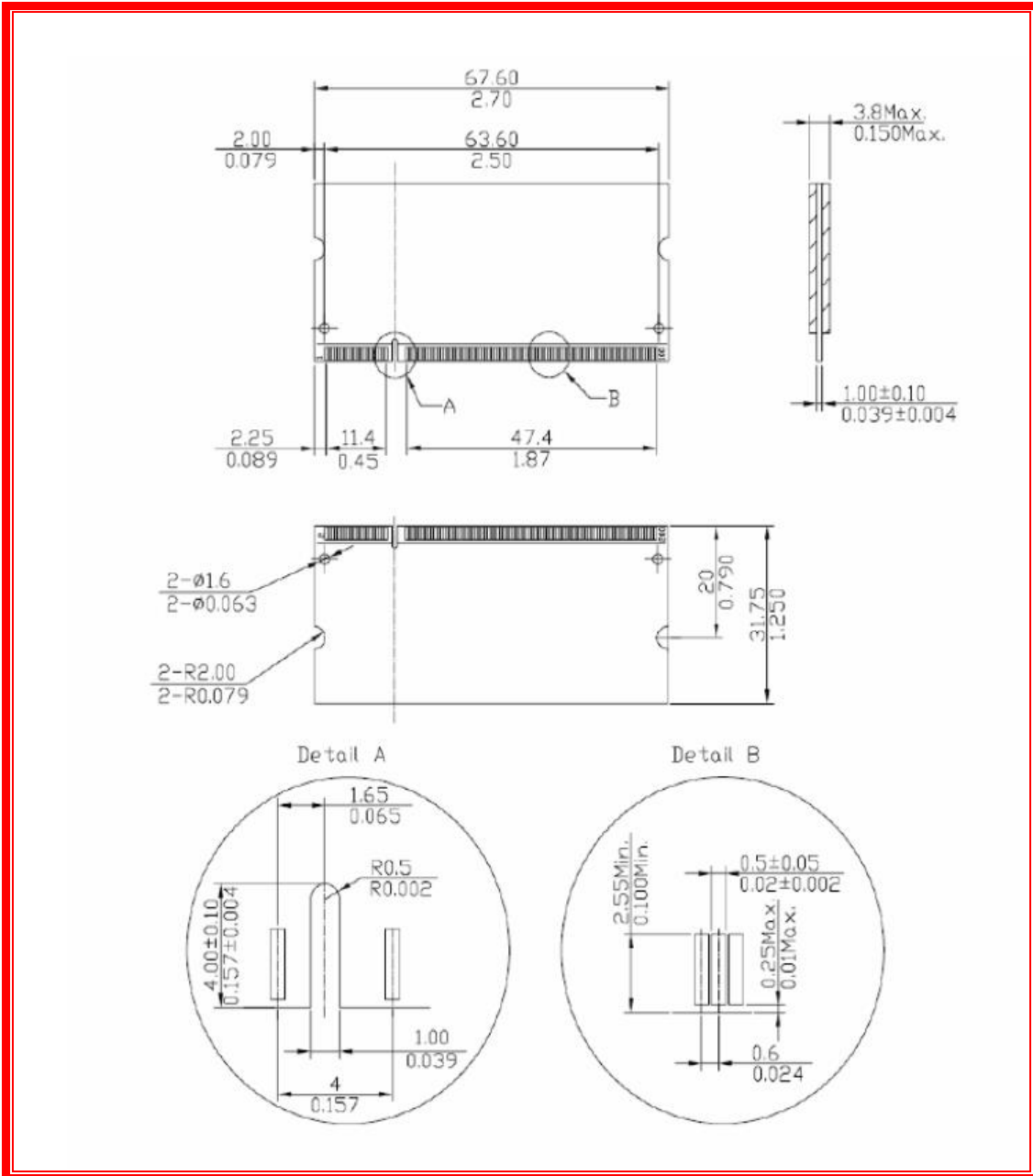
Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
		DDR-400 1GB E/T Grade SODIMM	
0	Number of Serial PD Bytes Written during Production	80	
1	Total Number of Bytes in Serial PD device	08	
2	Fundamental Memory Type	07	
3	Number of Row Addresses on Assembly	0D	
4	Number of Column Addresses on Assembly	0B	
5	Number of DIMM Bank, Package, and Height	02	
6	Data Width of this Assembly	40	
7	Reserved	00	
8	Voltage Interface Level of this Assembly	04	
9	DDR SDRAM Cycle Time at CL=5 (ns)	50	
10	DDR SDRAM Access Time from Clock at CL=5 (ns)	70	
11	DIMM Configuration Type	00	
12	Refresh Rate/Type	82	
13	Primary DDR SDRAM Width	08	
14	Error Checking DDR2 SDRAM Device Width	00	
15	Reserved	01	
16	DDR SDRAM Device Attributes: Burst Length Supported	0E	
17	DDR SDRAM Device Attributes: Number of Device Banks	04	
18	DDR SDRAM Device Attributes: /CAS Latencies Supported	1C	
19	Reserved	01	
20	DDR SDRAM DIMM Type Information	02	
21	DDR SDRAM Module Attributes:	20	
22	DDR SDRAM Device Attributes: General	C0	

23	Minimum Clock Cycle at CL=4	60	
24	Maximum Data Access Time (t_{ac}) from Clock at CL=4 (ns)	70	
25	Minimum Clock Cycle Time at CL=3 (ns)	75	
26	Maximum Data Access Time (t_{ac}) from Clock at CL=3 (ns)	75	
27	Minimum Row Precharge Time (t_{RP}) (ns)	3C	
28	Minimum Row Active to Row Active delay (t_{RRD})	28	
29	Minimum RAS to CAS delay (t_{RCD}) (ns)	3C	
30	Minimum RAS Pulse Width (t_{RAS})	28	
31	Module Bank Density	80	
32	Address and Command Setup Time Before Clock (t_{IS}) (ns)	60	
33	Address and Command Hold Time After Clock (t_{IH}) (ns)	60	
34	Data Input Setup Time Before Clock (t_{DS})	40	
35	Data Input Hold Time After Clock (t_{DH}) (ns)	40	
36	Write Recovery Time (t_{WR})	00	
37	Internal Write to Read Command delay (t_{WTR})	00	
38	Internal Read to Precharge delay (t_{RTP})	00	
39	Memory Analysis Probe Characteristics	00	
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	00	
41	Minimum Core Cycle Time (t_{RC}) (ns)	37	
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	46	
43	Maximum Clock Cycle Time (t_{CK})	28	
44	Max. DQS-DQ Skew Factor (t_{DOS}) (ns)	28	
45	Read Data Hold Skew Factor (t_{QHS}) (ns)	50	
46	PLL Relock Time	00	
47	Tcasemax DT4R4W Delta	00	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi-T-A DRAM)	00	
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	00	

50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	00	
51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down (DT2P)	00	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	00	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	00	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	00	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	00	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (ST5B)	00	
57	DRAM Case Temperature Rise from Ambient due to Bank interleave Reads with Auto-Precharge (DT7)	00	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00	
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00	
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00	
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00	
62	SPD Reversion	11	
63	Checksum for byte 0-62	B9	
64-71	Manufacturer's JEDEC ID Code	InnoDisk	
72	Module Manufacturing Location	Manufacturing Code	
73-91	Module Part number	Module Part Number in ASCII	
92-255	Reserved	Undefined	


12. PACKAGE DIMENSION

- (1GB, 2 Ranks 64Mx8 DDR SDRAMs)



Note: Device position is only for reference.

13. Declaration of hazardous substances controlled



Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M1SF-1GPCX103/-(X) complies with the requirement of RoHS directives 2011/65/EU and 2006/12/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

✦ RoHS Exemptions Applied Of 7(C)-I for Resist.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI (Cr+6)	< 1000 ppm
Polybromodiphenyl ether (PBDE)	< 1000 ppm
Polybrominated Biphenyls (PBB)	< 1000 ppm

Date issued: 2014/11/26

Manufacturer: : InnoDisk Co., Ltd.

Address : 9F, No. 100, Sec.1 Xintai 5th Rd., Xizhi City, Taipei 221, Taiwan

Authorized Signature :

QA Dept. Director – *Ryan Tsai*

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Revision Log

Rev	Date	Modification
0.1	12 th September 2014	Preliminary Edition
1.0	12 th September 2014	Official Released.
1.1	26 th November 2014	Update RoHS Declaration