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Approval Sheet

Customer	
Product Number	**M1SF-1GMCX103-JA61**
Module speed	**PC-3200**
Pin	**200 pin**
CAS Latency	**CL-3**
SDRAM Operating Temp	**-20 ℃ ~ 85 ℃**
SDRAM Information	**Micron 64Mx8**
Date	**23rd May 2017**

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=2	CL=2.5	CL=3			
PC-3200	F	266	333	400	15	15	55

- JEDEC Standard 200-pin Small Outline Dual In-Line Memory Module
- Intend for 400 MHz applications
- Inputs and Outputs are SSTL-2 compatible
- VDD=VDDQ= 2.6 Volt ± 0.1 (PC-3200)
- Differential clock input
- DLL aligns DQ and DQS transition with CK transition
- Bi-Directional data strobe with one clock cycle
- Built with 512Mb DDR SDRAMs
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Operation Temperature Rating
  - (-20°C ≤ TA ≤ +85°C)
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 2,2.5 and 3
  - Burst Length: 2, 4 or 8
- RoHS Compliant *(Section 13)*

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	-20 to +85	°C	1
TSTG	Storage Temperature	-50 to +100	°C	1
HOPR	Operating Humidity (relative)	10 to 90	%	2
HSTG	Storage Humidity (without condensation)	5 to 95	%	2
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	2,3

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.
2. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
3. Up to 9850 ft.

3. Ordering Information

DDR W/T SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M1SF-1GMCX103-JA61	1GB	PC-3200	128M x64	16	2	N/A

4. Pin Assignments and Descriptions

DDR SDRAM SO-DIMM Pinout

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{REF}	2	V_{REF}	51	V_{SS}	52	V_{SS}	101	A9	102	A8	151	DQ42	152	DQ46
3	V_{SS}	4	V_{SS}	53	DQ19	54	DQ23	103	V_{SS}	104	V_{SS}	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	V_{DD}	156	V_{DD}
7	DQ1	8	DQ5	57	V_{DD}	58	V_{DD}	107	A5	108	A4	157	V_{DD}	158	$\overline{CK1}$
9	V_{DD}	10	V_{DD}	59	DQ25	60	DQ29	109	A3	110	A2	159	V_{SS}	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	V_{SS}	162	V_{SS}
13	DQ2	14	DQ6	63	V_{SS}	64	V_{SS}	113	V_{DD}	114	V_{DD}	163	DQ48	164	DQ52
15	V_{SS}	16	V_{SS}	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	$\overline{RAS}$	167	V_{DD}	168	V_{DD}
19	DQ8	20	DQ12	69	V_{DD}	70	V_{DD}	119	$\overline{WE}$	120	$\overline{CAS}$	169	DQS6	170	DM6
21	V_{DD}	22	V_{DD}	71	CB0	72	CB4	121	$\overline{S0}$	122	$\overline{S1}$	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	CB1	74	CB5	123	A13	124	DU	173	V_{SS}	174	V_{SS}
25	DQS1	26	DM1	75	V_{SS}	76	V_{SS}	125	V_{SS}	126	V_{SS}	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	DQS8	78	DM8	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	CB2	80	CB6	129	DQ33	130	DQ37	179	V_{DD}	180	V_{DD}
31	DQ11	32	DQ15	81	V_{DD}	82	V_{DD}	131	V_{DD}	132	V_{DD}	181	DQ57	182	DQ61
33	V_{DD}	34	V_{DD}	83	CB3	84	CB7	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	V_{DD}	85	DU	86	DU ($\overline{RESET}$)	135	DQ34	136	DQ38	185	V_{SS}	186	V_{SS}
37	$\overline{CK0}$	38	V_{SS}	87	V_{SS}	88	V_{SS}	137	V_{SS}	138	V_{SS}	187	DQ58	188	DQ62
39	V_{SS}	40	V_{SS}	89	CK2	90	V_{SS}	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	$\overline{CK2}$	92	V_{DD}	141	DQ40	142	DQ44	191	V_{DD}	192	V_{DD}
43	DQ17	44	DQ21	93	V_{DD}	94	V_{DD}	143	V_{DD}	144	V_{DD}	193	SDA	194	SA0
45	V_{DD}	46	V_{DD}	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU	98	DU	147	DQS5	148	DM5	197	V_{DD}SPD	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	V_{SS}	150	V_{SS}	199	V_{DD}ID	200	NC, TEST

Note: Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are reserved for x72 variants of this module and are not used on the x64 versions.

Note: Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version.

Note: Pins 89, 91are reserved for x72 modules or registered modules.

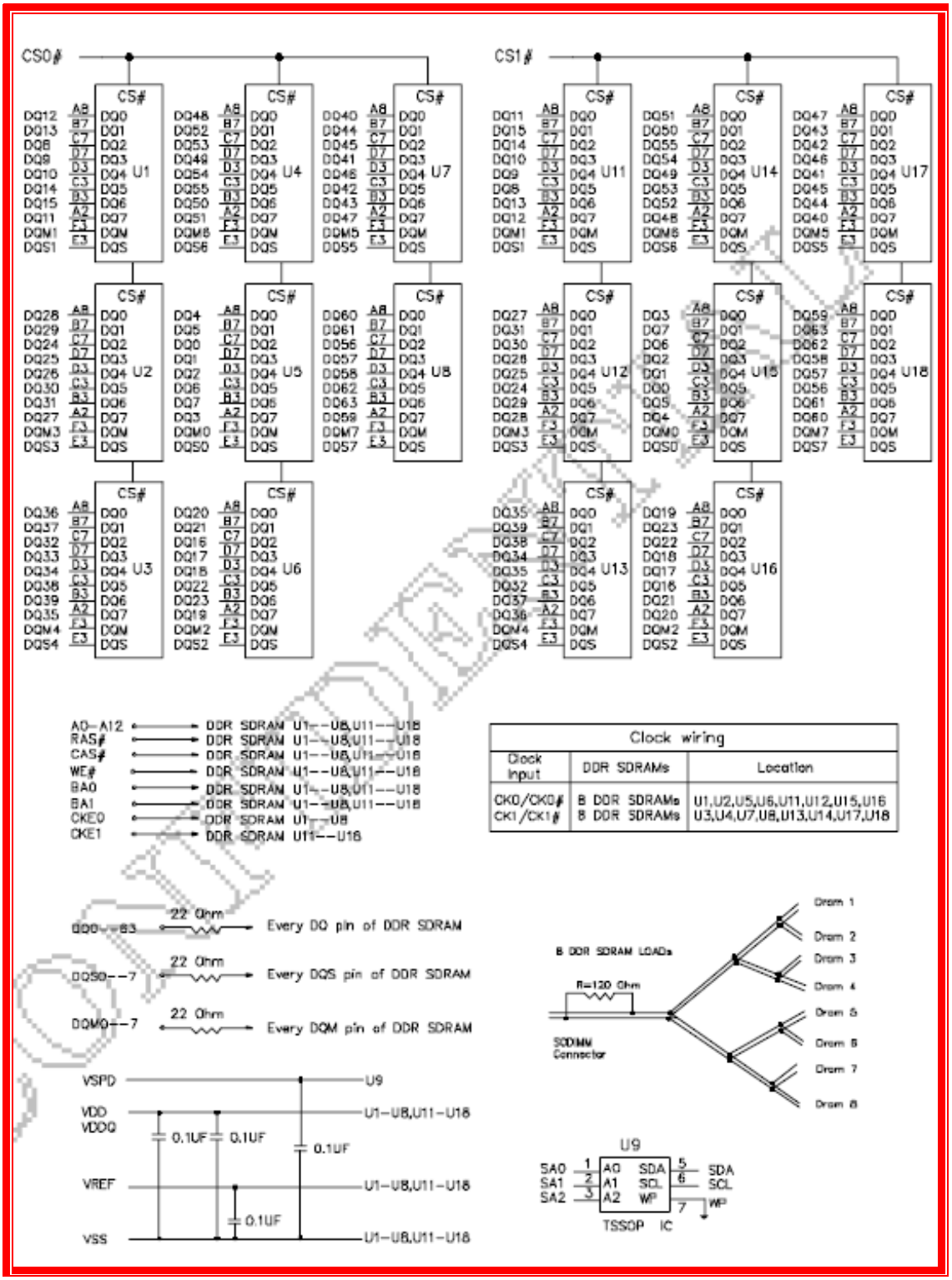
5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	CK0 – CK1 CK0# - CK1#	Differential SDRAM Clocks
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS#	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS#	SDRAM column address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
WE#	SDRAM write enable	V_{DD}	Power Supply
S0# - S1#	DIMM Rank Select Lines	V_{DDID}	V_{DD} Identification Flag
CK0 – CKE1	SDRAM clock enable lines	V_{DDQ}	SDRAM I/O Driver power supply
DQ0 – DQ63	DIMM memory data bus	V_{REF}	SDRAM I/O Reference supply
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0 – DQS17	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM7	SDRAM data masks	Reset	Reset enable
NC	Spare Pin		

6. Function Block Diagram:

- (1GB, 2 Ranks, 64Mx8 DDR SDRAM base SODIMM)



7. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
T_A	Operation Temperature	-20 to 85	°C
T_{STG}	Storage Temperature	-50 to 100	°C
V_{INPUT}	Voltage input pins relative to Vss	-1.0 to +3.6	V
V_{IO}	Voltage on I/O pins relative to Vss	-0.5 to +3.6	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +3.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-1.0 to +3.6	V
I_{OS}	Output short Circuit Current	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8. AC & DC Operating Conditions

- AC Operating Conditions

Symbol	Parameter	Value		Units	Notes
		Min	Max		
V_{IH} (AC)	Input High (Logic1) Voltage	V_{REF} + 0.31	-	V	
V_{IL} (AC)	Input Low (Logic0) Voltage	-	V_{REF} + 0.31	V	
V_{ID} (AC)	Input differential Voltage: CK, /CK	0.7	V_{DDQ} + 0.6	V	1
V_{IX} (AC)	Input crossing point Voltage: CK, /CK	0.5* V_{DDQ} + 0.2	0.5* V_{DDQ} - 0.2	V	2

Note:

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

- DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Units	Notes
V_{DD}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
V_{DDQ}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
V_{IH} (DC)	Input High (Logic1) Voltage	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	1
V_{IL} (DC)	Input Low (Logic0) Voltage	-0.3	-	V_{REF} - 0.15	V	1
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
V_{REF}	I/O Reference Voltage	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	2
V_{IN}(DC)	Input Voltage Level: CK, /CK	-0.3	-	V_{DDQ} + 0.3	V	
V_{ID}(DC)	Input Differential Voltage: CK, /CK	0.36	-	V_{DDQ} + 0.6	V	
V_{I}(RATIO)	V-I Matching	0.71	-	1.4	V	

Note:

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} of transmitting device must track V_{REF} of receiving device.

9. Operating, Standby, and Refresh Currents

- 1GB SODIMM (2 Rank, 64Mx8 DDR SDRAMs)

Symbol	Parameter/Condition	PC-3200	Unit
I DD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1200	mA
I DD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	1360	mA
I DD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	80	mA
I DD2F	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle.VIN=VREF for DQ, DQS and DM	368	mA
I DD3P	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	288	mA
I DD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge;tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	640	mA
I DD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	1920	mA
I DD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	1920	mA
I DD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	1920	mA
I DD6	CKE=<0.2V; External clock on; tCK=tCK(min)	80	mA
I DD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	3680	mA

10. AC Timing Specifications

Symbol	Parameter	PC2-3200		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.7	0.7	ns
tDQSCK	DQS output access time from CK/CK#	-0.55	0.55	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	min (tCL,tCH)	-	ns
tCK	Clock Cycle Time	5	10	ns
tDS	DQ and DM input setup time(differential data strobe)	0.4	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.4	-	ns
tIPW	Input pulse width	2.2	-	ns
tDIPW	DQ and DM input pulse width (each input)	1.75	-	ns
tHZ	Data-out high-impedance time from CK/CK	-0.7	0.7	ns
tLZ(DQS)	DQS low-impedance time from CK/CK	-0.7	0.7	ns
tLZ(DQ)	DQ low-impedance time from CK/CK	-0.7	0.7	ns
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.4	ns
tQHS	Data hold Skew Factor	-	0.5	ns
tQH	Data output hold time from DQS	tHP -tQHS	-	ns
tDQSS	Write command to 1st DQS latching transition	0.72	1.25	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.35	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.4	-	tCK
tMRD	Mode register set command cycle time	2	-	tCK
tWPST	Write postamble	0.4	0.6	tCK
tWPRE	Write preamble	0.9	1.1	tCK
tIH	Address and control input hold time	0.6	-	ns

tIS	Address and control input setup time	0.7	-	ns
tRPRE	Read preamble	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	tCK
tRRD	Active bank A to Active bank B command	10	-	ns
tREFI	Average Periodic Refresh Interval (85ºC < T_{CASE} ≤ 95ºC)	-	3.9	µs
	Average Periodic Refresh Interval (0ºC ≤ T_{CASE} ≤ 85ºC)	-	7.8	µs
tCCD	CAS# to CAS# delay	15	-	tCK
tWR	Write recovery time without Auto-Precharge	15		ns
tDAL	Auto precharge write recovery + precharge time	(tWR/tCK) +(tRP/tCK)	-	tCK
tWTR	Internal write to read command delay	2	-	ns
tXSNR	Exit self refresh to a Non-read command	75	-	ns
tXSRD	Exit self refresh to a Read command	200	-	tCK
tCKE	CKE minimum pulse width			tCK

11.SPD

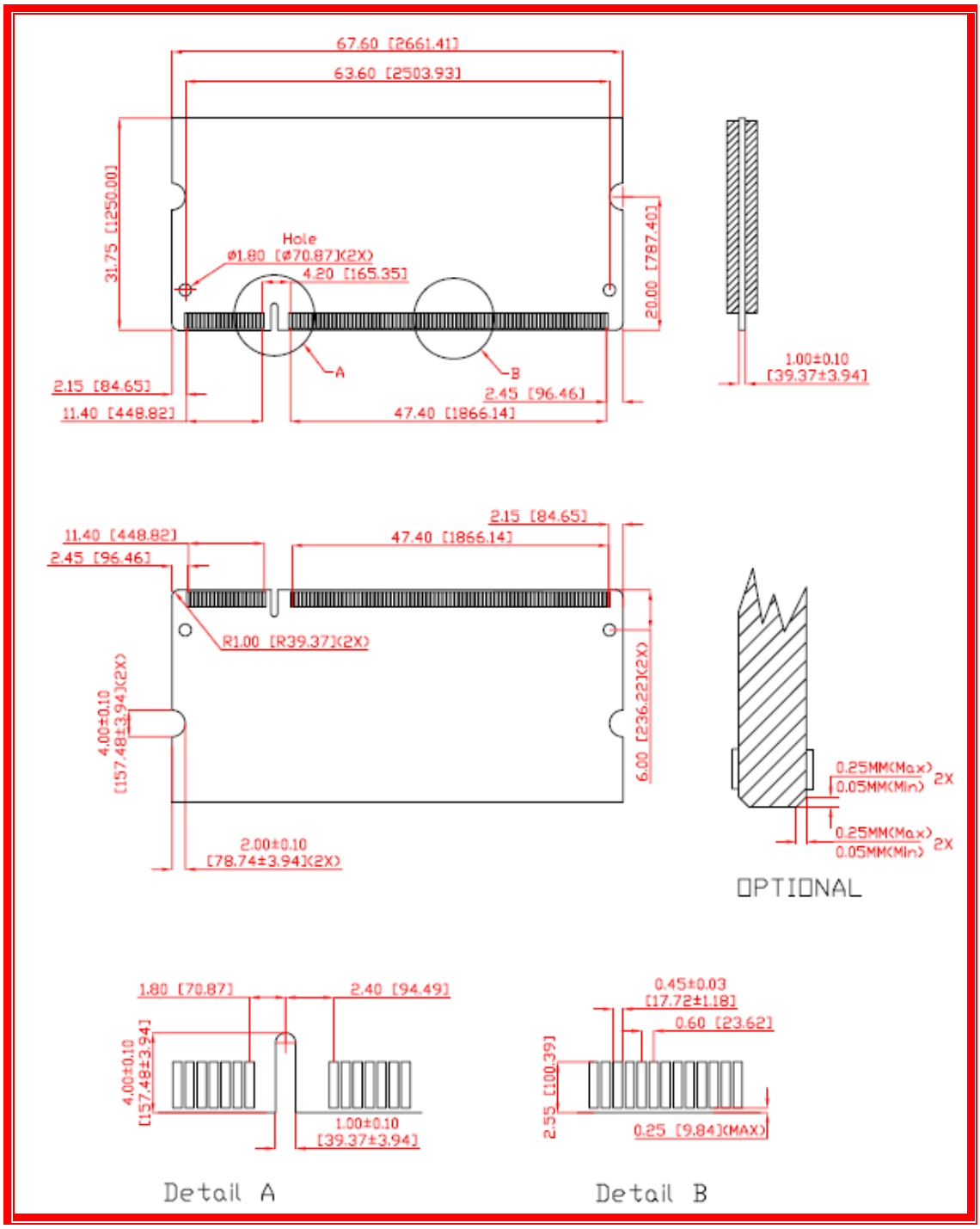
Byte	Description	Serial PD Data Entry (Hexadecimal)
0	Number of Serial PD Bytes Written during Production	80
1	Total Number of Bytes in Serial PD device	08
2	Fundamental Memory Type	07
3	Number of Row Addresses on Assembly	0D
4	Number of Column Addresses on Assembly	0B
5	NUMBER OF MODULE RANKS	02
6	MODULE DATA WIDTH	40
7	MODULE DATA WIDTH (CONTINUED)	00
8	Voltage Interface Level of this Assembly	04
9	DDR SDRAM CYCLE TIME	50
10	DDR SDRAM ACCESS FROM CLOCK	70
11	MODULE ERROR CORRECTION CONFIGURATION TYPE	00
12	Refresh Rate/Type	82
13	DDR SDRAM Width	08
14	Error Checking Width	00
15	MIN CLOCK DELAY FOR BACK TO BACK RANDOM COLUMN ADDRESSES	01
16	Burst Length Supported	0E
17	NUMBER OF BANKS INTERNAL TO DISCRETE SDRAM DEVICE	04
18	CAS Latencies Supported	1C
19	CS LATENCY	01
20	WE LATENCY	02
21	DDR SDRAM Module Attributes:	20
22	DDR SDRAM Device Attributes: General	C0
23	DDR SDRAM CYCLE TIME (TCK)	60

24	DDR SDRAM ACCESS FROM CLOCK (TAC)	70
25	DDR SDRAM CYCLE TIME (TCK)	75
26	DDR SDRAM ACCESS FROM CLOCK (TAC)	75
27	Minimum Row Precharge Time	3C
28	Minimum Row Active to Row Active delay	28
29	Minimum RAS to CAS delay	3C
30	Minimum RAS Pulse Width	28
31	Module Bank Density	80
32	Address and Command Setup Time Before Clock	60
33	Address and Command Hold Time After Clock	60
34	DATA SIGNAL INPUT SETUP	40
35	DATA SIGNAL INPUT HOLD	40
36-40	RESERVED	00
41	DEVICE MINIMUM ACTIVE/AUTO-REFRESH TIME	37
42	DEVICE MINIMUM AUTO-REFRESH TO ACTIVE/AUTO REFRESH COMMAND PERIOD	46
43	DEVICE MAXIMUM DEVICE CYCLE TIME	28
44	DEVICE DQS-DQ SKEW FOR DQS AND ASSOCIATED DQ SIGNALS	28
45	DEVICE READ DATA HOLD SKEW FACTOR	50
46	RESERVED	00
47	DIMM HEIGHT	01
48-61	RESERVED	00
62	SPD Reversion	11
63	Checksum for byte 0-62	B9
64-71	Manufacture's JEDEC ID Code	7F 7F 7F 7F 7F 7F F1 FF
72	Module Manufacturing Location	02
73-90	Module Part number	-
91	Module Manufacturer Revision Code	-
92	Module Manufacturer Revision Code	-

93	YEAR OF MANUFACTURE	-
94	WEEK OF MANUFACTURE	-
95-98	MODULE SERIAL NUMBER	-
99-127	MANUFACTURER SPECIFIC DATA	-
128-255	UNUSED	-

12. PACKAGE DIMENSION

- (1GB, 2 Ranks, 64Mx8 DDR SDRAMs)



Note: Device position is only for reference.

13. RoHS Declaration

innodisk

宜鼎國際股份有限公司

Innodisk Corporation

Page 1/1

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2016 / 08 / 04

14. Revision Log

Rev	Date	Modification
0.1	23rd May 2017	Preliminary Edition
1.0	23rd May 2017	Official Released.