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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



3-PHASE BRIDGE DRIVER

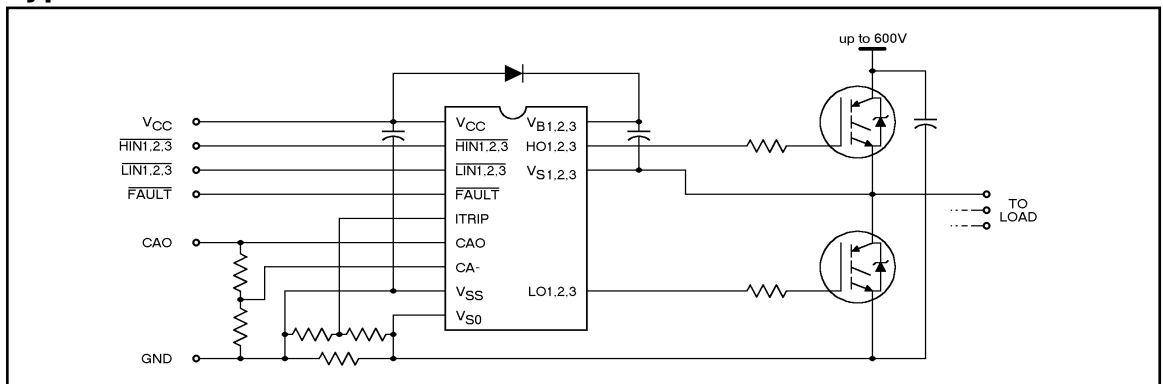
Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent half-bridge drivers
- Matched propagation delay for all channels
- Outputs out of phase with inputs

Description

The IR2132 is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with 5V CMOS or LSTTL outputs. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor. An open drain FAULT signal indicates if an over-current or undervoltage shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

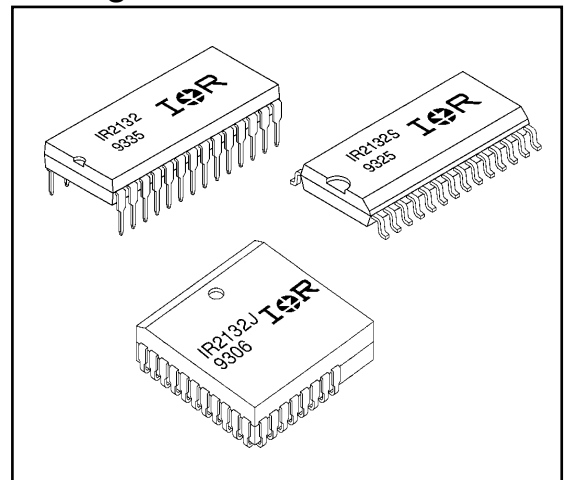
Typical Connection



Product Summary

V_{OFFSET}	600V max.
$I_{\text{O+/-}}$	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{\text{on/off (typ.)}}$	675 & 425 ns
Deadtime (typ.)	0.8 μs

Packages



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{S0} . The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 50 through 53.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	525	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	$V_{B1,2,3} - 25$	$V_{B1,2,3} + 0.3$	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3} - 0.3$	$V_{B1,2,3} + 0.3$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25	
V_{SS}	Logic Ground	$V_{CC} - 25$	$V_{CC} + 0.3$	
$V_{LO1,2,3}$	Low Side Output Voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$ & ITRIP)	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{FLT}	\overline{FAULT} Output Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{CAO}	Operational Amplifier Output Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{CA-}	Operational Amplifier Inverting Input Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$ (28 Lead DIP)	—	1.5	W
	(28 Lead SOIC)	—	1.6	
	(44 Lead PLCC)	—	2.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (28 Lead DIP)	—	83	$^\circ\text{C}/\text{W}$
	(28 Lead SOIC)	—	78	
	(44 Lead PLCC)	—	63	
T_J	Junction Temperature	—	150	$^\circ\text{C}$
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{S0} . The V_S offset rating is tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figure 54.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3} + 10$	$V_{S1,2,3} + 20$	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	Note 1	600	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$ & ITRIP)	V_{SS}	$V_{SS} + 5$	
V_{FLT}	\overline{FAULT} Output Voltage	V_{SS}	V_{CC}	
V_{CAO}	Operational Amplifier Output Voltage	V_{SS}	5	
V_{CA-}	Operational Amplifier Inverting Input Voltage	V_{SS}	5	
T_A	Ambient Temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of $(V_{S0} - 5V)$ to $(V_{S0} + 600V)$. Logic state held for V_S of $(V_{S0} - 5V)$ to $(V_{S0} - V_{BS})$.

Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS1,2,3}) = 15V$, $V_{S0,1,2,3} = V_{SS}$, $C_L = 1000 \text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The dynamic electrical characteristics are defined in Figures 3 through 5.

Symbol	Parameter Definition	Figure	Value			Units	Test Conditions
			Min.	Typ.	Max.		
t_{on}	Turn-On Propagation Delay	11	500	675	850	ns	$V_{IN} = 0 \text{ \& } 5V$ $V_{S1,2,3} = 0 \text{ to } 600V$
t_{off}	Turn-Off Propagation Delay	12	300	425	550		
t_r	Turn-On Rise Time	13	—	80	125		
t_f	Turn-Off Fall Time	14	—	35	55		
t_{itrip}	ITRIP to Output Shutdown Prop. Delay	15	400	660	920		
t_{bl}	ITRIP Blanking Time	—	—	400	—		
t_{fit}	ITRIP to FAULT Indication Delay	16	335	590	845		
$t_{fit,in}$	Input Filter Time (All Six Inputs)	—	—	310	—	μs	$V_{IN}, V_{ITRIP} = 0 \text{ \& } 5V$ $V_{IN} = 0 \text{ \& } 5V$
t_{fitclr}	LIN1,2,3 to FAULT Clear Time	17	6.0	9.0	12.0		
DT	Deadtime	18	0.4	0.8	1.2	V/μs	$V_{IN}, V_{ITRIP} = 0 \text{ \& } 5V$ $V_{IN} = 0 \text{ \& } 5V$
SR+	Operational Amplifier Slew Rate (+)	19	4.4	6.2	—		
SR-	Operational Amplifier Slew Rate (-)	20	2.4	3.2	—		

Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS1,2,3}) = 15V$, $V_{S0,1,2,3} = V_{SS}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1,2,3 & LIN1,2,3. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Parameter Definition	Figure	Value			Units	Test Conditions
			Min.	Typ.	Max.		
V_{IH}	Logic "0" Input Voltage (OUT = LO)	21	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	22	—	—	0.8		
$V_{IT,TH+}$	ITRIP Input Positive Going Threshold	23	400	490	580	mV	$V_{IN} = 0V, I_O = 0A$ $V_{IN} = 5V, I_O = 0A$
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	24	—	—	100		
V_{OL}	Low Level Output Voltage, V_O	25	—	—	100	μA	$V_B = V_S = 600V$ $V_{IN} = 0V \text{ or } 5V$
I_{LK}	Offset Supply Leakage Current	26	—	—	50		
I_{QBS}	Quiescent V_{BS} Supply Current	27	—	15	30	mA	$V_{IN} = 0V \text{ or } 5V$ $V_{IN} = 0V \text{ or } 5V$
I_{QCC}	Quiescent V_{CC} Supply Current	28	—	3.0	4.0		
I_{IN+}	Logic "1" Input Bias Current (OUT = HI)	29	—	450	650	μA	$V_{IN} = 0V$ $V_{IN} = 5V$
I_{IN-}	Logic "0" Input Bias Current (OUT = LO)	30	—	225	400		
I_{ITRIP+}	"High" ITRIP Bias Current	31	—	75	150	nA	ITRIP = 5V ITRIP = 0V
I_{ITRIP-}	"Low" ITRIP Bias Current	32	—	—	100		
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	33	7.5	8.35	9.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	34	7.1	7.95	8.8		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	35	8.3	9.0	9.7		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	36	8.0	8.7	9.4		
$R_{on,FLT}$	FAULT Low On-Resistance	37	—	55	75		

Static Electrical Characteristics -- Continued

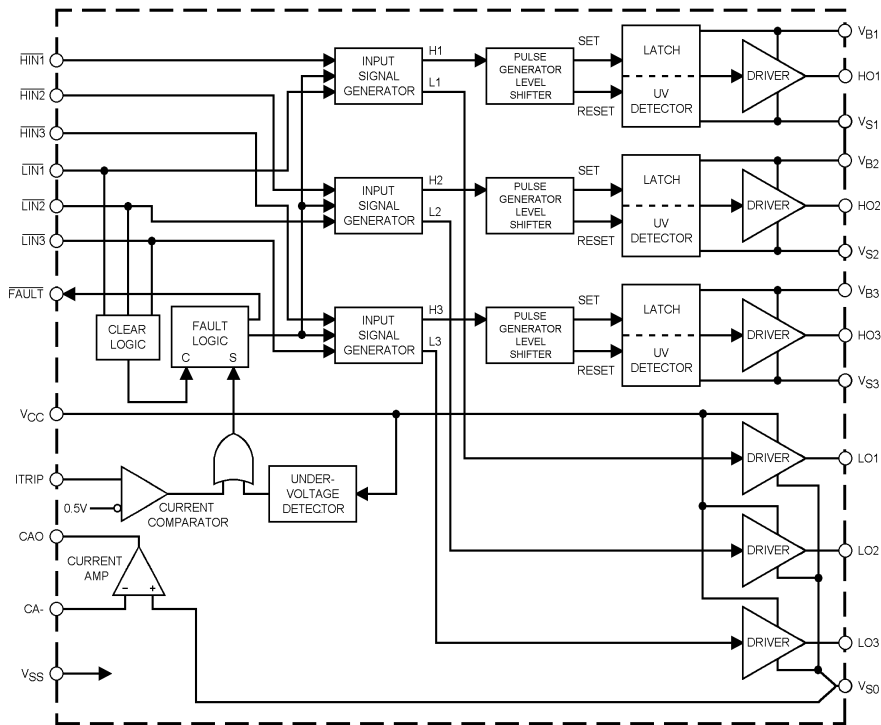
V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $HIN1,2,3$ & $LIN1,2,3$. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: $HO1,2,3$ or $LO1,2,3$.

Symbol	Parameter Definition	Figure	Value			Units	Test Conditions
			Min.	Typ.	Max.		
I_{O+}	Output High Short Circuit Pulsed Current	38	200	250	—	mA	$V_O = 0V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	39	420	500	—		$V_O = 15V$, $V_{IN} = 5V$ $PW \leq 10 \mu s$
V_{OS}	Operational Amplifier Input Offset Voltage	40	—	—	30	mV	$V_{S0} = V_{CA-} = 0.2V$
I_{CA-}	CA- Input Bias Current	41	—	—	4.0	nA	$V_{CA-} = 2.5V$
CMRR	Op. Amp. Common Mode Rejection Ratio	42	60	80	—	dB	$V_{S0} = V_{CA-} = 0.1V$ & 5V
PSRR	Op. Amp. Power Supply Rejection Ratio	43	55	75	—		$V_{S0} = V_{CA-} = 0.2V$ $V_{CC} = 10V$ & 20V
$V_{OH,AMP}$	Op. Amp. High Level Output Voltage	44	5.0	5.2	5.4	V	$V_{CA-} = 0V$, $V_{S0} = 1V$
$V_{OL,AMP}$	Op. Amp. Low Level Output Voltage	45	—	—	20	mV	$V_{CA-} = 1V$, $V_{S0} = 0V$
$I_{SRC,AMP}$	Op. Amp. Output Source Current	46	2.3	4.0	—	mA	$V_{CA-} = 0V$, $V_{S0} = 1V$ $V_{CAO} = 4V$
$I_{SRC,AMP}$	Op. Amp. Output Sink Current	47	1.0	2.1	—		$V_{CA-} = 1V$, $V_{S0} = 0V$ $V_{CAO} = 2V$
$I_{O+,AMP}$	Operational Amplifier Output High Short Circuit Current	48	—	4.5	6.5	mA	$V_{CA-} = 0V$, $V_{S0} = 5V$ $V_{CAO} = 0V$
$I_{O-,AMP}$	Operational Amplifier Output Low Short Circuit Current	49	—	3.2	5.2		$V_{CA-} = 5V$, $V_{S0} = 0V$ $V_{CAO} = 5V$

Lead Assignments

<p>28 Lead DIP</p>	<p>44 Lead PLCC w/o 12 Leads</p>	<p>28 Lead SOIC (Wide Body)</p>
IR2132	IR2132J	IR2132S
Part Number		

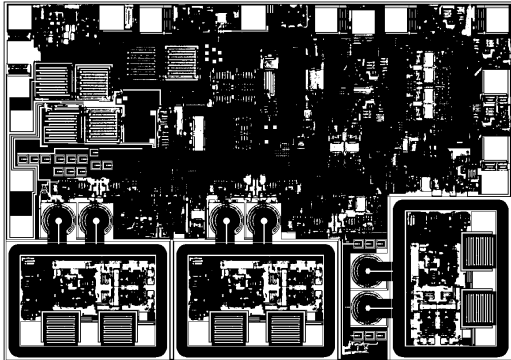
Functional Block Diagram



Lead Definitions

Lead	
Symbol	Description
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
LIN1,2,3	Logic inputs for low side gate driver output (LO1,2,3), out of phase
FAULT	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
V _{CC}	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
CAO	Output of current amplifier
CA-	Negative input of current amplifier
V _{SS}	Logic ground
V _{B1,2,3}	High side floating supplies
HO1,2,3	High side gate drive outputs
V _{S1,2,3}	High side floating supply returns
LO1,2,3	Low side gate drive outputs
V _{S0}	Low side return and positive input of current amplifier

Device Information

Process & Design Rule		HVDCMOS 4.0 μm	
Transistor Count		700	
Die Size		126 X 175 X 26 (mil)	
Die Outline			
Thickness of Gate Oxide		800Å	
Connections	Material	Poly Silicon	
	First Layer	Width	4 μm
	Layer	Spacing	6 μm
		Thickness	5000Å
Second Layer	Material	Al - Si (Si: 1.0% \pm 0.1%)	
	Width	6 μm	
	Spacing	9 μm	
	Thickness	20,000Å	
Contact Hole Dimension		8 μm X 8 μm	
Insulation Layer	Material	PSG (SiO_2)	
	Thickness	1.5 μm	
Passivation (1)	Material	PSG (SiO_2)	
	Thickness	1.5 μm	
Passivation (2)	Material	Proprietary*	
	Thickness	Proprietary*	
Method of Saw		Full Cut	
Method of Die Bond		Ablebond 84 - 1	
Wire Bond	Method	Thermo Sonic	
	Material	Au (1.0 mil / 1.3 mil)	
Leadframe	Material	Cu	
	Die Area	Ag	
	Lead Plating	Pb : Sn (37 : 63)	
Package	Types	28 Lead PDIP & SOIC / 44 Lead PLCC	
	Materials	EME6300 / MP150 / MP190	
Remarks: * Patent Pending			

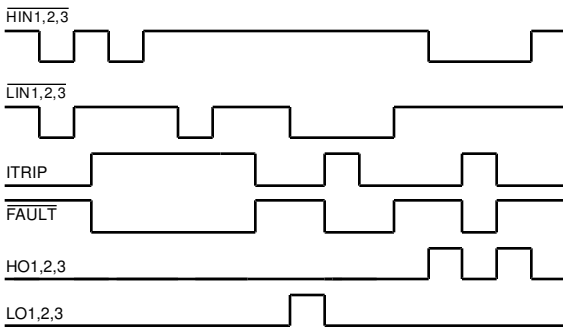


Figure 1. Input/Output Timing Diagram

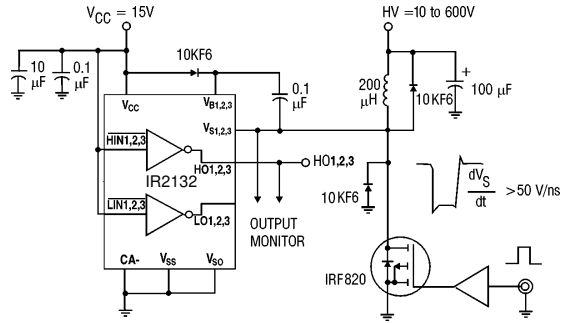


Figure 2. Floating Supply Voltage Transient Test Circuit

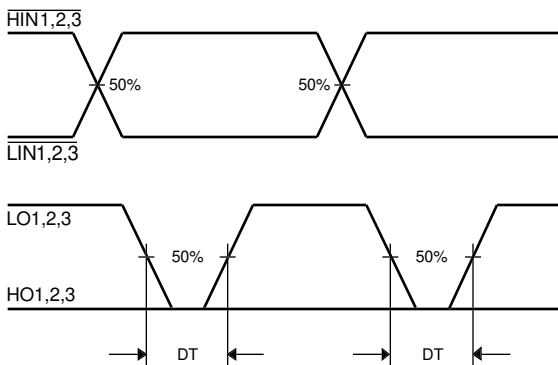


Figure 3. Deadtime Waveform Definitions

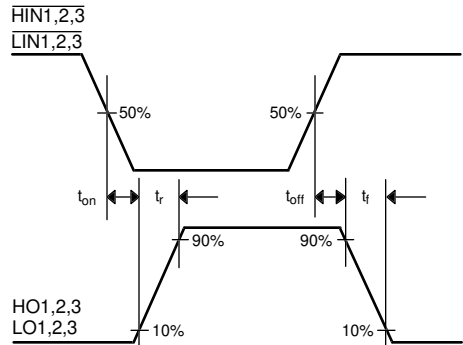


Figure 4. Input/Output Switching Time Waveform Definitions

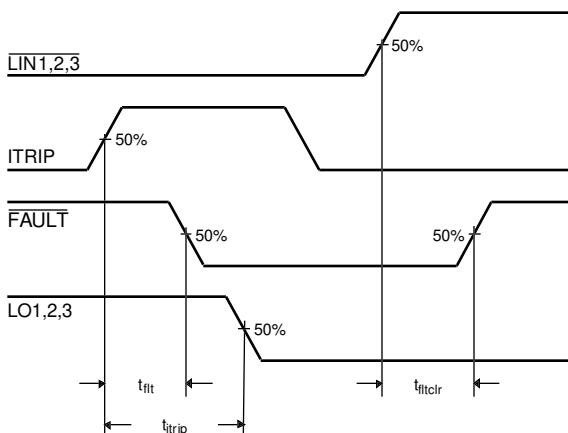


Figure 5. Overcurrent Shutdown Switching Time Waveform Definitions

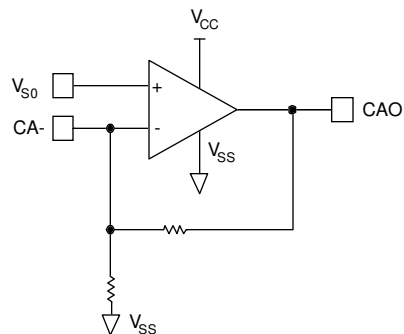


Figure 6. Diagnostic Feedback Operational Amplifier Circuit

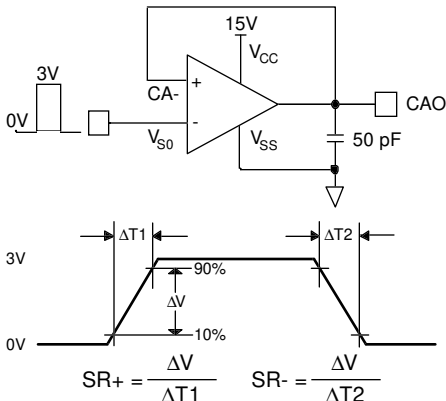


Figure 7. Operational Amplifier Slew Rate Measurement

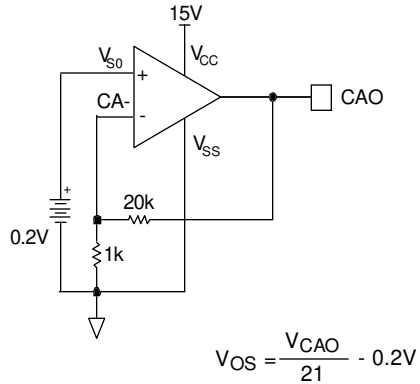
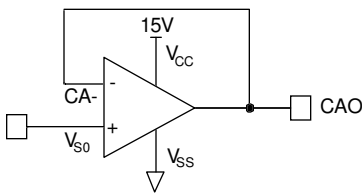


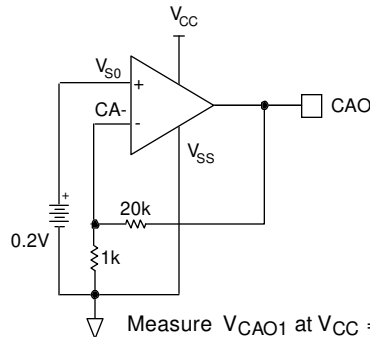
Figure 8. Operational Amplifier Input Offset Voltage Measurement



Measure V_{CAO1} at $V_{S0} = 0.1V$
 V_{CAO2} at $V_{S0} = 5V$

$$CMRR = -20 \cdot \text{LOG} \left| \frac{(V_{CAO1} - 0.1V) - (V_{CAO2} - 5V)}{4.9V} \right| \text{ (dB)}$$

Figure 9. Operational Amplifier Common Mode Rejection Ratio Measurements



Measure V_{CAO1} at $V_{CC} = 10V$
 V_{CAO2} at $V_{CC} = 20V$

$$PSRR = -20 \cdot \text{LOG} \left| \frac{V_{CAO1} - V_{CAO2}}{(10V)(21)} \right|$$

Figure 10. Operational Amplifier Power Supply Rejection Ratio Measurements

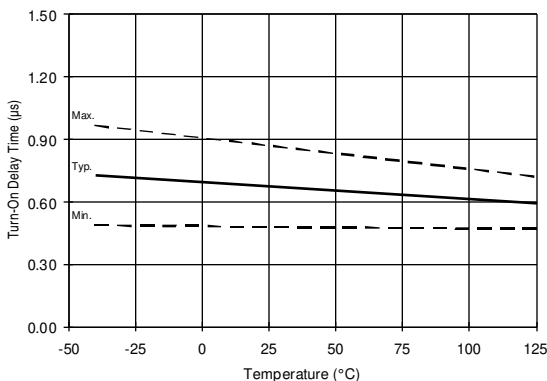


Figure 11A. Turn-On Time vs. Temperature

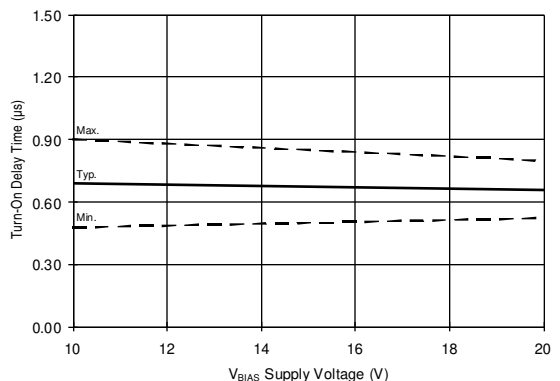


Figure 11B. Turn-On Time vs. Voltage

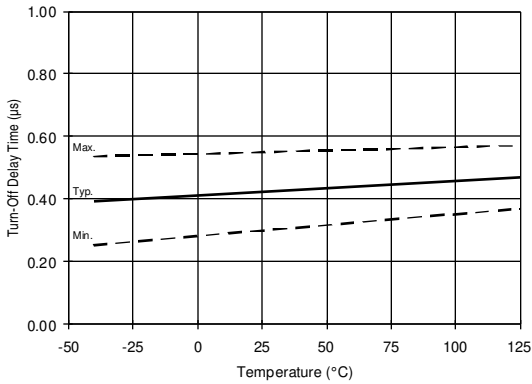


Figure 12A. Turn-Off Time vs. Temperature

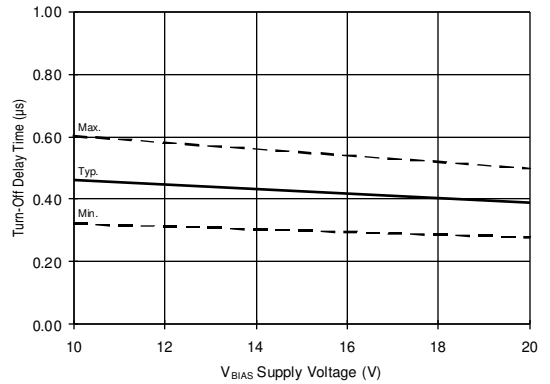


Figure 12B. Turn-Off Time vs. Voltage

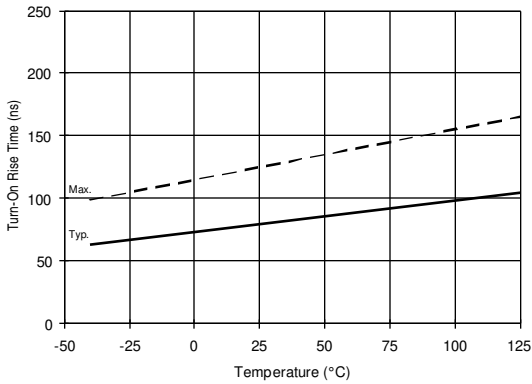


Figure 13A. Turn-On Rise Time vs. Temperature

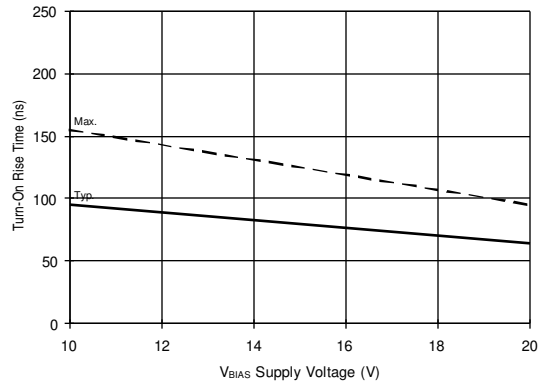


Figure 13B. Turn-On Rise Time vs. Voltage

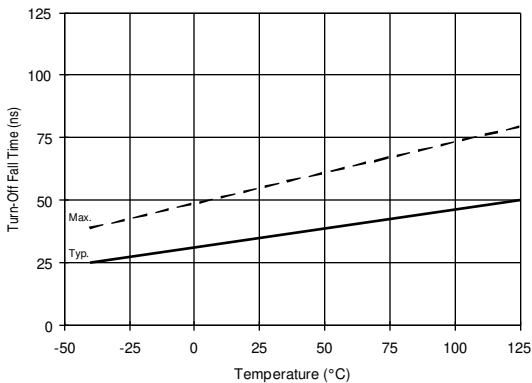


Figure 14A. Turn-Off Fall Time vs. Temperature

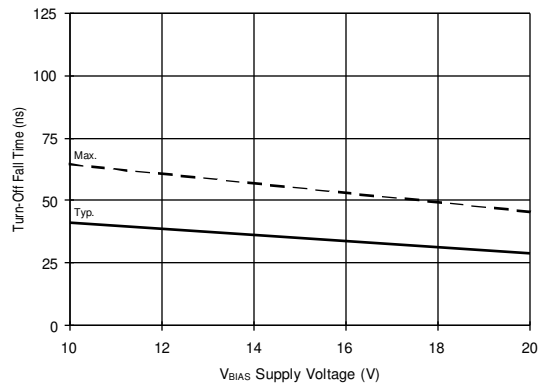


Figure 14B. Turn-Off Fall Time vs. Voltage

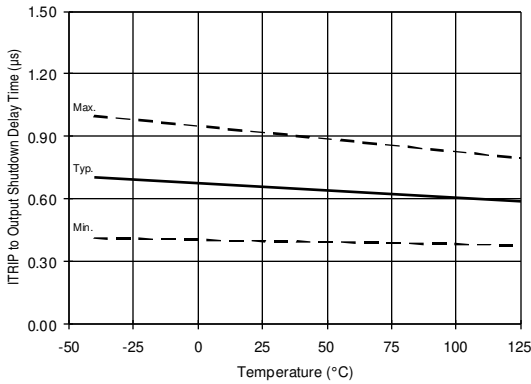


Figure 15A. ITRIP to Output Shutdown Time vs. Temperature

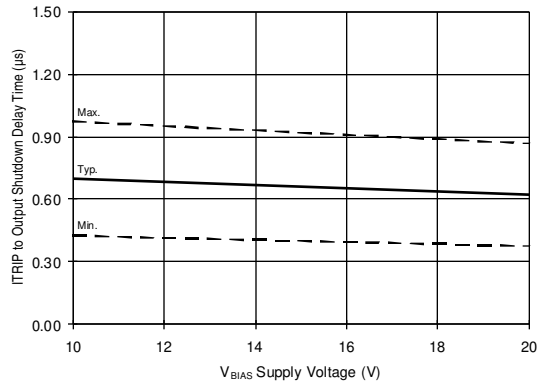


Figure 15B. ITRIP to Output Shutdown Time vs. Voltage

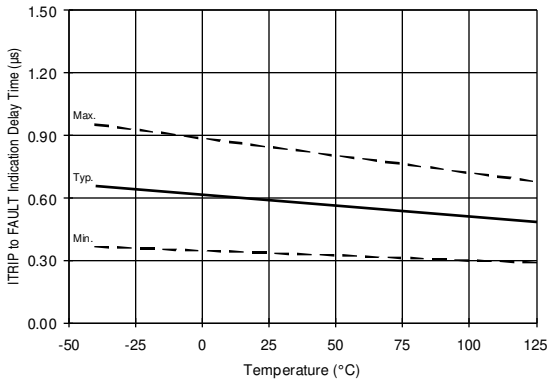


Figure 16A. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Temperature

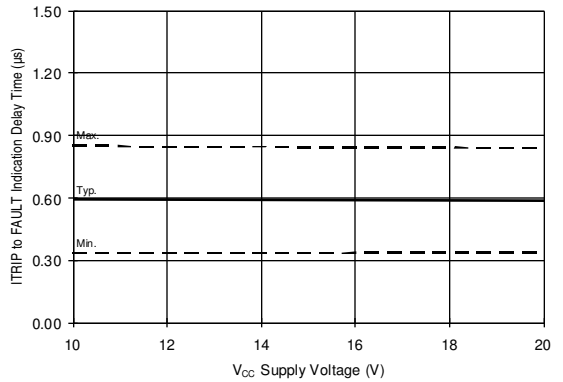


Figure 16B. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Voltage

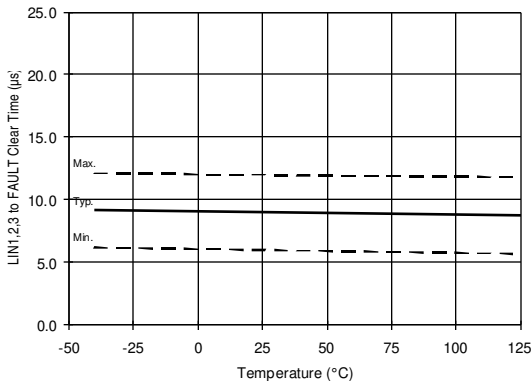


Figure 17A. $\overline{\text{LIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time vs. Temperature

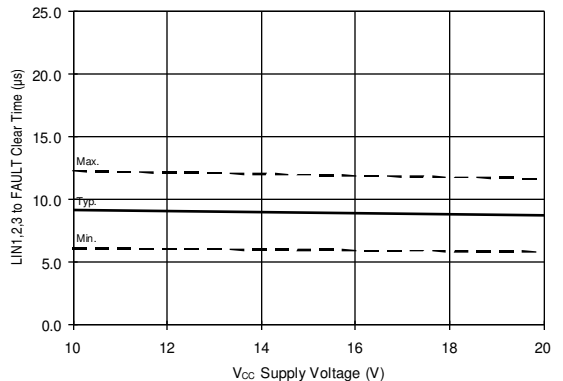


Figure 17B. $\overline{\text{LIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time vs. Voltage

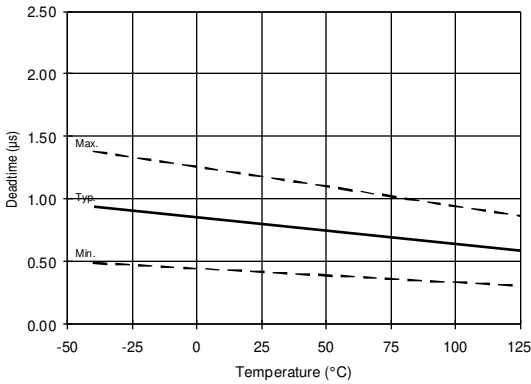


Figure 18A. Deadtime vs. Temperature

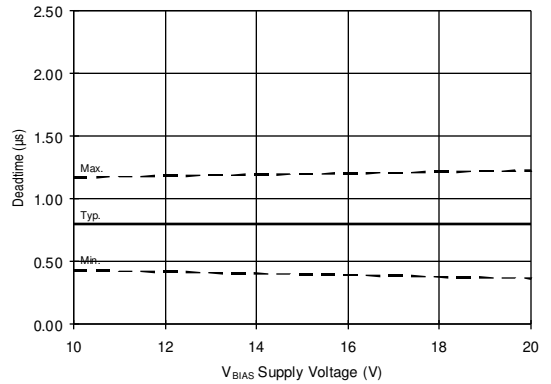


Figure 18B. Deadtime vs. Voltage

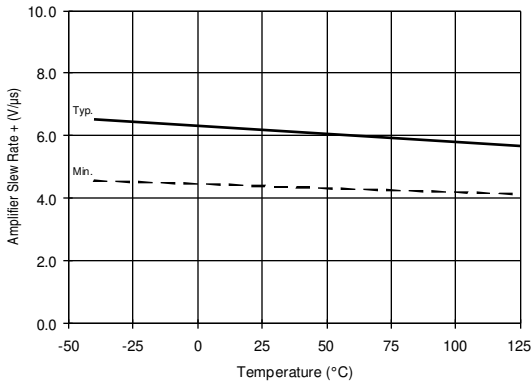


Figure 19A. Amplifier Slew Rate (+) vs. Temperature

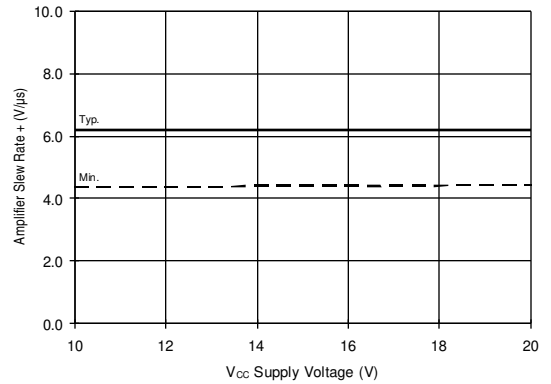


Figure 19B. Amplifier Slew Rate (+) vs. Voltage

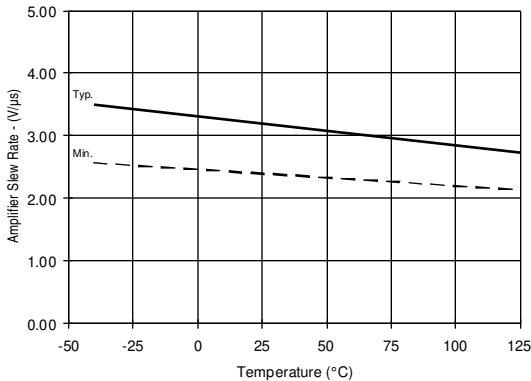


Figure 20A. Amplifier Slew Rate (-) vs. Temperature

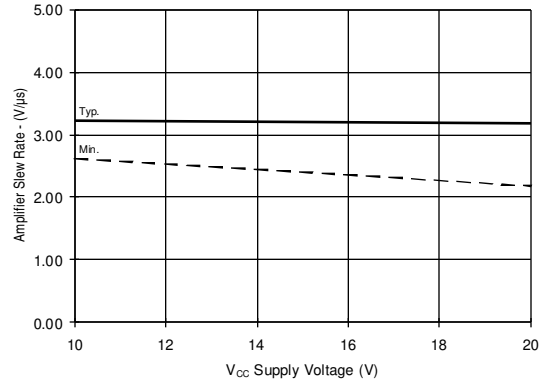


Figure 20B. Amplifier Slew Rate (-) vs. Voltage

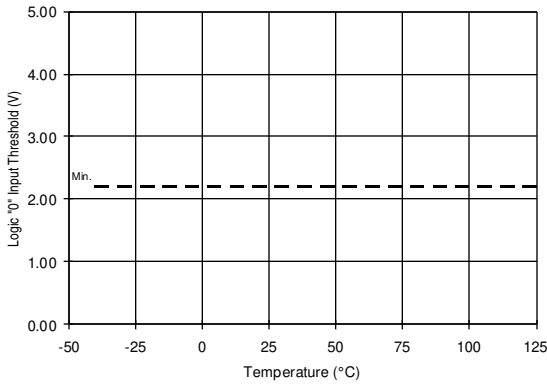


Figure 21A. Logic "0" Input Threshold vs. Temperature

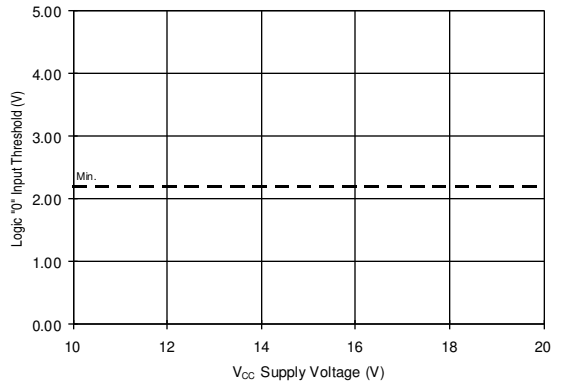


Figure 20B. Logic "0" Input Threshold vs. Voltage

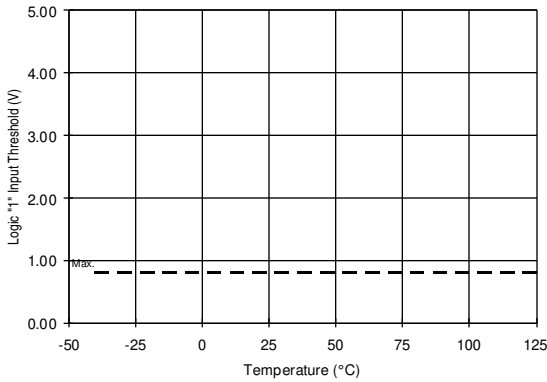


Figure 22A. Logic "1" Input Threshold vs. Temperature

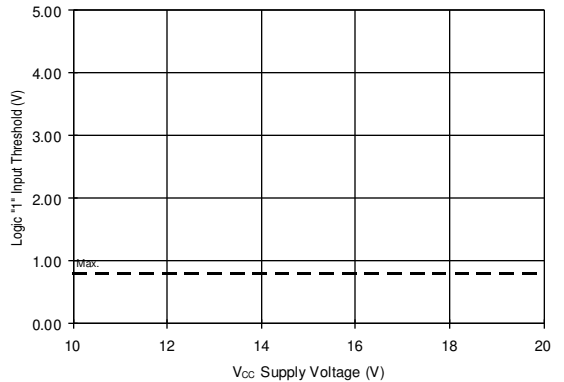


Figure 22B. Logic "1" Input Threshold vs. Voltage

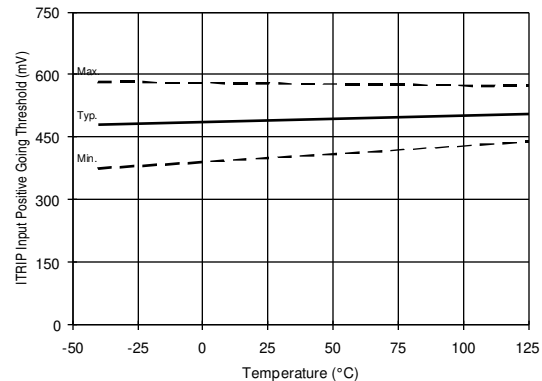


Figure 23A. ITRIP Input Positive Going Threshold vs. Temperature

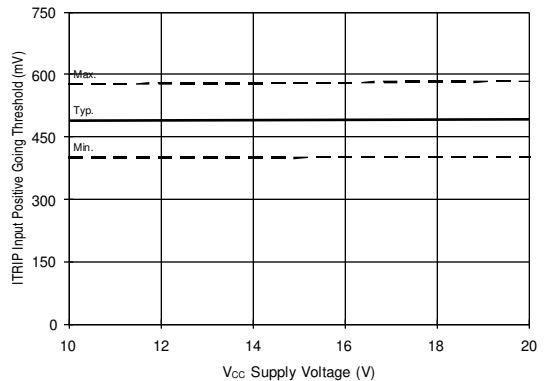


Figure 23B. ITRIP Input Positive Going Threshold vs. Voltage

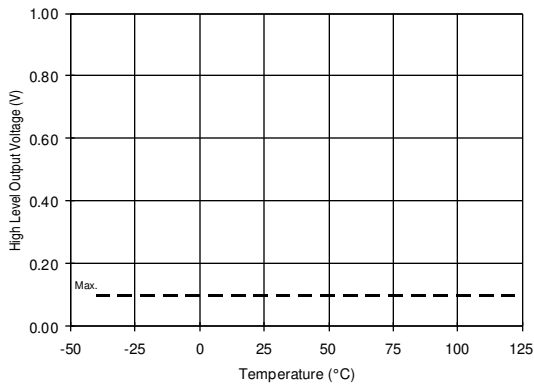


Figure 24A. High Level Output vs. Temperature

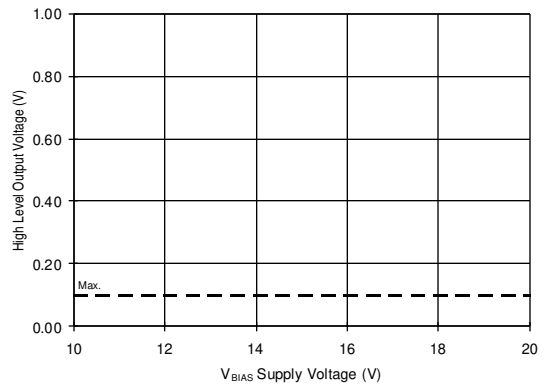


Figure 24B. High Level Output vs. Voltage

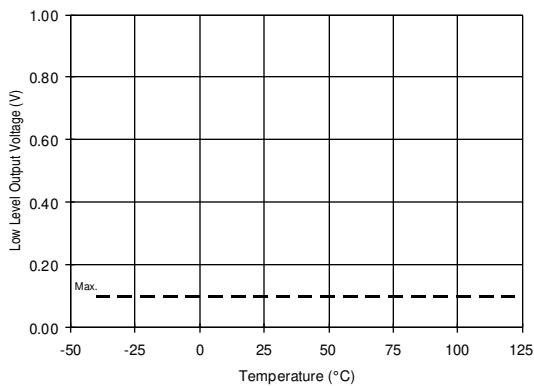


Figure 25A. Low Level Output vs. Temperature

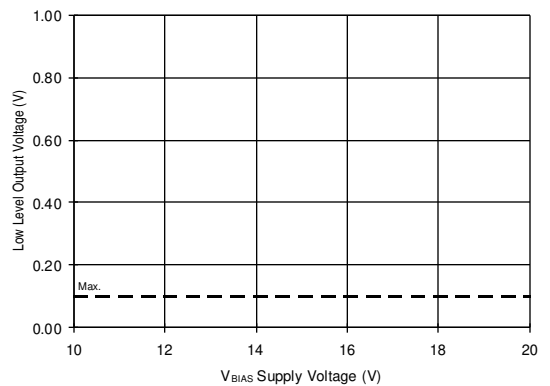


Figure 25B. Low Level Output vs. Voltage

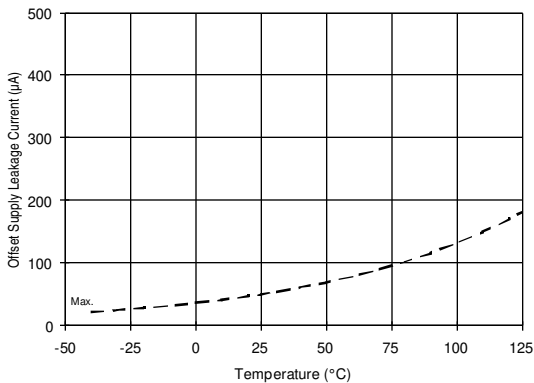


Figure 26A. Offset Supply Leakage Current vs. Temperature

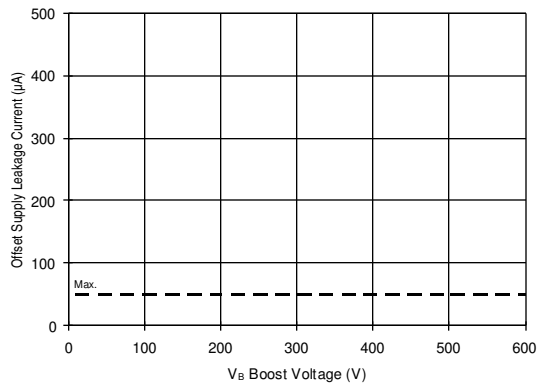


Figure 26B. Offset Supply Leakage Current vs. Voltage

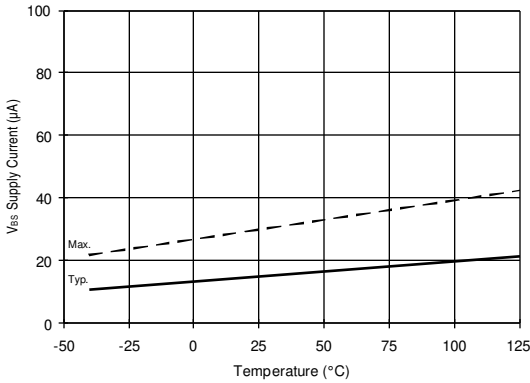


Figure 27A. V_{BS} Supply Current vs. Temperature

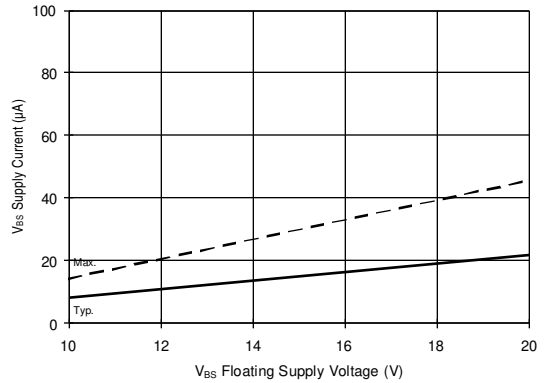


Figure 27B. V_{BS} Supply Current vs. Voltage

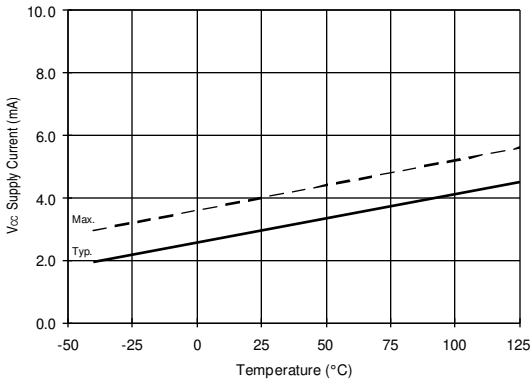


Figure 28A. V_{CC} Supply Current vs. Temperature

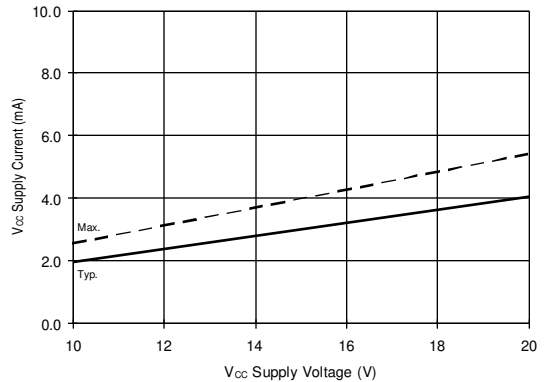


Figure 28B. V_{CC} Supply Current vs. Voltage

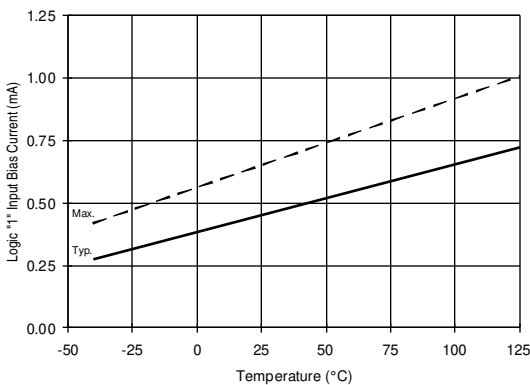


Figure 29A. Logic "1" Input Current vs. Temperature

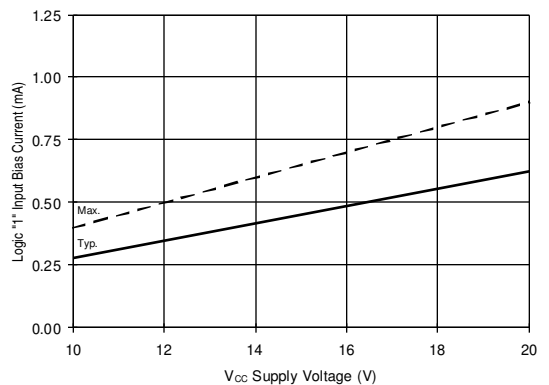


Figure 29B. Logic "1" Input Current vs. Voltage

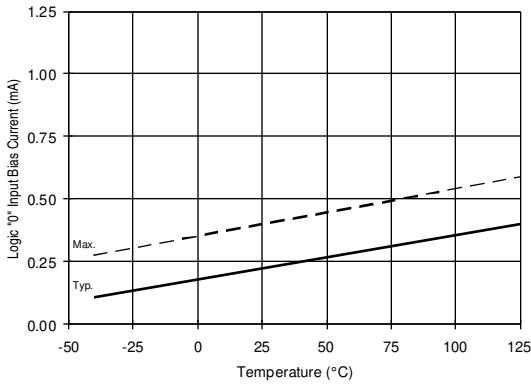


Figure 30A. Logic "0" Input Current vs. Temperature

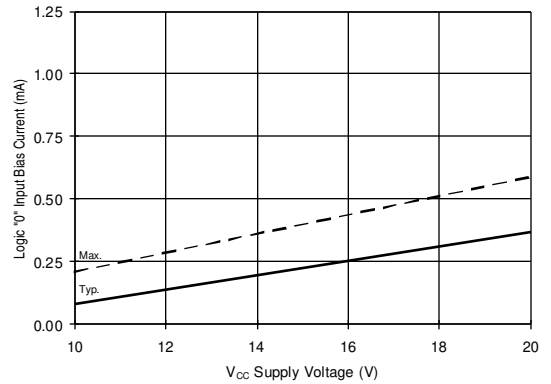


Figure 30B. Logic "0" Input Current vs. Voltage

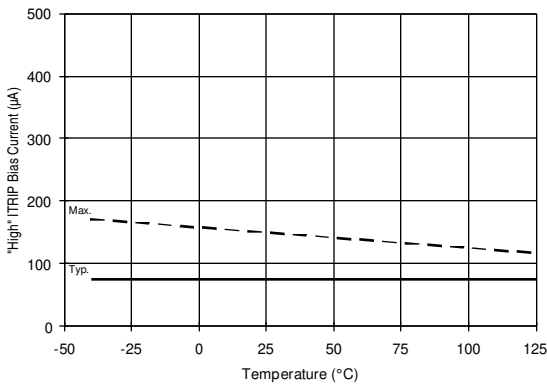


Figure 31A. "High" ITRIP Current vs. Temperature

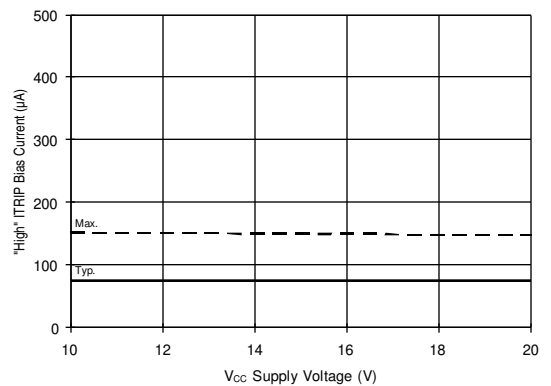


Figure 31B. "High" ITRIP Current vs. Voltage

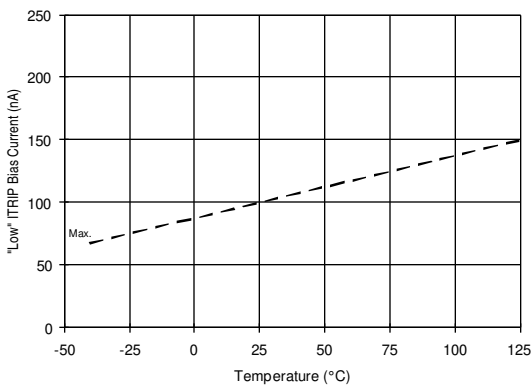


Figure 32A. "Low" ITRIP Current vs. Temperature

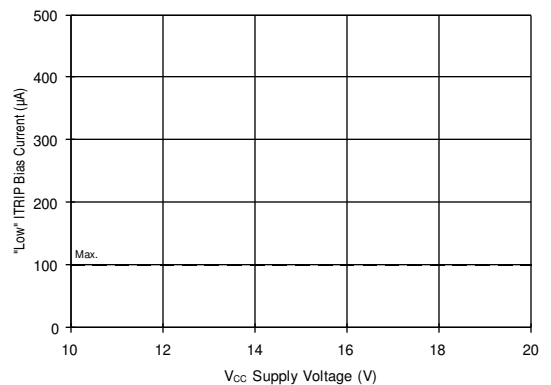


Figure 32B. "Low" ITRIP Current vs. Voltage

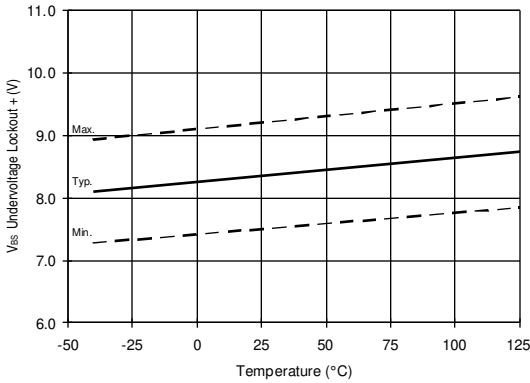


Figure 33. V_{BS} Undervoltage (+) vs. Temperature

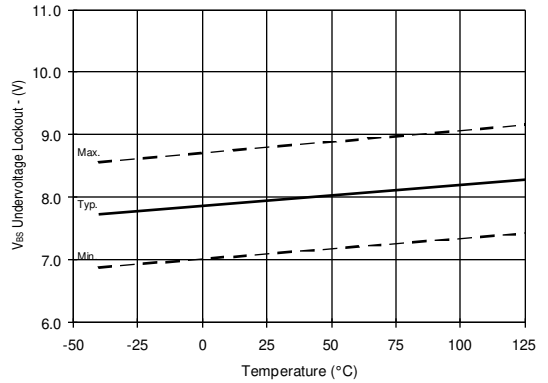


Figure 34. V_{BS} Undervoltage (-) vs. Temperature

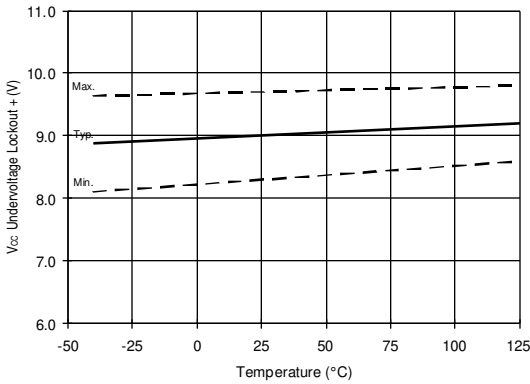


Figure 35. V_{CC} Undervoltage (+) vs. Temperature

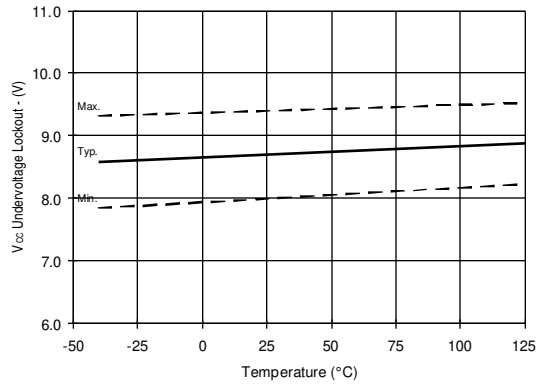


Figure 36. V_{CC} Undervoltage (-) vs. Temperature

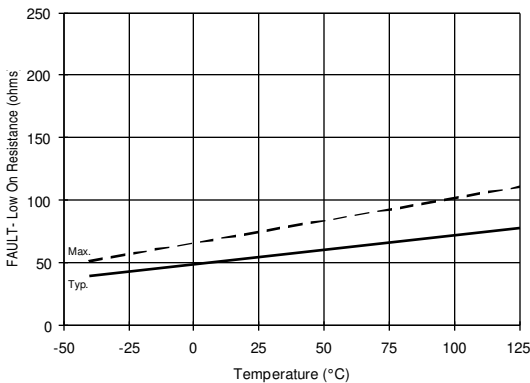


Figure 37A. $\overline{\text{FAULT}}$ Low On Resistance vs. Temperature

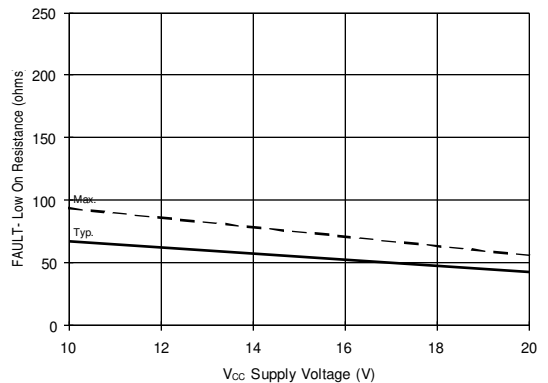


Figure 37B. $\overline{\text{FAULT}}$ Low On Resistance vs. Voltage

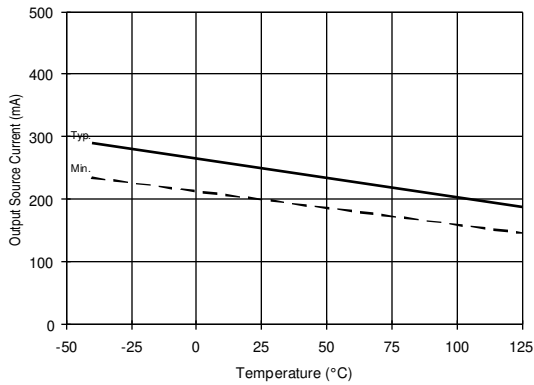


Figure 38A. Output Source Current vs. Temperature

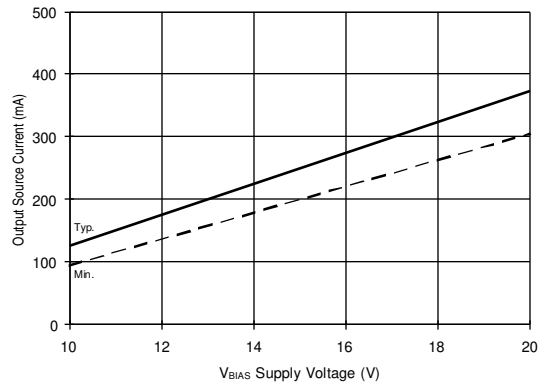


Figure 38B. Output Source Current vs. Voltage

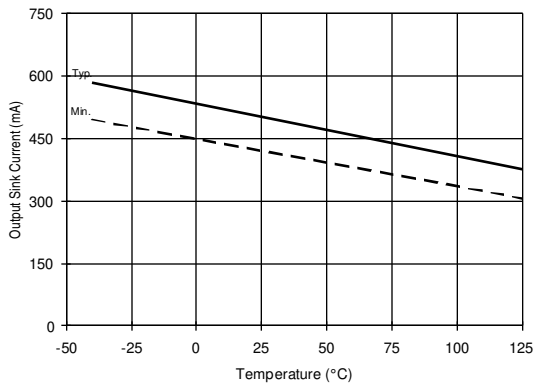


Figure 39A. Output Sink Current vs. Temperature

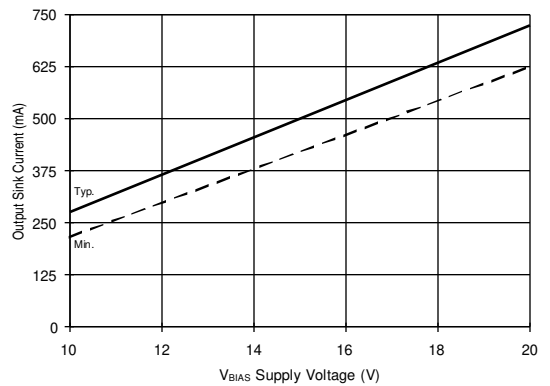


Figure 39B. Output Sink Current vs. Voltage

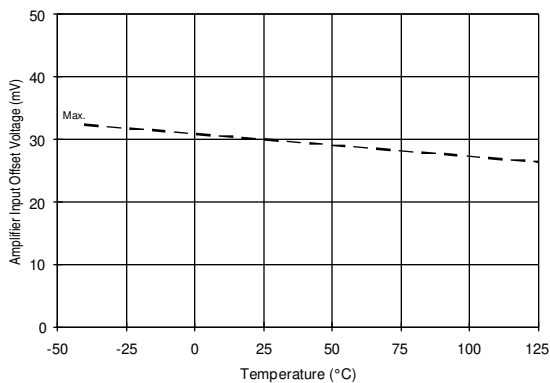


Figure 40A. Amplifier Input Offset vs. Temperature

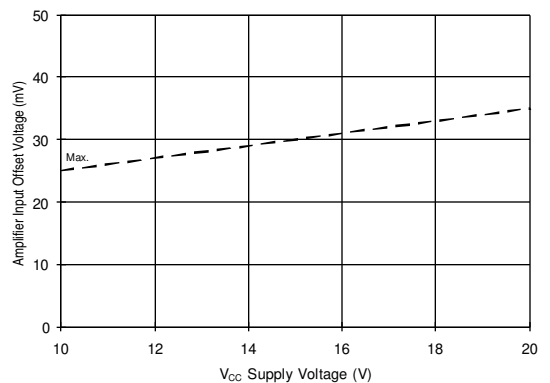


Figure 40B. Amplifier Input Offset vs. Voltage

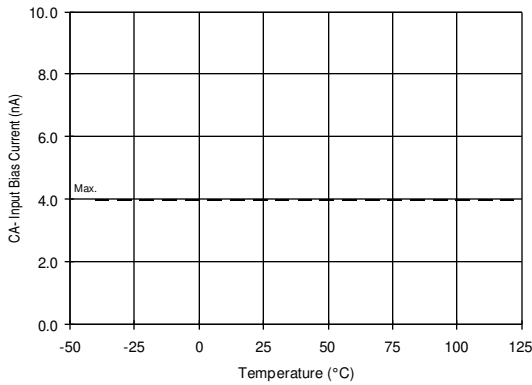


Figure 41A. CA- Input Current vs. Temperature

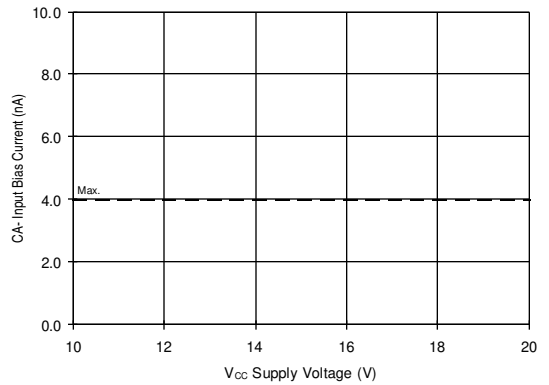


Figure 41B. CA- Input Current vs. Voltage

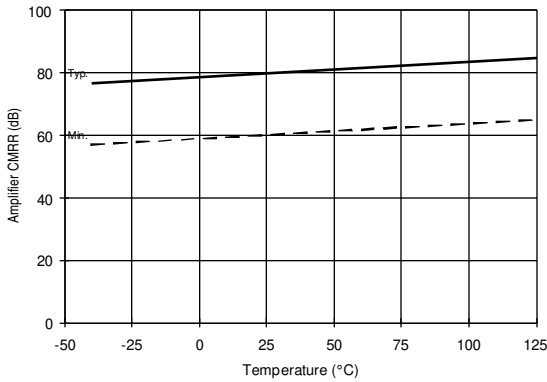


Figure 42A. Amplifier CMRR vs. Temperature

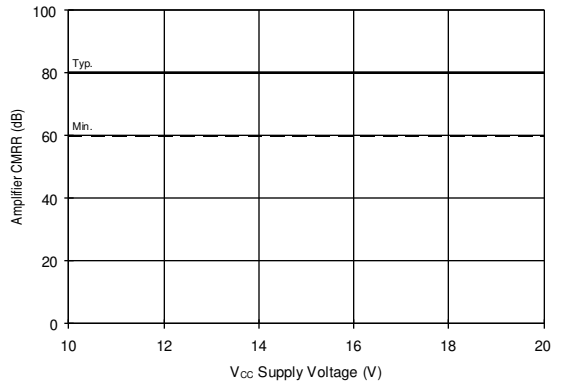


Figure 42B. Amplifier CMRR vs. Voltage

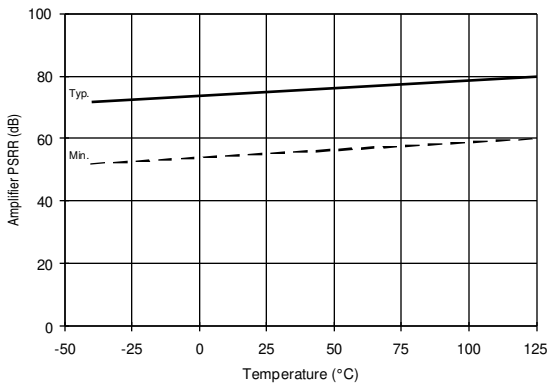


Figure 43A. Amplifier PSRR vs. Temperature

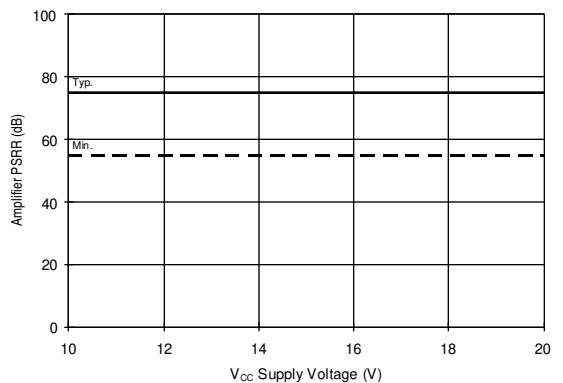


Figure 43B. Amplifier PSRR vs. Voltage

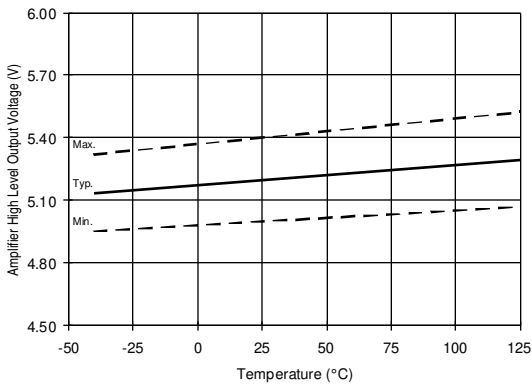


Figure 44A. Amplifier High Level Output vs. Temperature

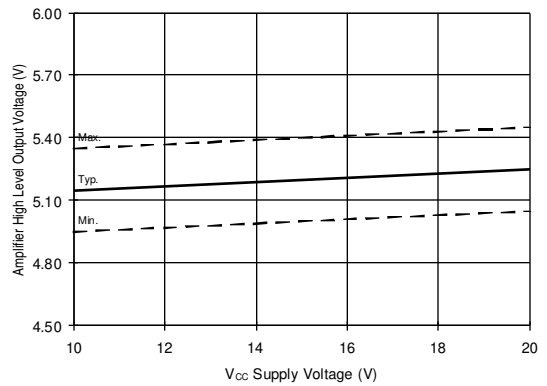


Figure 44B. Amplifier High Level Output vs. Voltage

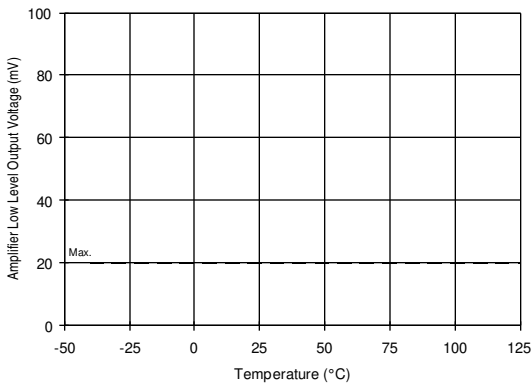


Figure 45A. Amplifier Low Level Output vs. Temperature

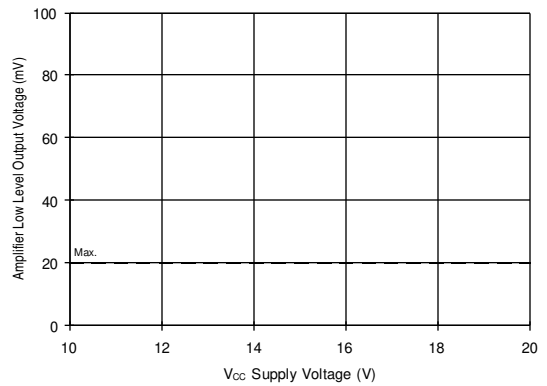


Figure 45B. Amplifier Low Level Output vs. Voltage

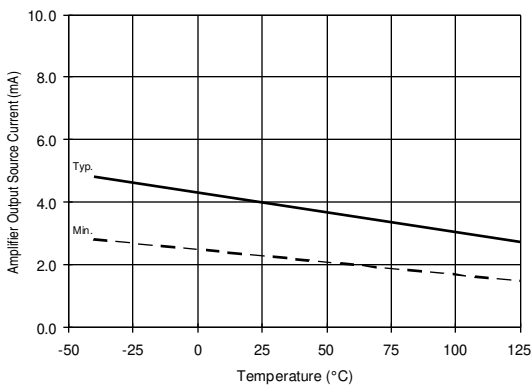


Figure 46A. Amplifier Output Source Current vs. Temperature

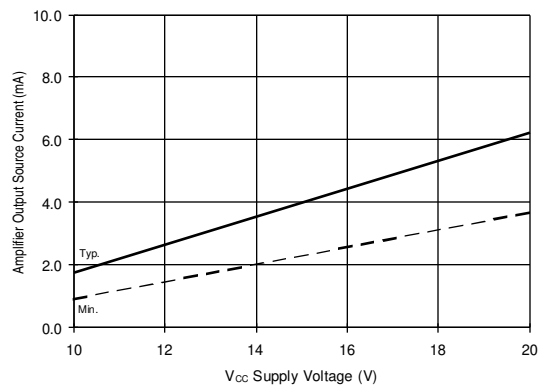


Figure 46B. Amplifier Output Source Current vs. Voltage

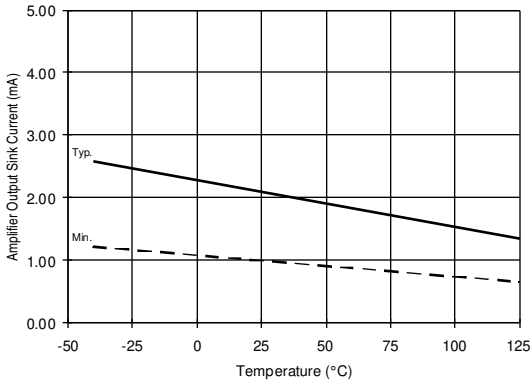


Figure 47A. Amplifier Output Sink Current vs. Temperature

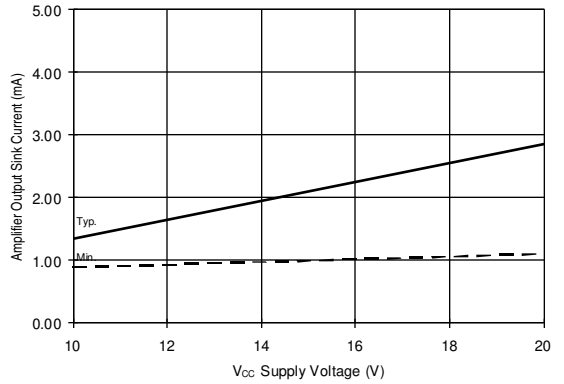


Figure 47B. Amplifier Output Sink Current vs. Voltage

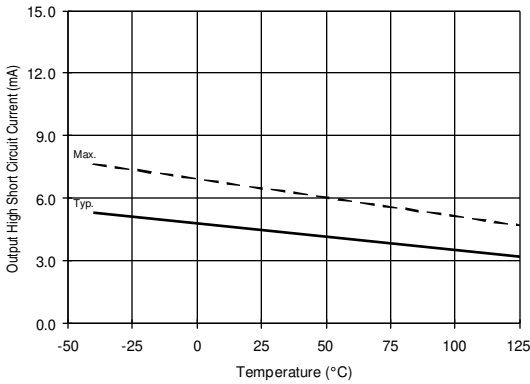


Figure 48A. Amplifier Output High Short Circuit Current vs. Temperature

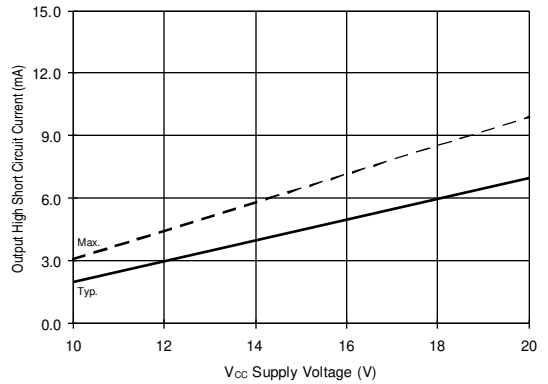


Figure 48B. Amplifier Output High Short Circuit Current vs. Voltage

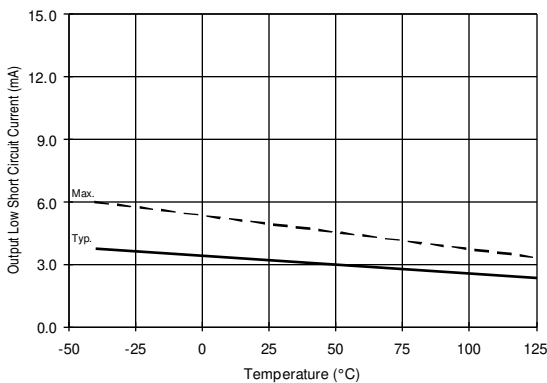


Figure 49A. Amplifier Output Low Short Circuit Current vs. Temperature

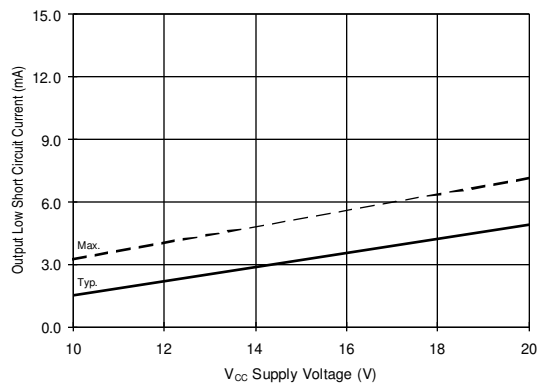


Figure 49B. Amplifier Output Low Short Circuit Current vs. Voltage

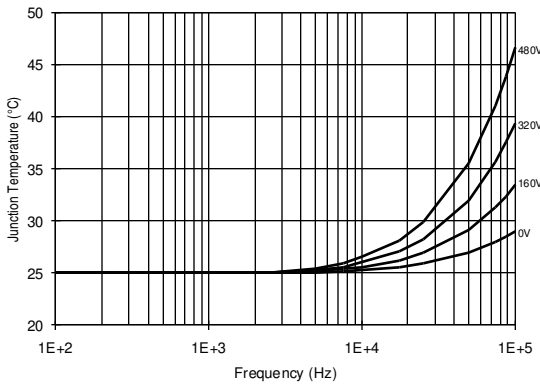


Figure 50. IR2132 T_J vs. Frequency (IRF820)
 $R_{GATE} = 33\Omega, V_{CC} = 15V$

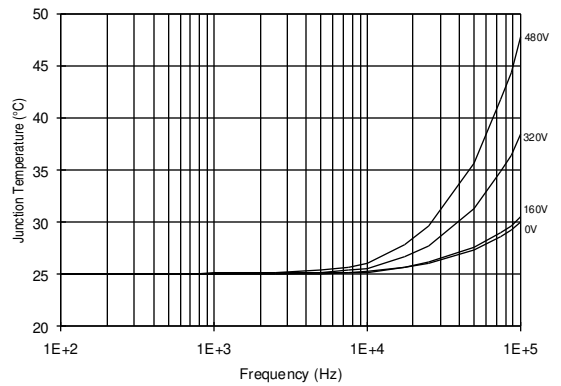


Figure 51. IR2132 T_J vs. Frequency (IRF830)
 $R_{GATE} = 20\Omega, V_{CC} = 15V$

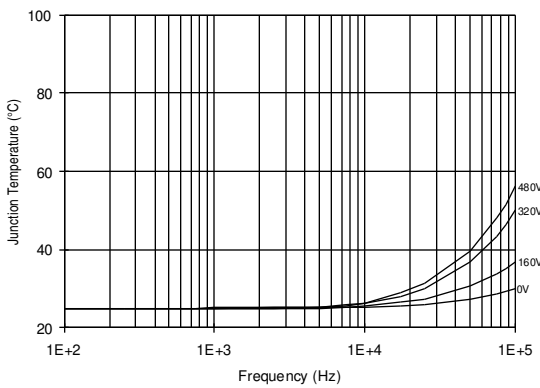


Figure 52. IR2132 T_J vs. Frequency (IRF840)
 $R_{GATE} = 15\Omega, V_{CC} = 15V$

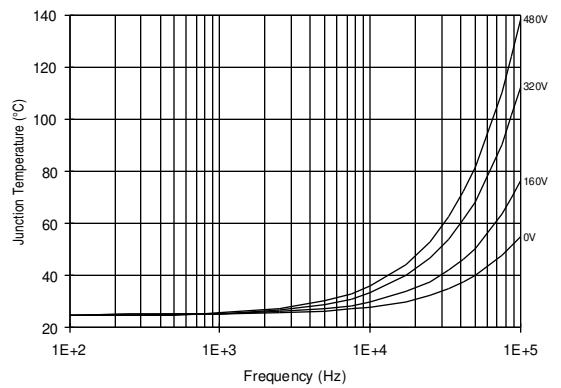


Figure 53. IR2132 T_J vs. Frequency (IRF450)
 $R_{GATE} = 10\Omega, V_{CC} = 15V$

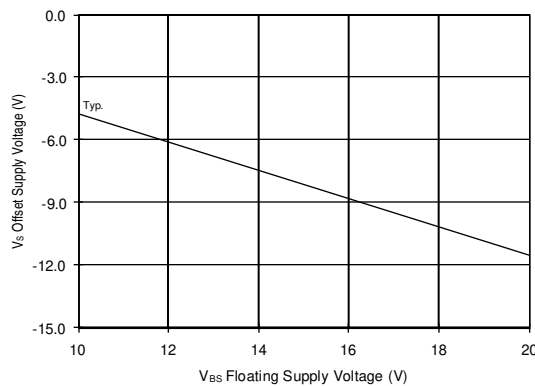


Figure 54. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage