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System Clock for Embedded AMDTM based Systems

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Recommended Application:

AMD M690T/780E systems

Output Features:

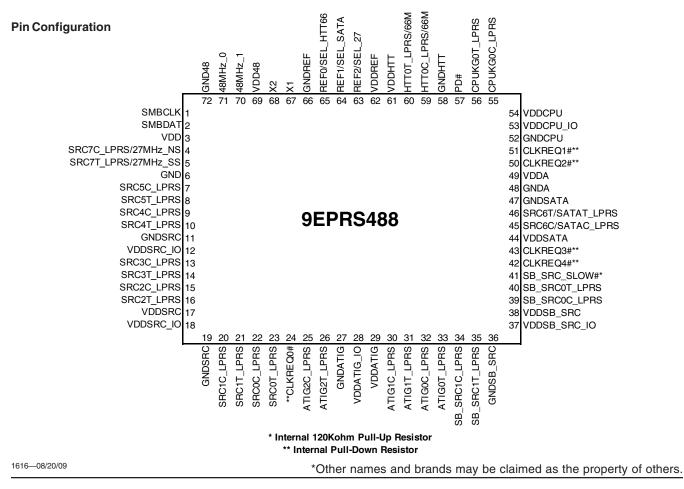
- Integrated series resistors on all differential outputs.
- 1 Greyhound compatible low-power CPU pair
- 6 low-power differential SRC pairs
- 2 low-power differential chipset SouthBridge SRC pairs
- 1 Selectable low-power differential 100MHz non-spread SATA/ SRC output
- 1 Selectable low-power differential SRC / 27MHz Single Ended output
- 1 Selectable HT3 100MHz low-power differential hypertransport clock / HT66MHz Single Ended output
- 2 48MHz USB clock
- 3 14.318MHz Reference clock
- 3 low-power differential ATIG pairs
- 5- Dedicated CLKREQ# pins

Key Specifications:

- CPU outputs cycle-to-cycle jitter < 150ps
- SRC outputs cycle-to-cycle jitter < 125ps
- SB_SRC outputs cycle-to-cycle jitter < 125ps
- +/- 100ppm frequency accuracy on CPU, SRC, ATIG
- Oppm frequency accuracy on 48MHz

Features/Benefits:

- Power Saving Features:
 SB_SRC_SLOW# input to throttle Chipset clocks (SB_SRC) to 80% of normal.
 Optional Separate supply rail for SRC low Voltage I/O
 ~33% power saving when 1.5V is used for this rail
 - Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- External crystal load capacitors for maximum frequency accuracy



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Pin Description

1 SMBCLK IN Clock pin of SMBus circuity, SV biernnt. 3 VDD PVR Power supply for SMBus circuity, SV biernnt. 3 VDD PVR Power supply for SMBus circuity, SV biernnt. 4 SRC7_LPRS,27MHz, SS OUT Two circuits of SMBus circuity, SV biernnt. 5 SRC7_LPRS,27MHz, SS OUT Complement clock of nor yower differential SRC clock pair. (no 500hm shunt resider to GND and no 33 ohm actics resider needed);27MHz 3.3 VS single-ended greading output for discrete graphics. 6 GND OND Complement clock of low power differential SRC clock pair. (no 500hm shunt resider to GND and no 33 ohm series resider needed). 7 SRC5C_LPRS OUT Complement clock of low power differential SRC clock pair. (no 500hm shunt resider to GND and no 33 ohm series resider needed). 8 SRC4_LPRS OUT Two clock of low power differential SRC clock pair. (no 500hm shunt resider to GND and no 33 ohm series resider needed). 10 SRC3_LPRS OUT Two clock of low power differential SRC clock pair. (no 500hm shunt resider to GND and no 33 ohm series resider needed). 11 GNDSRC GND Geude fire needed. 12 VDDSRC OUT Two clock of low power differential SRC clock	PIN #	PIN NAME	PIN TYPE	DESCRIPTION
VDD PWR Power supply for SRC 72/WHz SRC 7_LPRS27MH2_NS OUT There dock of low power differential SRC dock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)/27MH2 3.3 V Single-ended non-spread output of discrete graphics ohm series resistor needed)/27MH2 3.3 V Single-ended spreading output for discrete graphics SRC 5_LPRS OUT Complement dock of low power differential SRC dock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) SRC 5_LPRS OUT True dock of low power differential SRC dock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) SRC 4_LPRS OUT Complement dock of low power differential SRC dock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) VDDSRC OUT Complement dock of low power differential SRC dock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) VDDSRC OUT True dock of low power differential SRC dock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) VDSRC OUT Complement dock of low power differential SRC dock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) VDDSRC OUT Complement dock of low power differential SRC dock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) SRC LPRS OUT True dock of low power differential SRC dock				
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9 BMC/C_LPHS/C/MHZ_NS OUT Series resistor needed/J27MH2.3 3/V Single-ended non-spread outputs for discrete graphics 6 SRC7T_LPRS/27MHZ_SS OUT Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed/J27MH2.3.3/V Single-ended spreading output for discrete graphics 7 SRCSC_LPRS OUT Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed/) 8 SRCST_LPRS OUT Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed/) 9 SRC4C_LPRS OUT Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed/) 10 SRC3C_LPRS OUT True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed/) 11 RNDSRC GND Grouple informatiok GR clouputs. 12 VDDSRC IO PWP PWP Group series resistor needed/) 13 SRC3C_LPRS OUT Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed/) 14 SRC3T_LPRS OUT	3	VDD	PWR	Power supply for SRC7/27MHz
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14 SRC31_LPRS OUT series resistor needed) 15 SRC2_LPRS OUT Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 16 SRC2T_LPRS OUT True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 17 VDDSRC PWR Supply for SRC core, 3.3V nominal 18 VDDSRC_IO PWR Power supply for differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 20 SRC1C_LPRS OUT Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 21 SRC0C_LPRS OUT Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 23 SRC0T_LPRS OUT Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 24 **CLKREQ0# IN Clock Request pin for SRC0 outputs. If output is selected for control, then that output is controlled as to lows: 0 = enabled, 1 = Low-Low Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 24 **CLKREQ0# IN True cl				
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16 SRC1_LPRS OUT series resistor needed) 17 VDDSRC_IO PWR Supply for SRC core, 3.3 V nominal 18 VDDSRC_IO PWR Power supply for differential SRC outputs. 20 SRC1C_LPRS OUT Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 21 SRC1T_LPRS OUT True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 22 SRC0T_LPRS OUT Complement clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 23 SRC0T_LPRS OUT True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 24 **CLKREQO# IN To clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 25 ATIG2C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 26 ATIG2C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 26 ATIG2C_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 27 GNDATIG G	10		0.UT	
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21 Series resistor needed) 22 SRCOC_LPRS OUT Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 23 SRCOT_LPRS OUT True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 24 **CLKREQ0# IN Clock Request pin for SRC0 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low 25 ATIG2C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 26 ATIG2T_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 27 GNDATIG GND Ground pin for the ATIG outputs 28 VDDATIG_IO PWR Power supply for differential ATIG outputs, nominal 1.05V to 3.3V 29 VDDATIG PWR Power supply for differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 31 ATIG1C_LPRS OUT True clock folow-power differential push-pull	21	SBC1T LPBS	OUT	True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm
22 SRCOC_LPRS OUT ohm series resistor needed) 23 SRCOT_LPRS OUT True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 24 **CLKREQ0# IN Clock Request pin for SRC0 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low 25 ATIG2C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 26 ATIG2C_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 27 GNDATIG GND Ground pin for the ATIG outputs, nominal 1.05V to 3.3V 28 VDDATIG_IO PWR Power supply for ATIG core, nominal 1.05V to 3.3V 29 VDDATIG PWR Power supply for ATIG core, nominal 3.3V 30 ATIG1C_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 31 ATIG1C_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no	21		001	
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26ATIG2T_LPRSOUTTrue clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)27GNDATIGGNDGround pin for the ATIG outputs28VDDATIG_IOPWRPower supply for differential ATIG outputs, nominal 1.05V to 3.3V29VDDATIGPWRPower supply for ATIG core, nominal 3.3V30ATIG1C_LPRSOUTComplementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)31ATIG1T_LPRSOUTTrue clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)32ATIG0C_LPRSOUTComplementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)33ATIG0T_LPRSOUTTrue clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)34SB_SRC1C_LPRSOUTTrue clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)35SB_SRC1T_LPRSOUTTrue clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)	25	ATIG2C_LPRS	OUT	
26 ATIG21_LPRS OUT 500hm shunt resistor to GND and no 33 ohm series resistor needed) 27 GNDATIG GND Ground pin for the ATIG outputs 28 VDDATIG_IO PWR Power supply for differential ATIG outputs, nominal 1.05V to 3.3V 29 VDDATIG PWR Power supply for ATIG core, nominal 3.3V 30 ATIG1C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 31 ATIG1T_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 32 ATIG0C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIG0T_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT True clock of low power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT Complement clock of low power differential Chipset-to-Chipset SRC cloc				
27 GNDATIG GND Ground pin for the ATIG outputs 28 VDDATIG_IO PWR Power supply for differential ATIG outputs, nominal 1.05V to 3.3V 29 VDDATIG PWR Power supply for ATIG core, nominal 3.3V 30 ATIG1C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 31 ATIG1T_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 32 ATIG0C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIG0T_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIG0T_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 35 SB_SRC1T_LPRS OUT <td>26</td> <td>ATIG2T_LPRS</td> <td>OUT</td> <td></td>	26	ATIG2T_LPRS	OUT	
28 VDDATIG_IO PWR Power supply for differential ATIG outputs, nominal 1.05V to 3.3V 29 VDDATIG PWR Power supply for ATIG core, nominal 3.3V 30 ATIG1C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 31 ATIG1T_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 32 ATIG0C_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIG0C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIG0T_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm serie	27	GNDATIG	GND	· · · · · · · · · · · · · · · · · · ·
29 VDDATIG PWR Power supply for ATIG core, nominal 3.3V 30 ATIG1C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 31 ATIG1T_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 32 ATIG0C_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIG0C_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIG0T_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)				
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30 ATIGIC_LPRS OUT resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 31 ATIGIT_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 32 ATIGOC_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 33 ATIGOT_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIGOT_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)				11,2
31 ATIGHT_LPRS OUT 500hm shunt resistor to GND and no 33 ohm series resistor needed) 32 ATIGOC_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 33 ATIGOT_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIGOT_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)	30	ATIG1C_LPRS	001	
31 ATIGHT_LPRS OUT 500hm shunt resistor to GND and no 33 ohm series resistor needed) 32 ATIGOC_LPRS OUT Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor needed) 33 ATIGOT_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIGOT_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)			0.UT	True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no
32 ATIGOC_LPRS OUT resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 33 ATIGOT_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)	31	ATIGTT_LPRS	001	
33 ATIGOT_LPRS OUT True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)	00			Complementary clock of low-power differential push-pull PCI-Express pair with integrated series
33 A HigoT_LPRS OUT 500hm shunt resistor to GND and no 33 ohm series resistor needed) 34 SB_SRC1C_LPRS OUT Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed) 35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm series resistor needed)	32	ATIGOC_LPRS	001	resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
34 SB_SRC1C_LPRS OUT Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) 35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)	22			True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no
34 SB_SRC1C_LPRS OUT to GND and no 33 ohm series resistor needed 35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed	33	LERS	001	50ohm shunt resistor to GND and no 33 ohm series resistor needed)
35 SB_SRC1T_LPRS OUT True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed	24			Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor
and no 33 ohm series resistor needed	34		001	
and no 33 onm series resistor needed	35	SB_SBC1T_LPBS		True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND
36 GNDSB_SRC GND Ground pin for the SB_SRC outputs	35		001	and no 33 ohm series resistor needed
	36	GNDSB_SRC	GND	Ground pin for the SB_SRC outputs



Pin Description (Continued)

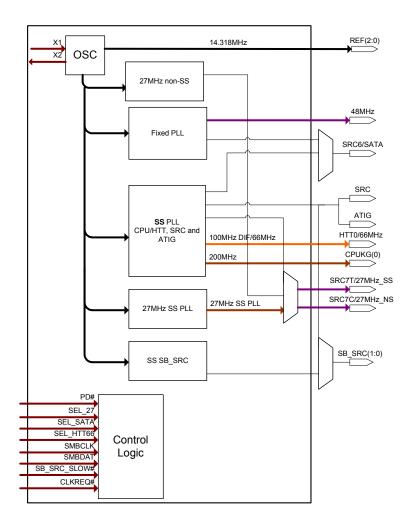
38 V 39 S 40 S 41 S 42 C 43 C 44 V 45 S 46 S 47 C 48 C	PIN NAME VDDSB_SRC_IO VDDSB_SRC SB_SRCOC_LPRS SB_SRCOT_LPRS SB_SRC_SLOW#* CLKREQ4#** CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA GNDA	PIN TYPE PWR PWR OUT OUT IN IN IN PWR OUT OUT	DESCRIPTION Power supply for differential SB_SRC outputs, nominal 1.05V to 3.3V Supply for SB SRC PLL core, 3.3V nominal Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed When low, this real-time, level-sensitive input slows down the SB_SRC outputs to a user determined lower frequency to save power. The default lower frequency is 80 MHz. 0 = Slow Down, 1 = normal operation. Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
38 V 39 S 40 S 41 S 42 C 43 C 44 V 45 S 46 S 47 C 48 C	VDDSB_SRC SB_SRCOC_LPRS SB_SRCOT_LPRS SB_SRC_SLOW#* CLKREQ4#** CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	PWR OUT IN IN IN PWR OUT	Supply for SB SRC PLL core, 3.3V nominal Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed When low, this real-time, level-sensitive input slows down the SB_SRC outputs to a user determined lower frequency to save power. The default lower frequency is 80 MHz. 0 = Slow Down, 1 = normal operation. Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Complement clock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GND and
39 S 40 S 41 S 42 C 43 C 44 V 45 S 46 S 47 C 48 C	SB_SRCOC_LPRS SB_SRCOT_LPRS SB_SRC_SLOW#* CLKREQ4#** CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	OUT OUT IN IN IN PWR OUT	Complement clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed When low, this real-time, level-sensitive input slows down the SB_SRC outputs to a user determined lower frequency to save power. The default lower frequency is 80 MHz. 0 = Slow Down, 1 = normal operation. Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GND and
40 S 41 S 42 C 43 C 43 C 44 V 45 S 46 S 47 C 48 C	SB_SRC0T_LPRS SB_SRC_SLOW#* CLKREQ4#** CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	OUT IN IN IN PWR OUT	to GND and no 33 ohm series resistor needed True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed When low, this real-time, level-sensitive input slows down the SB_SRC outputs to a user determined lower frequency to save power. The default lower frequency is 80 MHz. 0 = Slow Down, 1 = normal operation. Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Complement clock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GND and
40 S 41 S 42 C 43 C 43 C 44 V 45 S 46 S 47 C 48 C	SB_SRC0T_LPRS SB_SRC_SLOW#* CLKREQ4#** CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	IN IN IN PWR OUT	True clock of low power differential Chipset-to-Chipset SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed When low, this real-time, level-sensitive input slows down the SB_SRC outputs to a user determined lower frequency to save power. The default lower frequency is 80 MHz. 0 = Slow Down, 1 = normal operation. Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Complement clock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GND and
41 S 42 C 43 C 43 C 44 V 45 S 46 S 46 S 46 S	SB_SRC_SLOW#* CLKREQ4#** CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	IN IN IN PWR OUT	and no 33 ohm series resistor needed When low, this real-time, level-sensitive input slows down the SB_SRC outputs to a user determined lower frequency to save power. The default lower frequency is 80 MHz. 0 = Slow Down, 1 = normal operation. Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
41 S 42 C 43 C 43 C 44 V 45 S 46 S 46 S 46 S	SB_SRC_SLOW#* CLKREQ4#** CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	IN IN PWR OUT	When low, this real-time, level-sensitive input slows down the SB_SRC outputs to a user determined lower frequency to save power. The default lower frequency is 80 MHz. 0 = Slow Down, 1 = normal operation. Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
42 C 43 C 44 V 45 S 46 S 46 S 46 S	CLKREQ4#** CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	IN IN PWR OUT	lower frequency to save power. The default lower frequency is 80 MHz. 0 = Slow Down, 1 = normal operation. Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
42 C 43 C 44 V 45 S 46 S 46 S 46 S	CLKREQ4#** CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	IN IN PWR OUT	0 = Slow Down, 1 = normal operation. Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low 0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
43 C 44 V 45 S 46 S 47 C 48 C	CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	IN PWR OUT	Clock Request pin for SRC4/5 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low 0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
43 C 44 V 45 S 46 S 47 C 48 C	CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	IN PWR OUT	follows: 0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
43 C 44 V 45 S 46 S 47 C 48 C	CLKREQ3#** VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	IN PWR OUT	0 = enabled, 1 = Low-Low Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
44 V 45 S 46 S 47 C 48 C	VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	PWR OUT	Clock Request pin for SRC3 outputs. If output is selected for control, then that output is controlled as follows: 0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
44 V 45 S 46 S 47 C 48 C	VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	PWR OUT	follows: 0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
44 V 45 S 46 S 47 C 48 C	VDDSATA SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	PWR OUT	0 = enabled, 1 = Low-Low Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GND and
45 S 46 S 47 G 48 G	SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	OUT	Power supply for SATA core logic, nominal 3.3V Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
45 S 46 S 47 G 48 G	SRC6C/SATAC_LPRS SRC6T/SATAT_LPRS GNDSATA	OUT	Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
46 S 47 G 48 G	SRC6T/SATAT_LPRS		Complement clock of low power differential SRC/SATA clock pair. (no 500hm shunt resistor to GND and
46 S 47 G 48 G	SRC6T/SATAT_LPRS		
47 C 48 C	GNDSATA	OUT	
47 C 48 C	GNDSATA	OUT	True clock of low power differential SRC clock pair. (no 500hm shunt resistor to GND and no 33 ohm
48 0		1	series resistor needed)
48 0		GND	Ground pin for the SRC outputs
		GND	Ground for the Analog Core
49 V	VDDA	PWR	3.3V Power for the Analog Core
43 V	UDDA		Clock Request pin for SRC2 outputs. If output is selected for control, then that output is controlled as
50 (INI	follows:
50 C	CLKREQ2#**	IN	
			0 = enabled, 1 = Low-Low
			Clock Request pin for SRC1 outputs. If output is selected for control, then that output is controlled as
51 C	CLKREQ1#**	IN	follows:
			0 = enabled, 1 = Low-Low
	GNDCPU	GND	Ground pin for the CPU outputs
	VDDCPU_IO	PWR	Power supply for differential CPU outputs, nominal 1.05V to 3.3V
54 V	VDDCPU	PWR	Supply for CPU core, 3.3V nominal
55 C	CPUKG0C_LPRS	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated
00 0		001	series resistor. (no 33 ohm series resistor needed)
56 C	CPUKG0T_LPRS	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series
00 0		001	resistor.(no 33 ohm series resistor needed)
57 F	PD#	IN	Enter /Exit Power Down.
57 1	Δ#		0 = Power Down, 1 = normal operation.
58 0	GNDHTT	PWR	Ground pin for the HTT outputs
			Complementary signal of low-power differential push-pull hypertransport clock with integrated series
59 ⊦	HTT0C_LPRS/66M	OUT	resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) / 1.8V single ended
			66MHz hyper transport clock
			True signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no
60 ⊦	HTT0T_LPRS/66M	OUT	50ohm shunt resistor to GND and no 33 ohm series resistor needed) /1.8V single ended 66MHz hyper
			transport clock
61 V	VDDHTT	PWR	Supply for HTT clocks, nominal 3.3V.
	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
<u></u> '		1	14.318 MHz reference clock, 3.3V/3.3V Latched input to select 27MHz SS and non SS on SRC7
63 F	REF2/SEL_27	OUT	0 = 100 MHz differential spreading SRC clock, $1 = 27$ MHz non-spreading singled clock on pin 4 and
		001	27MHz spread clock on pin 5.
			14.318 MHz 3.3V reference clock / 3.3V tolerant latched input to select function of SRC6/SATA output
64 F	REF1/SEL_SATA	I/O	
<u> </u>			0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock
<u> </u>		1/0	14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select Hyper Transport Clock
65 F	REF0/SEL_HTT66	I/O	Frequency.
		0115	0 = 100MHz differential HTT clock, 1 = 66MHz 3.3V single ended HTT clock
	GNDREF	GND	Ground pin for the REF outputs.
	X1	IN	Crystal input, nominally 14.318MHz
	X2	OUT	Crystal output, nominally 14.318MHz
	VDD48	PWR	Power pin for the 48MHz outputs and core. 3.3V
	48MHz_1	OUT	48MHz clock output.
	48MHz_0	OUT	48MHz clock output.
	GND48	GND	Ground pin for the 48MHz outputs
616—08/2	20/09		



General Description

The **ICS9EPRS488** is a main clock synthesizer chip that provides all clocks required for AMD M690T or 780E embedded systems. An SMBus interface allows full control of the device.

Block Diagram



Power Groups

	Pin Number		Description
VDD	VDDIO	GND	Description
69		72	USB_48 outputs
3		6	SRC/27MHz Outputs
17		11,19	SRC Logic Core
	12,18		SRC differential outputs (IO's)
38		36	SB_SRC Core Logic
	37		SB_SRC differential outputs (IO's)
44		47	SRC/SATA differential output
29		27	ATIG Core Logic
	28		ATIG differential outputs (IO's)
49		48	3.3V Analog
54		52	CPUKG Core Logic
	53		CPUKG differential outputs (IO's)
61		58	HTTCLK output
62		66	REF outputs



Byte 0			te 3		arrequen	НТТ	Differential			
Bit0	Bit3	Bit2	Bit1	Bit0	CPU (MHz)	Single- ended	Differential HTT	SRC/ATIG	Spread %	CPU OverClock
SS_EN	CPU FS3	CPU FS2	CPU FS1	CPU FS0	(11172)	SEL_HTT66 = 1	SEL_HTT66 = 0		70	%
0	0	0	0	0	173.63	57.88	86.81	86.81		-13%
0	0	0	0	1	177.17	59.06	88.58	88.58		-11%
0	0	0	1	0	180.78	60.26	90.39	90.39		-10%
0	0	0	1	1	184.47	61.49	92.24	92.24		-8%
0	0	1	0	0	188.24	62.75	94.12	94.12		-6%
0	0	1	0	1	192.08	64.03	96.04	96.04		-4%
0	0	1	1	0	196.00	65.33	98.00	98.00		-2%
0	0	1	1	1	200.00	66.67	100.00	100.00	Off	0%
0	1	0	0	0	204.00	68.00	102.00	102.00		2%
0	1	0	0	1	208.08	69.36	104.04	104.04		4%
0	1	0	1	0	212.24	70.75	106.12	106.12		6%
0	1	0	1	1	216.49	72.16	108.24	108.24		8%
0	1	1	0	0	220.82	73.61	110.41	110.41		10%
0	1	1	0	1	225.23	75.08	112.62	112.62		13%
0	1	1	1	0	229.74	76.58	114.87	114.87		15%
0	1	1	1	1	234.33	78.11	117.17	117.17		17%
1	0	0	0	0	173.63	57.88	86.81	86.81		-13%
1	0	0	0	1	175.00	59.06	88.58	88.58		-11%
1	0	0	1	0	180.78	60.26	90.39	90.39		-10%
1	0	0	1	1	184.47	61.49	92.24	92.24		-8%
1	0	1	0	0	188.24	62.75	94.12	94.12		-6%
1	0	1	0	1	192.08	64.03	96.04	96.04		-4%
1	0	1	1	0	196.00	65.33	98.00	98.00		-2%
1	0	1	1	1	200.00	66.67	100.00	100.00	-0.5%	0%
1	1	0	0	0	204.00	68.00	102.00	102.00	-0.5 /6	2%
1	1	0	0	1	208.08	69.36	104.04	104.04		4%
1	1	0	1	0	212.24	70.75	106.12	106.12		6%
1	1	0	1	1	216.49	72.16	108.24	108.24		8%
1	1	1	0	0	220.82	73.61	110.41	110.41		10%
1	1	1	0	1	225.23	75.08	112.62	112.62		13%
1	1	1	1	0	229.74	76.58	114.87	114.87		15%
1	1	1	1	1	234.33	78.11	117.17	117.17		17%

Table1: CPU/HTT, SRC and ATIG Frequency Selection Table

Table 2	: SB_S	RC Fre	equenc	y Sele	ction Table	e	
Byte 0		By	te 4				
Bit0	Bit3	Bit2	Bit1	Bit0	SRC	Spread	SB_SRC
SS_EN	SB FS3	SB FS2	SB FS1	SB FS0	(MHz)	%	OverClock %
0	0	0	0	0	80.00		-20%
0	0	0	0	1	81.25	I	-19%
0	0	0	1	0	82.63	I	-17%
0	0	0	1	1	84.00	T F	-16%
0	0	1	0	0	85.25	1 [-15%
0	0	1	0	1	86.63	1	-13%
0	0	1	1	0	88.00	1	-12%
0	0	1	1	1	89.25	Off	-11%
0	1	0	0	0	90.63		-9%
0	1	0	0	1	92.00	1	-8%
0	1	0	1	0	93.25	1	-7%
0	1	0	1	1	94.63	1	-5%
0	1	1	0	0	96.00	1	-4%
0	1	1	0	1	97.25	1 1	-3%
0	1	1	1	0	98.63	1	-1%
0	1	1	1	1	100.00		0%
1	0	0	0	0	80.00		20%
1	0	0	0	1	175.00	Ι	-19%
1	0	0	1	0	82.63	I	-17%
1	0	0	1	1	84.00	I	-16%
1	0	1	0	0	85.25		-15%
1	0	1	0	1	86.63] [-13%
1	0	1	1	0	88.00] [-12%
1	0	1	1	1	89.25	-0.50%	-11%
1	1	0	0	0	90.63	0.0070	-9%
1	1	0	0	1	92.00		-8%
1	1	0	1	0	93.25		-7%
1	1	0	1	1	94.63] [-5%
1	1	1	0	0	96.00	1 [-4%
1	1	1	0	1	97.25] [-3%
1	1	1	1	0	98.63	↓ ↓	-1%
1	1	1	1	1	100.00		0%

Table 2: SB_SBC F Selection Tabl



	SS3	SS2	SS1	SS0		Spr	ead
SS Enable B2b1	Byte 4 bit 7	Byte 4 bit 6	Byte 4 bit 5	Byte 4 bit 4	27MHz_Spread (MHz)	% (when	enabled)
0	0	0	0	0	27.00		
0	0	0	0	1	27.00		
0	0	0	1	0	27.00		
0	0	0	1	1	27.00		
0	0	1	0	0	27.00		
0	0	1	0	1	27.00		
0	0	1	1	0	27.00		
0	0	1	1	1	27.00	No S	pread
0	1	0	0	0	27.00	110.5	pieau
0	1	0	0	1	27.00		
0	1	0	1	0	27.00		
0	1	0	1	1	27.00		
0	1	1	0	0	27.00		
0	1	1	0	1	27.00		
0	1	1	1	0	27.00		
0	1	1	1	1	27.00		
1	0	0	0	0	27.00	-0.50	Down
1	0	0	0	1	27.00	-1.00	Down
1	0	0	1	0	175.00	-1.50	Down
1	0	0	1	1	27.00	-2.00	Down
1	0	1	0	0	27.00	-0.75	Down
1	0	1	0	1	27.00	-1.25	Down
1	0	1	1	0	27.00	-1.75	Down
1	0	1	1	1	27.00	-2.25	Down
1	1	0	0	0	27.00	+/-0.25	Center
1	1	0	0	1	27.00	+/-0.5	Center
1	1	0	1	0	27.00	+/-0.75	Center
1	1	0	1	1	27.00	+/-1.0	Center
1	1	1	0	0	27.00	+/-0.25	Center
1	1	1	0	1	27.00	+/-0.5	Center
1	1	1	1	0	27.00	+/-0.75	Center
1	1	1	1	1	27.00	+/-1.0	Center

Table 3: 27Mhz_Spread and Frequency Selection Table



Table 4: CPU Divider Ratios

				Divi	der	(3:2)			
	Bit	00		01		10		11	MSB
(1:0)	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	0101	6	1001	12	1101	24
Divider	10	0010	5	0110	10	1010	20	1110	40
è	11	0011	15	0111	30	1011	60	1111	120
	LSB	Address	Div	Address		Address	Div	Address	Div

Table 5: SRC, SB_SRC, ATIG Divider Ratios

				Divi	der	(3:2)			
	Bit	00		01		10		11	MSB
(1:0)	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	0101	6	1001	12	1101	24
Divider	10	0010	5	0110	10	1010	20	1110	40
<u>è</u>	11	0011	15	0111	14	1011	28	1111	56
	LSB	Address	Div	Address		Address	Div	Address	Div

Differential Output Power Management Table

PD#	CLKREQ#	SMBus	True output	Complement Output	True output	Complement Output	
		Register OE	Fre	ee-Run	CLKREQ# Selected		
1	0	Enable	Running	Running	Running	Running	
0	Х	Х	Low/20K	Low	Low/20K	Low	
1	1	Enable	Running	Running	Low/20K	Low	
Х	Х	Disable	Low/20K	Low	Low/20K	Low	

Note: 20K means 20Kohm Pull Down

Singled-ended Power Management Table

PD#	SMBus Register OE	48MHz	27MHz	HTT66MHz	REF(2:0)	
1	Enable	Running	Running	Running	Running	
0	Enable	Low	Low	Low	Hi-Z	

Absolute Max

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Supply Voltage	VDDxxx	-		3.3	GND + 3.9V	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDDxxx	-	3.135	3.3	3.465	V	1
Input High Voltage	VDDAAA	VDD = 3.3 V +/-5%	2	0.0	V _{DD} + 0.3	V	1
Input Low Voltage	V _{IH}	VDD = 3.3 V +/-5%	V _{SS} - 0.3		0.8	V	1
Input High Current	I _{IH}	$V_{\rm IN} = V_{\rm DD}$	-5		5	uA	1
input high Current	ЧН	$V_{IN} = 0$ V; Inputs with no pull-	-5		5	uA	1
Input Low Current	I _{IL1}	up resistors	-5			uA	1
	I _{IL2}	V _{IN} = 0 V; Inputs with pull-up resistors	-200	V _{DD} + 0.3 V	1		
Low Threshold Input- High Voltage	V _{IH_FS}	VDD = 3.3 V +/-5%	0.7		V _{DD} + 0.3	v	1
Low Threshold Input- Low Voltage	V _{IL_FS}	VDD = 3.3 V +/-5%	V _{SS} - 0.3		0.35	v	1
Operating Current	I _{DD3.3OP}	3.3V VDD current, all outputs driven			175	mA	1
Powerdown Current	I _{DD3.3PD}	all diff pairs low/low			2	mA	1
Input Frequency	Fi	VDD = 3.3 V +/-5%		14.31818		MHz	2
Pin Inductance	L _{pin}				7	nH	1
	CIN	Logic Inputs			5	pF	1
Input Capacitance	C _{OUT}	Output pin capacitance			6	pF	1
	C _{INX}	X1 & X2 pins			5	mA MHz nH pF pF pF ms	1
Clk Stabilization	T _{STAB}	From VDD Power-Up or de- assertion of PD to 1st clock			3	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V _{DDSMB}		2.7		5.5	V	1
Low-level Output Voltage	V _{OLSMB}	@ I _{PULLUP}			0.4	V	1
Current sinking at V _{OL} = 0.4 V	I _{PULLUPSMB}		4	6		mA	1
SMBCLK/SMBDAT Clock/Data Rise Time	T _{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SMBCLK/SMBDAT Clock/Data Fall Time	T _{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

¹Guaranteed by design and characterization, not 100% tested in production.

² Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

AC Electrical	Characteristics -	I ow-Power DIF	Outputs:	CPUKG and HTT
AC LICCIIICAI	Unaracteristics -		Outputs.	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement			140	mV	1,2,5
Frequency - CPU	f _{CPU}	Spread Specturm On	198.8		200	MHz	1,3
Frequency - HTT	f _{нтт}	Spread Specturm On	99.4		100	MHz	1,3
Long Term Accuracy	ppm	Spread Specturm Off	-300		+300	ppm	1,11
Rising Edge Slew Rate	S _{RISE}	Differential Measurement	0.5		10	V/ns	1,4
Falling Edge Slew Rate	S _{FALL}	Differential Measurement	0.5		10	V/ns	1,4
Slew Rate Variation	t _{SLVAR}	Single-ended Measurement			20	%	1
CPU, DIF HTT Jitter - Cycle to Cycle	CPUJ _{C2C}	Differential Measurement			150	ps	1,6
Accumulated Jitter	t _{JACC}	See Notes			1	ns	1,7
Peak to Peak Differential Voltage	V _{D(PK-PK)}	Differential Measurement	400		2400	mV	1,8
Differential Voltage	VD	Differential Measurement	200		1200	mV	1,9
Duty Cycle	D _{CYC}	Differential Measurement	45		55	%	1
Amplitude Variation	ΔV_D	Change in $V_D DC$ cycle to cycle	-75		75	mV	1,10
CPU[1:0] Skew	CPU _{SKEW10}	Differential Measurement			100	ps	1

Notes on Electrical Characteristics:

¹Guaranteed by design and characterization, not 100% tested in production.

²Single-ended measurement at crossing point. Value is maximum – minimum over all time. DC value of common mode is not ³Minimum Frequency is a result of 0.5% down spread spectrum

⁴Differential measurement through the range of ±100 mV, differential signal must remain monotonic and within slew rate spec when crossing through this region.

⁵ Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

 $^{\rm 6}$ Max difference of $t_{\rm CYCLE}$ between any two adjacent cycles.

⁷ Accumulated tjc.over a 10 µs time period, measured with JIT2 TIE at 50ps interval.

⁸ VD(PK-PK) is the overall magnitude of the differential signal.

⁹ VD(min) is the amplitude of the ring-back differential measurement, guaranteed by design, that ring-back will not cross 0V VD. VD(max) is the largest amplitude allowed.

¹⁰ The difference in magnitude of two adjacent VD_DC measurements. VD_DC is the stable post overshoot and ring-back part of

¹¹ All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz



AC Electrical Characteristics - Low-Power DIF Outputs: SRC, SB_SRC and ATIG

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	t _{SLR}	Differential Measurement	0.6		4	V/ns	1,2
Falling Edge Slew Rate	t _{FLR}	Differential Measurement	0.6		4	V/ns	1,2
Slew Rate Variation	t _{SLVAR}	Single-ended Measurement			20	%	1
Maximum Output Voltage	V _{HIGH}	Includes overshoot			1150	mV	1
Minimum Output Voltage	V _{LOW}	Includes undershoot	-300			mV	1
Differential Voltage Swing	V _{SWING}	Differential Measurement	300			mV	1
Crossing Point Voltage	V _{XABS}	Single-ended Measurement	300		550	mV	1,3,4
Crossing Point Variation	VXABSVAR	Single-ended Measurement			140	mV	1,3,5
Duty Cycle	D _{CYC}	Differential Measurement	45		55	%	1
SRC, ATIG, Jitter - Cycle to Cycle	SRCJ _{C2C}	Differential Measurement			125	ps	1
SRC[5:0] Skew	SRC _{SKEW}	Differential Measurement			250	ps	1
SB_SRC[1:0] Skew	SRC _{SKEW}	Differential Measurement			100	ps	1
ATIG[2:0] Skew	SRC _{SKEW}	Differential Measurement			100	ps	1

Notes on Electrical Characteristics:

¹Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through Vswing centered around differential zero

³ Vxabs is defined as the voltage where CLK = CLK#

⁴ Only applies to the differential rising edge (CLK rising and CLK# falling)

⁵ Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of

⁶ All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - Single-ended HTT 66MHz Clock

Electrical enalactoriotice							
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
HTT66 Clock period	т	66.67MHz output nominal	14.9955		15.0045	ns	2
	T _{period}	66.67MHz output spread	ns ns pread 14.9955 15.0045 ns 14.9955 15.0799 ns 1.6 1.8 3.3 V 0 0.2 V 1.44 V 1.5 ns	2			
Output High Voltage	V _{OH}	I _{OH} = -1 mA	1.6	1.8	3.3	V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA		0	0.2	V	1
Rise Time	t _{r1}	$V_{OL} = 0.36 \text{ V}, V_{OH} = 1.44 \text{ V}$			1.5	ns	1
Fall Time	t _{f1}	$V_{OH} = 1.44 \text{ V}, V_{OL} = 0.36 \text{ V}$			1.5	ns	1
Duty Cycle	d _{t1}	$V_{T} = 0.9 V$	45		55	%	1
Jitter, Cycle to cycle	t _{jcyc-cyc}	$V_{T} = 0.9 V$			300	ps	1
Jitter, Long Term	t _{LTJ}	$V_{T} = 0.9 V$			1	ns	1
		-					

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

Electrical enalactoriotice	000 101						
PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Clock period	T _{period}	48.00MHz output nominal	20.8229		20.8344	ns	2
Clock Low Time	T _{low}	Measure from < 0.6V	9.3750		11.4580	ns	2
Clock High Time	T _{high}	Measure from > 2.0V	9.3750		11.4580	ns	2
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output Lligh Current		V _{OH} @MIN = 1.0 V	-33			mA	1
Output High Current	I _{OH}	V _{OH} @MAX = 3.135 V			-33	mA	1
Output Low Current	1	V _{OL} @ MIN = 1.95 V	30			mA	1
Output Low Current	I _{OL}	V _{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t _{r_USB}	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$	0.5		1.5	ns	1
Fall Time	t _{f_USB}	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$	0.5		1.5	ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45		55	%	1
Group Skew	t _{skew}	V _T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	t _{jcyc-cyc}	V _T = 1.5 V			130	ps	1,2
					-	•	•

Electrical Characteristics - USB - 48MHz

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

²ICS recommended and/or chipset vendor layout guidelines must be followed to meet this specification

Electrical Characteristics - 27MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	nnm	see Tperiod min-max values	-50		50	000	1,2
Long Accuracy	ppm	see ipenou min-max values	-15		15	ppm	1,2,3
Clock period	T _{period}	27.000MHz output nominal	37.0365		37.0376	ns	2
Output High Voltage(27SS)	V _{OH}	I _{OH} = -1 mA	2.1			V	1,10
Output High Voltage (27NSS)	V _{OH}	I _{OH} = -1 mA	0.8			V	1,11
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output High Current	Law	V _{OH} = 1.0 V	-29			mA	1,10
	I _{ОН}	V _{OH} = 3.135 V			-23	mA	1,10
Output Low Current		V _{OL} = 1.95 V	29			mA	1,10
Output Low Current	I _{OL}	$V_{OL} = 0.4 V$			27	mA	1,10
Edge Rate	t _{slewr/f}	Rising/Falling edge rate	1	2	4	V/ns	1
	slewr/f	V _T @ 20%-80%	<u>'</u>	L		V/113	
Duty Cycle	d _{t1}	$V_{T} = 1.5 V$	45		55	%	1
Jitter	t _{iti}	Long Term (10us)			300	ps	1
Sitter	t _{jcyc-cyc}	V _T = 1.5 V			200	ps	1

¹Guaranteed by design and characterization, not 100% tested in production.

 $^{\rm 2}\,{\rm Slew}$ rate measured through Vswing centered around differential zero

 3 Vxabs is defined as the voltage where CLK = CLK#

10
 V_{DD} = 3.3V

 $^{11}\,V_{DD}=\,1.1V$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T _{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Clock Low Time	T _{low}	Measure from < 0.6V	30.9290		37.9130	ns	2
Clock High Time	T _{high}	Measure from > 2.0V	30.9290		37.9130	ns	2
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.4	V	1
Output High Current	I _{ОН}	V _{OH} @MIN = 1.0 V, V _{OH} @MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I _{OL}	V _{OL} @MIN = 1.95 V, V _{OL} @MAX = 0.4 V	29		27	mA	1
Rise Time	t _{r1}	V _{OL} = 0.4 V, V _{OH} = 2.4 V	1		1.5	ns	1
Fall Time	t _{f1}	V _{OH} = 2.4 V, V _{OL} = 0.4 V	1		1.5	ns	1
Skew	t _{sk1}	V _T = 1.5 V			250	ps	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45		55	%	1
Jitter	t _{jcyc-cyc}	V _T = 1.5 V			200	ps	1

Electrical Characteristics - REF-14.318MHz

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz



General SMBus serial interface information for the ICS9EPRS488

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will acknowledge
- Controller (host) sends the begining byte location = N
- ICS clock will *acknowledge*
- Controller (host) sends the data byte count = X
- ICS clock will acknowledge
- Controller (host) starts sending *Byte N through Byte N + X -1*
- ICS clock will acknowledge each byte one at a time
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will acknowledge
- Controller (host) sends the begining byte location = N
- ICS clock will acknowledge
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will *acknowledge*
- ICS clock will send the data byte count = X
- ICS clock sends Byte N + X -1
- ICS clock sends Byte 0 through byte X (if X_(H) was written to byte 8).
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

In	dex Block W	/rit	e Operation
Coi	ntroller (Host)		ICS (Slave/Receiver)
Т	T starT bit		
Slav	e Address D2 _(H)		
WR	WRite		
			ACK
Beg	inning Byte = N		
			ACK
Data	Byte Count = X		
			ACK
Begir	nning Byte N		
			ACK
	0	te	
	0	X Byte	0
	0	×	0
			0
Byte	e N + X - 1		
			ACK
Р	stoP bit	_	

In	Index Block Read Operation							
Con	troller (Host)	IC	S (Slave/Receiver)					
Т	starT bit							
Slave	e Address D2 _(H)							
WR	WRite							
			ACK					
Begi	nning Byte = N							
			ACK					
RT	Repeat starT							
Slave	e Address D3 _(H)							
RD	ReaD							
			ACK					
		D	ata Byte Count = X					
	ACK							
			Beginning Byte N					
	ACK							
		yte.	0 0					
	0	X Byte	0					
	<u> </u>		0					
	0		Byte N + X - 1					
N	Not acknowledge							
P	stoP bit							
1								



ICS9EPRS488 Datasheet

Byte	0	Name	Description	Туре	0	1	Default
	Bit 7	SEL_HTT66 readback	Hypertransport Select	R	100MHz Differential HTT clock	66 MHz 3.3V Single- ended HTT clock	Latch
	Bit 6	SEL_SATA readback	SATA Select	R	SRC6/SATA pair is SRC SS capable output	SRC6/SATA pair is SATA non-spread output	Latch
	Bit 5	REF0_OE	Output Enable	RW	Hi-Z	Enabled	1
	Bit 4	REF1_OE	Output Enable	RW	Hi-Z	Enabled	1
	Bit 3	REF2_OE	Output Enable	RW	Hi-Z	Enabled	1
	Bit 2	48MHz_1_OE	Output Enable	RW	Low	Enabled	1
	Bit 1	48MHz_0_OE	Output Enable	RW	Low	Enabled	1
	Bit 0	SS_Enable	Spread Spectrum Enable (CPU, SRC, SB_SRC, ATIG)	RW	Spread Off	Spread On	0

SMBus Table: Latched Input Readback Output Enable Control Register

SMBus Table:Output Enable Control Register

Byte	1	Name	Control Function	Туре	0	1	Default
	Bit 7	SRC7/27MHz_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 6	SRC6/SATA_OE Enable	Output Enable	RW	Low/Low	Enabled	1
	Bit 5	SRC5_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 4	SRC4_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 3	SRC3_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 2	SRC2_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 1	SRC1_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 0	SRC0_OE	Output Enable	RW	Low/Low	Enabled	1

SMBus Table: Output Enable and 48MHz Slew Rate Control Register

Byte	2	Name	Control Function	Туре	0	1	Default	
	Bit 7	SB_SRC1_OE	Output Enable	RW	Low/Low	Enabled	1	
	Bit 6	SB_SRC0_OE	Output Enable	RW	Low/Low	Enabled	1	
	Bit 5	48MHz_0_Slew Rate	Slew Rate Control	RW	ended outputs. The m 1.9V/ns and the minimu The slew rate selec 11 = 1.	hese bits program the slew rate of the single ended outputs. The maximum slew rate is 9V/ns and the minimum slew rate is $1.1V/ns$. The slew rate selection is as follows: 11 = 1.9V/ns 10 = 1.6V/ns		
	Bit 4				01 = 1. 00 = tri	1V/ns	1	
Ĩ	Bit 3	ATIG1_OE	Output Enable	RW	Low/Low	Enabled	1	
	Bit 2	ATIG0_OE	Output Enable	RW	Low/Low	Enabled	1	
	Bit 1	27MHz_SS_Enable	Spread Spectrum Enable 27MHz_SS	RW	Spread Off	Spread On	0	
	Bit 0	Reserved	Reserved	RW	-	-	Х	

SMBus Table: CPU/HTT Frequency Control Register

Byte	3	Name	Control Function	Туре	0	1	Default
	Bit 7	CPU0_OE	Output enable	RW	Low/Low	Enable	1
	Bit 6	SEL_27 readback	SRC7/27MHz Select	R	SRC7 Output	27MHz Output	Latch
	Bit 5	ATIG2_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 4	HTT/66MHz_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 3	CPU_FS3	CPU Frequency Select	RW	See CPU/HTT/SRC/A1	IG Frequency Select	0
	Bit 2	CPU_FS2	CPU Frequency Select	RW	Tat Default value corres		1
	Bit 1	CPU_FS1	CPU Frequency Select	RW	Note that the HTT frequ		1
	Bit 0	CPU_FS0	CPU Frequency Select LSB	RW	freque	ency.	1



SMBus Table: SB_SRC Frequency Control Register										
Byte	4	Name	Control Function	Туре	0	1	Default			
	Bit 7	S3		RW	S[1:0]: 00 = -0).5% Default,	0			
	Bit 6	S2	27 SSC	RW	01 =1.0%, 10 = -	1.5%, 11 = -2%.	0			
	Bit 5	S1	Spread Select	RW		Table 3: 27Mhz_Spread, LCDCLK Spread				
ſ	Bit 4	SO		RW	and Frequency Selection Table for additional selections.		0			
	Bit 3	SB_SRC_FS3	SB_SRC Frequency Select	RW			1			
	Bit 2	SB_SRC_FS2	SB_SRC Frequency Select	RW	See SB_SRC Frequ	See SB_SRC Frequency Select Table.				
	Bit 1	SB_SRC_FS1	SB_SRC Frequency Select	RW						
	Bit 0	SB_SRC_FS0	SB_SRC Freq. Select LSB	RW			1			

SMBus Table: 27MHz Slew Rate Control Register

Byte	5	Name	Control Function	Туре	0	1	Default
	Bit 7	27M SS Slew Rate	Slew Bate Control	RW	These bits program the ended outputs. The n	Ũ	1
	Bit 6			1100		minimum slew rate is 1.1V/ns. te selection is as follows:	
	Bit 5	27M NS Slew Rate	Slew Bate Control	BW	10 = 1.	1.9V/ns 1.6V/ns 1.1V/ns ristated	1
	Bit 4	27M_NO_SIEW hate	Siew Hale Control	ΠVV	•••••		1
	Bit 3	SB_SRC Source	SB_SRC Source Selection	RW	SB_SRC PLL SRC PLL	1	
	Bit 2		Reserv	ved	· · · ·		0
	Bit 1		Reserv	ved			0
	Bit 0		Reserv	ved			0

SMBus Table: I/O Vout Control Register

Byte	6	Name	Control Function	Туре	0	1	Default
	Bit 7	SRC Diff AMP	SRC Differential output	RW	00 = 700mV	01 = 800mV	0
	Bit 6	SRC Diff AMP	Amplitude Control	RW	10 = 900mV	11 = 1000mV	1
	Bit 5	CPU Diff AMP	CPU Differential output	RW	00 = 700mV	01 = 800mV	0
	Bit 4	CPU Diff AMP	Amplitude Control	RW	10 = 900mV	11 = 1000mV	1
	Bit 3	SB_SRC Diff AMP	SB_SRC Differential output	RW	00 = 700mV	01 = 800mV	0
	Bit 2	SB_SRC Diff AMP	Amplitude Control	RW	10 = 900mV	11 = 1000mV	1
	Bit 1		Reserv	/ed			X
	Bit 0		Reserv	/ed			Х

SMBus Table: Vendor & Revision ID Register

Byte	7	Name	Control Function	Туре	0	1	Default
	Bit 7	RID3		R	-	-	0
	Bit 6	RID2	REVISION ID	R	-	-	1
	Bit 5	RID1		R	-	-	0
	Bit 4	RID0		R	-	-	0
	Bit 3	VID3		R	-	-	0
	Bit 2	VID2	VENDOR ID	R	-	-	0
	Bit 1	VID1	VENDONID	R	-	-	0
	Bit 0	VID0		R	-	-	1



		SMBus Table: Byte Count	t Register				
Byte	8	Name	Control Function	Туре	0	1	Default
	Bit 7		Reser	ved			0
	Bit 6	Bit 6 Reserved					0
Ē	Bit 5	BC5 Byte Count bit 5 (MSB) RW					0
	Bit 4	BC4	Byte Count bit 4	RW			0
[Bit 3	BC3	Byte Count bit 3	RW	Determines the numbe	r of bytes that are read	1
	Bit 2	BC2	Byte Count bit 2 RW back from the device. Default is 0F hex.				1
	Bit 1	BC1	Byte Count bit 1	RW			1
	Bit 0	BC0	Byte Count bit 0 (LSB)	RW			1

SMBus Table: WatchDog Timer Control Register

Byte	9	Name	Control Function	Туре	0	1	Default
	Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable and Reload Hartd Alarm Timer, Clear WD Hard status bit.	Enable Timer	0
	Bit 6	SWD_EN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0
	Bit 5	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	Х
	Bit 4	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	Х
Γ	Bit 3	WDTCtrl	Watch Dog Alarm Time base Control	RW	290ms Base	1160ms Base	0
	Bit 2	HWD2	WD Hard Alarm Timer Bit 2	RW	These bits represent the	number of Watch Dog	1
	Bit 1	HWD1	WD Hard Alarm Timer Bit 1	RW	Time Base Units that p	ass before the Watch	1
F	Bit 0	HWD0	WD Hard Alarm Timer Bit 0	RW	Alarm expires. Defau	lt is 7 X 290ms = 2s.	1

SMBus Table: WD Timer Safe Frequency Control Register

Byte	10	Name	Control Function	Туре	0	1	Default		
	Bit 7	SWD2	WD Soft Alarm Timer Bit 2	RW	These bits represent the	e number of Watch Dog	1		
	Bit 6	SWD1	WD Soft Alarm Timer Bit 1	RW	Time Base Units that p	ass before the Watch	1		
	Bit 5	SWD0	WD Soft Alarm Timer Bit 0	RW	Alarm expires. Defau	lt is 7 X 290ms = 2s.	1		
	Bit 4	WD SF4		RW	These bits configure the	safe frequency that the	0		
	Bit 3	WD SF3		RW	device returns to if the W	atchdog Timer expires.	0		
	Bit 2	WD SF2	Watch Dog Safe Freq	RW	The value show here co	rresponds to the power	1		
	Bit 1	WD SF1	Programming bits	RW		efault of the device. See the various	1		
	Bit 0	WD SF0		RW		Select Tables for the exact frequencies.			

SMBus Table: CPU PLL Frequency Control Register

Byte	11	Name	Control Function	Туре	0	1	Default
	Bit 7	N Div2	N Divider Prog bit 2	RW			Х
	Bit 6	N Div1	N Divider Prog bit 1	RW]		Х
	Bit 5	M Div5		RW	The decimal representati	al representation of M and N Divider in	
	Bit 4	M Div4		RW	Byte 11 and 12 will configure the VCO frequency.	Х	
	Bit 3	M Div3	M Divider Programming bits	RW	Default at power up = E	,	Х
	Bit 2	M Div2		RW	Frequency = 14.318 x	Ndiv(10:0)/Mdiv(5:0) .	Х
	Bit 1	M Div1		RW		Х	
	Bit 0	M Div0		RW			Х

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	SMBus Table: CPU PLL Frequency Control Register										
Byte	12	Name	Control Function	Туре	0	1	Default				
	Bit 7	N Div10		RW			Х				
[Bit 6	N Div9		RW			Х				
ſ	Bit 5	N Div8		RW	The decimal representat	mal representation of M and N Divider in					
	Bit 4	N Div7	N Divider Programming	RW	Byte 11 and 12 will config						
	Bit 3	N Div6	b(10:3)	RW	Default at power up = E	Byte 3 Rom table. VCO	Х				
ľ	Bit 2	N Div5		RW	Frequency = 14.318 x	Ndiv(10:0)/Mdiv(5:0) .	Х				
	Bit 1	N Div4	1	RW			Х				
ſ	Bit 0	N Div3]	RW			Х				

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte	13	Name	Control Function	Туре	0	1	Default
	Bit 7	SSP7		RW			Х
	Bit 6	SSP6	7	RW			Х
	Bit 5	SSP5		RW	Buton 12 and 14 pat the		Х
	Bit 4	SSP4	Spread Spectrum	RW	Bytes 13 and 14 set the spread pecentage.Plea		Х
	Bit 3	SSP3	Programming b(7:0)	RW	appropriat		Х
	Bit 2	SSP2		RW	appropriat	inale values.	Х
	Bit 1	SSP1		RW			Х
	Bit 0	SSP0		RW			Х

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte	14	Name	Control Function	Туре	0	1	Default
	Bit 7		Reserv	/ed			Х
	Bit 6	SSP14		RW			Х
	Bit 5	SSP13		RW	Bytes 13 and 14 set the CPU/HTT/SRC/ATIG spread pecentage.Please contact ICS for the appropriate values.		Х
	Bit 4	SSP12	Sprood Spootrum	RW			Х
	Bit 3	SSP11	Spread Spectrum Programming b(14:8)	RW			Х
	Bit 2	SSP10	1 Togramming b(14.0)	RW			Х
	Bit 1	SSP9		RW			Х
	Bit 0	SSP8		RW			Х

SMBUS Table: CPU Output Divider Register

Byte	15	Name	Control Function	Туре	0	1	Default
	Bit 7	CPU NDiv0	LSB N Divider Programming	RW	CPU M/N pr	ogramming.	Х
	Bit 6		Reserv	red			Х
	Bit 5		Reserved				
	Bit 4		Reserved				
	Bit 3	CPUDiv3		RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	Х
ſ	Bit 2	CPUDiv2	CPU Divider Ratio	RW	0001:/3 ; 0101:/6	1001:/12 ; 1101:/24	Х
	Bit 1	CPUDiv1	Programming Bits	RW	0010:/5 ; 0110:/10	1010:/20 ; 1110:/40	Х
	Bit 0	CPUDiv0		RW	0011:/15 ; 0111:/18	1011:/36 ; 1111:/72	Х

SMBUS Table: SB_SRC Frequency Control Register

Byte	16	Name	Control Function	Туре	0	1	Default
	Bit 7	N Div2	N Divider Prog bit 2	RW			Х
	Bit 6	N Div1	N Divider Prog bit 1	RW			Х
	Bit 5	M Div5		RW	The decimal representati	on of M and N Divider in	Х
	Bit 4	M Div4		RW	Byte 16 and 17 configu	Ire the SB_SRC VCO	Х
	Bit 3	M Div3	M Divider Programming	RW	frequency. See M/N Cac		Х
	Bit 2	M Div2	bit (5:0)	RW	frequency	formulas.	Х
	Bit 1	M Div1		RW			Х
	Bit 0	M Div0		RW			Х



SMBUS Table: SB_SRC Frequency Control Register							
Byte	17	Name	Control Function	Туре	0	1	Default
	Bit 7	N Div10		RW			Х
	Bit 6	N Div9		RW			Х
	Bit 5	N Div8		RW	The decimal representation of M and N Divider in Byte 16 and 17 configure the SB_SRC VCO		Х
	Bit 4	N Div7	N Divider Programming	RW			Х
	Bit 3	N Div6	Byte16 bit(7:0) and Byte15 bit(7:6)	RW	frequency. See M/N Cad	culation Tables for VCO	Х
	Bit 2	N Div5	Dit(7.8)	RW	frequency formulas.		Х
	Bit 1	N Div4	1	RW			Х
	Bit 0	N Div3		RW			Х

SMBUS Table: SB_SRC Spread Spectrum Control Register

Byte	18	Name	Control Function	Туре	0	1	Default	
	Bit 7	SSP7		RW			Х	
	Bit 6	SSP6		RW			Х	
	Bit 5	SSP5		RW	Butes 19 and 10 act th	a the CR CRC aproad	Х	
	Bit 4	SSP4	Spread Spectrum	RW	Bytes 18 and 19 set the the SB_SRC spread pecentages. Please contact ICS for the		Х	
	Bit 3	SSP3	Programming bit(7:0)	RW		appropriate values.		
	Bit 2	SSP2		RW	appropriat	appi opriate values.		
	Bit 1	SSP1		RW			Х	
	Bit 0	SSP0		RW			Х	

SMBUS Table: SB_SRC Spread Spectrum Control Register

Byte	19	Name	Control Function	Туре	0	1	Default
	Bit 7	SSP15		RW			Х
	Bit 6	SSP14		RW			Х
	Bit 5	SSP13		RW	Duton 19 and 10 act th	the CR CRC enreed	Х
	Bit 4	SSP12	Spread Spectrum RW pecentages. Please contact ICS for the		Х		
	Bit 3	SSP11	Programming bit(14:8)	RW	appropriat		Х
	Bit 2	SSP10		RW	appropriat		Х
	Bit 1	SSP9		RW			Х
	Bit 0	SSP8		RW			Х

SMBUS Table: SB_SRC Output Divider Control Register

Byte	20	Name	Control Function	Туре	0	1	Default
	Bit 7	SB_SRC NDiv0	LSB N Divider Programming	RW	SB_SRC M/N	orogramming.	Х
	Bit 6		Reserv	'ed			Х
	Bit 5		Reserv	/ed			Х
	Bit 4		Reserved				Х
	Bit 3	SB_SRCDiv3		RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	Х
	Bit 2	SB_SRCDiv2	SRC Divider Ratio	RW	0001:/3 ; 0101:/6	1001:/12 ; 1101:/24	Х
	Bit 1	SB_SRCDiv1	Programming Bits	RW	0010:/5 ; 0110:/10	1010:/20 ; 1110:/40	Х
	Bit 0	SB_SRCDiv0	Ī	RW	0011:/15 ; 0111:/18	1011:/36 ; 1111:/72	Х

SMBus Table: Device ID register

	0								
Byte	21	Name	Control Function	Туре	0	1	Default		
	Bit 7	Device ID7		R			0		
	Bit 6	Device ID6		R		1			
	Bit 5	Device ID5		R			1		
	Bit 4	Device ID4	Davia a ID	R	76 hex		1		
F	Bit 3	Device ID3	Device ID	R	/61	lex	0		
	Bit 2	Device ID2		R	1	1			
F	Bit 1	Device ID1		R	1				
	Bit 0	Device ID0		R			0		



		SMBus Table: CLKREQ#	Configuration Register				
Byte	22	Name	Control Function	Туре	0	1	Default
	Bit 7	CPU/HTT/SRC/ATIG M/N En	CPU/HTT/SRC/ATIG PLL M/N Prog. Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
ſ	Bit 6 SB_SRC M/		SB_SRC M/N Prog. Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
	Bit 5	Reserved	Reserved	RW	-	-	0
ſ	Bit 4	Reserved	Reserved	RW	-	-	0
[Bit 3	Reserved	Reserved	RW	-	-	0
ſ	Bit 2	Reserved	Reserved	RW	-	-	Х
F	Bit 1	Reserved	Reserved	RW	-	-	Х
F	Bit 0 Reserved		Reserved	RW	-	-	Х

SMBus Table: CLKREQ# Configuration Register

	SMBUS Table. CLAREQ# Configuration Register							
Byte	23	Name	Control Function	Туре	0	1	Default	
	Bit 7	Reserved	Reserved	RW	-	-	0	
	Bit 6	Reserved	Reserved	RW	-	-	0	
	Bit 5	CLKREQ4#_Enable	CLKREQ4# controls SRC5	RW	Not Controlled	Controlled	1	
	Bit 4	CLKREQ4#_Enable	CLKREQ4# controls SRC4	RW	Not Controlled	Controlled	1	
	Bit 3	CLKREQ3#_Enable	CLKREQ3# controls SRC3	RW	Not Controlled	Controlled	1	
	Bit 2	CLKREQ2#_Enable	CLKREQ2# controls SRC2	RW	Not Controlled	Controlled	1	
	Bit 1	CLKREQ1#_Enable	CLKREQ1# controls SRC1	RW	Not Controlled	Controlled	1	
	Bit 0	CLKREQ0#_Enable	CLKREQ0# controls SRC0	RW	Not Controlled	Controlled	1	

SMBus Table: Test Mode Configuration Register

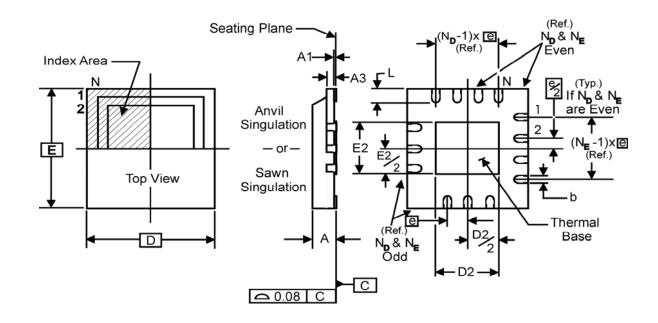
Byte	24	Name	Control Function	Туре	0	1	Default
	Bit 7	Test_Md_Sel	Selects Test Mode	RW	Normal mode	All ouputs are REF/N	0
	Bit 6	DIAG Enable#	DIAG enable CPU and LCD PLL	RW	Reset forces B24[6:4,2,0] to 0	DIAG mode Enabled	0
	Bit 5	CPU PLL_LOCK signal	CPU PLL Lock Detect	R	unlocked	Locked	HW
	Bit 4	27MHz PLL_LOCK signal	27MHz PLL Lock Detect	R	unlocked	Locked	HW
	Bit 3	Fixed PLL_LOCK signal	Fixed PLL Lock Detect	R	unlocked	Locked	HW
	Bit 2	SRC PLL_LOCK signal	Fixed PLL Lock Detect	R	unlocked	Locked	HW
	Bit 1	Frequency Check	Primary PLL or external crystal Frequency Accuracy	R	Not Accurate	Accurate	HW
	Bit 0	PWRGD Status	Power on Reset Status	R	Invalid voltage levels on any of the VDDs. CKPWRGD is not asserted or external XTAL not detected.	Valid voltage levels exist on all the VDD. CKPWRGD is asserted and external XTAL is detected.	нw

SMBus Table:Slew Rate Select Register

Byte	25	Name	Control Function	Туре	0	1	Default
	Bit 7	48MHz 1 Slew Rate	Slew Rate Control	BW	These bits program the slew rate of the single		1
	Bit 6			1100	ended outputs. The maximum slew rate is	1	
	Bit 5	REF2 Slew Rate	Slew Rate Control	вW	1.9V/ns and the minimu	m slew rate is 1.1V/ns.	1
	Bit 4			1100	The slew rate selec	rate selection is as follows:	1
	Bit 3	REF1 Slew Rate	Slew Rate Control	RW	11 = 1.9V/ns 10 = 1.6V/ns		1
	Bit 2			1100		1	
	Bit 1	BEED Slow Bate	F0_Slew RateSlew Rate ControlRW01 = 1.1V/ns00 = tristated		1		
	Bit 0	REFU_Slew Hale		00 = tri	stated	1	

1616-08/20/09





THERMALLY ENHANCED, VERY THIN, FINE PITCH QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS							
SYMBOL	MIN.	MAX.					
STIVIDUL	IVIIIN.	IVIAA.					
A	0.8	1.0					
A1	0	0.05					
A3	0.25 Re	eference					
b	0.18	0.3					
e 0.50 BASIC							

DIMENSIONS

SYMBOL	ICS 72L TOLERANCE	
N	72	
N _D	18	
N _E	18	
D x E BASIC	10.00 x 10.00	
D2 MIN. / MAX.	5.75 / 6.15	
E2 MIN. / MAX.	5.75 / 6.15	
L MIN. / MAX.	0.30/ 0.50	

Ordering Information

Part/Order Number	Shipping Packaging	Package	Temperature
9EPRS488CKLF	Tubes	72-pin MLF	0 to +70° C
9EPRS488CKLFT	Tape and Reel	72-pin MLF	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant. Due to package size constraints, actual top-side marking may differ from the full orderable part number.



Revision History

Rev.	Issue Date	Description	Page #
0.1	7/31/2009	Initial Release	-
А	8/20/2009	Release to final	-