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Frequency Generator for CPU, PCIe Gen 1, PCIe Gen 2 & FBD

Recommended Application:

DB1900GS/GSO with 15:4 output grouping

Features:

- Power up default is all outputs in 1:1 mode
- DIF_(14:0) can be “gear-shifted” from the input CPU Host Clock
- DIF_(18:15) can be “gear-shifted” from the input CPU Host Clock
- Spread spectrum compatible
- Supports output clock frequencies up to 400 MHz
- 8 Selectable SMBus addresses
- SMBus address determines PLL or Bypass mode

Key Specifications:

- DIF output cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 100ps within a group

Functionality at Power Up (PLL Mode)

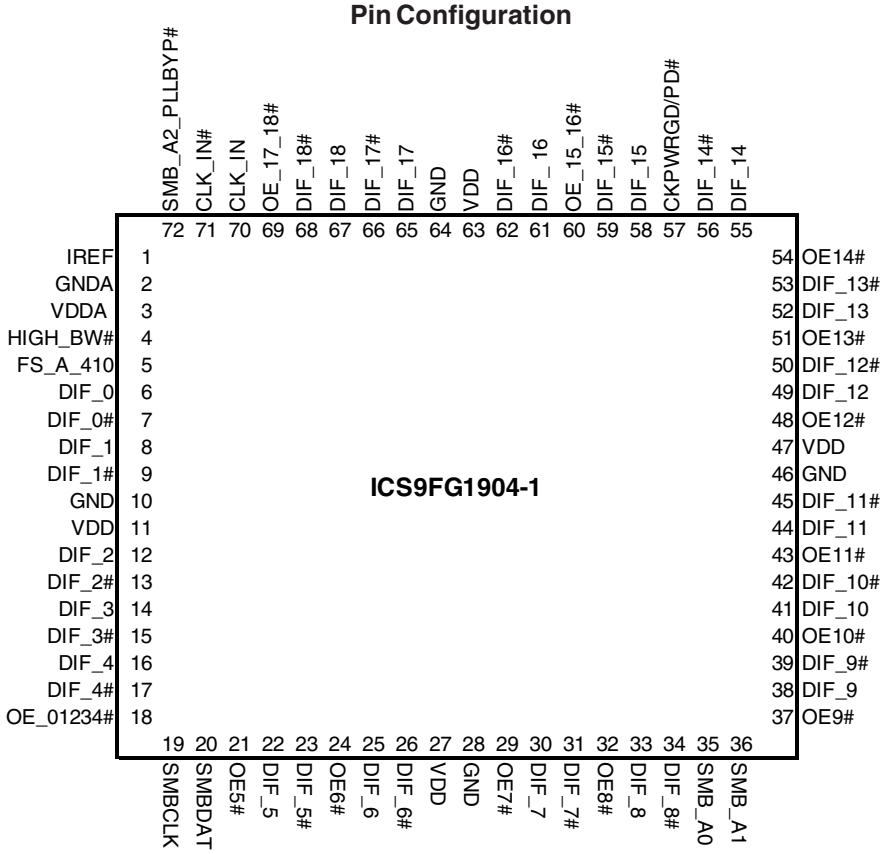
FS_A_410[1]	CLK_IN (CPU FSB) MHz	DIF_(18:0) MHz
1	100 <= CLK_IN < 200	CLK_IN
0	200<= CLK_IN <= 400	CLK_IN

1. FS_A_410 is a low-threshold input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Power Down Functionality

INPUTS		OUTPUTS	PLL State
CKPWRGD/ PD#	CLK_IN/ CLK_IN#	DIF/DIF#	
1	Running	Running	ON
0	X	Hi-Z	OFF

Pin Configuration



72-pin MLF

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
2	GNDA	PWR	Ground pin for the PLL core.
3	VDDA	PWR	3.3V power for the PLL core.
4	HIGH_BW#	IN	3.3V input for selecting PLL Band Width 0 = High, 1= Low
5	FS_A_410	IN	3.3V tolerant low threshold input for CPU frequency selection. This pin requires CK410 FSA. Refer to input electrical characteristics for Vil_FS and Vih_FS threshold values.
6	DIF_0	OUT	0.7V differential true clock output
7	DIF_0#	OUT	0.7V differential complement clock output
8	DIF_1	OUT	0.7V differential true clock output
9	DIF_1#	OUT	0.7V differential complement clock output
10	GND	PWR	Ground pin.
11	VDD	PWR	Power supply, nominal 3.3V
12	DIF_2	OUT	0.7V differential true clock output
13	DIF_2#	OUT	0.7V differential complement clock output
14	DIF_3	OUT	0.7V differential true clock output
15	DIF_3#	OUT	0.7V differential complement clock output
16	DIF_4	OUT	0.7V differential true clock output
17	DIF_4#	OUT	0.7V differential complement clock output
18	OE_01234#	IN	Active low input for enabling DIF pairs 0, 1, 2, 3 and 4. 1 = tri-state outputs, 0 = enable outputs
19	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
20	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
21	OE5#	IN	Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs
22	DIF_5	OUT	0.7V differential true clock output
23	DIF_5#	OUT	0.7V differential complement clock output
24	OE6#	IN	Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs
25	DIF_6	OUT	0.7V differential true clock output
26	DIF_6#	OUT	0.7V differential complement clock output
27	VDD	PWR	Power supply, nominal 3.3V
28	GND	PWR	Ground pin.
29	OE7#	IN	Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs
30	DIF_7	OUT	0.7V differential true clock output
31	DIF_7#	OUT	0.7V differential complement clock output
32	OE8#	IN	Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs
33	DIF_8	OUT	0.7V differential true clock output
34	DIF_8#	OUT	0.7V differential complement clock output
35	SMB_A0	IN	SMBus address bit 0 (LSB)
36	SMB_A1	IN	SMBus address bit 1

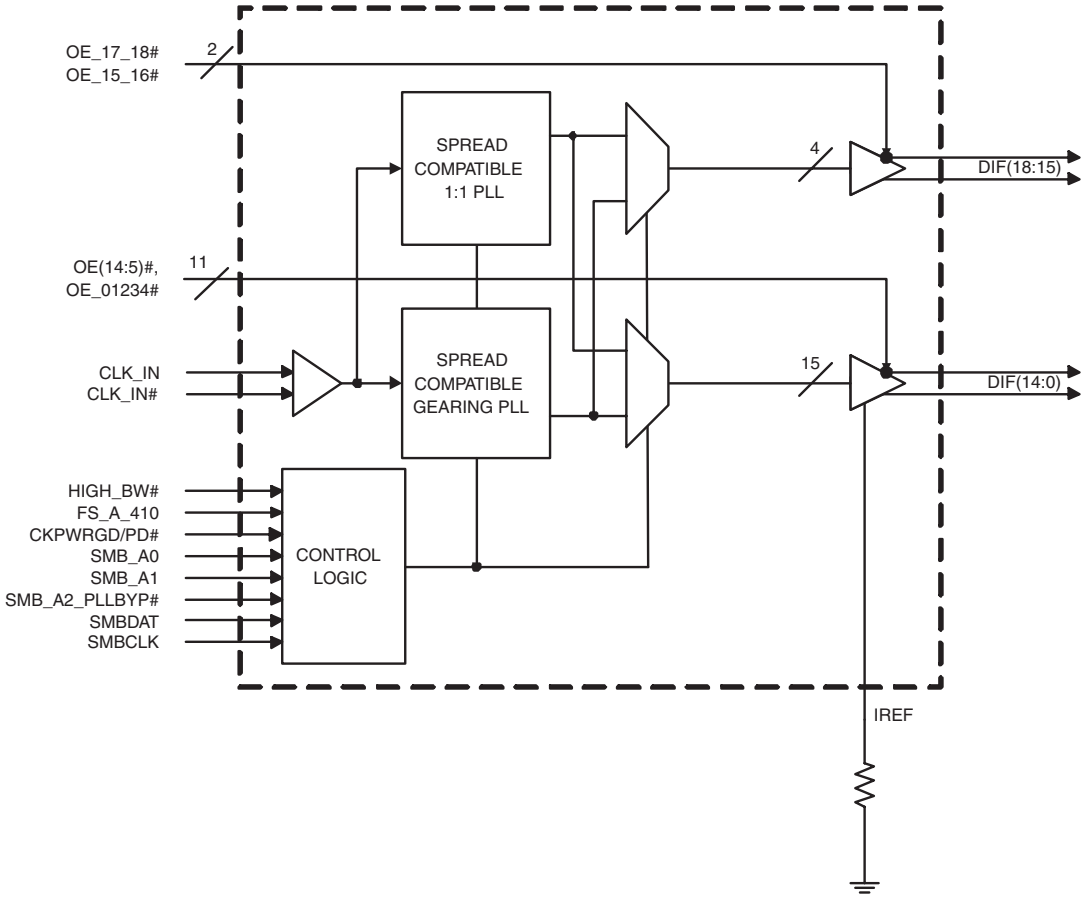
Pin Description (Continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
37	OE9#	IN	Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs
38	DIF_9	OUT	0.7V differential true clock output
39	DIF_9#	OUT	0.7V differential complement clock output
40	OE10#	IN	Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs
41	DIF_10	OUT	0.7V differential true clock output
42	DIF_10#	OUT	0.7V differential complement clock output
43	OE11#	IN	Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs
44	DIF_11	OUT	0.7V differential true clock output
45	DIF_11#	OUT	0.7V differential complement clock output
46	GND	PWR	Ground pin.
47	VDD	PWR	Power supply, nominal 3.3V
48	OE12#	IN	Active low input for enabling DIF pair 12. 1 = tri-state outputs, 0 = enable outputs
49	DIF_12	OUT	0.7V differential true clock output
50	DIF_12#	OUT	0.7V differential complement clock output
51	OE13#	IN	Active low input for enabling DIF pair 13. 1 = tri-state outputs, 0 = enable outputs
52	DIF_13	OUT	0.7V differential true clock output
53	DIF_13#	OUT	0.7V differential complement clock output
54	OE14#	IN	Active low input for enabling DIF pair 14. 1 = tri-state outputs, 0 = enable outputs
55	DIF_14	OUT	0.7V differential true clock output
56	DIF_14#	OUT	0.7V differential complement clock output
57	CKPWRGD/PD#	IN	A rising edge samples latched inputs and release Power Down Mode, a low puts the part into power down mode and tristates all outputs.
58	DIF_15	OUT	0.7V differential true clock output
59	DIF_15#	OUT	0.7V differential complement clock output
60	OE_15_16#	IN	Active low input for enabling DIF pair 15 and 16. 1 = tri-state outputs, 0 = enable outputs
61	DIF_ 16	OUT	0.7V differential true clock output
62	DIF_16#	OUT	0.7V differential complement clock output
63	VDD	PWR	Power supply, nominal 3.3V
64	GND	PWR	Ground pin.
65	DIF_17	OUT	0.7V differential true clock output
66	DIF_17#	OUT	0.7V differential complement clock output
67	DIF_18	OUT	0.7V differential true clock output
68	DIF_18#	OUT	0.7V differential complement clock output
69	OE_17_18#	IN	Active low input for enabling DIF pair 17, 18. 1 = tri-state outputs, 0 = enable outputs
70	CLK_IN	IN	Input for reference clock.
71	CLK_IN#	IN	"Complementary" reference clock input.
72	SMB_A2_PLLBYP#	IN	SMBus address bit 2. When Low, the part operates as a fanout buffer with the PLL bypassed. When High, the part operates as a zero-delay buffer (ZDB) with the PLL operating. 0 = fanout mode (PLL bypassed), 1 = ZDB mode (PLL used)

General Description

ThThe **ICS9FG1904-1** follows the Intel DB1900GS Differential Buffer Specification, except for the output groupings and gear table. The gear table is a blend of the GS and GSO gearing. This buffer provides 19 output clocks for CPU Host Bus, PCI-Express, or Fully Buffered DIMM applications. The outputs are configured with two groups. Both groups, DIF_(14:0) and DIF_(18:15) can be equal to or have a gear ratio to the input clock. A differential CPU clock from a CK410B+ main clock generator, such as the ICS932S421, drives the **ICS9FG1904-1**. The **ICS9FG1904-1** can provide outputs up to 400MHz.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
3	2	Main PLLs, Analog
11,27,47,63	10,28,46,64	DIF clocks

ICS 9FG1904B-1 Programmable Gear Ratios

CLK_IN (CPU FSB) MHz	Geared DIF Outputs MHz	M	n	Gear Ratio n/M	(FS_A_410#) Byte 0, bit 4 FS4	Byte 0, bit 3 FS3	Byte 0, bit 2 FS2	Byte 0, bit 1 FS1	Byte 0, bit 0 FS0	Notes
100.00	133.33	3	4	1.333	0	0	0	0	0	
100.00	166.67	3	5	1.667	0	0	0	0	1	
100.00	200.00	1	2	2.000	0	0	0	1	0	
100.00	266.67	3	8	2.667	0	0	0	1	1	
100.00	333.33	3	10	3.333	0	0	1	0	0	
100.00	400.00	1	4	4.000	0	0	1	0	1	
133.33	166.67	4	5	1.250	0	0	1	1	0	1
133.33	200.00	2	3	1.500	0	0	1	1	1	1
133.33	266.67	1	2	1.250	0	1	0	0	0	
133.33	333.33	2	5	1.500	0	1	0	0	1	
133.33	100.00	4	3	0.750	0	1	0	1	0	
166.67	**133.33**	**5**	**4**	**0.800**	**0**	**1**	**0**	**1**	**1**	1,3
166.67	200.00	5	6	1.200	0	1	1	0	0	1
166.67	266.67	5	8	1.600	0	1	1	0	1	
160/ 166.67	320/ 333.33	1	2	2.000	0	1	1	1	0	1,2
166.67	400.00	5	12	2.400	0	1	1	1	1	
200.00	133.33	3	2	0.667	1	0	0	0	0	1
200.00	166.67	6	5	0.833	1	0	0	0	1	1
200.00	266.67	3	4	1.333	1	0	0	1	0	1
200.00	333.33	3	5	1.667	1	0	0	1	1	1
200.00	400.00	1	2	2.000	1	0	1	0	0	1
266.67	133.33	2	1	0.500	1	0	1	0	1	1
266.667/ 320.00	166.67/ 200.00	8	5	0.625	1	0	1	1	0	1, 6
266.67	200.00	4	3	0.750	1	0	1	1	1	1
333.33	133.33	5	2	0.400	1	1	0	0	0	1
320/ 333.33	160/ 166.67	2	1	0.500	1	1	0	0	1	1,5
333.33	200.00	5	3	0.600	1	1	0	1	0	1
400.00	**133.33**	**3**	**1**	**0.333**	**1**	**1**	**0**	**1**	**1**	1,4
400.00	160.00	5	2	0.400	1	1	1	0	0	1
400.00	166.67	12	5	0.417	1	1	1	0	1	1
400.00	320.00	5	4	0.800	1	1	1	1	0	1
400.00	333.33	6	5	0.833	1	1	1	1	1	1

Notes:

1. Targetted input/output frequency pairs
2. This Gear is also used for 160MHz/320 MHz.
3. Gear Ratio 5/4 is power up default for FS_A_410 = 1
4. Gear Ratio 3/1 is power up default for FS_A_410 = 0
5. This Gear is also used for 400MHz/200MHz
6. This Gear is also used for 320MHz/200MHz

ICS 9FG1904B-1 1:1 PLL Programming

Byte 9, bit 2 FSC	Byte9, bit 1 FSB	Byte 9, bit 0 FS_A_410	CLK_IN (CPU FSB) MHz	1:1 DIF Outputs MHz	Notes
1	0	1	100.00	100.00	3
0	0	1	133.33	133.33	3
0	**1**	**1**	**166.67**	**166.67**	1
0	1	0	200.00	200.00	3
0	0	0	266.67	266.67	3
1	0	0	333.33	333.33	3
1	**1**	**0**	**400.00**	**400.00**	2
1	1	1	Reserved		

Notes:FS_A_410 = 1

1. Powerup Default for FS_A_410 = 1
2. Powerup Default for FS_A_410 = 0
3. Setting the exact FSB frequency after Power is required for best phase noise performance.

Output Divider Ratios

Desired Decimal Value	Binary Value to write to Register
2	0000
3	0001
5	0010
7	0011
4	0100
6	0101
10	0110
14	0111
8	1000
12	1001
20	1010
28	1011
16	1100
24	1101
40	1110
56	1111

Absolute Max

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A		GND - 0.5		V_{DD} + 0.5V	V	1
3.3V Logic Supply Voltage	VDD_In		GND - 0.5		V_{DD} + 0.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Ambient Operating Temp	Tambient		0		70	°C	1
Case Temperature	Tcase				115	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%, Applies to FS_A_410 pin	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%, Applies to FS_A_410 pin	V_{SS} - 0.3		0.35	V	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			500	mA	1
Powerdown Current	$I_{DD3.3PD}$	all differential pairs tri-stated			30	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V	100		400	MHz	3
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance		2.5		pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up or de-assertion of PD# to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		DIF output enable after PD# de-assertion			300	us	1
Tfall_Pd#		PD# fall time of			5	ns	1
Trise_Pd#		PD# rise time of			5	ns	2
SMBus Voltage	V_{MAX}	Maximum input voltage			5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	0		0	ppm	1,2,7
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	$t_{JCYC-CYC}$	PLL mode, from differential wavefrom			50	ps	1,4,5
	t_{JBYP}	Bypass mode as additive jitter			50	ps	1,4

Notes:

1.Guaranteed by design and characterization, not 100% tested in production.

2. All Long Term Accuracy and Clock Period specifications are guaranteed assuming that the input frequency meets CK410 accuracy requirements

3.IREF = VDD/(3xRR). For RR = 475Ω (1%), IREF = 2.32mA. IOH = 6 x IREF and VOH = 0.7V @ ZO=50Ω.

4. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

5. Measured from differential cross-point to differential cross-point

6. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

7. This device does not introduce any ppm errors to the input clock.

Electrical Characteristics - Skew and Differential Jitter Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

Group	Parameter	Description	Min	Max	Units	Notes
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-Output Skew in PLL mode (1:1 only), nominal value @ 25°C, 3.3V	-500	500	ps	1,2,4,5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-Output Skew in Bypass mode (1:1 only), nominal value @ 25°C, 3.3V	2.5	4.5	ns	1,2,3,5
CLK_IN, DIF [x:0]	Δt_{SPO_PLL}	Input-to-Output Skew Variation in PLL mode (over specified voltage / temperature operating ranges)		|350|	ps	1,2,4,5,6, 10
CLK_IN, DIF [x:0]	Δt_{PD_BYP}	Input-to-Output Skew Variation in Bypass mode (over specified voltage / temperature operating ranges)		|500|	ps	1,2,3,4,5, 6,10
DIF[14:0]	t_{SKEW_G15}	Output-to-Output Skew Group of 15 (Common to Bypass and PLL mode)		100	ps	1,2
DIF[18:15]	tSKEW_G4	Output-to-Output Skew Group of 4 (Common to Bypass and PLL mode)		50	ps	1.2
DIF[18:0]	t_{SKEW_A19}	Output-to-Output Skew across all 19 outputs (Common to Bypass and PLL mode - all outputs at same gear)		150	ps	1,2,3
DIF[18:0]	t_{JPH}	Differential Phase Jitter (RMS Value)		10	ps	1,4,7
DIF[18:0]	$t_{SSTERROR}$	Differential Spread Spectrum Tracking Error (peak to peak)		80	ps	1,4,9

NOTES:

1. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
2. Measured from differential cross-point to differential cross-point
3. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
4. This parameter is deterministic for a given device
5. Measured with scope averaging on to find mean value.
6. Long-term variation from nominal of input-to-output skew over temperature and voltage for a single device.
7. This parameter is measured at the outputs of two separate ICS9FG1900 devices driven by a single CK410B. The ICS9FG1900's must be set to high bandwidth. Differential phase jitter is the accumulation of the phase jitter not shared by the outputs (eg. not including the affects of spread spectrum). Target ranges of consideration are agents with BW of 1-22Mhz and 11-33Mhz.
8. t is the period of the input clock
9. Differential spread spectrum tracking error is the difference in spread spectrum tracking between two ICS9FG1900 devices This parameter is measured at the outputs of two separate ICS9FG1900 devices driven by a single CK410B in Spread Spectrum mode. The ICS9FG1900's must be set to high bandwidth. The spread spectrum characteristics are: maximum of 0.5%, 30-33KHz modulation frequency, linear profile.
10. This parameter is an absolute value. It is not a double-sided figure.

Electrical Characteristics - Phase Jitter Parameters

TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, when driven by 932S421B or equivalent

PARAMETER	Symbol	Conditions	Min	Typ	Max	Units	Notes
Jitter, Phase	$t_{jphPCIe1}$	PCIe Gen 1			108	ps (p-p)	1,2
	$t_{jphPCIe2Lo}$	PCIe Gen 2 10kHz < f < 1.5MHz			3	ps (RMS)	1,2
	$t_{jphPCIe2Hi}$	PCIe Gen 2 1.5MHz < f < Nyquist (50MHz)			3.1	ps (RMS)	1,2
	$t_{jphFBD1\_3.2G}$	FBD1 3.2/4G 11MHz to 33MHz			3	ps (RMS)	1,2
	$t_{jphFBD1\_4.0G}$	FBD1 4.8G 11MHz to 33MHz			2.5	ps (RMS)	1,2

Notes:

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See http://www.pcisig.com for complete specs

Programming the 9FG1904B-1

The 9FG1904B-1 uses advanced power saving features to detect when only geared outputs or only 1:1 outputs are needed. It then shuts down the unused PLL. At power up all outputs are coming from the 1:1 PLL and the Gear PLL is shut down. This power saving feature requires a little care when configuring the gear outputs in the device.

Configuring Gear Outputs of the 9FG1904B-1

Selecting Pre-configured Gear Ratios

Byte 0 contains both the bits that enable the gear ratio outputs (Bits 7 and 6), and the bits that select the actual gear ratio (bits (4:0)). It is tempting to enable the gearing outputs and select the gear ratio at the same time. However, this can result in the inability to obtain the proper output frequency. Due to the power saving feature, it is necessary to perform this operation as two steps:

1. First, enable outputs to the gear ratio PLL, which actually powers up the gear ratio PLL (Set Byte 0, bits 7 and 6)
2. Then select the desired gear ratio in a separate write to byte 0 (Set Byte 0, bits (4:0)

The actual order of the two operations is unimportant, so steps 1 and 2 could be reversed if desired.

Programming Gear Ratios that are not Pre-Configured

Most applications using the 9FG1904B-1 can obtain the desired output frequencies from the selections built into the gear table. There are two gear tables defined for these devices. There is the original GS gear set indicated by the DBxxxxGS yellow cover designation and the newer optimized GSO gear set indicated by DBxxxxGSO yellow cover designation. The 9FG1904B-1 contains a gear set that is a combination of the GS and GSO gear sets. The differences between the GS and GSO gear sets are highlighted in Figure 1 GS versus GSO versus 9FG1904B-1 Gear Ratios.

Any gear in the GS or the GSO table that is not pre-configured in the 9FG1904B-1, and virtually any other input/output combination can be obtained by use of M/N programming. Note that care must be used or the jitter/bandwidth characteristics of the PLL can be compromised.

The values provided later in this document have been verified to preserve the PLL performance of the device. Refer to the section *Using M/N Programming to Obtain Other Gear Ratios* for additional details.

	GS Gear Ratios					GSO Gear Ratios					9FG1904-1 Gear Ratios				
	CLK_IN (CPU FSB) MHz	Geared DIF Outputs MHz	M	n	Gear Ratio n/M	CLK_IN (CPU FSB) MHz	Geared DIF Outputs MHz	M	n	Gear Ratio n/M	CLK_IN (CPU FSB) MHz	Geared DIF Outputs MHz	M	n	Gear Ratio n/M
1	100.00	133.33	3	4	1.33	100.00	133.33	3	4	1.33	100.00	133.33	3	4	1.33
2	100.00	166.67	3	5	1.67	100.00	166.67	3	5	1.67	100.00	166.67	3	5	1.67
3	100.00	200.00	1	2	2.00	100.00	200.00	1	2	2.00	100.00	200.00	1	2	2.00
4	100.00	266.67	3	8	2.67	100.00	266.67	3	8	2.67	100.00	266.67	3	8	2.67
5	100.00	333.33	3	10	3.33	100.00	333.33	3	10	3.33	100.00	333.33	3	10	3.33
6	100.00	400.00	1	4	4.00	*133.33*	*100.00*	*4*	*3*	*0.75*	*100.00*	*400.00*	*1*	*4*	*4.00*
7	133.33	166.67	4	5	1.25	*133.33*	*166.67*	*4*	*5*	*1.25*	133.33	166.67	4	5	1.25
8	133.33	200.00	2	3	1.50	*133.33*	*200.00*	*2*	*3*	*1.50*	133.33	200.00	2	3	1.50
9	133.33	266.67	1	2	1.25	*133.33*	*266.67*	*1*	*2*	*2.00*	133.33	266.67	1	2	1.25
10	133.33	333.33	2	5	1.50	*133.33*	*333.33*	*2*	*5*	*2.50*	133.33	333.33	2	5	1.50
11	133.33	400.00	1	3	3.00	133.33	400.00	1	3	3.00	*133.33*	*100.00*	*4*	*3*	*0.75*
12	**166.67**	**133.33**	**5**	**4**	**0.80**	**166.67**	**133.33**	**5**	**4**	**0.80**	**166.67**	**133.33**	**5**	**4**	**0.80**
13	166.67	200.00	5	6	1.20	166.67	200.00	5	6	1.20	166.67	200.00	5	6	1.20
14	166.67	266.67	5	8	1.60	166.67	266.67	5	8	1.60	166.67	266.67	5	8	1.60
15	160/ 166.67	320/ 333.33	1	2	2.00	166.67	333.33	1	2	2.00	160/ 166.67	320/ 333.33	1	2	2.00
16	166.67	400.00	5	12	2.40	166.67	400.00	5	12	2.40	166.67	400.00	5	12	2.40
17	200.00	133.33	3	2	0.67	200.00	133.33	3	2	0.67	200.00	133.33	3	2	0.67
18	200.00	166.67	6	5	0.83	200.00	166.67	6	5	0.83	200.00	166.67	6	5	0.83
19	200.00	266.67	3	4	1.33	200.00	266.67	3	4	1.33	200.00	266.67	3	4	1.33
20	200.00	333.33	3	5	1.67	200.00	333.33	3	5	1.67	200.00	333.33	3	5	1.67
21	200.00	400.00	1	2	2.00	200.00	400.00	1	2	2.00	200.00	400.00	1	2	2.00
22	266.67	133.33	2	1	0.50	266.67	133.33	2	1	0.50	266.67	133.33	2	1	0.50
23	266.667/ 320	166.67/ 200	8	5	0.63	266.67	166.67	8	5	0.63	266.667/ 320.00	166.67/ 200.00	8	5	0.63
24	266.67	200.00	4	3	0.75	266.67	200.00	4	3	0.75	266.67	200.00	4	3	0.75
25	333.33	133.33	5	2	0.40	333.33	133.33	5	2	0.40	333.33	133.33	5	2	0.40
26	320/ 333.33	160/ 166.67	2	1	0.50	333.33	166.67	2	1	0.50	320/ 333.33	160/ 166.67	2	1	0.50
27	333.33	200.00	5	3	0.60	333.33	200.00	5	3	0.60	333.33	200.00	5	3	0.60
28	**400.00**	**133.33**	**3**	**1**	**0.33**	**400.00**	**133.33**	**3**	**1**	**0.33**	**400.00**	**133.33**	**3**	**1**	**0.33**
29	400.00	160.00	5	2	0.40	*400.00*	*166.67*	*12*	*5*	*0.42*	*400.00*	*160.00*	*5*	*2*	*0.40*
30	400.00	166.67	12	5	0.42	*400.00*	*200.00*	*2*	*1*	*0.50*	*400.00*	*166.67*	*12*	*5*	*0.42*
31	400.00	320.00	5	4	0.80	*400.00*	*266.67*	*6*	*4*	*0.67*	*400.00*	*320.00*	*5*	*4*	*0.80*
32	400.00	333.33	6	5	0.83	400.00	333.33	6	5	0.83	400.00	333.33	6	5	0.83

Figure 1 GS versus GSO versus 9FG1904B-1 Gear Ratios

Using M/N Programming to Obtain Other Gear Ratios

M/N programming can be used to obtain input output frequency combinations that are not preconfigured in the 9FG1904B-1. Refer to Figure 2 PLL Block Diagram.

The internal architecture of the 9FG1904B-1 is standard pseudo-ZDB architecture with internal feedback. This means that the REF divider, the Output divider and the Feedback divider all play a role in determining the output frequency. The output frequency is given by the equation:

Output Frequency = (Input Frequency x N x Output Div)/M

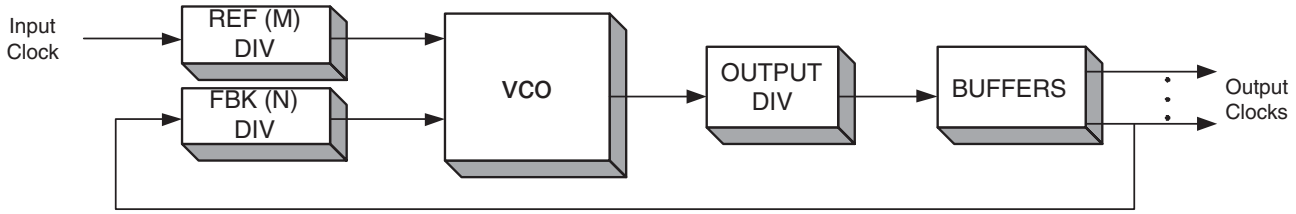


Figure 2 PLL Block Diagram

The DBxxxxGSO input/output combinations that are not in the 9FG1904B-1 gear table are shown in *Table 1 DBxxxxGSO Gears Not Present in the 9FG1904B-1*. This table also gives the values needed to program the gearing PLL to provide the desired input/output combination.

					1:1 PLL Bytes			Byte 17	Byte 18	Byte 19
					Gear PLL Bytes			Byte 11	Byte 12	Byte 13
Line	FS_A_410#	Input Frequency (Fref)	Output Frequency	Decimal M Value	Decimal N Value	Decimal Post Divider	Gear	REF M Div (Hex)	VCO N Div (Hex)	Output Div (Hex)
1	0	133.33	400.00	4	12	2	3.000	2	A	0
2	1	400.00	200.00	12	6	4	0.500	A	4	4
3	1	400.00	266.67	12	8	3	0.667	A	6	1

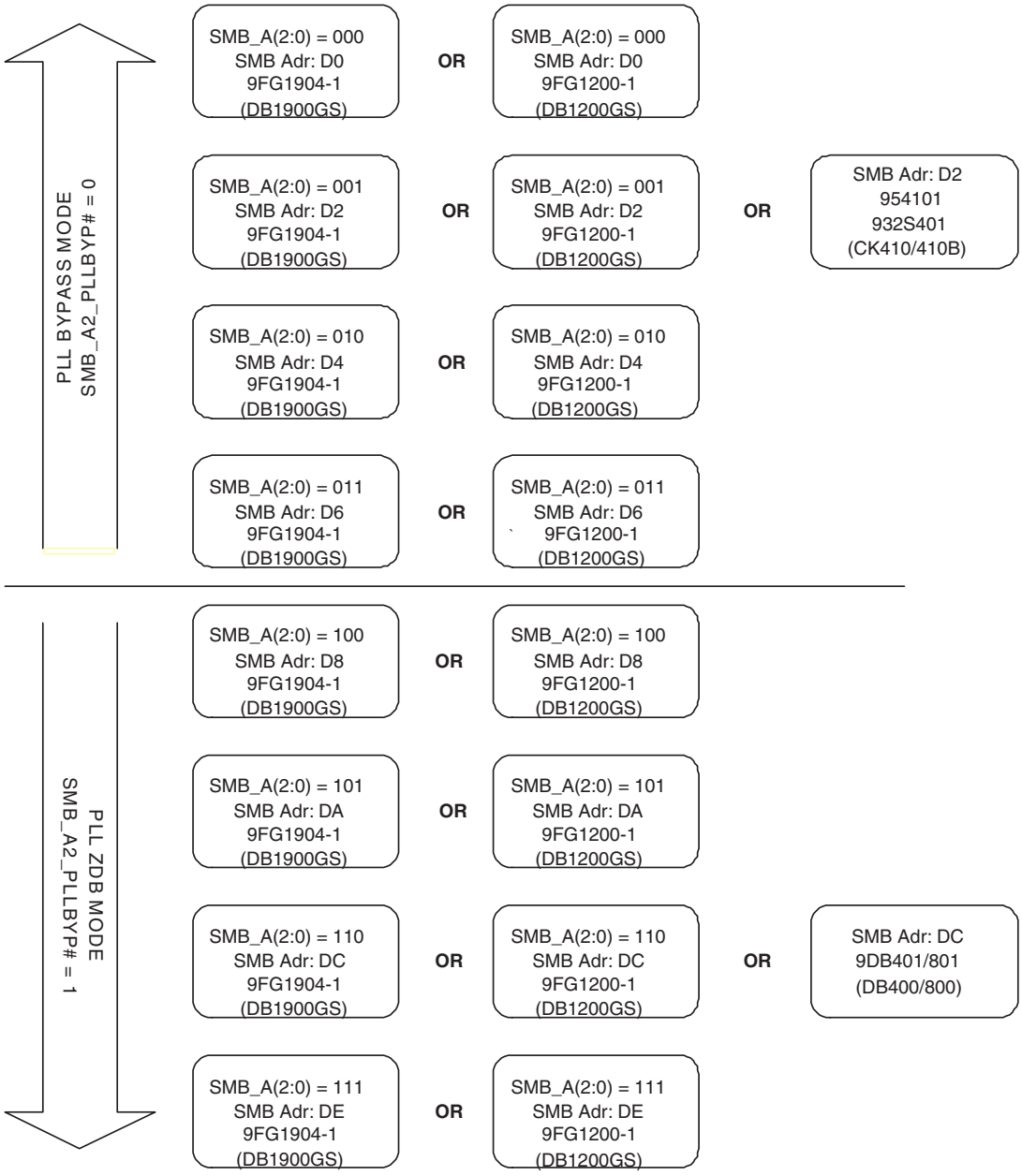
Table 1 DBxxxxGSO Gears Not Present in the 9FG1904B-1

Note before the M/N programming can be accomplished, Byte 10, bit 7 (the M/N_Enable bit) must be set to a '1'. The values provided in the table above have been verified to meet the specified performance of the 9FG1901B-1. Performance is not guaranteed for any other values that have not been pre-approved by IDT. Contact your local IDT representative for other values not mentioned here.

Setting the 1:1 PLL Operating Point

After configuring the Gearing outputs, it is also necessary to set the 1:1 PLL operating point by writing the input frequency value to Byte 9 bits (2:0). The input frequency is usually the CPU HCLK frequency.

9FG1904-1 SMBus Address Mapping when using CK410/CK410B, 9FG1200, and 9DB401/801



General SMBus serial interface information for the ICS9FG1904B-1

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address *D0 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address *D0 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address *D1 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address *D0(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address *D0(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address *D1(H)			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

* The SMBus Address of this device is programmable. See the preceding page for details on how to set the SMBus address.

SMBusTable: Gear Ratio Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	DIF(14:0)	Group of 15 gear ratio enable		RW	Gear Ratio	1:1	1
Bit 6	DIF(18:15)	Group of 4 gear ratio enable		RW	Gear Ratio	1:1	1
Bit 5	-	Reserved		RW			1
Bit 4	-	Gear Ratio FS4 (Inverse of FS_A_410 input!)		RW	See ICS9FG1904-1 Programmable Gear Ratios Table		Latch
Bit 3	-	Gear Ratio FS3		RW			1
Bit 2	-	Gear Ratio FS2		RW			0
Bit 1	-	Gear Ratio FS1		RW			1
Bit 0	-	Gear Ratio FS0		RW			1

SMBusTable: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		DIF_7	Output Control	RW	Hi-Z	Enable	1
Bit 6		DIF_6	Output Control	RW	Hi-Z	Enable	1
Bit 5		DIF_5	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_4	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_3	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_2	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_1	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_0	Output Control	RW	Hi-Z	Enable	1

SMBusTable: Output and PLL BW Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	see note	PLL_BW# adjust		RW	High BW	Low BW	1
Bit 6	see note	BYPASS# test mode / PLL		RW	Bypass	PLL	1
Bit 5		DIF_13	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_12	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_11	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_10	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_9	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_8	Output Control	RW	Hi-Z	Enable	1

Note: Bit 7 is wired OR to the HIGH_BW# input, any 0 selects High BW

Note: Bit 6 is wired OR to the SMB_A2_PLLBYP# input, any 0 selects Fanout Bypass mode

SMBusTable: Output Enable Readback Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Readback - OE9# Input		R	Readback		X
Bit 6		Readback - OE8# Input		R	Readback		X
Bit 5		Readback - OE7# Input		R	Readback		X
Bit 4		Readback - OE6# Input		R	Readback		X
Bit 3		Readback - OE5# Input		R	Readback		X
Bit 2		Readback - OE_01234# Input		R	Readback		X
Bit 1	8	Readback - HIGH_BW# In		R	Readback		X
Bit 0	72	Readback - SMB_A2_PLLBYP# In		R	Readback		X

SMBusTable: Output Enable Readback Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	69	Readback - OE17_18# Input		R	Readback		X
Bit 6	60	Readback - OE15_16# Input		R	Readback		X
Bit 5	Reserved						X
Bit 4	54	Readback - OE14# Input		R	Readback		X
Bit 3	51	Readback - OE13# Input		R	Readback		X
Bit 2	48	Readback - OE12# Input		R	Readback		X
Bit 1	43	Readback - OE11# Input		R	Readback		X
Bit 0	40	Readback - OE10# Input		R	Readback		X

SMBusTable: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID 7 (MSB)		RW	Reserved		1
Bit 6	-	Device ID 6		RW	Reserved		0
Bit 5	-	Device ID 5		RW	Reserved		0
Bit 4	-	Device ID 4		RW	Reserved		1
Bit 3	-	Device ID 3		RW	Reserved		0
Bit 2	-	Device ID 2		RW	Reserved		1
Bit 1	-	Device ID 1		RW	Reserved		0
Bit 0	-	Device ID 0		RW	Reserved		0

SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

SMBusTable: Control Pin Readback Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	5	Readback - FS_A_410		R	Readback		X
Bit 6		RESERVED					X
Bit 5		RESERVED					X
Bit 4		DIF_18	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_17	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_16	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_15	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_14	Output Control	RW	Hi-Z	Enable	1

SMBusTable: 1:1 PLL Operating Set Point Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2	-	Frequency Select C		RW	See ICS9FG1904 1:1 PLL Programming Table		x
Bit 1	-	Frequency Select B		RW			1
Bit 0	-	FS_A_410		RW			Latch

SMBus Table: M/N Programming & Watchdog Safe Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	Gear and 1:1 PLL M/N Programming Enable	RW	Disable	Enable	0
Bit 6		RESERVED					X
Bit 5		RESERVED					X
Bit 4		RESERVED					X
Bit 3		RESERVED					X
Bit 2		RESERVED					X
Bit 1		RESERVED					X
Bit 0		RESERVED					X

SMBus Table: Gear PLL Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					X
Bit 6		RESERVED					X
Bit 5	-	Gear PLL M Div5	M Divider	RW	See M/N Programming Section of the Data Sheet		X
Bit 4	-	Gear PLL M Div4		RW			X
Bit 3	-	Gear PLL M Div3		RW			X
Bit 2	-	Gear PLL M Div2		RW			X
Bit 1	-	Gear PLL M Div1		RW			X
Bit 0	-	Gear PLL M Div0		RW			X

SMBus Table: Gear PLL Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Gear PLL N Div7	N Divider	RW	See M/N Programming Section of the Data Sheet		X
Bit 6	-	Gear PLL N Div6		RW			X
Bit 5	-	Gear PLL N Div5		RW			X
Bit 4	-	Gear PLL N Div4		RW			X
Bit 3	-	Gear PLL N Div3		RW			X
Bit 2	-	Gear PLL N Div2		RW			X
Bit 1	-	Gear PLL N Div1		RW			X
Bit 0	-	Gear PLL N Div0		RW			X

SMBusTable: Reserved Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		Gear PLL Out Div 3	Gear PLL Output Divider	RW	See Output Divider Ratios Table		x
Bit 2		Gear PLL Out Div 2	Gear PLL Output Divider	RW			x
Bit 1		Gear PLL Out Div 1	Gear PLL Output Divider	RW			x
Bit 0		Gear PLL Out Div 0	Gear PLL Output Divider	RW			x

SMBusTable: Reserved Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

SMBusTable: Reserved Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

SMBusTable: Reserved Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

SMBus Table: 1:1 PLL Frequency Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					X
Bit 6		RESERVED					X
Bit 5	-	1:1 PLL M Div5	M Divider Programming bits	RW	See M/N Programming Section of the Data Sheet		X
Bit 4	-	1:1 PLL M Div4		RW			X
Bit 3	-	1:1 PLL M Div3		RW			X
Bit 2	-	1:1 PLL M Div2		RW			X
Bit 1	-	1:1 PLL M Div1		RW			X
Bit 0	-	1:1 PLL M Div0		RW			X

SMBus Table: 1:1 PLL Frequency Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	1:1 PLL N Div7	N Divider Programming b(7:0)	RW	See M/N Programming Section of the Data Sheet		X
Bit 6	-	1:1 PLL N Div6		RW			X
Bit 5	-	1:1 PLL N Div5		RW			X
Bit 4	-	1:1 PLL N Div4		RW			X
Bit 3	-	1:1 PLL N Div3		RW			X
Bit 2	-	1:1 PLL N Div2		RW			X
Bit 1	-	1:1 PLL N Div1		RW			X
Bit 0	-	1:1 PLL N Div0		RW			X

SMBusTable: Reserved Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		1:1 PLL Out Div 3	1:1 PLL Output Divider	RW	See Output Divider Ratios Table		x
Bit 2		1:1 PLL Out Div 2	1:1 PLL Output Divider	RW			x
Bit 1		1:1 PLL Out Div 1	1:1 PLL Output Divider	RW			x
Bit 0		1:1 PLL Out Div 0	1:1 PLL Output Divider	RW			x

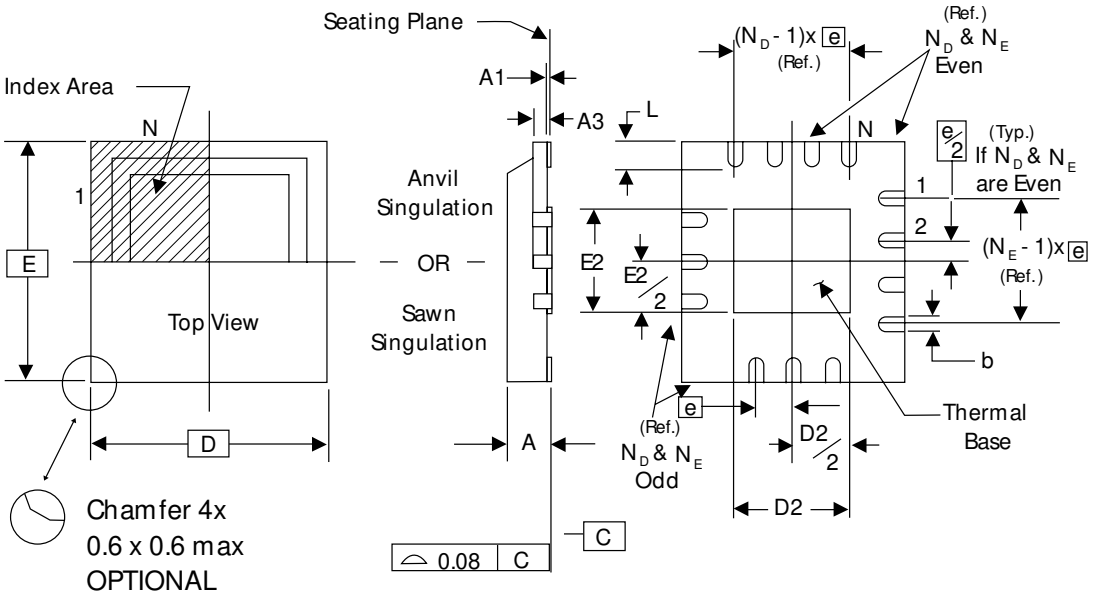
SMBusTable: Reserved Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

SMBusTable: Test Byte Register

Byte 21	Test	Test Function	Type	Test Result	PWD
Bit 7	`	ICS ONLY TEST	RW	Reserved	0
Bit 6		ICS ONLY TEST	RW	Reserved	0
Bit 5		ICS ONLY TEST	RW	Reserved	0
Bit 4		ICS ONLY TEST	RW	Reserved	0
Bit 3		ICS ONLY TEST	RW	Reserved	0
Bit 2		ICS ONLY TEST	RW	Reserved	0
Bit 1		ICS ONLY TEST	RW	Reserved	0
Bit 0		ICS ONLY TEST	RW	Reserved	0

Note: Do NOT write to Bit 21. Erratic device operation will result!



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	

DIMENSIONS

SYMBOL	ICS 72L TOLERANCE
N	72
N_D	18
N_E	18
D x E BASIC	10.00 x 10.00
D2 MIN. / MAX.	5.75 / 6.15
E2 MIN. / MAX.	5.75 / 6.15
L MIN. / MAX.	0.30/ 0.50

Ordering Information

ICS 9FG1904BK-1LFT

Example:

ICS XXXX B K - V LF T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Variation Number**
- **Package Type**
  K = MLF
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 to 7 digit numbers)**

Revision History

Rev.	Issue Date	Description	Page #
A	05/04/07	1. Added Output Divider Table. 2. Added Phase Jitter Table to electrical characteristics. 3. Added M/N programming information. 4. Changed part number to reference 9FG1904B-1.	Various
B	08/03/07	Release to Final.	-