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### Description

The 9FGL06 devices are 3.3V members of IDT's 3.3V Full-Featured PCIe family. The devices have 6 output enables for clock management and support 2 different spread spectrum levels in addition to spread off. The 9FGL06 supports PCIe Gen1-4 Common Clocked architectures (CC) and PCIe Separate Reference no-Spread (SRnS) and Separate Reference Independent Spread (SRIS) clocking architectures. The 9FGL06P1 can be programmed with a user-defined power up default SMBus configuration.

### Recommended Application

PCIe Gen1-4 clock generation for Riser Cards, Storage, Networking, JBOD, Communications, Access Points

### Output Features

- 6 – 100 MHz Low-Power HCSL (LP-HCSL) DIF pairs
  - 9FGL0641 default  $Z_{OUT} = 100\Omega$
  - 9FGL0651 default  $Z_{OUT} = 85\Omega$
  - 9FGL06P1 factory programmable defaults
- 1 - 3.3V LVCMOS REF output w/Wake-On-LAN (WOL) support
- Easy AC-coupling to other logic families, see IDT application note [AN-891](#)

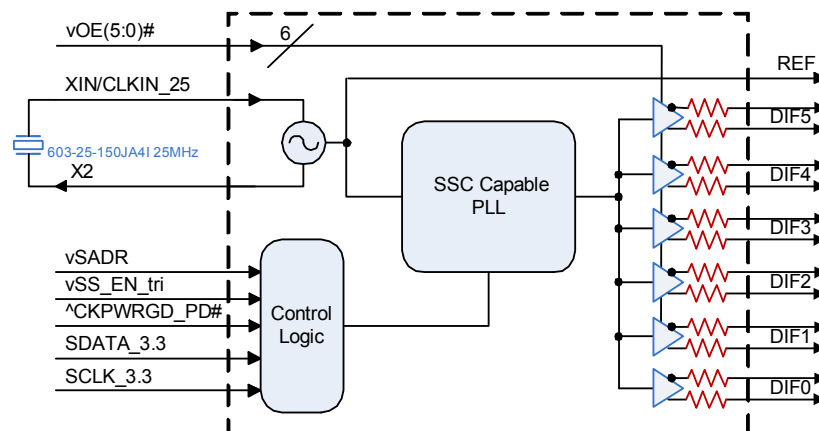
### Key Specifications

- PCIe Gen1-2-3-4 CC-compliant
- PCIe Gen2-3 SRIS-compliant
- DIF cycle-to-cycle jitter <50ps
- DIF output-to-output skew <50ps
- DIF 12k-20M phase jitter is <2ps rms when SSC is off
- REF phase jitter is <300fs rms, SSC off, and <1.5ps rms, SSC is On
- $\pm 100$ ppm frequency accuracy on all clocks

### Features/Benefits

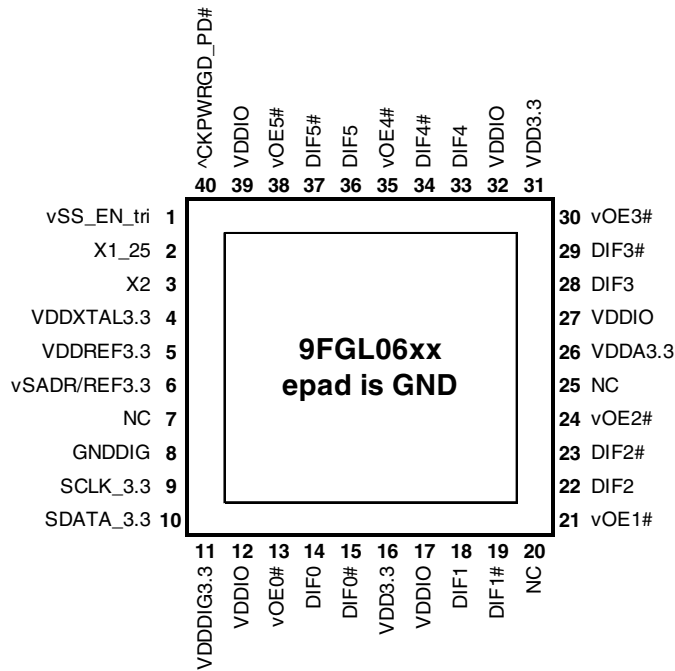
- Direct connection to  $100\Omega$  (xx41) or  $85\Omega$  (xx51) transmission lines; saves 24 resistors compared to standard PCIe devices
- 172mW typical power consumption (@3.3V); eliminates thermal concerns
- SMBus-selectable features allows optimization to customer requirements:
  - control input polarity
  - control input pull up/downs
  - slew rate for each output
  - differential output amplitude
  - 33, 85 or  $100\Omega$  output impedance for each output
  - spread spectrum amount
- 41 and 51 devices contain default configuration; SMBus interface not required for device operation
- P1 device allows factory programming of customer-defined SMBus power up default; allows exact optimization to customer requirements
- 8MHz - 40MHz input frequency with 9FGL08P1 device (25MHz default); flexibility
- OE# pins; support DIF power management
- Pin/SMBus selectable 0%, -0.25% or -0.5% spread on DIF outputs; minimize EMI and phase jitter for each application
- DIF outputs blocked until PLL is locked; clean system start-up
- Two selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Space saving 40-pin 5x5mm VFQFPN; minimal board space

### Block Diagram



**Note:** Resistors default to internal on 41/51 devices. P1 devices have programmable default impedances on an output-by-output basis.

## Pin Configuration



### 40-pin VFQFPN, 5x5 mm, 0.4mm pitch

- v prefix indicates internal 120KOhm pull down resistor
- ^ prefix indicates internal 120KOhm pull up resistor

## SMBus Address Selection Table

|   | SADR | Address | + Read/Write Bit |
|---|------|---------|------------------|
| State of SADR on first application of CKPWRGD_PD# | 0    | 1101000 | x                |
|   | 1    | 1101010 | x                |

## Power Management Table<sup>3</sup>

| CKPWRGD_PD# | SMBus OE bit | OEx# Pin | DIFx                  |                       | REF                   |
|-------------|--------------|----------|-----------------------|-----------------------|-----------------------|
|             |              |          | True O/P              | Comp. O/P             |                       |
| 0           | X            | X        | Low <sup>1</sup>      | Low <sup>1</sup>      | Hi-Z <sup>2</sup>     |
| 1           | 1            | 0        | Running               | Running               | Running               |
| 1           | 1            | 1        | Disabled <sup>1</sup> | Disabled <sup>1</sup> | Running               |
| 1           | 0            | X        | Disabled <sup>1</sup> | Disabled <sup>1</sup> | Disabled <sup>4</sup> |

1. The output state is set by B11[1:0] (Low/Low default)
2. REF is Hi-Z until the 1st assertion of CKPWRGD\_PD# high. After this, when CKPWRGD\_PD# is low, REF is disabled unless Byte3[5]=1, in which case REF is running.
3. Input polarities defined at default values for 9FGL0641/0651.
4. See SMBus description for Byte 3, bit 4

## Power Connections

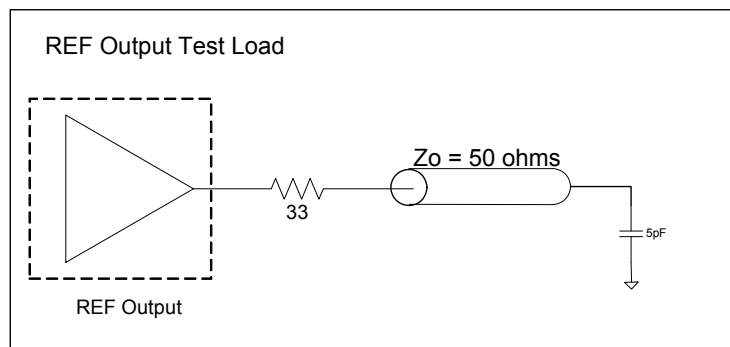
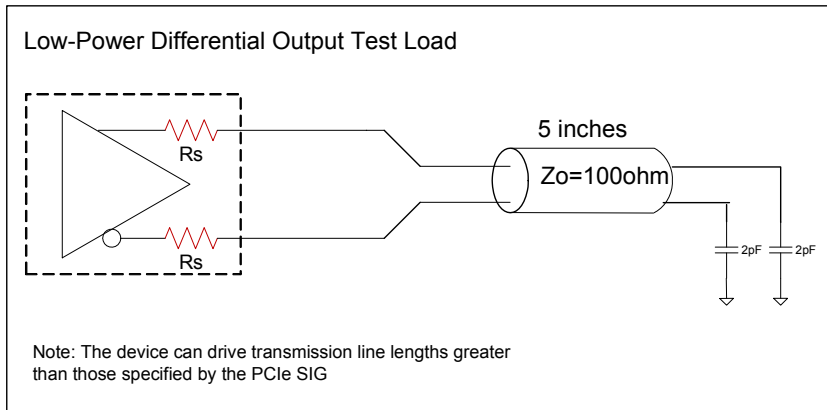
| Pin Number |                | GND | Description           |
|------------|----------------|-----|-----------------------|
| VDD        | VDDIO          |     |                       |
| 4          |                | 41  | XTAL OSC              |
| 5          |                | 41  | REF Power             |
| 11         |                | 8   | Digital (dirty) Power |
|            | 12,17,27,32,39 | 41  | DIF outputs           |
| 26         |                | 41  | PLL Analog            |



## Pin Descriptions

| PIN # | PIN NAME     | PIN TYPE       | DESCRIPTION   |
|-------|--------------|----------------|---|
| 1     | vSS_EN_tri   | LATCHED<br>IN  | Latched select input to select spread spectrum amount at initial power up :<br>1 = -0.5% spread, M = -0.25%, 0 = Spread Off   |
| 2     | X1_25        | IN             | Crystal input, Nominally 25.00MHz.  |
| 3     | X2           | OUT            | Crystal output.   |
| 4     | VDDXTAL3.3   | PWR            | Power supply for XTAL, nominal 3.3V   |
| 5     | VDDREF3.3    | PWR            | VDD for REF output. nominal 3.3V.   |
| 6     | vSADR/REF3.3 | LATCHED<br>I/O | Latch to select SMBus Address/3.3V LVCMOS copy of X1/REFIN pin  |
| 7     | NC           | N/A            | No Connection.  |
| 8     | GNDDIG       | GND            | Ground pin for digital circuitry  |
| 9     | SCLK_3.3     | IN             | Clock pin of SMBus circuitry, 3.3V tolerant.  |
| 10    | SDATA_3.3    | I/O            | Data pin for SMBus circuitry, 3.3V tolerant.  |
| 11    | VDDDIG3.3    | PWR            | 3.3V digital power (dirty power)  |
| 12    | VDDIO        | PWR            | Power supply for differential outputs   |
| 13    | voE0#        | IN             | Active low input for enabling DIF pair 0. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs   |
| 14    | DIF0         | OUT            | Differential true clock output  |
| 15    | DIF0#        | OUT            | Differential Complementary clock output   |
| 16    | VDD3.3       | PWR            | Power supply, nominal 3.3V  |
| 17    | VDDIO        | PWR            | Power supply for differential outputs   |
| 18    | DIF1         | OUT            | Differential true clock output  |
| 19    | DIF1#        | OUT            | Differential Complementary clock output   |
| 20    | NC           | N/A            | No Connection.  |
| 21    | voE1#        | IN             | Active low input for enabling DIF pair 1. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs   |
| 22    | DIF2         | OUT            | Differential true clock output  |
| 23    | DIF2#        | OUT            | Differential Complementary clock output   |
| 24    | voE2#        | IN             | Active low input for enabling DIF pair 2. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs   |
| 25    | NC           | N/A            | No Connection.  |
| 26    | VDDA3.3      | PWR            | 3.3V power for the PLL core.  |
| 27    | VDDIO        | PWR            | Power supply for differential outputs   |
| 28    | DIF3         | OUT            | Differential true clock output  |
| 29    | DIF3#        | OUT            | Differential Complementary clock output   |
| 30    | voE3#        | IN             | Active low input for enabling DIF pair 3. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs   |
| 31    | VDD3.3       | PWR            | Power supply, nominal 3.3V  |
| 32    | VDDIO        | PWR            | Power supply for differential outputs   |
| 33    | DIF4         | OUT            | Differential true clock output  |
| 34    | DIF4#        | OUT            | Differential Complementary clock output   |
| 35    | voE4#        | IN             | Active low input for enabling DIF pair 4. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs   |
| 36    | DIF5         | OUT            | Differential true clock output  |
| 37    | DIF5#        | OUT            | Differential Complementary clock output   |
| 38    | voE5#        | IN             | Active low input for enabling DIF pair 5. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs   |
| 39    | VDDIO        | PWR            | Power supply for differential outputs   |
| 40    | ^CKPWRGD_PD# | IN             | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |
| 41    | ePAD         | GND            | Connect paddle to ground.   |

## Test Loads



### Terminations

| Device   | Zo ( $\Omega$ ) | Rs ( $\Omega$ ) |
|----------|-----------------|-----------------|
| 9FGL0641 | 100             | None needed     |
| 9FGL0651 | 100             | 7.5             |
| 9FGL06P1 | 100             | Prog.           |
| 9FGL0641 | 85              | N/A             |
| 9FGL0651 | 85              | None needed     |
| 9FGL06P1 | 85              | Prog.           |

## Alternate Terminations

The 9FGL family can easily drive LVPECL, LVDS, and CML logic. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs”](#) for details.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9FGL06. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER                 | SYMBOL             | CONDITIONS                                  | MIN  | TYP | MAX                    | UNITS | NOTES |
|---------------------------|--------------------|---|------|-----|------------------------|-------|-------|
| 3.3V Supply Voltage       | VDDxx              | Applies to VDD, VDDA and VDDIO, if present. | -0.5 |     | 3.9                    | V     | 1,2   |
| Input Voltage             | V <sub>IN</sub>    |   | -0.5 |     | V <sub>DD</sub> + 0.5V | V     | 1, 3  |
| Input High Voltage, SMBus | V <sub>IHSMB</sub> | SMBus clock and data pins                   |      |     | 3.9                    | V     | 1     |
| Storage Temperature       | T <sub>S</sub>     |   | -65  |     | 150                    | °C    | 1     |
| Junction Temperature      | T <sub>J</sub>     |   |      |     | 125                    | °C    | 1     |
| Input ESD protection      | ESD prot           | Human Body Model                            | 2500 |     |                        | V     | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

<sup>3</sup>Not to exceed 4.5V.

## Electrical Characteristics–SMBus Parameters

TA = T<sub>AMB</sub>; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER                 | SYMBOL              | CONDITIONS                           | MIN | TYP | MAX  | UNITS | NOTES |
|---------------------------|---------------------|--------------------------------------|-----|-----|------|-------|-------|
| SMBus Input Low Voltage   | V <sub>ILSMB</sub>  | V <sub>DDSMB</sub> = 3.3V            |     |     | 0.8  | V     |       |
| SMBus Input High Voltage  | V <sub>IHSMB</sub>  | V <sub>DDSMB</sub> = 3.3V            | 2.1 |     | 3.6  | V     |       |
| SMBus Output Low Voltage  | V <sub>OLSMB</sub>  | @ I <sub>PULLUP</sub>                |     |     | 0.4  | V     |       |
| SMBus Sink Current        | I <sub>PULLUP</sub> | @ V <sub>OL</sub>                    | 4   |     |      | mA    |       |
| Nominal Bus Voltage       | V <sub>DDSMB</sub>  |                                      | 2.7 |     | 3.6  | V     |       |
| SCLK/SDATA Rise Time      | t <sub>RSMB</sub>   | (Max VIL - 0.15) to (Min VIH + 0.15) |     |     | 1000 | ns    | 1     |
| SCLK/SDATA Fall Time      | t <sub>FSMB</sub>   | (Min VIH + 0.15) to (Max VIL - 0.15) |     |     | 300  | ns    | 1     |
| SMBus Operating Frequency | f <sub>SMB</sub>    | SMBus operating frequency            |     |     | 500  | kHz   | 2     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>The device must be powered up for the SMBus to function.

## Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = T<sub>AMB</sub>; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER                     | SYMBOL              | CONDITIONS  | MIN                   | TYP                  | MAX                    | UNITS  | NOTES |
|-------------------------------|---------------------|---|-----------------------|----------------------|------------------------|--------|-------|
| Supply Voltage                | VDD <sub>xxx</sub>  | Supply voltage for core, analog and single-ended LVCMOS outputs.  | 3.135                 | 3.3                  | 3.465                  | V      |       |
| IO Supply Voltage             | VDDIO               | Supply voltage for differential Low Power outputs.  | 0.9975                | 1.05-3.3             | 3.465                  | V      |       |
| Ambient Operating Temperature | T <sub>AMB</sub>    | Industrial range  | -40                   | 25                   | 85                     | °C     |       |
| Input High Voltage            | V <sub>IH</sub>     | Single-ended inputs, except SMBus   | 0.75 V <sub>DDx</sub> |                      | V <sub>DDx</sub> + 0.3 | V      |       |
| Input Low Voltage             | V <sub>IL</sub>     |   | -0.3                  |                      | 0.25 V <sub>DDx</sub>  | V      |       |
| Input High Voltage            | V <sub>IHtri</sub>  | Single-ended tri-level inputs ('_tri' suffix)   | 0.75 V <sub>DDx</sub> |                      | V <sub>DD</sub> + 0.3  | V      |       |
| Input Mid Voltage             | V <sub>IMtri</sub>  |   | 0.4 V <sub>DDx</sub>  | 0.5 V <sub>DDx</sub> | 0.6 V <sub>DDx</sub>   | V      |       |
| Input Low Voltage             | V <sub>ILtri</sub>  |   | -0.3                  |                      | 0.25 V <sub>DDx</sub>  | V      |       |
| Input Current                 | I <sub>IN</sub>     | Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD   | -5                    |                      | 5                      | uA     |       |
|                               | I <sub>INP</sub>    | Single-ended inputs<br>V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors<br>V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors | -50                   |                      | 50                     | uA     |       |
| Input Frequency               | F <sub>in</sub>     | XTAL, or X1 input   | 8                     | 25                   | 40                     | MHz    | 4     |
| Pin Inductance                | L <sub>pin</sub>    |   |                       |                      | 7                      | nH     | 1     |
| Capacitance                   | C <sub>IN</sub>     | Logic Inputs, except DIF_IN   | 1.5                   |                      | 5                      | pF     | 1     |
|                               | C <sub>OUT</sub>    | Output pin capacitance  |                       |                      | 6                      | pF     | 1     |
| Clk Stabilization             | T <sub>STAB</sub>   | From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock   |                       | 0.3                  | 1.8                    | ms     | 1,2   |
| SS Modulation Frequency       | f <sub>MOD</sub>    | (Triangular Modulation)   | 30                    | 31.6                 | 33                     | kHz    | 1     |
| OE# Latency                   | t <sub>LATOE#</sub> | DIF start after OE# assertion<br>DIF stop after OE# deassertion   | 1                     | 2                    | 3                      | clocks | 1,3   |
| Tdrive_PD#                    | t <sub>DRVPD</sub>  | DIF output enable after PD# de-assertion  |                       | 28                   | 300                    | us     | 1,3   |
| Tfall                         | t <sub>F</sub>      | Fall time of single-ended control inputs  |                       |                      | 5                      | ns     | 1,2   |
| Trise                         | t <sub>R</sub>      | Rise time of single-ended control inputs  |                       |                      | 5                      | ns     | 1,2   |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup> Time from deassertion until outputs are >200 mV

<sup>4</sup> The 9FGLxxP1 devices can be programmed for various input frequencies from 8 to 40MHz. The 9FGLxx41/51 devices use 25MHz.

## Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = T<sub>AMB</sub>; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER                  | SYMBOL                  | CONDITIONS  | MIN     | TYP  | MAX     | UNITS | NOTES   |
|----------------------------|-------------------------|---|---------|------|---------|-------|---------|
| Slew rate                  | Trf                     | Scope averaging on, fast setting  | 2       | 2.7  | 4       | V/ns  | 2,3     |
|                            |                         | Scope averaging, slow setting   | 1       | 1.9  | 3       | V/ns  | 2,3     |
| Crossing Voltage (abs)     | V <sub>cross_abs</sub>  | Scope averaging off   | 250     | 409  | 550     | mV    | 1,4,5   |
| Crossing Voltage (var)     | ΔV <sub>cross</sub>     | Scope averaging off   |         | 14   | 140     | mV    | 1,4,9   |
| Avg. Clock Period Accuracy | T <sub>PERIOD_AVG</sub> |   | -100    | 0.0  | +2600   | ppm   | 2,10,13 |
| Absolute Period            | T <sub>PERIOD_ABS</sub> | Includes jitter and Spread Spectrum Modulation  | 9.94906 | 10.0 | 10.1011 | ns    | 2,6     |
| Jitter, Cycle to cycle     | t <sub>ICVC-CYC</sub>   |   |         | 16   | 50      | ps    | 2       |
| Voltage High               | V <sub>HIGH</sub>       | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660     | 761  | 850     | mV    | 1       |
| Voltage Low                | V <sub>LOW</sub>        |   | -150    | -7   | 150     |       | 1       |
| Absolute Max Voltage       | V <sub>max</sub>        | Measurement on single ended signal using absolute value. (Scope averaging off)                        |         | 819  | 1150    | mV    | 1,7,15  |
| Absolute Min Voltage       | V <sub>min</sub>        |   | -300    | -46  |         |       | 1,8,15  |
| Duty Cycle                 | t <sub>DC</sub>         |   | 45      | 49   | 55      | %     | 2       |
| Slew rate matching         | ΔTrf                    |   |         | 6    | 20      | %     | 1,14    |
| Skew, Output to Output     | t <sub>sk3</sub>        | Averaging on, V <sub>T</sub> = 50%  |         | 35   | 50      | ps    | 2       |

<sup>1</sup> Measured from single-ended waveform.

<sup>2</sup> Measured from differential waveform.

<sup>3</sup> Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

<sup>4</sup> Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

<sup>5</sup> Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

<sup>6</sup> Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation.

<sup>7</sup> Defined as the maximum instantaneous voltage including overshoot.

<sup>8</sup> Defined as the minimum instantaneous voltage including undershoot.

<sup>9</sup> Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V<sub>CROSS</sub> for any particular system.

<sup>10</sup> Refer to Section 4.3.7.1.1 of the PCI Express Base Specification, Revision 3.0 for information regarding PPM considerations.

<sup>11</sup> System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL = 2 pF.

<sup>12</sup> T<sub>STABLE</sub> is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range.

<sup>13</sup> PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 PPM, then we have an error budget of 100 Hz/PPM \* 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum Clocking, or that use common clock source. For systems employing Spread Spectrum Clocking, there is an additional 2,500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,800 PPM.

<sup>14</sup> Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

<sup>15</sup> At default SMBus amplitude settings.



## Electrical Characteristics—Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

$T_{AMB}$  = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER          | SYMBOL  | CONDITIONS  | MIN | TYP  | MAX  | INDUSTRY LIMIT | UNITS    | Notes |
|--------------------|---|---|-----|------|------|----------------|----------|-------|
| Phase Jitter       | $t_{jphPCIeG1-CC}$                                      | PCIe Gen 1  |     | 19   | 28   | 86             | ps (p-p) | 1,2,3 |
|                    | $t_{jphPCIeG2-CC}$                                      | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz<br>(PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)             |     | 0.4  | 0.6  | 3              | ps (rms) | 1,2   |
|                    |   | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz)<br>(PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz) |     | 1.2  | 1.9  | 3.1            | ps (rms) | 1,2   |
|                    | $t_{jphPCIeG3-CC}$                                      | PCIe Gen 3<br>(PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)   |     | 0.3  | 0.45 | 1              | ps (rms) | 1,2   |
| $t_{jphPCIeG4-CC}$ | PCIe Gen 4<br>(PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz) |   | 0.3 | 0.45 | 0.5  | ps (rms)       | 1,2      |       |

<sup>1</sup> Applies to all outputs.

<sup>2</sup> Based on PCIe Base Specification Rev4.0 version 0.7draft. See <http://www.pcisig.com> for latest specifications.

<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

## Electrical Characteristics—Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures

$T_{AMB}$  = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER              | SYMBOL               | CONDITIONS  | MIN | TYP | MAX  | INDUSTRY LIMIT | UNITS    | Notes |
|------------------------|----------------------|---|-----|-----|------|----------------|----------|-------|
| Phase Jitter, PLL Mode | $t_{jphPCIeG2-SRIS}$ | PCIe Gen 2<br>(PLL BW of 16MHz, CDR = 5MHz)             |     | 0.7 | 1.1  | 2              | ps (rms) | 1,2   |
|                        | $t_{jphPCIeG3-SRIS}$ | PCIe Gen 3<br>(PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz) |     | 0.5 | 0.65 | 0.7            | ps (rms) | 1,2   |

<sup>1</sup> Applies to all outputs.

<sup>2</sup> Based on PCIe Base Specification Rev3.1a. These filters are different than Common Clock filters. See <http://www.pcisig.com> for latest specifications. There is a proposal to reduce the PCIe Gen3 limit to 0.5ps.

<sup>3</sup> As of PCIe Base Specification Rev4.0 draft 0.7, SRIS is not currently defined for Gen1 or Gen4.

## Electrical Characteristics—DIF LP-HCSL Output Unfiltered Phase Jitter Parameters

$T_A = T_{AMB}$ . Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER             | SYMBOL          | CONDITIONS  | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS    |
|-----------------------|-----------------|---|-----|-----|-----|----------------|----------|
| Phase Jitter, 12k-20M | $t_{jph12k20M}$ | 100MHz outputs with REF output enabled<br>SSC Off |     | 1.5 | 2   | N/A            | ps (rms) |

## Electrical Characteristics–Current Consumption

TA = T<sub>AMB</sub>; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER   | SYMBOL              | CONDITIONS  | MIN | TYP  | MAX | UNITS | NOTES |
|---|---------------------|---|-----|------|-----|-------|-------|
| Operating Supply Current  | I <sub>DDAOP</sub>  | VDDA, All outputs active @100MHz                                    |     | 13   | 18  | mA    |       |
|   | I <sub>DDOP</sub>   | All VDD, except VDDA and VDDIO, All outputs active @100MHz          |     | 16   | 22  | mA    |       |
|   | I <sub>DDIOOP</sub> | VDDIO, All outputs active @100MHz                                   |     | 24   | 28  | mA    |       |
| Wake-on-LAN Current<br>(Power down state and Byte 3, bit 5 = '1') | I <sub>DDAPD</sub>  | VDDA, DIF outputs off, REF output running                           |     | 0.9  | 1.5 | mA    | 1     |
|   | I <sub>DDPD</sub>   | All VDD, except VDDA and VDDIO, DIF outputs off, REF output running |     | 6.2  | 9.0 | mA    | 1     |
|   | I <sub>DDIOPD</sub> | VDDIO, DIF outputs off, REF output running                          |     | 0.04 | 0.1 | mA    | 1     |
| Powerdown Current<br>(Power down state and Byte 3, bit 5 = '0')   | I <sub>DDAPD</sub>  | VDDA, all outputs off   |     | 0.9  | 1.5 | mA    |       |
|   | I <sub>DDPD</sub>   | All VDD, except VDDA and VDDIO, all outputs off                     |     | 1.8  | 2.5 | mA    |       |
|   | I <sub>DDIOPD</sub> | VDDIO, all outputs off  |     | 0.04 | 0.1 | mA    |       |

<sup>1</sup> This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1)

## Electrical Characteristics– REF

TA = T<sub>AMB</sub>; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER              | SYMBOL               | CONDITIONS  | MIN                    | TYP   | MAX                    | UNITS   | Notes |
|------------------------|----------------------|---|------------------------|-------|------------------------|---------|-------|
| Long Accuracy          | ppm                  | see T <sub>period</sub> min-max values                            | 0                      |       |                        | ppm     | 1,2   |
| Clock period           | T <sub>period</sub>  | REF output  | 40                     |       |                        | ns      | 2     |
| High output Voltage    | V <sub>HIGH</sub>    | I <sub>oh</sub> = -2mA  | 0.8xV <sub>DDREF</sub> |       |                        | V       |       |
| Low output Voltage     | V <sub>LOW</sub>     | I <sub>ol</sub> = 2mA   |                        |       | 0.2xV <sub>DDREF</sub> | V       |       |
| Rise/Fall Slew Rate    | t <sub>rf1</sub>     | Byte 3 = 1F, V <sub>OH</sub> = 0.8*VDD, V <sub>OL</sub> = 0.2*VDD | 0.5                    | 0.9   | 1.5                    | V/ns    | 1     |
| Rise/Fall Slew Rate    | t <sub>rf1</sub>     | Byte 3 = 5F, V <sub>OH</sub> = 0.8*VDD, V <sub>OL</sub> = 0.2*VDD | 1.0                    | 1.5   | 2.5                    | V/ns    | 1,3   |
| Rise/Fall Slew Rate    | t <sub>rf1</sub>     | Byte 3 = 9F, V <sub>OH</sub> = 0.8*VDD, V <sub>OL</sub> = 0.2*VDD | 1.5                    | 2.1   | 3.1                    | V/ns    | 1     |
| Rise/Fall Slew Rate    | t <sub>rf1</sub>     | Byte 3 = DF, V <sub>OH</sub> = 0.8*VDD, V <sub>OL</sub> = 0.2*VDD | 2.0                    | 2.7   | 3.8                    | V/ns    | 1     |
| Duty Cycle             | d <sub>t1X</sub>     | V <sub>T</sub> = VDD/2 V  | 45                     | 49.7  | 55                     | %       | 1,4   |
| Duty Cycle Distortion  | d <sub>tcd</sub>     | V <sub>T</sub> = VDD/2 V  | -1                     | 0     | 0                      | %       | 1,5   |
| Jitter, cycle to cycle | t <sub>jyc-cyc</sub> | V <sub>T</sub> = VDD/2 V  |                        | 35    | 125                    | ps      | 1,4   |
| Noise floor            | t <sub>dBc1k</sub>   | 1kHz offset   |                        | -145  | -135                   | dBc     | 1,4   |
| Noise floor            | t <sub>dBc10k</sub>  | 10kHz offset to Nyquist   |                        | -150  | -140                   | dBc     | 1,4   |
| Jitter, phase          | t <sub>phREF</sub>   | 12kHz to 5MHz, DIF SSC Off  |                        | 0.132 | 0.3                    | ps (ms) | 1,4   |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00 MHz

<sup>3</sup> Default SMBus Value

<sup>4</sup> When driven by a crystal.

<sup>5</sup> When driven by an external oscillator via the X1 pin, X2 should be floating.

## General SMBus Serial Interface Information

### How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation |           |                      |
|-----------------------------|-----------|----------------------|
| Controller (Host)           |           | IDT (Slave/Receiver) |
| T                           | starT bit |                      |
| Slave Address               |           |                      |
| WR                          | WRite     |                      |
|                             |           | ACK                  |
| Beginning Byte = N          |           |                      |
|                             |           | ACK                  |
| Data Byte Count = X         |           |                      |
|                             |           | ACK                  |
| Beginning Byte N            |           |                      |
|                             |           | ACK                  |
| O                           |           | O                    |
| O                           |           | O                    |
| O                           |           | O                    |
| Byte N + X - 1              |           |                      |
|                             |           | ACK                  |
| P                           | stoP bit  |                      |

**Note: SMBus Address is Latched on SADR pin. Unless otherwise indicated, default values are for the xx41 and xx51. P1 devices are fully factory programmable.**

### How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation |                 |                      |
|----------------------------|-----------------|----------------------|
| Controller (Host)          |                 | IDT (Slave/Receiver) |
| T                          | starT bit       |                      |
| Slave Address              |                 |                      |
| WR                         | WRite           |                      |
|                            |                 | ACK                  |
| Beginning Byte = N         |                 |                      |
|                            |                 | ACK                  |
| RT                         | Repeat starT    |                      |
| Slave Address              |                 |                      |
| RD                         | ReaD            |                      |
|                            |                 | ACK                  |
|                            |                 | Data Byte Count=X    |
| ACK                        |                 |                      |
| ACK                        |                 | Beginning Byte N     |
|                            |                 | O                    |
| O                          |                 | O                    |
| O                          |                 | O                    |
| O                          |                 |                      |
|                            |                 | Byte N + X - 1       |
| N                          | Not acknowledge |                      |
| P                          | stoP bit        |                      |

**SMBus Table: Output Enable Register <sup>1</sup>**

| Byte 0 | Name     | Control Function | Type | 0            | 1              | Default |
|--------|----------|------------------|------|--------------|----------------|---------|
| Bit 7  | DIF OE5  | Output Enable    | RW   | See B11[1:0] | Pin controlled | 1       |
| Bit 6  | DIF OE4  | Output Enable    | RW   |              | Pin controlled | 1       |
| Bit 5  | Reserved |                  |      |              |                | X       |
| Bit 4  | DIF OE3  | Output Enable    | RW   | See B11[1:0] | Pin controlled | 1       |
| Bit 3  | DIF OE2  | Output Enable    | RW   |              | Pin controlled | 1       |
| Bit 2  | DIF OE1  | Output Enable    | RW   |              | Pin controlled | 1       |
| Bit 1  | Reserved |                  |      |              |                | X       |
| Bit 0  | DIF OE0  | Output Enable    | RW   | See B11[1:0] | Pin controlled | 1       |

1. A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

**SMBus Table: Spread Spectrum and Vhigh Control Register**

| Byte 1 | Name         | Control Function            | Type            | 0   | 1                                    | Default |
|--------|--------------|-----------------------------|-----------------|---|--------------------------------------|---------|
| Bit 7  | SSENRB1      | SS Enable Readback Bit1     | R               | 00' for SS_EN= 0,<br>'11 for SS_EN = '1'                            |                                      | Latch   |
| Bit 6  | SSENRB1      | SS Enable Readback Bit0     | R               |   |                                      | Latch   |
| Bit 5  | SSEN_SWCNTRL | Enable SW control of SS     | RW              | SS controlled by latch (B1[7:6]).                                   | Values in B1[4:3] control SS amount. | 0       |
| Bit 4  | SSENSW1      | SS Enable Software Ctl Bit1 | RW <sup>1</sup> | 00' = SS Off, '01' = -0.25% SS,<br>'10' = Reserved, '11' = -0.5% SS |                                      | 0       |
| Bit 3  | SSENSW0      | SS Enable Software Ctl Bit0 | RW <sup>1</sup> |   |                                      | 0       |
| Bit 2  | Reserved     |                             |                 |   |                                      | X       |
| Bit 1  | AMPLITUDE 1  | Controls Output Amplitude   | RW              | 00 = 0.6V   | 01 = 0.68V                           | 1       |
| Bit 0  | AMPLITUDE 0  |                             | RW              | 10 = 0.75V  | 11 = 0.85V                           | 0       |

1. Spread must be selected OFF or ON with the hardware latch pin. These bits should not be used to turn spread ON or OFF after power up. These bits can be used to change the spread amount, and B1[5] must be set to a 1 for these bits to have any effect on the part. If These bits are used to turn spread OFF or ON, the system will need to be reset.

**SMBus Table: DIF Slew Rate Control Register**

| Byte 2 | Name             | Control Function         | Type | 0            | 1            | Default |
|--------|------------------|--------------------------|------|--------------|--------------|---------|
| Bit 7  | SLEWRATESEL DIF5 | Adjust slew rate of DIF5 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 6  | SLEWRATESEL DIF4 | Adjust slew rate of DIF4 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 5  | Reserved         |                          |      |              |              | X       |
| Bit 4  | SLEWRATESEL DIF3 | Adjust slew rate of DIF3 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 3  | SLEWRATESEL DIF2 | Adjust slew rate of DIF2 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 2  | SLEWRATESEL DIF1 | Adjust slew rate of DIF1 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 1  | Reserved         |                          |      |              |              | X       |
| Bit 0  | SLEWRATESEL DIF0 | Adjust slew rate of DIF0 | RW   | Slow Setting | Fast Setting | 1       |

Note: See "Low-Power HCSL Outputs" table for slew rates.

**SMBus Table: Nominal Vhigh Amplitude Control/ REF Control Register**

| Byte 3 | Name                    | Control Function           | Type | 0                          | 1                      | Default |
|--------|-------------------------|----------------------------|------|----------------------------|------------------------|---------|
| Bit 7  | REF                     | Slew Rate Control          | RW   | 00 = Slowest               | 01 = Slow              | 0       |
| Bit 6  |                         |                            | RW   | 10 = Fast                  | 11 = Fastest           | 1       |
| Bit 5  | REF Power Down Function | Wake-on-Lan Enable for REF | RW   | REF disabled in Power Down | REF runs in Power Down | 0       |
| Bit 4  | REF OE                  | REF Output Enable          | RW   | Disabled <sup>1</sup>      | Enabled                | 1       |
| Bit 3  | Reserved                |                            |      |                            |                        | X       |
| Bit 2  | Reserved                |                            |      |                            |                        | X       |
| Bit 1  | Reserved                |                            |      |                            |                        | X       |
| Bit 0  | Reserved                |                            |      |                            |                        | X       |

1. The disabled state depends on Byte11[1:0]. '00' = Low, '01'=HiZ, '10'=Low, '11'=Hlgh

Byte 4 is Reserved

**SMBus Table: Revision and Vendor ID Register**

| Byte 5 | Name | Control Function | Type | 0            | 1 | Default |
|--------|------|------------------|------|--------------|---|---------|
| Bit 7  | RID3 | Revision ID      | R    | B rev = 0001 |   | 0       |
| Bit 6  | RID2 |                  | R    |              |   | 0       |
| Bit 5  | RID1 |                  | R    |              |   | 0       |
| Bit 4  | RID0 |                  | R    |              |   | 1       |
| Bit 3  | VID3 | VENDOR ID        | R    | 0001 = IDT   |   | 0       |
| Bit 2  | VID2 |                  | R    |              |   | 0       |
| Bit 1  | VID1 |                  | R    |              |   | 0       |
| Bit 0  | VID0 |                  | R    |              |   | 1       |

**SMBus Table: Device Type/Device ID**

| Byte 6 | Name         | Control Function | Type | 0   | 1 | Default |
|--------|--------------|------------------|------|---|---|---------|
| Bit 7  | Device Type1 | Device Type      | R    | 00 = FGx, 01 = DBx,<br>10 = DMx, 11= DBx w/oPLL |   | 0       |
| Bit 6  | Device Type0 |                  | R    |   |   | 0       |
| Bit 5  | Device ID5   | Device ID        | R    | 000110 binary or 06 hex                         |   | 0       |
| Bit 4  | Device ID4   |                  | R    |   |   | 0       |
| Bit 3  | Device ID3   |                  | R    |   |   | 0       |
| Bit 2  | Device ID2   |                  | R    |   |   | 1       |
| Bit 1  | Device ID1   |                  | R    |   |   | 1       |
| Bit 0  | Device ID0   |                  | R    |   |   | 0       |

**SMBus Table: Byte Count Register**

| Byte 7 | Name | Control Function       | Type | 0   | 1 | Default |
|--------|------|------------------------|------|---|---|---------|
| Bit 7  |      | Reserved               |      |   |   | X       |
| Bit 6  |      | Reserved               |      |   |   | X       |
| Bit 5  |      | Reserved               |      |   |   | X       |
| Bit 4  | BC4  | Byte Count Programming | RW   | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. |   | 0       |
| Bit 3  | BC3  |                        | RW   |   |   | 1       |
| Bit 2  | BC2  |                        | RW   |   |   | 0       |
| Bit 1  | BC1  |                        | RW   |   |   | 0       |
| Bit 0  | BC0  |                        | RW   |   |   | 0       |

Bytes 8 and 9 are Reserved.

**SMBus Table: PLL MN Enable, PD\_Restore**

| Byte 10 | Name                    | Control Function              | Type | 0                  | 1                 | Default |
|---------|-------------------------|-------------------------------|------|--------------------|-------------------|---------|
| Bit 7   | PLL M/N En <sup>1</sup> | M/N Programming Enable        | RW   | M/N Prog. Disabled | M/N Prog. Enabled | 0       |
| Bit 6   | Power-Down (PD) Restore | Restore Default Config. In PD | RW   | Clear Config in PD | Keep Config in PD | 1       |
| Bit 5   |                         | Reserved                      |      |                    |                   | X       |
| Bit 4   |                         | Reserved                      |      |                    |                   | X       |
| Bit 3   |                         | Reserved                      |      |                    |                   | X       |
| Bit 2   |                         | Reserved                      |      |                    |                   | X       |
| Bit 1   |                         | Reserved                      |      |                    |                   | X       |
| Bit 0   |                         | Reserved                      |      |                    |                   | X       |

1. This bit is a '1' on 9FGL0xP1 devices



**SMBus Table: Stop State Control**

| Byte 11 | Name   | Control Function                         | Type | 0            | 1             | Default |
|---------|--------|--|------|--------------|---------------|---------|
| Bit 7   |        | Reserved                                 |      |              |               | X       |
| Bit 6   |        | Reserved                                 |      |              |               | X       |
| Bit 5   |        | Reserved                                 |      |              |               | X       |
| Bit 4   |        | Reserved                                 |      |              |               | X       |
| Bit 3   |        | Reserved                                 |      |              |               | X       |
| Bit 2   |        | Reserved                                 |      |              |               | X       |
| Bit 1   | STP[1] | True/Complement DIF Output Disable State | RW   | 00 = Low/Low | 10 = High/Low | 0       |
| Bit 0   | STP[0] |  | RW   | 01 = HiZ/HiZ | 11 = Low/High | 0       |

**SMBus Table: Impedance Control**

| Byte 12 | Name        | Control Function | Type | 0               | 1                | Default  |
|---------|-------------|------------------|------|-----------------|------------------|----------|
| Bit 7   | DIF2_imp[1] | DIF2 Zout        | RW   | 00=33Ω DIF Zout | 10=100Ω DIF Zout | see Note |
| Bit 6   | DIF2_imp[0] | DIF2 Zout        | RW   | 01=85Ω DIF Zout | 11 = Reserved    |          |
| Bit 5   | DIF1_imp[1] | DIF1 Zout        | RW   | 00=33Ω DIF Zout | 10=100Ω DIF Zout |          |
| Bit 4   | DIF1_imp[0] | DIF1 Zout        | RW   | 01=85Ω DIF Zout | 11 = Reserved    |          |
| Bit 3   |             | Reserved         |      |                 |                  | X        |
| Bit 2   |             | Reserved         |      |                 |                  | X        |
| Bit 1   | DIF0_imp[1] | DIF0 Zout        | RW   | 00=33Ω DIF Zout | 10=100Ω DIF Zout | see Note |
| Bit 0   | DIF0_imp[0] | DIF0 Zout        | RW   | 01=85Ω DIF Zout | 11 = Reserved    |          |

**SMBus Table: Impedance Control**

| Byte 13 | Name        | Control Function | Type | 0               | 1                | Default  |
|---------|-------------|------------------|------|-----------------|------------------|----------|
| Bit 7   | DIF5_imp[1] | DIF5 Zout        | RW   | 00=33Ω DIF Zout | 10=100Ω DIF Zout | see Note |
| Bit 6   | DIF5_imp[0] | DIF5 Zout        | RW   | 01=85Ω DIF Zout | 11 = Reserved    |          |
| Bit 5   | DIF4_imp[1] | DIF4 Zout        | RW   | 00=33Ω DIF Zout | 10=100Ω DIF Zout |          |
| Bit 4   | DIF4_imp[0] | DIF6 Zout        | RW   | 01=85Ω DIF Zout | 11 = Reserved    |          |
| Bit 3   |             | Reserved         |      |                 |                  | X        |
| Bit 2   |             | Reserved         |      |                 |                  | X        |
| Bit 1   | DIF3_imp[1] | DIF3 Zout        | RW   | 00=33Ω DIF Zout | 10=100Ω DIF Zout | see Note |
| Bit 0   | DIF3_imp[0] | DIF3 Zout        | RW   | 01=85Ω DIF Zout | 11 = Reserved    |          |

**SMBus Table: Pull-up Pull-down Control**

| Byte 14 | Name         | Control Function                          | Type | 0       | 1             | Default |
|---------|--------------|---|------|---------|---------------|---------|
| Bit 7   | OE2_pu/pd[1] | OE2 Pull-up(PuP)/ Pull-down(Pdwn) control | RW   | 00=None | 10=Pup        | 0       |
| Bit 6   | OE2_pu/pd[0] |   | RW   | 01=Pdwn | 11 = Pup+Pdwn | 1       |
| Bit 5   | OE1_pu/pd[1] | OE1 Pull-up(PuP)/ Pull-down(Pdwn) control | RW   | 00=None | 10=Pup        | 0       |
| Bit 4   | OE1_pu/pd[0] |   | RW   | 01=Pdwn | 11 = Pup+Pdwn | 1       |
| Bit 3   |              | Reserved                                  |      |         |               | X       |
| Bit 2   |              | Reserved                                  |      |         |               | X       |
| Bit 1   | OE0_pu/pd[1] | OE0 Pull-up(PuP)/ Pull-down(Pdwn) control | RW   | 00=None | 10=Pup        | 0       |
| Bit 0   | OE0_pu/pd[0] |   | RW   | 01=Pdwn | 11 = Pup+Pdwn | 1       |

**SMBus Table: Pull-up Pull-down Control**

| Byte 15 | Name         | Control Function                             | Type | 0       | 1             | Default |
|---------|--------------|--|------|---------|---------------|---------|
| Bit 7   | OE5_pu/pd[1] | OE5 Pull-up(PuP)/<br>Pull-down(Pdwn) control | RW   | 00=None | 10=Pup        | 0       |
| Bit 6   | OE5_pu/pd[0] |  | RW   | 01=Pdwn | 11 = Pup+Pdwn | 1       |
| Bit 5   | OE4_pu/pd[1] | OE4 Pull-up(PuP)/<br>Pull-down(Pdwn) control | RW   | 00=None | 10=Pup        | 0       |
| Bit 4   | OE4_pu/pd[0] |  | RW   | 01=Pdwn | 11 = Pup+Pdwn | 1       |
| Bit 3   | Reserved     |  |      |         |               | X       |
| Bit 2   | Reserved     |  |      |         |               | X       |
| Bit 1   | OE3_pu/pd[1] | OE3 Pull-up(PuP)/<br>Pull-down(Pdwn) control | RW   | 00=None | 10=Pup        | 0       |
| Bit 0   | OE3_pu/pd[0] |  | RW   | 01=Pdwn | 11 = Pup+Pdwn | 1       |

**SMBus Table: Pull-up Pull-down Control**

| Byte 16 | Name                | Control Function                                    | Type | 0       | 1             | Default |
|---------|---------------------|---|------|---------|---------------|---------|
| Bit 7   | Reserved            |   |      |         |               | X       |
| Bit 6   | Reserved            |   |      |         |               | X       |
| Bit 5   | Reserved            |   |      |         |               | X       |
| Bit 4   | Reserved            |   |      |         |               | X       |
| Bit 3   | Reserved            |   |      |         |               | X       |
| Bit 2   | Reserved            |   |      |         |               | X       |
| Bit 1   | CKPWRGD_PD_pu/pd[1] | CKPWRGD_PD Pull-up(PuP)/<br>Pull-down(Pdwn) control | RW   | 00=None | 10=Pup        | 1       |
| Bit 0   | CKPWRGD_PD_pu/pd[0] |   | RW   | 01=Pdwn | 11 = Pup+Pdwn | 0       |

Bytes 17 is Reserved

**SMBus Table: Polarity Control**

| Byte 18 | Name         | Control Function  | Type | 0                | 1                 | Default |
|---------|--------------|-------------------|------|------------------|-------------------|---------|
| Bit 7   | OE5_polarity | Sets OE5 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 6   | OE4_polarity | Sets OE4 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 5   | Reserved     |                   |      |                  |                   | X       |
| Bit 4   | OE3_polarity | Sets OE3 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 3   | OE2_polarity | Sets OE2 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 2   | OE1_polarity | Sets OE1 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 1   | Reserved     |                   |      |                  |                   | X       |
| Bit 0   | OE0_polarity | Sets OE0 polarity | RW   | Enabled when Low | Enabled when High | 0       |

**SMBus Table: Polarity Control**

| Byte 19 | Name       | Control Function                  | Type | 0                      | 1                       | Default |
|---------|------------|-----------------------------------|------|------------------------|-------------------------|---------|
| Bit 7   | Reserved   |                                   |      |                        |                         | X       |
| Bit 6   | Reserved   |                                   |      |                        |                         | X       |
| Bit 5   | Reserved   |                                   |      |                        |                         | X       |
| Bit 4   | Reserved   |                                   |      |                        |                         | X       |
| Bit 3   | Reserved   |                                   |      |                        |                         | X       |
| Bit 2   | Reserved   |                                   |      |                        |                         | X       |
| Bit 1   | Reserved   |                                   |      |                        |                         | X       |
| Bit 0   | CKPWRGD_PD | Determines<br>CKPWRGD_PD polarity | RW   | Power Down when<br>Low | Power Down when<br>High | 0       |

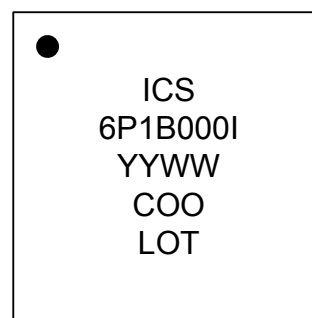
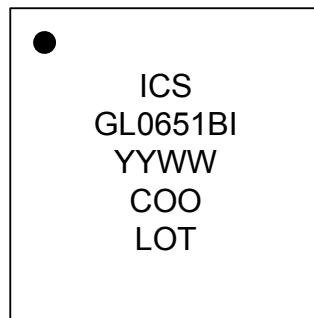
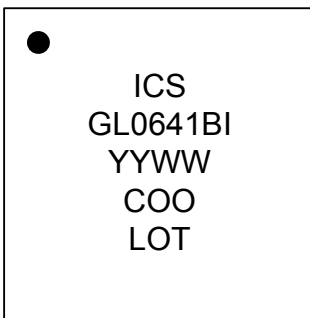
## Recommended Crystal Characteristics (3225 package)

| PARAMETER  | VALUE       | UNITS   | NOTES |
|--|-------------|---------|-------|
| Frequency  | 25          | MHz     | 1     |
| Resonance Mode   | Fundamental | -       | 1     |
| Frequency Tolerance @ 25°C                                       | ±20         | PPM Max | 1     |
| Frequency Stability, ref @ 25°C Over Operating Temperature Range | ±20         | PPM Max | 1     |
| Temperature Range (commercial)                                   | 0~70        | °C      | 1     |
| Temperature Range (industrial)                                   | -40~85      | °C      | 1     |
| Equivalent Series Resistance (ESR)                               | 50          | Ω Max   | 1     |
| Shunt Capacitance (C <sub>0</sub> )                              | 7           | pF Max  | 1     |
| Load Capacitance (C <sub>L</sub> )                               | 8           | pF Max  | 1     |
| Drive Level  | 0.3         | mW Max  | 1     |
| Aging per year   | ±5          | PPM Max | 1     |

### Notes:

1. FOX 603-25-150JA4C

## Marking Diagrams



### Notes:

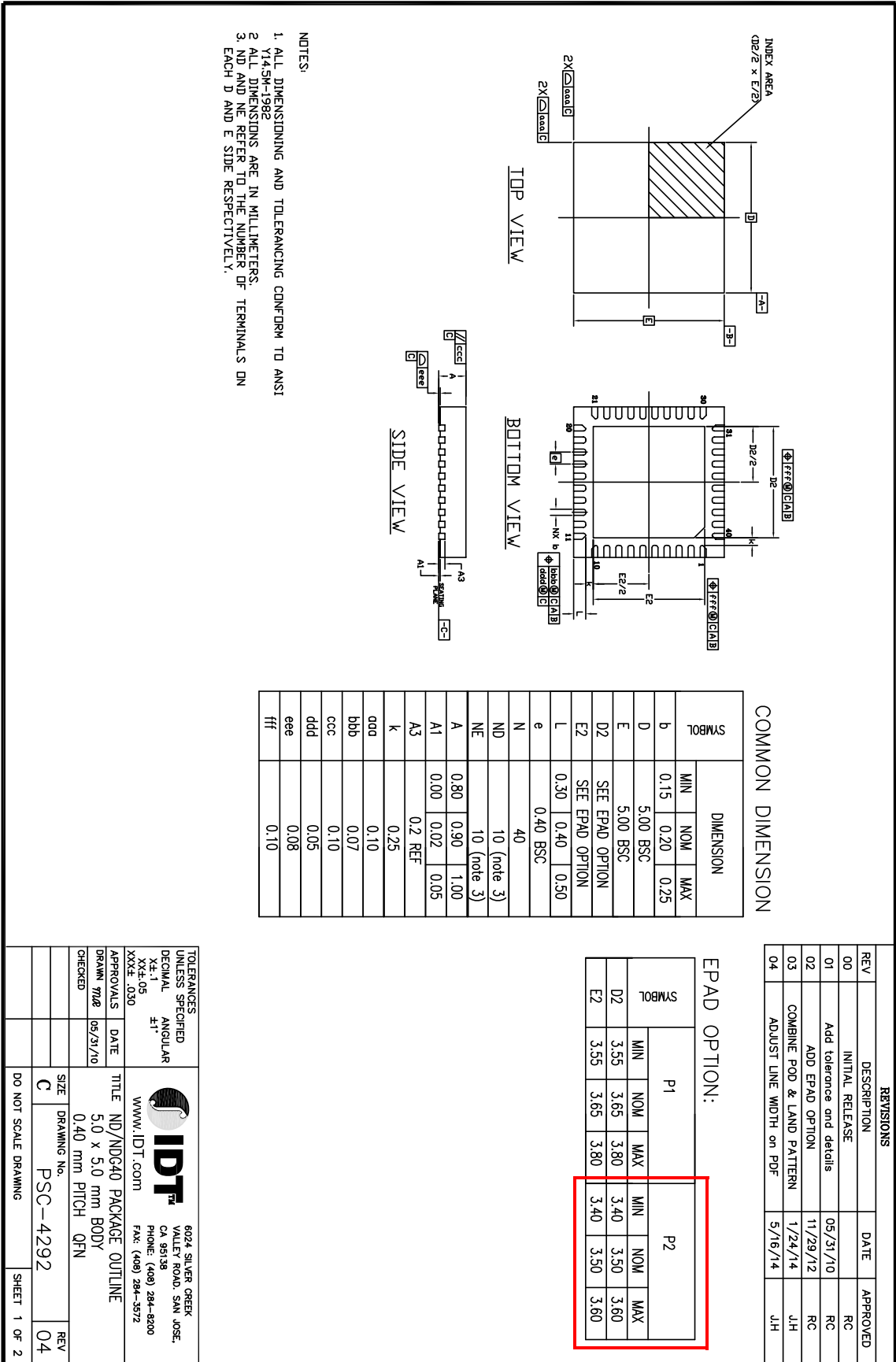
1. "LOT" is the lot sequence number.
2. "COO" denotes country of origin.
3. "YYWW" is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. "L" denotes RoHS compliant package.
6. "I" denotes industrial temperature range device.
7. "P" denotes factory programmable defaults

## Thermal Characteristics

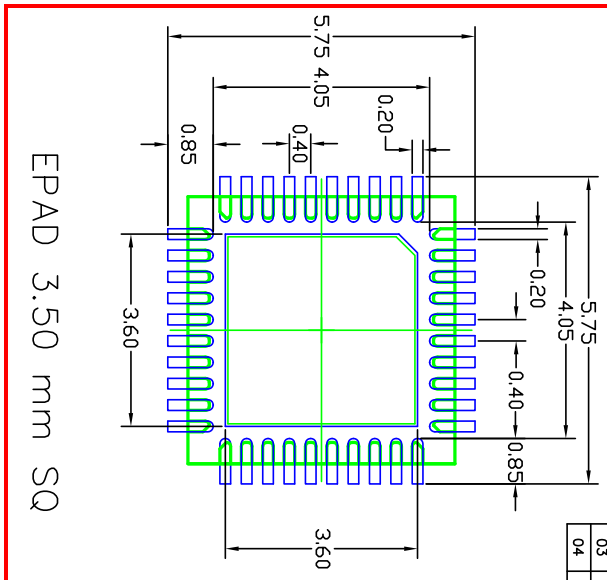
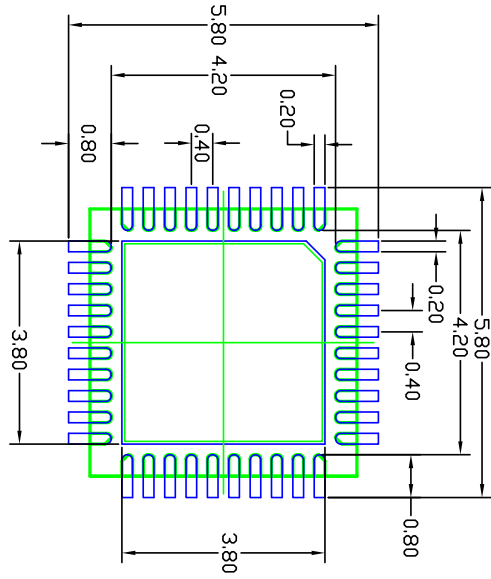
| PARAMETER          | SYMBOL         | CONDITIONS                      | PKG   | TYP. | UNITS | NOTES |
|--------------------|----------------|---------------------------------|-------|------|-------|-------|
| Thermal Resistance | $\theta_{JC}$  | Junction to Case                | NDG40 | 42   | °C/W  | 1     |
|                    | $\theta_{Jb}$  | Junction to Base                |       | 2.4  | °C/W  | 1     |
|                    | $\theta_{JA0}$ | Junction to Air, still air      |       | 39   | °C/W  | 1     |
|                    | $\theta_{JA1}$ | Junction to Air, 1 m/s air flow |       | 33   | °C/W  | 1     |
|                    | $\theta_{JA3}$ | Junction to Air, 3 m/s air flow |       | 28   | °C/W  | 1     |
|                    | $\theta_{JA5}$ | Junction to Air, 5 m/s air flow |       | 27   | °C/W  | 1     |

<sup>1</sup>ePad soldered to board

# Package Outline and Package Dimensions (NDG40) – use EPAD Option P2



Package Outline and Package Dimensions (NDG40) – use EPAD 3.50 mm SQ



- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
  2. TOP DOWN VIEW AS VIEWED ON PCB.
  3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
  4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
  5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| REVISIONS |                            |          |          |
|-----------|----------------------------|----------|----------|
| REV       | DESCRIPTION                | DATE     | APPROVED |
| 00        | INITIAL RELEASE            |          | RC       |
| 01        | Add tolerance and details  | 05/31/10 | RC       |
| 02        | ADD EPAD OPTION            | 11/29/12 | RC       |
| 03        | COMBINE POD & LAND PATTERN | 1/24/14  | JJH      |
| 04        | ADJUST LINE WIDTH on PDF   | 5/16/14  | JJH      |

|                             |             |  |              |
|-----------------------------|-------------|--|--------------|
| TOLERANCES UNLESS SPECIFIED |             | 6024 SILVER CREEK VALLEY ROAD SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572 |              |
| DECIMAL                     | ANGULAR     |  |              |
| XX.X .1                     | ±1°         |  |              |
| XXX.X .030                  |             | WWW.IDT.COM  |              |
| APPROVALS                   | DATE        | TITLE ND/NDG40 PACKAGE OUTLINE   |              |
| DRAWN 7/02                  | 05/31/10    | 5.0 x 5.0 mm BODY  |              |
| CHECKED                     |             | 0.40 mm PITCH QFN  |              |
| SIZE                        | DRAWING No. | REV  |              |
| C                           | PSC-4292    | 04   |              |
| DO NOT SCALE DRAWING        |             |  | SHEET 2 OF 2 |



## Ordering Information

| Part / Order Number | Notes   | Shipping Packaging | Package       | Temperature   |
|---------------------|---|--------------------|---------------|---------------|
| 9FGL0641BKILF       | 100Ω  | Trays              | 40-pin VFQFPN | -40 to +85° C |
| 9FGL0641BKILFT      |   | Tape and Reel      | 40-pin VFQFPN | -40 to +85° C |
| 9FGL0651BKILF       | 85Ω   | Trays              | 40-pin VFQFPN | -40 to +85° C |
| 9FGL0651BKILFT      |   | Tape and Reel      | 40-pin VFQFPN | -40 to +85° C |
| 9FGL06P1BxxxKILF    | Factory configurable.<br>Contact IDT for<br>additional information. | Trays              | 40-pin VFQFPN | -40 to +85° C |
| 9FGL06P1BxxxKILFT   |   | Tape and Reel      | 40-pin VFQFPN | -40 to +85° C |

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“B” is the device revision designator (will not correlate with the datasheet revision).

“xxx” is a unique factory assigned number to identify a particular default configuration.

## Revision History

| Rev. | Issue Date | Initiator | Description   | Page #  |
|------|------------|-----------|---|---------|
| E    | 6/3/2016   | RDW       | <ol style="list-style-type: none"> <li>1. Update electrical tables for B rev production release</li> <li>2. Added PCIe SRIS and PCIe Gen4 CC to phase jitter tables.</li> <li>3. Updated front page text.</li> <li>4. Removed '000' blank device from ordering information.</li> <li>5. Updated Byte0 wording for clarity</li> <li>6. Updated Byte1[1:0] descriptions.</li> </ol> | Various |
| F    | 6/22/2016  | RDW       | <ol style="list-style-type: none"> <li>1. Updated electrical labels with final data from PE/TE</li> <li>2. Minor cleanup of the SMBus descriptions.</li> <li>3. Release</li> </ol>  | Various |
| G    | 9/2/2016   | RDW       | 1. Corrected Byte 2 to properly indicate slew rate control bits   | 11      |
| H    | 10/19/2016 | RDW       | Removed IDT crystal part number   | 15      |
| J    | 12/1/2016  | RDW       | 1. Updated Byte 1 and its footnote for clarity.   | 11      |



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