Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

HiRel FPGAs

Features

- Highly Predictable Performance with 100% Automatic Placement and Routing
- Device Sizes from 1,200 to 20,000 Gates
- Up to 6 Fast, Low-Skew Clock Networks
- Up to 202 User-Programmable I/O Pins
- More Than 500 Macro Functions
- Up to 1,276 Dedicated Flip-Flops
- I/O Drive to 10 mA
- Devices Available to DSCC SMD
- CQFP and CPGA Packaging
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment
- 100% Military Temperature Tested (–55°C to +125°C)
- QML Certified Devices
- Proven Reliability Data Available
- Successful Military/Avionics Supplier for Over 10 Years

ACT 3 Features

- Highest-Performance, Highest-Capacity FPGA Family
- System Performance to 60 MHz over Military Temperature
- Low-Power 0.8µ CMOS Technology

3200DX Features

- 100 MHz System Logic Integration
- Highest Speed FPGA SRAM, up to 2.5 kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Low-Power 0.6µ CMOS Technology

1200XL Features

- Pin for Pin Compatible with ACT 2
- System Performance to 50 MHz over Military Temperature
- Low-Power 0.6µ CMOS Technology

ACT 2 Features

- Best-Value, High-Capacity FPGA Family
- System Performance to 40 MHz over Military Temperature
- Low-Power 1.0µ CMOS Technology

ACT 1 Features

- Lowest-Cost FPGA Family
- System Performance to 20 MHz over Military Temperature
- Low-Power 1.0µ CMOS Technology

Product Family Profile (more devices on page 2)

Family	3200DX		ACT 3			1200XL
Device	A32100DX	A32200DX	A1425A	A1460A	A14100A	A1280XL
Capacity						
System Gates	15,000	30,000	3,750	9,000	15,000	12,000
Logic Gates	10,000	20,000	2,500	6,000	10,000	8,000
SRAM Bits	2,048	2,560	NA	NA	NA	
Logic Modules	1,362	2,414	310	848	1,377	1,232
S-Modules	700	1,230	160	432	697	624
C-Modules	662	1,184	150	416	680	608
Decode	20	24	NA	NA	NA	NA
Flip-Flops (Maximum)	738	1,276	435	976	1,493	998
User I/Os (Maximum)	152	202	100	168	228	140
Performance						
System Speed (maximum)	55 MHz	55 MHz	60 MHz	60 MHz	60 MHz	50 MHz
Packages (by Pin Count)						
CPGA			133	207	257	176
CQFP	84	208, 256	132	196	256	172

Product Family Profile

Family / Device	ACT 2 A1240A	ACT 2 A1280A	ACT 1 A1010B	ACT 1 A1020B
Capacity				
System Gates	6,000	12,000	1,800	3,000
Logic Gates	4,000	8,000	1,200	2,000
SRAM Bits	NA	NA	NA	NA
Logic Modules	684	1,232	295	547
S-Modules	348	624	—	—
C-Modules	336	608	295	547
Decode	NA	NA	NA	NA
Flip-Flops (maximum)	568	998	147	273
User I/Os (maximum)	104	140	57	69
Packages (by pin count)				
CPGA	132	176	84	84
CQFP	—	172	—	84
Performance				
System Speed (maximum)	40 MHz	40 MHz	20 MHz	20 MHz

High-Reliability, Low-Risk Solution

Actel builds the most reliable field programmable gate arrays (FPGAs) in the industry, with overall antifuse reliability ratings of less than 10 Failures-In-Time (FITs), corresponding to a useful life of more than 40 years. Actel FPGAs have been production proven, with more than five million devices shipped and more than one trillion antifuses manufactured. Actel devices are fully tested prior to shipment, with an outgoing defect level of less than 100 ppm. (Further reliability data is available in the *Actel Device Reliability Report*, at http://www.actel.com/hirel).

Benefits

Minimized Cost Risk

With Actel's line of development tools, designers can produce as many chips as they choose for just the cost of the device itself. There will be no NRE charges to cut into the development budget each time a new design is tried.

Minimized Time Risk

After the design is entered, placement and routing is automatic, and programming the device takes only about 5 to 15 minutes for an average design. Designers save time in the design entry process by using tools with which they are familiar.

Minimized Reliability Risk

The PLICE antifuse is a one-time programmable, nonvolatile connection. Since Actel devices are permanently programmed, no downloading from EPROM or SRAM storage is required. Inadvertent erasure is impossible, and there is no need to reload the program after power disruptions. Fabrication using a low-power CMOS process means cooler junction temperatures. Actel's non-PLD architecture delivers lower dynamic operating current. Our reliability tests show a very low failure rate of 6.6 FITs at 90°C junction temperature with no degradation in AC performance. Special stress testing at wafer test eliminates infant mortalities prior to packaging.

Minimized Security Risk

Reverse engineering of programmed Actel devices from optical or electrical data is extremely difficult. Programmed antifuses cannot be identified from a photograph or by using an SEM. The antifuse map cannot be deciphered either electrically or by microprobing. Each device has a silicon signature that identifies its origins, down to the wafer lot and fabrication facility.

Minimized Testing Risk

Unprogrammed Actel parts are extensively tested at the factory. Routing tracks, logic modules, and programming, debug and test circuits are 100 percent tested before shipment. AC performance is ensured by special speed path tests, and programming circuitry is verified on test antifuses. During the programming process, an algorithm is run to ensure that all antifuses are correctly programmed. In addition, Actel's Silicon Explorer diagnostic tool uses ActionProbe circuitry, allowing 100 percent observability of all internal nodes to check and debug the design.

Actel FPGA Description

The Actel families of FPGAs offer a variety of packages, speed/performance characteristics, and processing levels for use in all high reliability and military applications. Devices are implemented in a silicon gate, two-level metal CMOS process, utilizing Actel's PLICE antifuse technology. This

unique architecture offers gate array flexibility, high performance, and quick turnaround through user programming. Device utilization is typically 95 percent of available logic modules. All Actel devices include on-chip clock drivers and a hard-wired distribution network.

User-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages for the military are the Ceramic Quad Flat Pack (CQFP) and the Ceramic Pin Grid Array (CPGA). See the "Product Plan" section on page 6 for details.

QML Certification

Actel has achieved full QML certification, demonstrating that quality management, procedures, processes, and controls are in place and comply with MIL-PRF-38535, the performance specification used by the Department of Defense for monolithic integrated circuits. QML certification is a good example of Actel's commitment to supplying the highest quality products for all types of high-reliability, military and space applications.

Many suppliers of microelectronics components have implemented QML as their primary worldwide business system. Appropriate use of this system not only helps in the implementation of advanced technologies, but also allows for a quality, reliable and cost-effective logistics support throughout QML products' life cycles.

Development Tool Support

The HiRel devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP series and Designer Advantage tools. The Actel DeskTOP Series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place and route tools. Designer Advantage is Actel's suite of FPGA development point tools for PCs and Workstations that includes the ACTgen Macro Builder, Designer with DirectTime timing driven place and route and analysis tools, and device programming software.

In addition, the HiRel devices contain ActionProbe circuitry that provides built-in access to every node in a design, enabling 100 percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer, an easy to use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer attaches to a PC's standard COM port, turning the PC into a fully functional 18 channel logic analyzer. Silicon Explorer allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

ACT 3 Description

The ACT 3 family is the third-generation Actel FPGA family. This family offers the highest-performance and highest-capacity devices, ranging from 2,500 to 10,000 gates, with system performance up to 60 MHz over the military temperature range. The devices have four clock distribution networks, including dedicated array and I/O clocks. In addition, the ACT 3 family offers the highest I/O-to-gate ratio available. ACT 3 devices are manufactured using 0.8µ CMOS technology.

1200XL/3200DX Description

3200DX and 1200XL FPGAs were designed to integrate system logic which is typically implemented in multiple CPLDs, PALs, and FPGAs. These devices provide the features and performance required for today's complex, high-speed digital logic systems. The 3200DX family offers the industry's fastest dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage.

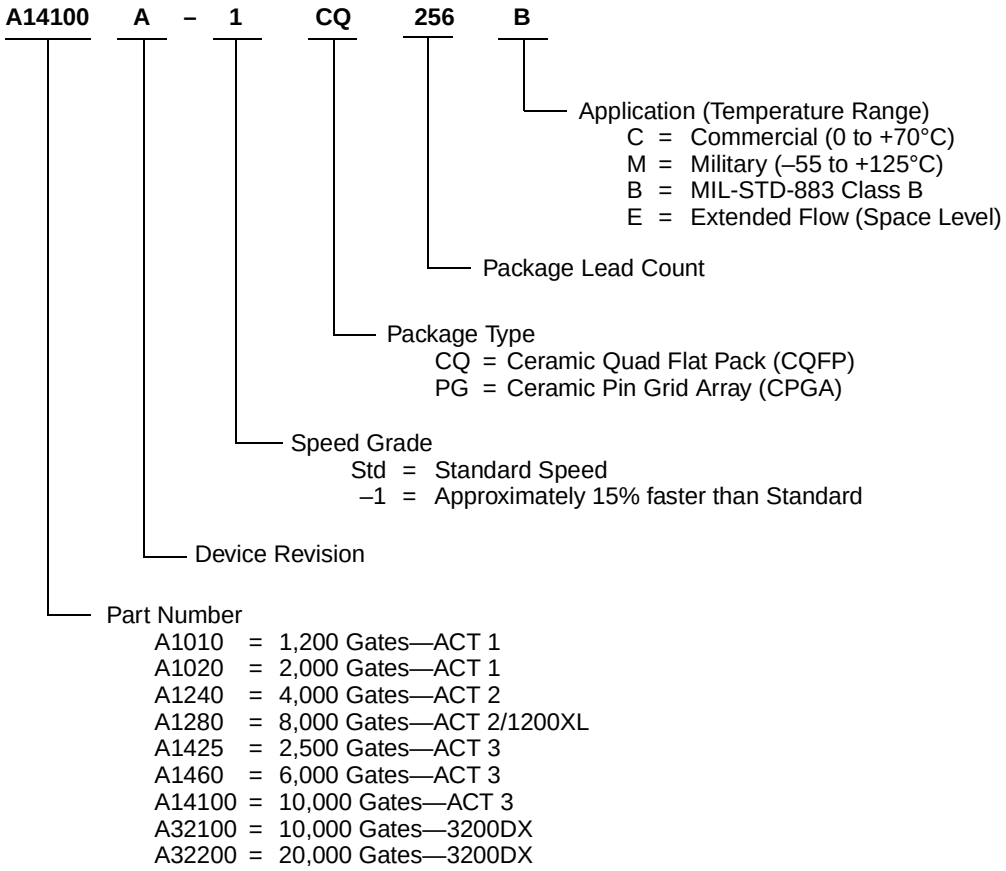
ACT 2 Description

The ACT 2 family is the second-generation Actel FPGA family. This family offers the best-value, high-capacity devices, ranging from 4,000 to 8,000 gates, with system performance up to 40 MHz over the military temperature range. The devices have two routed array clock distribution networks. ACT 2 devices are manufactured using 1.0µ CMOS technology.

ACT 1 Description

The ACT 1 family is the first Actel FPGA family and the first antifuse-based FPGA. This family offers the lowest-cost logic integration, with devices ranging from 1,200 to 2,000 gates, with system performance up to 20 MHz over the military temperature range. The devices have one routed array clock distribution network. ACT 1 devices are manufactured using 1.0µ CMOS technology.

Military Device Ordering Information



DESC SMD/Actel Part Number Cross Reference

Actel Part Number (Gold Leads)	DSCC SMD (Gold Leads)	DSCC SMD (Solder Dipped)
A1010B-PG84B	5962-9096403MXC	5962-9096403MXA
A1010B-1PG84B	5962-9096404MXC	5962-9096404MXA
A1020B-PG84B	5962-9096503MUC	5962-9096503MUA
A1020B-1PG84B	5962-9096504MUC	5962-9096504MUA
A1020B-CQ84B	5962-9096503MTC	5962-9096503MTA
A1020B-1CQ84B	5962-9096504MTC	5962-9096504MTA
A1240A-PG132B	5962-9322101MXC	5962-9322101MXA
A1240A-1PG132B	5962-9322102MXC	5962-9322102MXA
A1280A-PG176B	5962-9215601MXC	5962-9215601MXA
A1280A-1PG176B	5962-9215602MXC	5962-9215602MXA
A1280A-CQ172B	5962-9215601MYC	5962-9215601MYA
A1280A-1CQ172B	5962-9215602MYC	5962-9215602MYA
A1425A-PG133B	5962-9552001MXC	N/A
A1425A-1PG133B	5962-9552002MXC	N/A
A1425A-CQ132B	5962-9552001MYC	N/A
A1425A-1CQ132B	5962-9552002MYC	N/A
A1460A-PG207B	5962-9550801MXC	N/A
A1460A-1PG207B	5962-9550802MXC	N/A
A1460A-CQ196B	5962-9550801MYC	N/A
A1460A-1CQ196B	5962-9550802MYC	N/A
A14100A-PG257B	5962-9552101MXC	N/A
A14100A-1PG257B	5962-9552102MXC	N/A
A14100A-CQ256B	5962-9552101MYC	N/A
A14100A-1CQ256B	5962-9552102MYC	N/A
A32100DX-CQ84B	5962-9875901QXC	N/A
A32100DX-1CQ84B	5962-9857902QXC	N/A
A32200DX-CQ256B	5962-9952701QXC	N/A
A32200DX-1CQ256B	5962-9952702QXC	N/A
A32200DX-CQ208B	5962-9952701QYC	N/A
A32200DX-1CQ208B	5962-9952702QYC	N/A

Product Plan

	Speed Grade		Application			
3200DX Family	**Std**	**–1***	**C**	**M**	**B**	**E**
A32100DX Device						
84-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
A32200DX Device						
208-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
256-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
ACT 3 Family						
A1425A Device						
132-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
133-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
A1460A Device						
196-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
207-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
A14100A Device						
256-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
257-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
1200XL Family						
A1280XL Device						
172-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	—
176-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—
ACT 2 Family						
A1240A Device						
132-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—
A1280A Device						
172-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
176-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔
ACT 1 Family						
A1010B Device						
84-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—
A1020B Device						
84-pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	✔	✔	✔
84-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	✔

Applications: *C = Commercial* *M = Military* *B = MIL-STD-883* *E = Extended Flow*

Availability: ✔ = *Available* — = *Not Planned*

**Speed Grade:* *–1 = Approx. 15% faster than Standard*

3200DX Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os		
			CQFP		
			84-pin	208-pin	256-pin
A32100DX	1,362	10,000	60	—	—
A32200DX	2,414	20,000	—	176	202

ACT 3 Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os					
			CQFP			CPGA		
			132-pin	196-pin	256-pin	133-pin	207-pin	257-pin
A1425A	310	2,500	100	—	—	100	—	—
A1460A	848	6,000	—	168	—	—	168	—
A14100A	1,377	10,000	—	—	228	—	—	228

1200XL Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os	
			CQFP	CPGA
			172-pin	176-pin
A1280XL	1,232	8,000	140	140

ACT 2 Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os		
			CQFP	CPGA	
			172-pin	132-pin	176-pin
A1240A	684	4,000	—	104	—
A1280A	1,232	8,000	140	—	140

ACT 1 Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os	
			CQFP	CPGA
			84-pin	84-pin
A1010B	295	1,200	—	57
A1020B	547	2,000	69	69

Actel MIL-STD-883 Product Flow

Step	Screen	883 Method	883—Class B Requirement
1.	Internal Visual	2010, Test Condition B	100%
2.	Temperature Cycling	1010, Test Condition C	100%
3.	Constant Acceleration	2001, Test Condition D or E, Y_1, Orientation Only	100%
4.	Seal a. Fine b. Gross	1014	 100% 100%
5.	Visual Inspection	2009	100%
6.	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
7.	Burn-in Test	1015, Condition D, 160 hours @ 125°C or 80 hours @ 150°C	100%
8.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
9.	Percent Defective Allowable	5%	All Lots
10.	Final Electrical Test	In accordance with applicable Actel device specification, which includes a, b, and c:	
	a. Static Tests (1) 25°C (Subgroup 1, Table I) (2) –55°C and +125°C (Subgroups 2, 3, Table I)	 5005 5005	100%
	b. Functional Tests (1) 25°C (Subgroup 7, Table I) (2) –55°C and +125°C (Subgroups 8A and 8B, Table I)	 5005 5005	100%
	c. Switching Tests at 25°C (Subgroup 9, Table I)	 5005	100%
11.	External Visual	2009	100%

Note: *When Destructive Physical Analysis (DPA) is performed on Class B devices, the step coverage requirement as specified in Method 2018 must be waived.*

Actel Extended Flow[1]

Step	Screen	Method	Require-ment
1.	Wafer Lot Acceptance[2]	5007 with Step Coverage Waiver	All Lots
2.	Destructive In-Line Bond Pull[3]	2011, Condition D	Sample
3.	Internal Visual	2010, Condition A	100%
4.	Serialization		100%
5.	Temperature Cycling	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition D or E, Y_1 Orientation Only	100%
7.	Particle Impact Noise Detection	2020, Condition A	100%
8.	Radiographic	2012 (one view only)	100%
9.	Pre-Burn-In Test	In accordance with applicable Actel device specification	100%
10.	Burn-in Test	1015, Condition D, 240 hours @ 125°C minimum	100%
11.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
12.	Reverse Bias Burn-In	1015, Condition C, 72 hours @ 150°C minimum	100%
13.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
14.	Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters @ 25°C	All Lots
15.	Final Electrical Test	In accordance with Actel applicable device specification which includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table1)	5005	
	(2) –55°C and +125°C (Subgroups 2, 3, Table 1)	5005	
	b. Functional Tests		100%
	(1) 25°C (Subgroup 7, Table 15)	5005	
	(2) –55°C and +125°C (Subgroups 8A and B, Table 1)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table 1)	5005	100%
16.	Seal	1014	100%
	a. Fine		
	b. Gross		
17.	External Visual	2009	100%

Notes:

1. *Actel offers the extended flow for customers who require additional screening beyond the requirements of the MIL-STD-833, Class B. Actel is compliant to the requirements of MIL-STD-883, Paragraph 1.2.1, and MIL-I-38535, Appendix A. Actel is offering this extended flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S. The exceptions to Method 5004 are shown in notes 2 and 3 below.*
2. *Wafer lot acceptance is performed to Method 5007; however, the step coverage requirement as specified in Method 2018 must be waived.*
3. *MIL-STD-883, Method 5004 requires 100 percent Radiation latch-up testing (Method 1020). Actel will not be performing any radiation testing, and this requirement must be waived in its entirety.*

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2, 3, 4]	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[5]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.*
2. *$V_{PP} = V_{CC}$, except during device programming.*
3. *$V_{SV} = V_{CC}$, except during device programming.*
4. *$V_{KS} = GND$, except during device programming.*
5. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diode will be forward biased and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Military	Units
Temperature Range[1]	0 to +70	–55 to +125	°C
Power Supply Tolerance[2]	±5	±10	%V_{CC}

Notes:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*
2. *All power supplies must be in the recommended operating range. For more information, refer to the* Power-Up Design Considerations *application note at http://www.actel.com/appnotes.*

Electrical Specifications

Symbol	Parameter	Test Condition	Commercial		Military		Units
			Min.	Max.	Min.	Max.	
V_{OH}[1, 2]	HIGH Level Output	I_{OH} = –4 mA (CMOS)			3.7		V
		I_{OH} = –6 mA (CMOS)	3.84				V
V_{OL}[1, 2]	LOW Level Output	I_{OL} = +6 mA (CMOS)		0.33		0.4	V
V_{IH}	HIGH Level Input	TTL Inputs	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	LOW Level Input	TTL Inputs	–0.3	0.8	–0.3	0.8	V
I_{IN}	Input Leakage	$V_I = V_{CC}$ or GND	–10	+10	–10	+10	µA
I_{OZ}	3-state Output Leakage	$V_O = V_{CC}$ or GND	–10	+10	–10	+10	µA
C_{IO}	I/O Capacitance[3, 4]			10		10	pF
$I_{CC(S)}$	Standby V_{CC} Supply Current	$V_I = V_{CC}$ or GND, I_O = 0 mA					
		ACT 1		3		20	mA
		ACT 2/3/1200XL/3200DX		2		20	mA
$I_{CC(D)}$	Dynamic V_{CC} Supply Current	See the "Power Dissipation" section on page 11.					

Notes:

1. *Actel devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.*
2. *Tested one output at a time, V_{CC} = min.*
3. *Not tested; for information only.*
4. *V_{OUT} = 0V, f = 1 MHz*

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 176-pin package at military temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp.}}{\theta_{ja}\ (°C/W)} = \frac{150°C - 125°C}{23°C/W} = 1.1\ W$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Ceramic Pin Grid Array	84	6.0	33	20	°C/W
	132	4.8	25	16	°C/W
	133	4.8	25	15	°C/W
	176	4.6	23	12	°C/W
	207	3.5	21	10	°C/W
	257	2.8	15	8	°C/W
Ceramic Quad Flat Pack	84	7.8	40	30	°C/W
	132	7.2	35	25	°C/W
	172	6.8	25	20	°C/W
	196	6.4	23	15	°C/W
	256	6.2	20	10	°C/W

Power Dissipation

General Power Equation

$$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

where:

$I_{CC}standby$ is the current flowing when no inputs or outputs are changing.

$I_{CC}active$ is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

Accurate values for N and M are difficult to determine because they depend on the family type, on the design, and on the system I/O. The power can be divided into two components—static and active.

Static Power Component

Actel FPGAs have small static power components that result in power dissipation lower than that of PALs or PLDs. By integrating multiple PALs or PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst-case conditions.

Family	I_{CC}	V_{CC}	Power
ACT 3	2 mA	5.25V	10.5 mW
1200XL/3200DX	2 mA	5.25V	10.5 mW
ACT 2	2 mA	5.25V	10.5 mW
ACT 1	3 mA	5.25V	15.8 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totempole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that

can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1:

$$\text{Power (uW)} = C_{EQ} * V_{CC}^2 * F \quad (1)$$

where:

C_{EQ} = Equivalent capacitance in pF

V_{CC} = Power supply in volts (V)

F = Switching frequency in MHz

Equivalent capacitance is calculated by measuring I_{CC} active at a specified frequency and voltage for each circuit component of interest. Measurements are made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency independent so that the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

CEQ Values for Actel FPGAs

	ACT 3	1200XL 3200DX	ACT 2	ACT 1
Modules (C_{EQM})	6.7	5.2	5.8	3.7
Input Buffers (C_{EQI})	7.2	11.6	12.9	22.1
Output Buffers (C_{EQO})	10.4	23.8	23.8	31.2
Routed Array Clock Buffer Loads (C_{EQCR})	1.6	3.5	3.9	4.6
Dedicated Clock Buffer Loads (C_{EQCD})	0.7	N/A	N/A	N/A
I/O Clock Buffer Loads (C_{EQCI})	0.9	N/A	N/A	N/A

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piecewise linear summation over all components that applies to all ACT 1, 1200XL, 3200DX, ACT 2, and ACT 3 devices. Since the ACT 1 family has only one routed array clock, the terms labeled routed_Clk2, dedicated_Clk, and IO_Clk do not apply. Similarly, the ACT 2 family has two routed array clocks, and the dedicated_Clk and IO_Clk terms do not apply. For ACT 3 devices, all terms will apply.

$$\text{Power} = V_{CC}^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk} + (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}] \quad (2)$$

where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q_1 = Number of clock loads on the first routed array clock (all families)

q_2 = Number of clock loads on the second routed array clock (ACT 2, 1200XL, 3200DX, ACT 3 only)

r_1 = Fixed capacitance due to first routed array clock (all families)

r_2 = Fixed capacitance due to second routed array clock (ACT 2, 1200XL, 3200DX, ACT 3 only)

s_1 = Fixed number of clock loads on the dedicated array clock (ACT 3 only)

s_2 = Fixed number of clock loads on the dedicated I/O clock (ACT 3 only)

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_{EQCD} = Equivalent capacitance of dedicated array clock in pF

C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz (all families)

f_{q2} = Average second routed array clock rate in MHz (ACT 2, 1200XL, 3200DX, ACT 3 only)

f_{s1} = Average dedicated array clock rate in MHz (ACT 3 only)

f_{s2} = Average dedicated I/O clock rate in MHz (ACT 3 only)

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A1010B	41	n/a
A1020B	69	n/a
A1240A	134	134
A1280A	168	168
A1280XL	168	168
A1425A	75	75
A1460A	165	165
A14100A	195	195
A32100DX	178	178
A32200DX	230	230

Fixed Clock Loads (s_1/s_2—ACT 3 Only)

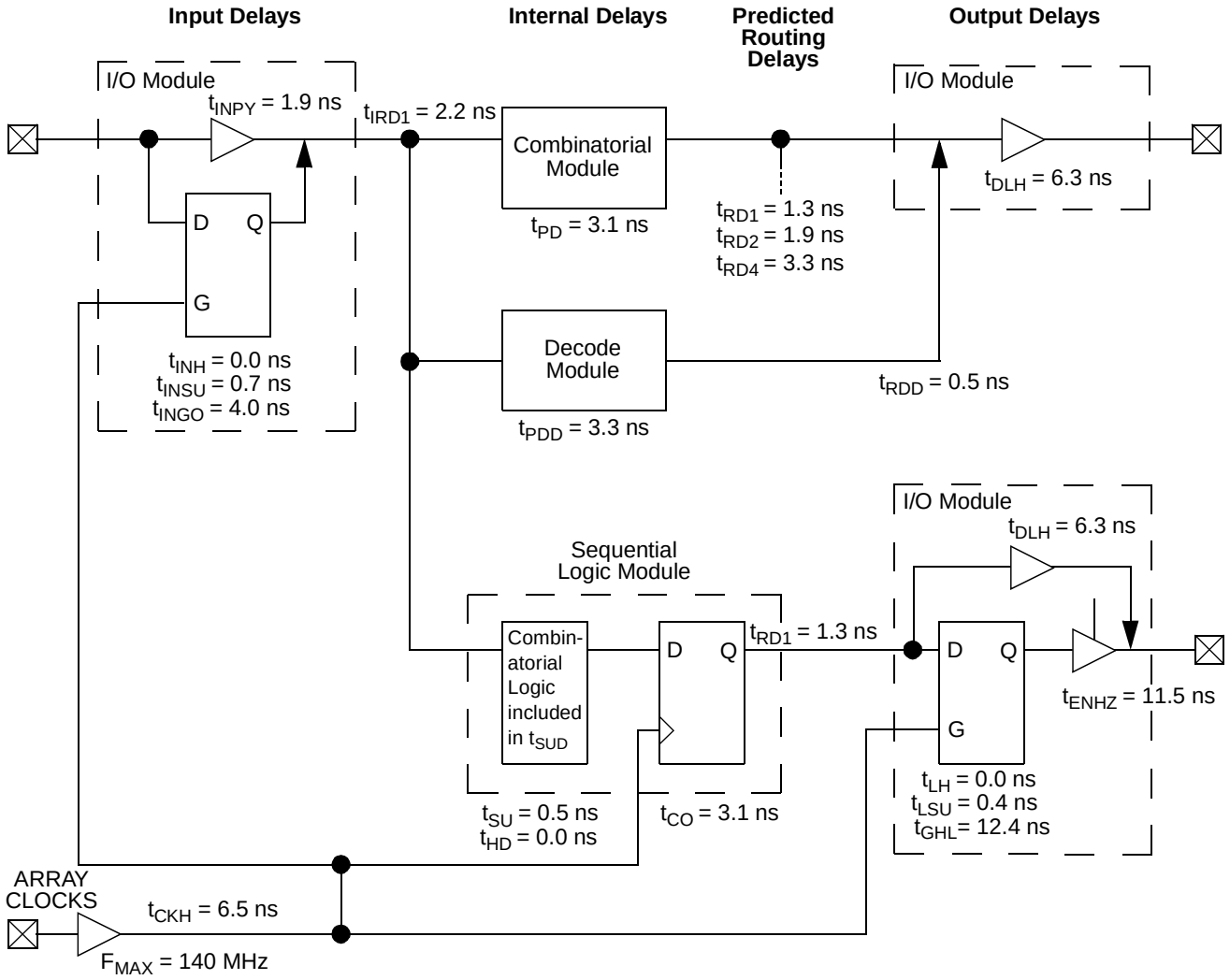
Device Type	s_1 Clock Loads on Dedicated Array Clock	s_2 Clock Loads on Dedicated I/O Clock
A1425A	160	100
A1460A	432	168
A14100A	697	228

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data values input to the circuit. The guidelines in the table below are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation.

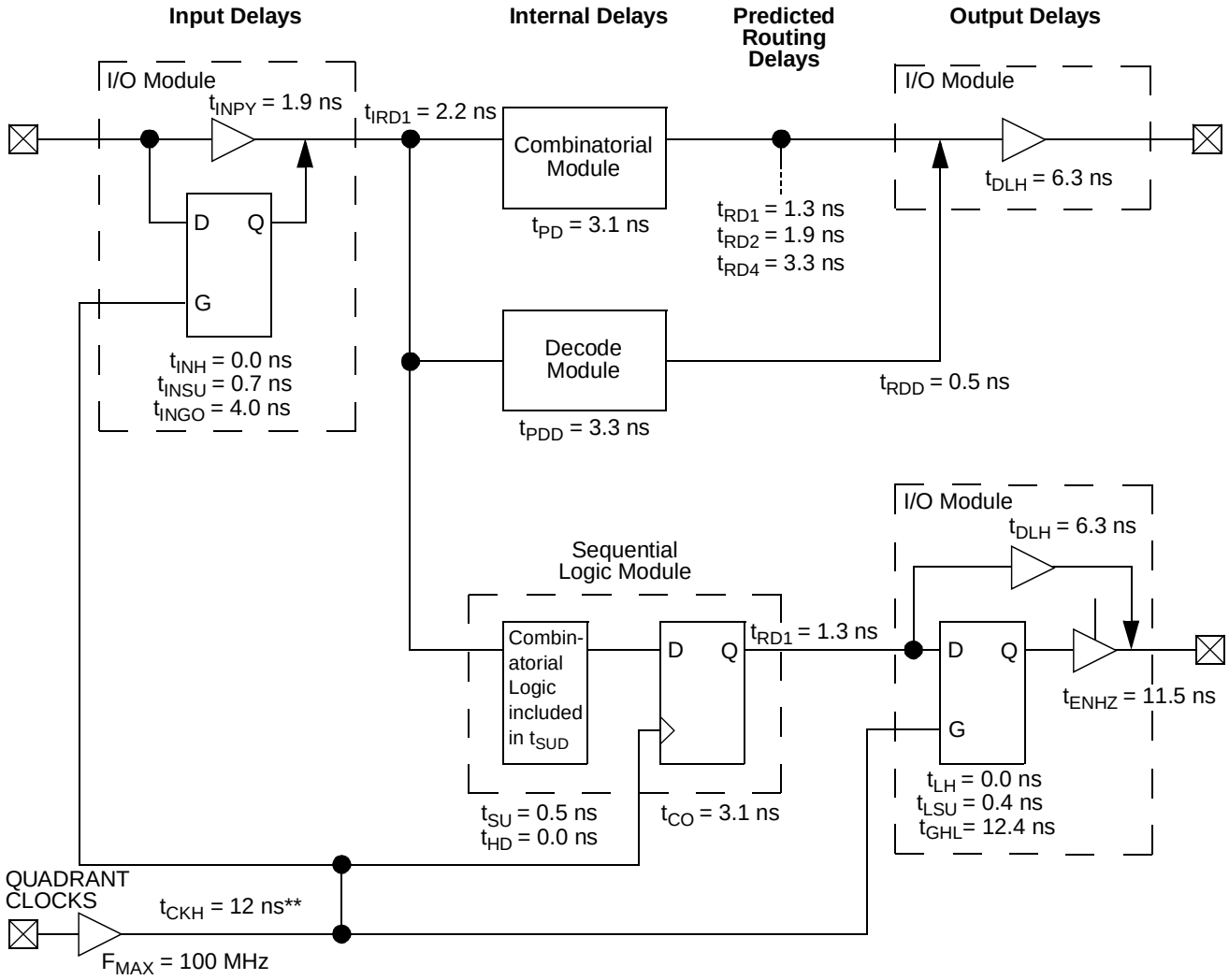
Type	ACT 3	3200DX/ACT 2/1200XL	ACT 1
Logic modules (m)	80% of modules	80% of modules	90% of modules
Input switching (n)	# inputs/4	# inputs/4	# inputs/4
Outputs switching (p)	#outputs/4	#outputs/4	#outputs/4
First routed array clock loads (q_1)	40% of sequential modules	40% of sequential modules	40% of modules
Second routed array clock loads (q_2)	40% of sequential modules	40% of sequential modules	n/a
Load capacitance (C_L)	35 pF	35 pF	35 pF
Average logic module switching rate (f_m)	F/10	F/10	F/10
Average input switching rate (f_n)	F/5	F/5	F/5
Average output switching rate (f_p)	F/10	F/10	F/10
Average first routed array clock rate (f_{q1})	F/2	F	F
Average second routed array clock rate (f_{q2})	F/2	F/2	n/a
Average dedicated array clock rate (f_{s1})	F	n/a	n/a
Average dedicated I/O clock rate (f_{s2})	F	n/a	n/a

3200DX Timing Model (Logic Functions using Array Clocks)*



**Values shown for A32100DX–1 at worst-case military conditions.*

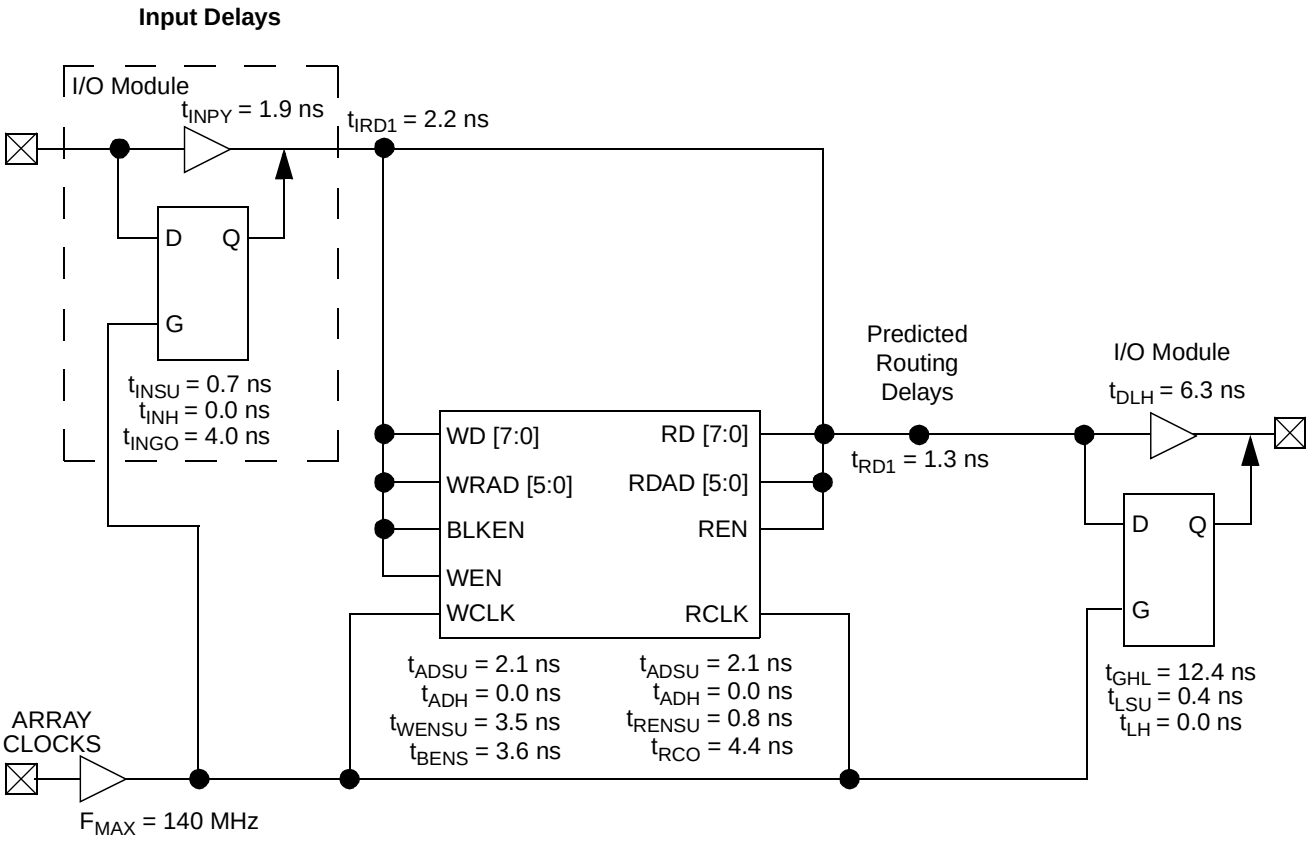
3200DX Timing Model (Logic Functions using Quadrant Clocks)*



** Values shown for A32100DX–1 at worst-case military conditions.*

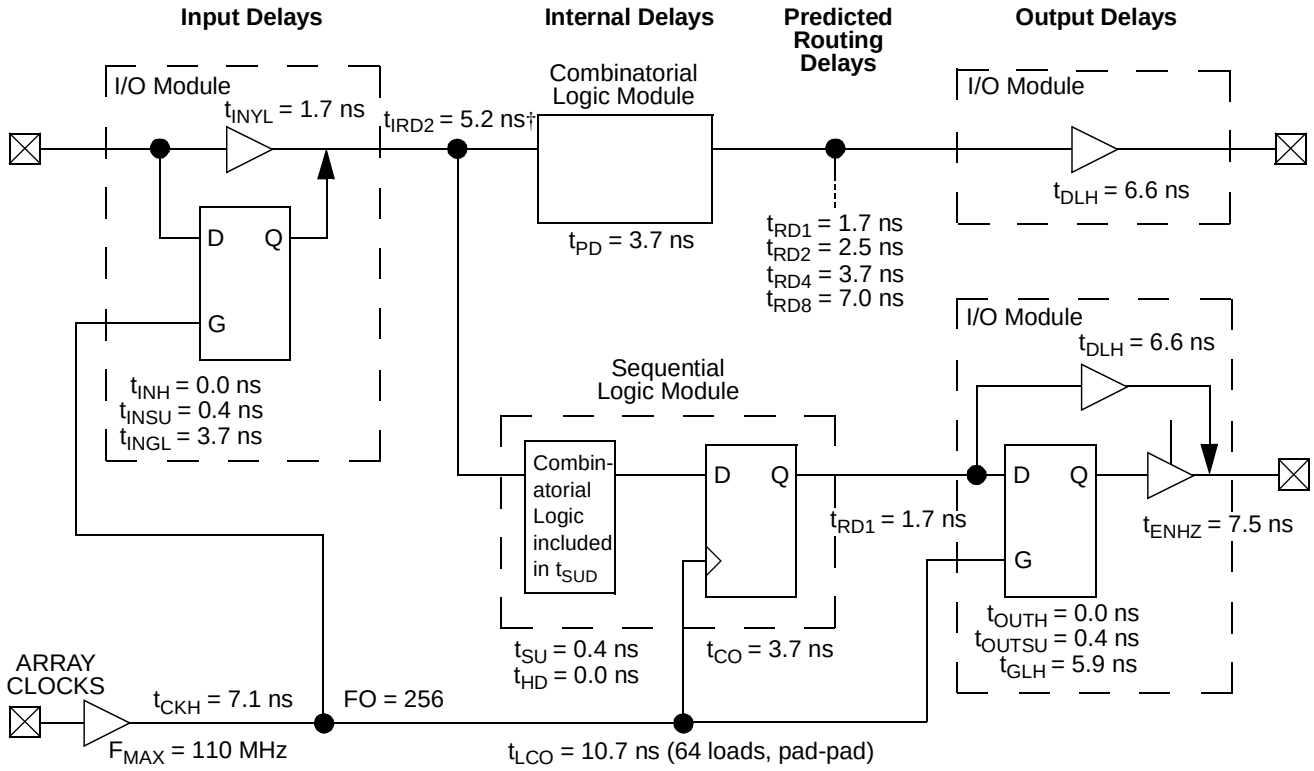
*** Load dependent.*

3200DX Timing Model (SRAM Functions)*



**Values shown for A32100DX–1 at worst-case military conditions.*

1200XL Timing Model*

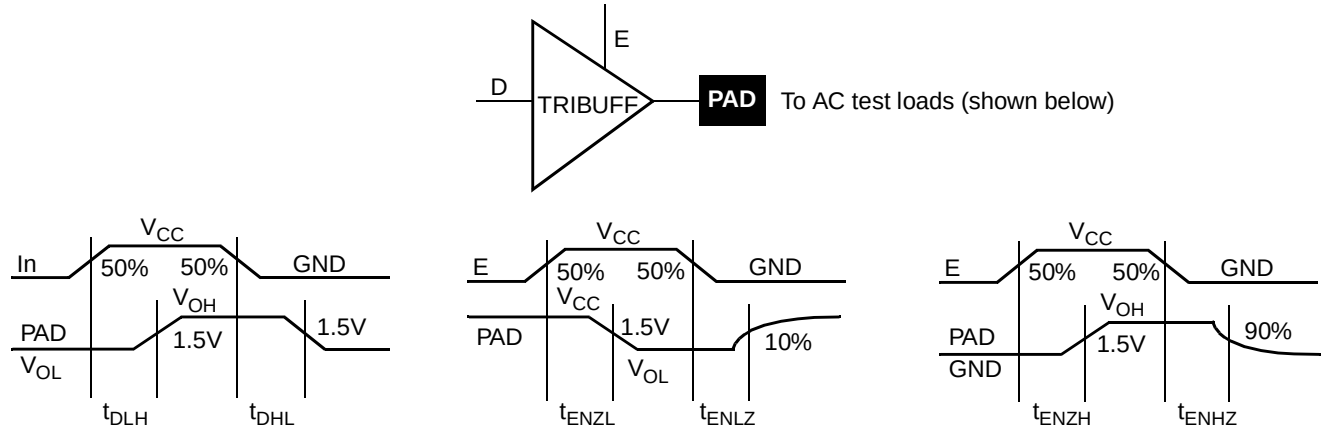


**Values shown for A1280XL–1 at worst-case military conditions.*

† Input module predicted routing delay.

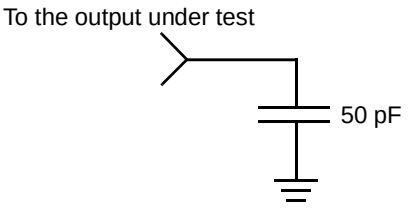
Parameter Measurement

Output Buffer Delays

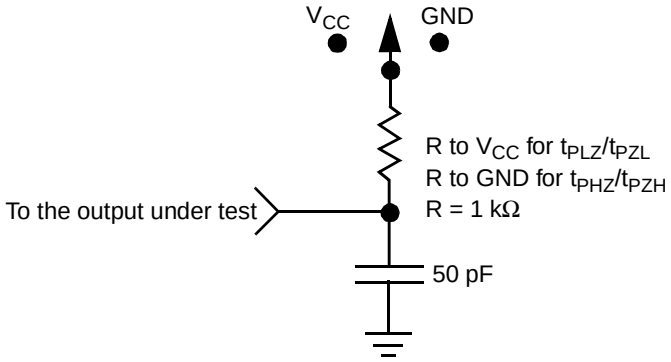


AC Test Load

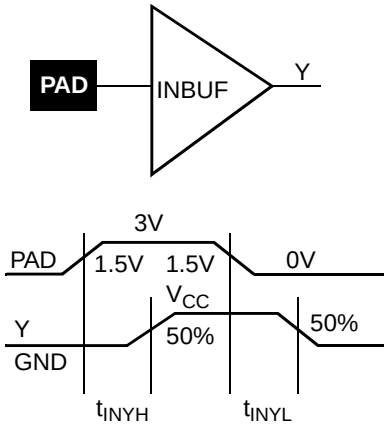
Load 1
(Used to measure propagation delay)



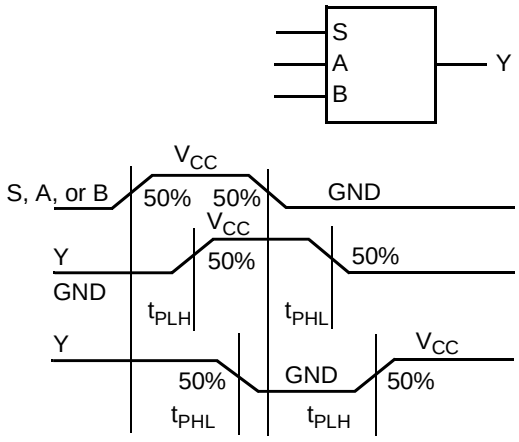
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

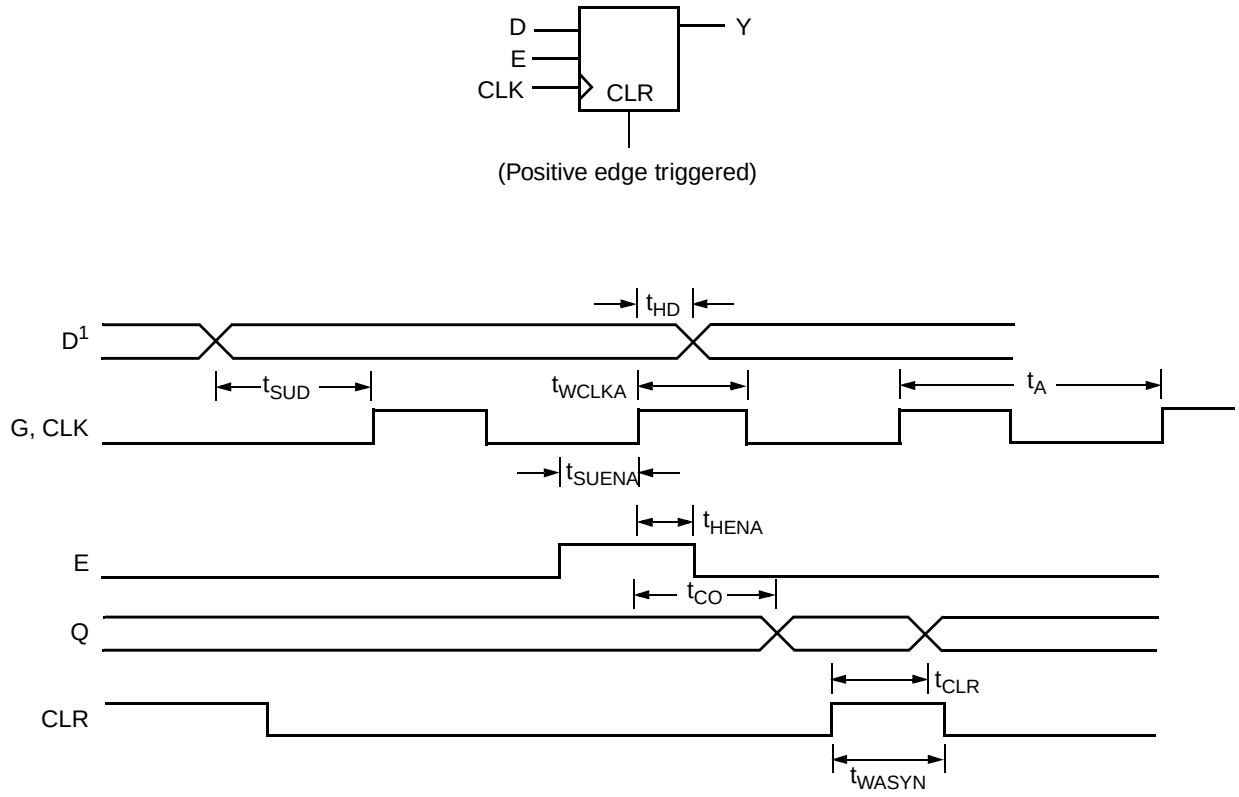


Combinatorial Macro Delays



Sequential Timing Characteristics

Flip-Flops and Latches (ACT 3)

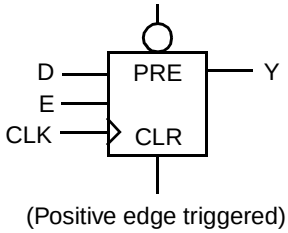


Note:

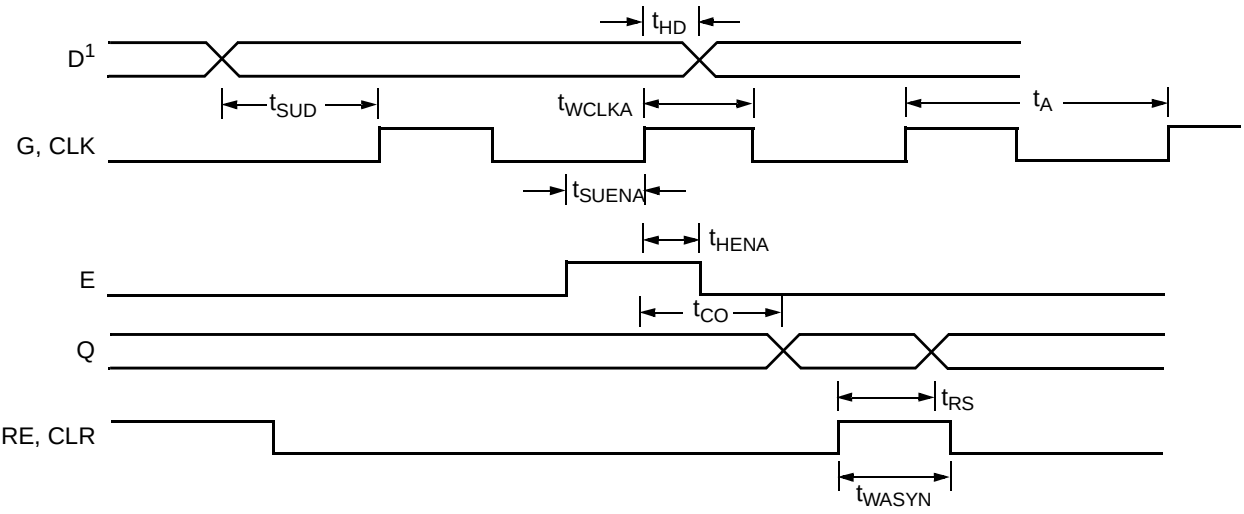
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

Flip-Flops and Latches (1200XL/3200DX, ACT 2, and ACT 1)



(Positive edge triggered)

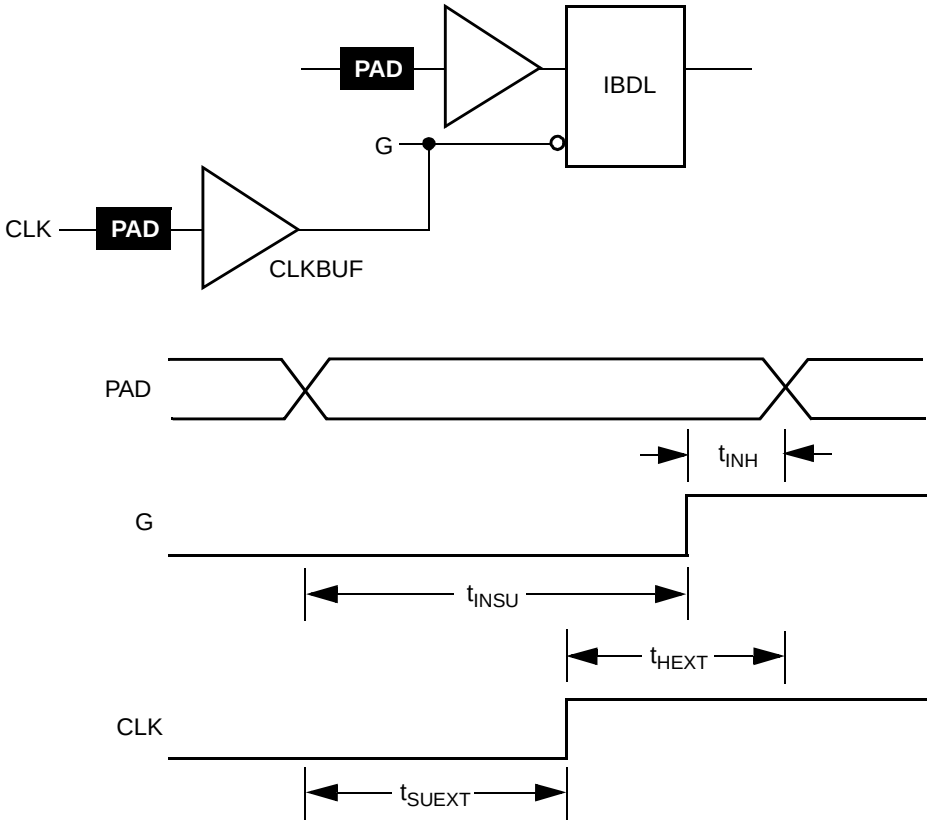


Note:

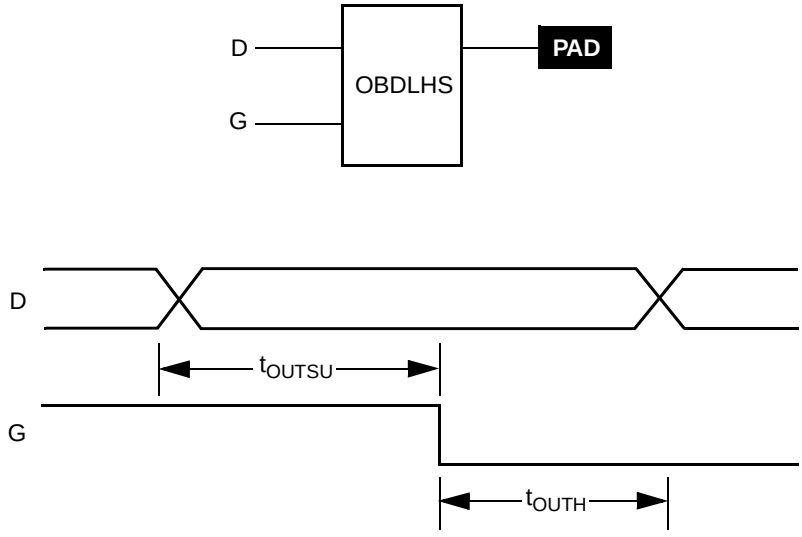
1. *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

Sequential Timing Characteristics (continued)

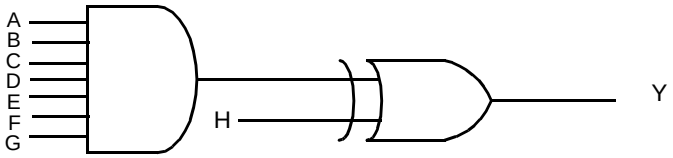
Input Buffer Latches (ACT 2 and 1200XL/3200DX)

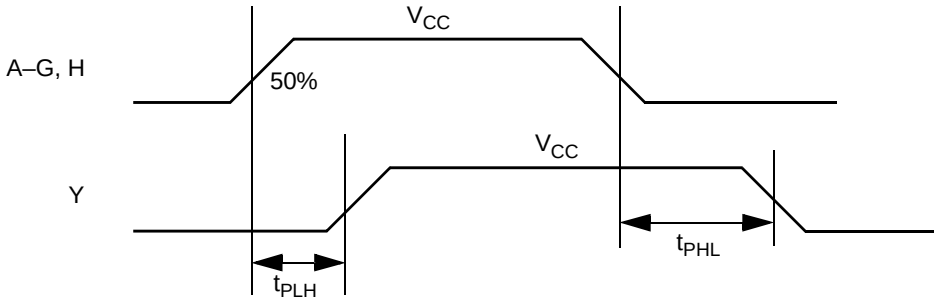


Output Buffer Latches (ACT 2 and 1200XL/3200DX)

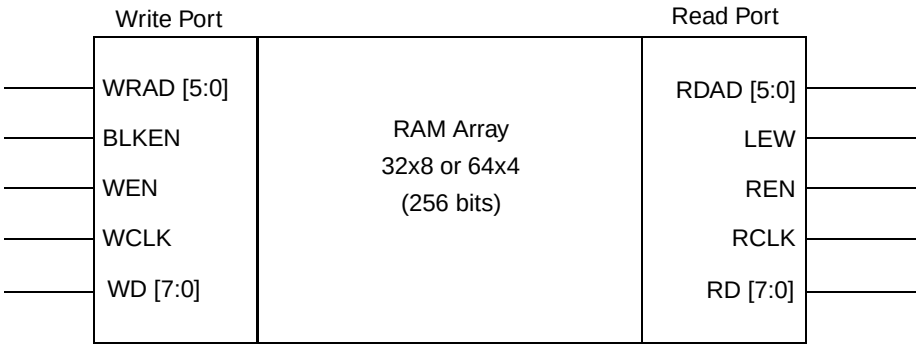


Decode Module Timing



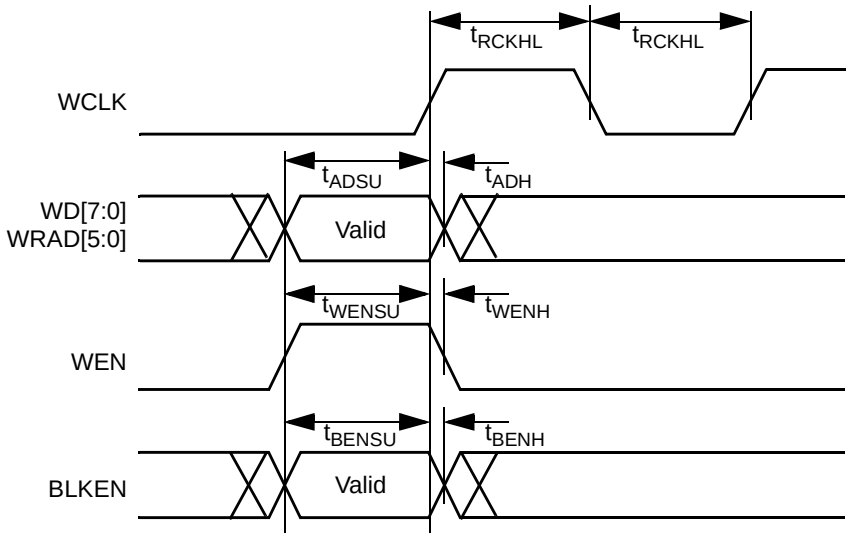


SRAM Timing Characteristics



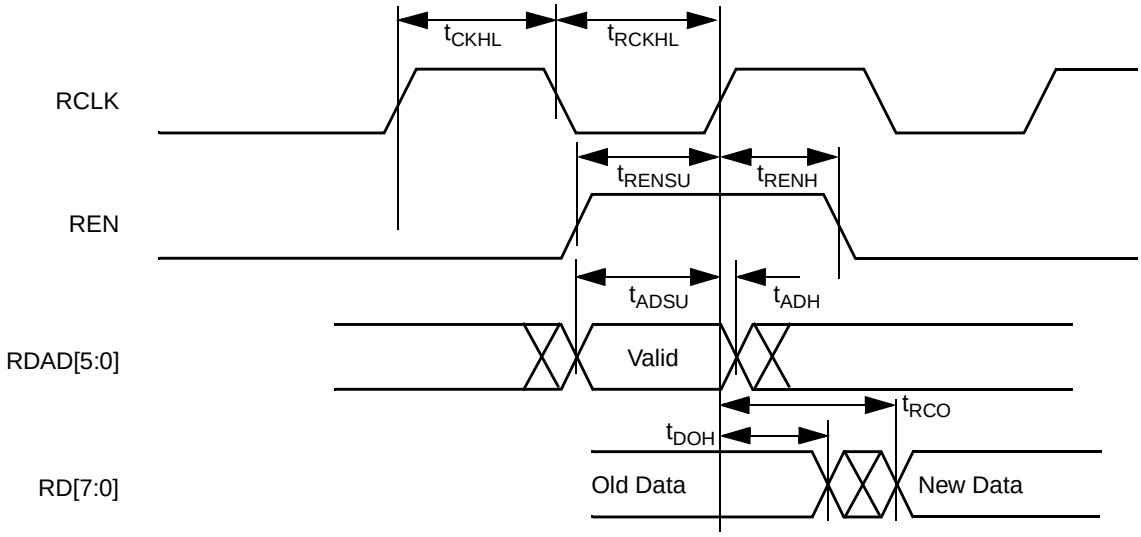
Dual-Port SRAM Timing Waveforms

3200DX SRAM Write Operation



Note: *Identical timing for falling-edge clock.*

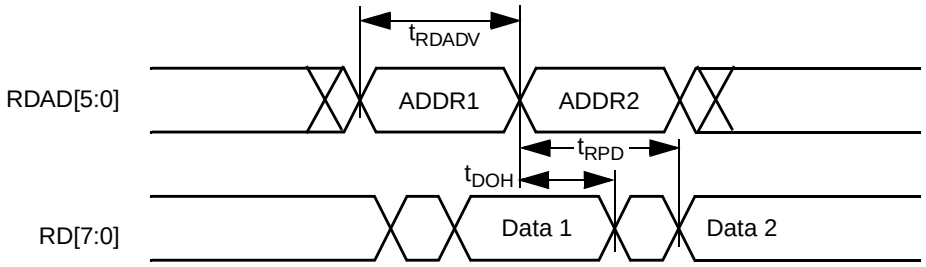
3200DX SRAM Synchronous Read Operation



Note: *Identical timing for falling-edge clock.*

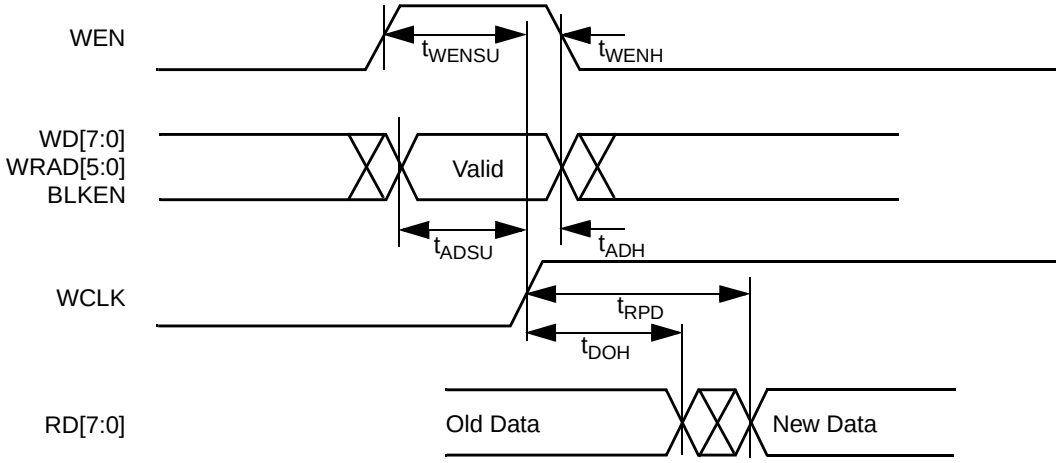
3200DX SRAM Asynchronous Read Operation—Type 1

(Read Address Controlled)



3200DX SRAM Asynchronous Read Operation—Type 2

(Write Address Controlled)



ACT 1 Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays						
t_{PD1}	Single Module		4.7		5.5	ns
t_{PD2}	Dual Module Macros		10.8		12.7	ns
t_{CO}	Sequential Clk to Q		4.7		5.5	ns
t_{GO}	Latch G to Q		4.7		5.5	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		4.7		5.5	ns
Logic Module Predicted Routing Delays[1]						
t_{RD1}	FO=1 Routing Delay		1.5		1.7	ns
t_{RD2}	FO=2 Routing Delay		2.3		2.7	ns
t_{RD3}	FO=3 Routing Delay		3.4		4.0	ns
t_{RD4}	FO=4 Routing Delay		5.0		5.9	ns
t_{RD8}	FO=8 Routing Delay		10.6		12.5	ns
Logic Module Sequential Timing [2]						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	8.8		10.4		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	8.8		10.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	10.9		12.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	10.9		12.9		ns
t_A	Flip-Flop Clock Input Period	23.2		27.3		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		44		37	MHz
Input Module Propagation Delays						
t_{INYH}	Pad to Y High		4.9		5.8	ns
t_{INYL}	Pad to Y Low		4.9		5.8	ns
Input Module Predicted Routing Delays[1, 3]						
t_{IRD1}	FO=1 Routing Delay		1.5		1.7	ns
t_{IRD2}	FO=2 Routing Delay		2.3		2.7	ns
t_{IRD3}	FO=3 Routing Delay		3.4		4.0	ns
t_{IRD4}	FO=4 Routing Delay		5.0		5.9	ns
t_{IRD8}	FO=8 Routing Delay		10.6		12.5	ns

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Setup times assume fanout of 3. Further derating information can be obtained from the DirectTime Analyzer utility.*
3. *Optimization techniques may further reduce delays by 0 to 4 ns.*