ACT 2 Family FPGAs

Features

- Up to 8,000 Gate Array Gates (20,000 PLD equivalent gates)
- Replaces up to 200 TTL Packages
- Replaces up to eighty 20-Pin PAL® Packages
- Design Library with over 500 Macro Functions
- Single-Module Sequence Functions
- Wide-Input Combinatorial Functions
- Up to 1,232 Programmable Logic Modules
- Up to 998 Flip-Flops
- Datapath Performance at 105 MHz
- 16-Bit Accumulator Performance to 39 MHz
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Two High-Speed, Low-Skew Clock Networks
- I/O Drive to 10 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment
- 1.0 micron CMOS Technology

Table 1 • ACT 2 Product Family Profile

Device	A1225A	A1240A	A1280A
Capacity			
Gate Array Equivalent Gates	2,500	4,000	8,000
PLD Equivalent Gates	6,250	10,000	20,000
TTL Equivalent Package	63	100	200
20-Pin PAL Equivalent Packages	25	40	80
Logic Modules	451	684	1,232
S-Module	231	348	624
C-Module	220	336	608
Flip-Flops (maximum)	382	568	998
Routing Resources			
Horizontal Tracks/Channel	36	36	36
Vertical Tracks/Channel	15	15	15
PLICE Antifuse Elements	250,000	400,000	750,000
User I/Os (maximum)	83	104	140
Performance[1]			
16-Bit Prescaled Counters	105 MHz	100 MHz	85 MHz
16-Bit Loadable Counters	70 MHz	69 MHz	67 MHz
16-Bit Accumulators	39 MHz	38 MHz	36 MHz
Packages[2]			
CPGA	PG100	PG132	PG176
PLCC	PL84	PL84	PL84
PQFP	PQ100	PQ144	PQ160
VQFP	VQ100	–	–
TQFP	–	TQ176	TQ176
CQFP	–	–	CQ172

Notes:

1. *Performance is based on –2 speed devices at commercial worst-case operating conditions using PREP Benchmarks, Suite #1, Version 1.2, dated 3-28-93. Any analysis is not endorsed by PREP.*
2. *See the "Product Plan" on page III for package availability.*

Ordering Information

A1280 A – 1 PG G 176 C

- **Application (Temperature Range)** (C)
  - C = Commercial (0 to +70°C)
  - I = Industrial (–40 to +85°C)
  - M = Military (–55 to +125°C)
  - B = MIL-STD-883
- **Package Lead Count** (176)
- **Lead-Free Packaging** (G)
  - Blank = Standard Packaging
  - G = RoHS Compliant Packaging
- **Package Type** (PG)
  - PL = Plastic J-Leaded Chip Carrier
  - PQ = Plastic Quad Flat Pack
  - CQ = Ceramic Quad Flat Pack
  - PG = Ceramic Pin Grid Array
  - TQ = Thin (1.4 mm) Quad Flat Pack
  - VQ = Very Thin (1.0 mm) Quad Flat Pack
- **Speed Grade** (1)
  - Blank = Standard Speed
  - –1 = Approximately 15% faster than Standard
  - –2 = Approximately 25% faster than Standard
- **Die Revision** (A)
  - A = 1.0 µm CMOS Process
- **Part Number** (A1280)
  - A1225 = 2,500 Gates
  - A1240 = 4,000 Gates
  - A1280 = 8,000 Gates

Product Plan

Device/Package	Speed Grade[1]			Application[1]			
	Std.	–1	–2	C	I	M	B
A1225A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
100-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQ)	✓	✓	✓	✓	–	–	–
100-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	–	–
A1240A Device							
84-Pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–
132-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
144-Pin Plastic Quad Flat Pack (PQ)	✓	✓	✓	✓	✓	–	–
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–
A1280A Device							
160-Pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–
172-Pin Ceramic Quad Flatpack (CQ)	✓	✓	✓	✓	–	✓	✓
176-Pin Ceramic Pin Grid Array (PG)	✓	✓	✓	✓	–	✓	✓
176-Pin Thin (1.4 mm) Quad Flat Pack (TQ)	✓	✓	✓	✓	–	–	–

Notes:

1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
   B = MIL-STD-883

Availability:
✓ = Available
P = Planned
– = Not planned

Speed Grade:
–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.

2. *Contact your Microsemi SoC Products Group sales representative for product availability.*

Device Resources

Device Series	Logic Modules	Gates	User I/Os									
			PG176	PG132	PG100	PQ160	PQ144	PQ100	PL84	CQ172	TQ176	VQ100
A1225A	451	2,500	–	–	83	–	–	83	72	–	–	83
A1240A	684	4,000	–	104	–	–	104	–	72	–	104	–
A1280A	1,232	8,000	140	–	–	125	–	–	72	140	140	–

Contact your local Microsemi SoC Products Group representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx.

Table of Contents

1 – ACT 2 Family Overview

General Description

The ACT 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-modules and S-modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining downward compatibility with the ACT 1 design environment and upward compatibility with the ACT 3 design environment. The devices are implemented in silicon gate, 1.0-µm, two-level metal CMOS, and employ Actel's PLICE® antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast time-to-production with user programming. The ACT 2 family is supported by the Designer and Designer Advantage Systems, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and diagnostic probe capabilities. The systems are supported on the following platforms: 386/486™ PC, Sun™, and HP™ workstations. The systems provide CAE interfaces to the following design environments: Cadence, Viewlogic®, Mentor Graphics®, and OrCAD™.

2 – Detailed Specifications

Operating Conditions

Table 2-1 • **Absolute Maximum Ratings[1]**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	–0.5 to +7.0	V
VI	Input voltage	–0.5 to VCC + 0.5	V
VO	Output voltage	–0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will be forward biased and can draw excessive current.*

Table 2-2 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	–40 to +85	–55 to +125	°C
Power supply tolerance	±5	±10	±10	%VCC

*Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Table 2-3 • **Electrical Specifications**

Symbol	Parameter	Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
VOH[1]	(IOH = –10 mA)[2]	2.4	–	–	–	–	–	V
	(IOH = –6 mA)	3.84	–	–	–	–	–	V
	(IOH = –4 mA)	–	–	3.7	–	3.7	–	V
VOL[1]	(IOL = 10 mA)[2]	–	0.5	–	–	–	–	V
	(IOL = 6 mA)	–	0.33	–	0.40	–	0.40	V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
Input Transition Time t_R, t_F[2]		–	500	–	500	–	500	ns
C_{IO} I/O capacitance[2,3]		–	10	–	10	–	10	pF
Standby Current, ICC[4] (typical = 1 mA)		–	2	–	10	–	20	mA
Leakage Current[5]		–10	+10	–10	+10	–10	+10	µA
ICC(D)	Dynamic VCC supply current. See the Power Dissipation section.							

Notes:

1. *Only one output tested at a time. VCC = minimum.*
2. *Not tested, for information only.*
3. *Includes worst-case PG176 package capacitance. VOUT = 0 V, f = 1 MHz*
4. *All outputs unloaded. All inputs = VCC or GND, typical ICC = 1 mA. ICC limit includes IPP and ISV during normal operations.*
5. *VOUT, VIN = VCC or GND.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQ160 package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{°C/W}} = \frac{150\text{°C} - 70\text{°C}}{33\text{°C/W}} = 2.4\text{ W}$$

EQ 1

Table 2-4 • **Package Thermal Characteristics**

Package Type*	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft./min.	Units
Ceramic Pin Grid Array	100	5	35	17	°C/W
	132	5	30	15	°C/W
	176	8	23	12	°C/W
Ceramic Quad Flatpack	172	8	25	15	°C/W
Plastic Quad Flatpack[1]	100	13	48	40	°C/W
	144	15	40	32	°C/W
	160	15	38	30	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	15	32	25	°C/W

Notes: (Maximum Power in Still Air)

1. *Maximum power dissipation values for PQFP packages are 1.9 W (PQ100), 2.3 W (PQ144), and 2.4 W (PQ160).*
2. *Maximum power dissipation for PLCC packages is 2.7 W.*
3. *Maximum power dissipation for VQFP packages is 2.3 W.*
4. *Maximum power dissipation for TQFP packages is 3.1 W.*

Power Dissipation

P = [ICC standby + ICCactive] * VCC + IOL * VOL * N + IOH* (VCC – VOH) * M

EQ 2

where:

ICC standby is the current flowing when no inputs or outputs are changing

ICCactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source currents.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M is the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-5 for commercial, worst case conditions.

***Table 2-5 •* Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 3.

$$\text{Power } (\mu W) = C_{EQ} * VCC^2 * F$$

EQ 3

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Table 2-6.

***Table 2-6 •* CEQ Values for Microsemi FPGAs**

Item	CEQ Value
Modules (C_{EQM})	5.8
Input Buffers (C_{EQI})	12.9
Output Buffers (C_{EQO})	23.8
Routed Array Clock Buffer Loads (C_{EQCR})	3.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 4 shows a piece-wise linear summation over all components.

$$\text{Power} = VCC^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs}$$
$$+ (p * (C_{EQO} + C_L) * fp)outputs$$
$$+ 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r1 * f_{q1})_{routed\_Clk1}$$
$$+ 0.5 * (q2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2}$$

EQ 4

Where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q1 = Number of clock loads on the first routed array clock

q2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Table 2-7 • **Fixed Capacitance Values for Microsemi FPGAs**

Device Type	r1, routed_Clk1	r2, routed_Clk2
A1225A	106	106.0
A1240A	134	134.2
A1280A	168	167.8

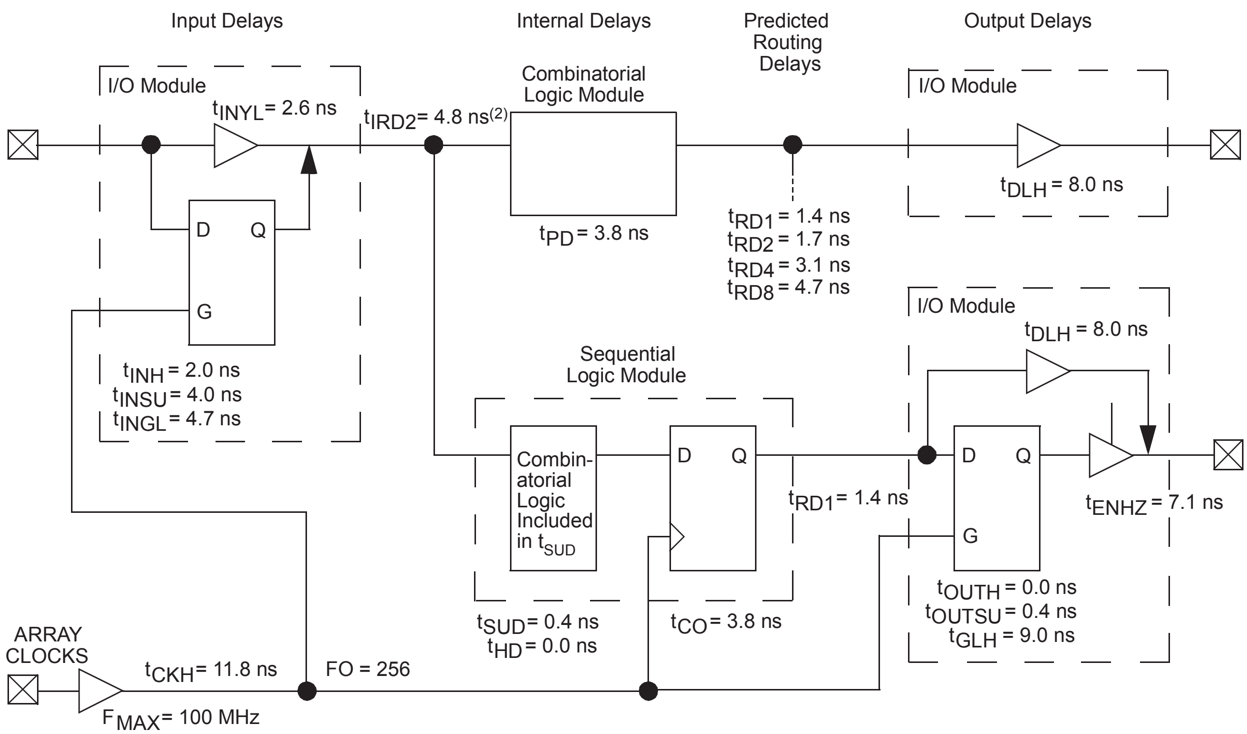
Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are given in Table 2-8.

Table 2-8 • **Guidelines for Predicting Power Dissipation**

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (C_L)	35 pF
Average logic module switching rate (f_m)	F/10
Average input switching rate (f_n)	F/5
Average output switching rate (f_p)	F/10
Average first routed array clock rate (f_{q1})	F
Average second routed array clock rate (f_{q2})	F/2

ACT 2 Timing Model[1]



Notes:

1. *Values shown for A1240A-2 at worst-case commercial conditions.*
2. *Input module predicted routing delay*

Figure 2-1 • **Timing Model**

Parameter Measurement

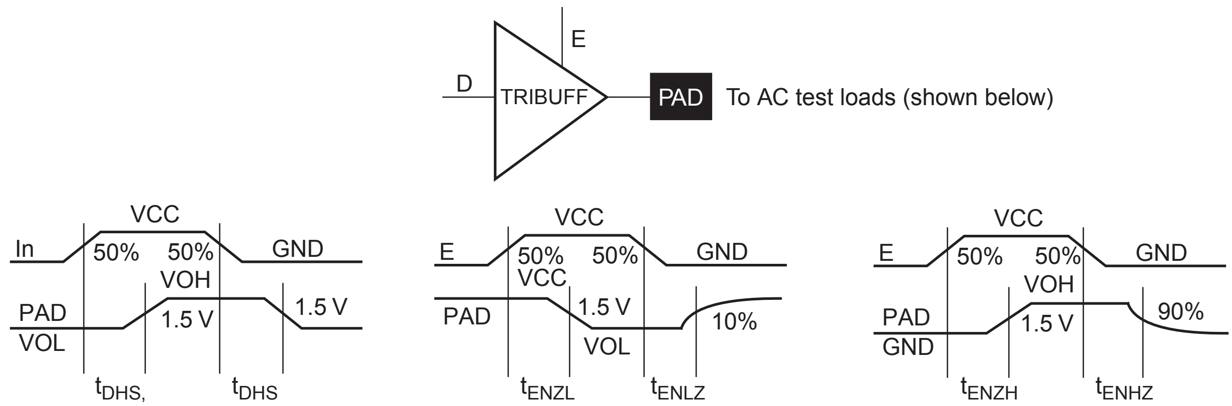


Figure 2-2 • **Output Buffer Delays**

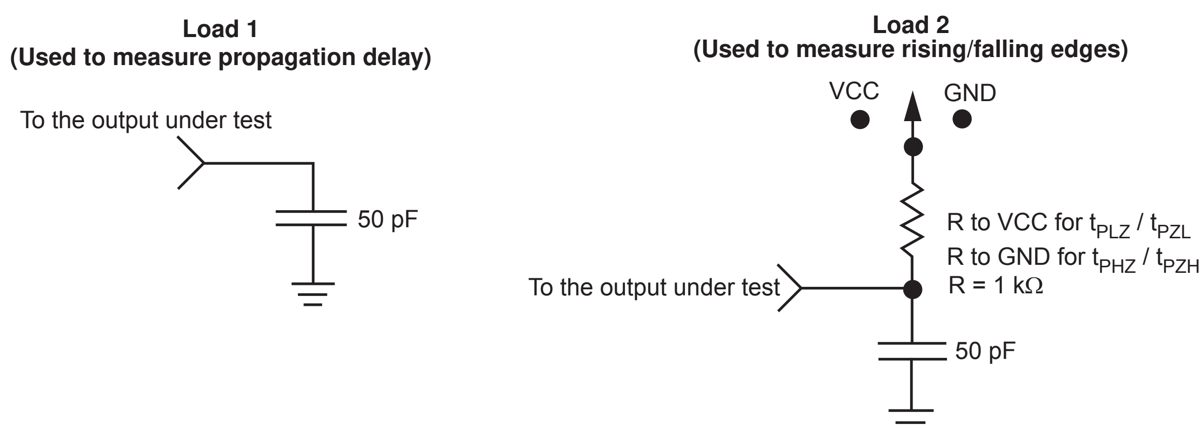


Figure 2-3 • **AC Test Loads**

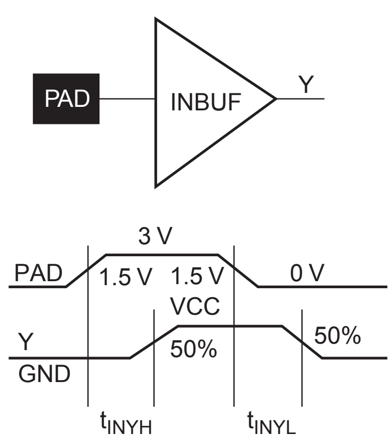


Figure 2-4 • **Input Buffer Delays**

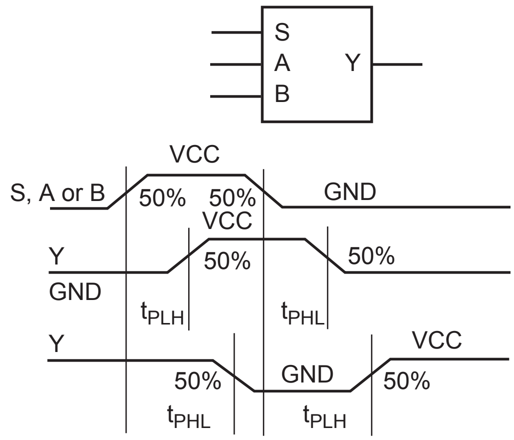
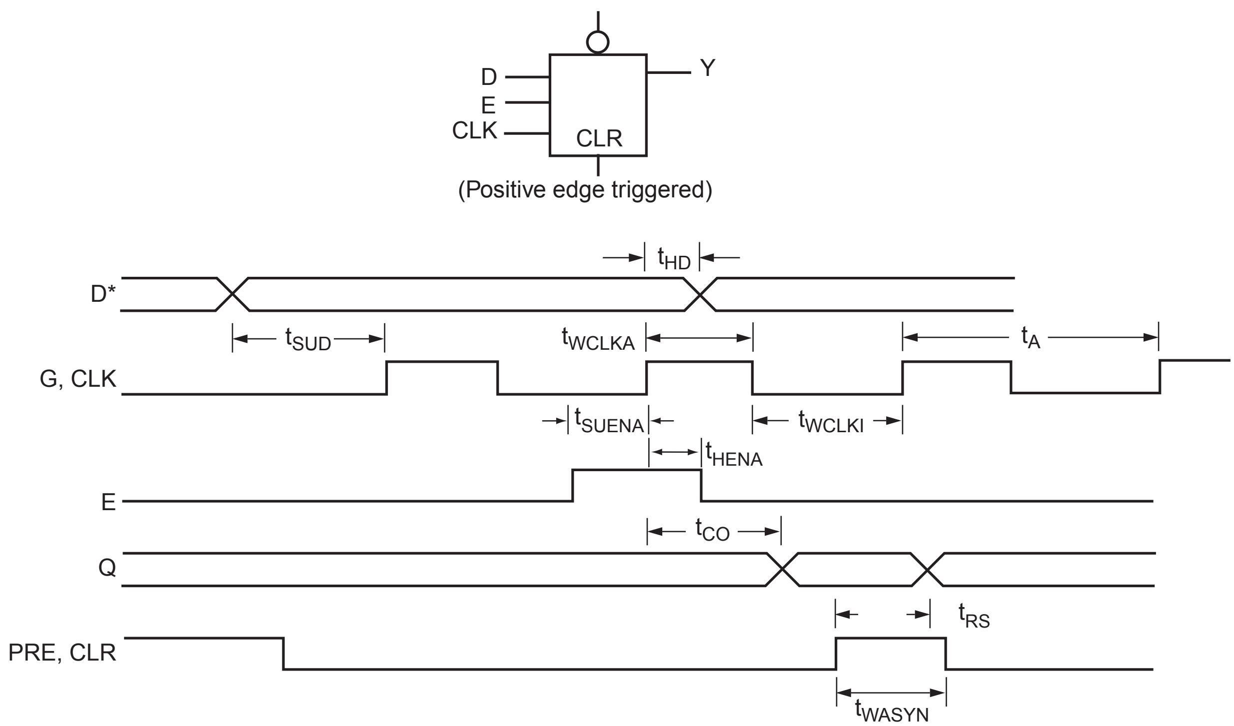


Figure 2-5 • **Module Delays**

Sequential Module Timing Characteristics



Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

Figure 2-6 • **Flip-Flops and Latches**

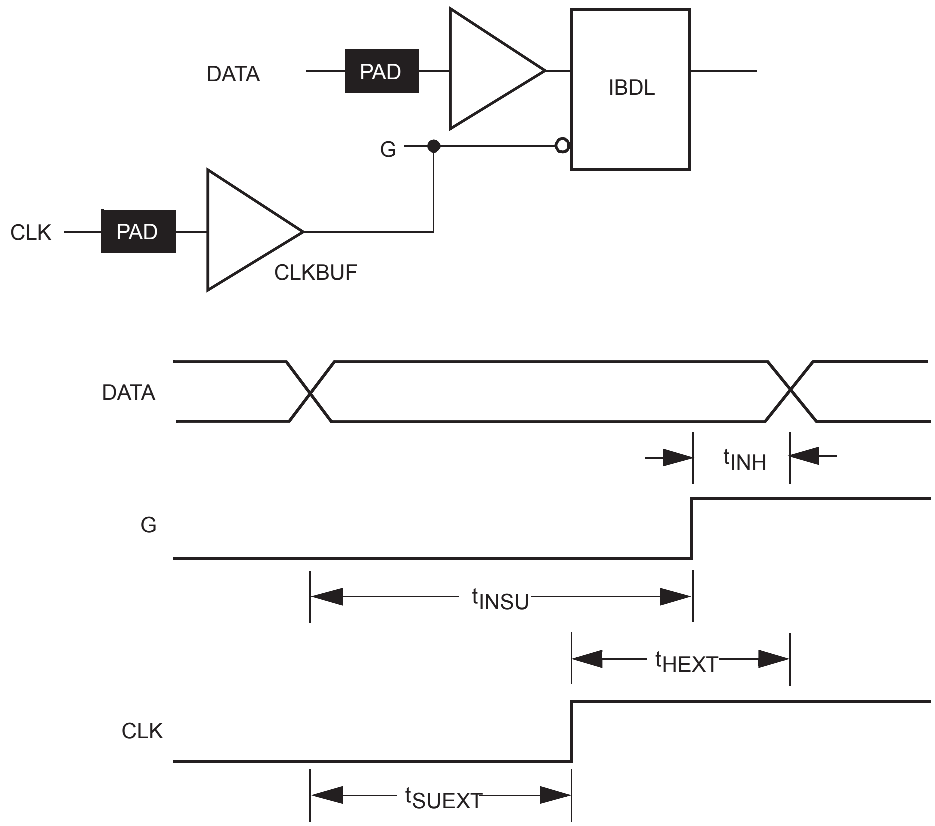


Figure 2-7 • **Input Buffer Latches**

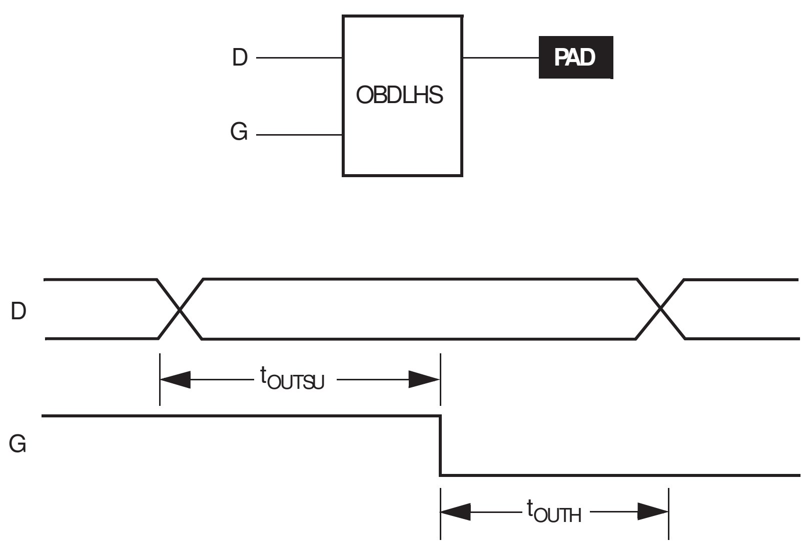


Figure 2-8 • **Output Buffer Latches**

Timing Derating Factor (Temperature and Voltage)

Table 2-9 • **Timing Derating Factor (Temperature and Voltage)**

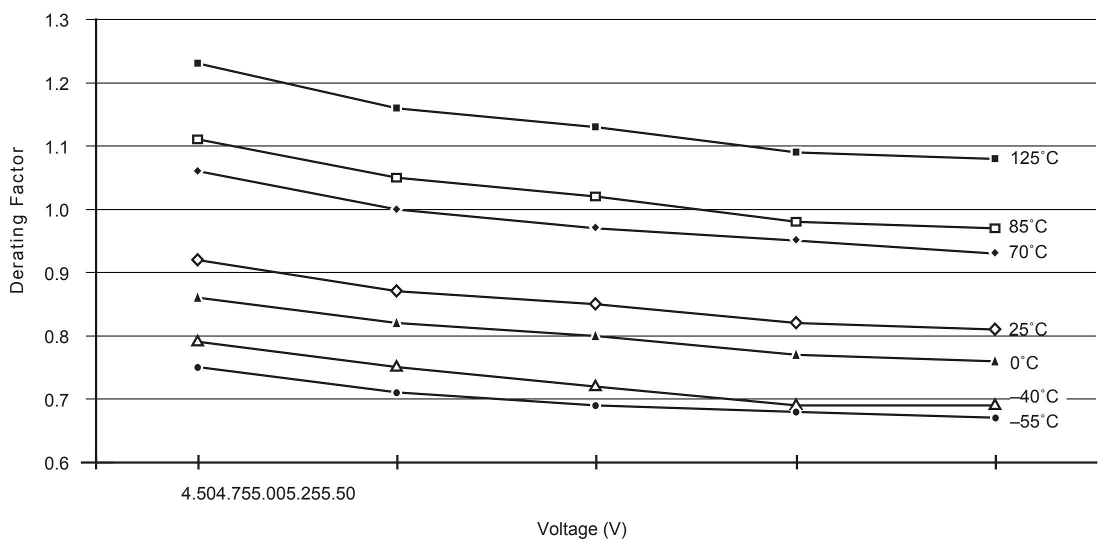
(Commercial Minimum/Maximum Specification) x	Industrial		Military	
	Min.	**Max.**	**Min.**	Max.
	0.69	1.11	0.67	1.23

Table 2-10 • **Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0 V)**

(Commercial Maximum Specification) x	0.85

Table 2-11 • **Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, TJ = 4.75 V, 70°C)**

	–55	**–40**	**0**	**25**	**70**	**85**	**125**
4.50	0.75	0.79	0.86	0.92	1.06	1.11	1.23
4.75	0.71	0.75	0.82	0.87	1.00	1.05	1.13
5.00	0.69	0.72	0.80	0.85	0.97	1.02	1.13
5.25	0.68	0.69	0.77	0.82	0.95	0.98	1.09
5.50	0.67	0.69	0.76	0.81	0.93	0.97	1.08



Note: This derating factor applies to all routing and propagation delays.

Figure 2-9 • **Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)**

A1225A Timing Characteristics

***Table 2-12* • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Logic Module Propagation Delays[1]		**–2 Speed**[3]		**–1 Speed**		**Std. Speed**		**Units**
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{PD1}	Single Module		3.8		4.3		5.0	ns
t_{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t_{GO}	Latch G to Q		3.8		4.3		5.0	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays[2]								
t_{RD1}	FO = 1 Routing Delay		1.1		1.2		1.4	ns
t_{RD2}	FO = 2 Routing Delay		1.7		1.9		2.2	ns
t_{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t_{RD4}	FO = 4 Routing Delay		2.8		3.1		3.7	ns
t_{RD8}	FO = 8 Routing Delay		4.4		4.9		5.8	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		5.0		6.0		ns
t_{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		5.0		6.0		ns
t_A	Flip-Flop Clock Input Period	9.4		11.0		13.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		105.0		90.0		75.0	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$—whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1225A Timing Characteristics (continued)

Table 2-13 • **A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t_{INYL}	Pad to Y Low			2.6		3.0		3.5	ns
t_{INGH}	G to Y High			5.0		5.7		6.6	ns
t_{INGL}	G to Y Low			4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t_{IRD1}	FO = 1 Routing Delay			4.1		4.6		5.4	ns
t_{IRD2}	FO = 2 Routing Delay			4.6		5.2		6.1	ns
t_{IRD3}	FO = 3 Routing Delay			5.3		6.0		7.1	ns
t_{IRD4}	FO = 4 Routing Delay			5.7		6.4		7.6	ns
t_{IRD8}	FO = 8 Routing Delay			7.4		8.3		9.8	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t_{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t_{PWH}	Minimum Pulse Width High	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t_{PWL}	Minimum Pulse Width Low	FO = 32	3.4		4.1		4.5		ns
		FO = 256	3.8		4.5		5.0		
t_{CKSW}	Maximum Skew	FO = 32		0.7		0.7		0.7	ns
		FO = 256		3.5		3.5		3.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t_P	Minimum Period	FO = 32	7.7		8.3		9.1		ns
		FO = 256	8.1		8.8		10.0		
f_{MAX}	Maximum Frequency	FO = 32		130.0		120.0		110.0	ns
		FO = 256		125.0		115.0		100.0	

Note: **These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1225A Timing Characteristics (continued)

Table 2-14 • **A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

TTL Output Module Timing[1]		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t_{DLH}	Data to Pad High		8.0		9.0		10.6	ns
t_{DHL}	Data to Pad Low		10.1		11.4		13.4	ns
t_{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t_{ENZL}	Enable Pad Z to Low		11.6		13.2		15.5	ns
t_{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t_{ENLZ}	Enable Pad Low to Z		8.3		9.5		11.1	ns
t_{GLH}	G to Pad High		8.9		10.2		11.9	ns
t_{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d_{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d_{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing[1]								
t_{DLH}	Data to Pad High		10.1		11.5		13.5	ns
t_{DHL}	Data to Pad Low		8.4		9.6		11.2	ns
t_{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t_{ENZL}	Enable Pad Z to Low		11.6		13.2		15.5	ns
t_{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t_{ENLZ}	Enable Pad Low to Z		8.3		9.5		11.1	ns
t_{GLH}	G to Pad High		8.9		10.2		11.9	ns
t_{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d_{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d_{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.*

A1240A Timing Characteristics

Table 2-15 • **A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Logic Module Propagation Delays[1]		–2 Speed[3]		–1 Speed		Std. Speed		Units
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{PD1}	Single Module		3.8		4.3		5.0	ns
t_{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t_{GO}	Latch G to Q		3.8		4.3		5.0	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays[2]								
t_{RD1}	FO = 1 Routing Delay		1.4		1.5		1.8	ns
t_{RD2}	FO = 2 Routing Delay		1.7		2.0		2.3	ns
t_{RD3}	FO = 3 Routing Delay		2.3		2.6		3.0	ns
t_{RD4}	FO = 4 Routing Delay		3.1		3.5		4.1	ns
t_{RD8}	FO = 8 Routing Delay		4.7		5.4		6.3	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.5		6.0		6.5		ns
t_{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	4.5		6.0		6.5		ns
t_A	Flip-Flop Clock Input Period	9.8		12.0		15.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		100.0		80.0		66.0	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$—whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1240A Timing Characteristics (continued)

***Table 2-16* • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t_{INYL}	Pad to Y Low			2.6		3.0		3.5	ns
t_{INGH}	G to Y High			5.0		5.7		6.6	ns
t_{INGL}	G to Y Low			4.7		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t_{IRD1}	FO = 1 Routing Delay			4.2		4.8		5.6	ns
t_{IRD2}	FO = 2 Routing Delay			4.8		5.4		6.4	ns
t_{IRD3}	FO = 3 Routing Delay			5.4		6.1		7.2	ns
t_{IRD4}	FO = 4 Routing Delay			5.9		6.7		7.9	ns
t_{IRD8}	FO = 8 Routing Delay			7.9		8.9		10.5	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		11.8		13.0		15.7	
t_{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		12.0		13.2		15.9	
t_{PWH}	Minimum Pulse Width High	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t_{PWL}	Minimum Pulse Width Low	FO = 32	3.8		4.5		5.5		ns
		FO = 256	4.1		5.0		5.8		
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t_P	Minimum Period	FO = 32	8.1		9.1		11.1		ns
		FO = 256	8.8		10.0		11.7		
f_{MAX}	Maximum Frequency	FO = 32		125.0		110.0		90.0	ns
		FO = 256		115.0		100.0		85.0	

Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1240A Timing Characteristics (continued)

Table 2-17 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

TTL Output Module Timing[1]		–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	
t_{DLH}	Data to Pad High		8.0		9.0		10.6	ns
t_{DHL}	Data to Pad Low		10.1		11.4		13.4	ns
t_{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t_{ENZL}	Enable Pad Z to Low		11.7		13.2		15.5	ns
t_{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t_{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t_{GLH}	G to Pad High		9.0		10.2		11.9	ns
t_{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d_{TLH}	Delta Low to High		0.07		0.08		0.09	ns/pF
d_{THL}	Delta High to Low		0.12		0.13		0.16	ns/pF
CMOS Output Module Timing[1]								
t_{DLH}	Data to Pad High		10.2		11.5		13.5	ns
t_{DHL}	Data to Pad Low		8.4		9.6		11.2	ns
t_{ENZH}	Enable Pad Z to High		8.9		10.0		11.8	ns
t_{ENZL}	Enable Pad Z to Low		11.7		13.2		15.5	ns
t_{ENHZ}	Enable Pad High to Z		7.1		8.0		9.4	ns
t_{ENLZ}	Enable Pad Low to Z		8.4		9.5		11.1	ns
t_{GLH}	G to Pad High		9.0		10.2		11.9	ns
t_{GHL}	G to Pad Low		11.2		12.7		14.9	ns
d_{TLH}	Delta Low to High		0.12		0.13		0.16	ns/pF
d_{THL}	Delta High to Low		0.09		0.10		0.12	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.*

A1280A Timing Characteristics

***Table 2-18* • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Logic Module Propagation Delays[1]		–2 Speed[3]		–1 Speed		Std. Speed		Units
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{PD1}	Single Module		3.8		4.3		5.0	ns
t_{CO}	Sequential Clock to Q		3.8		4.3		5.0	ns
t_{GO}	Latch G to Q		3.8		4.3		5.0	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.8		4.3		5.0	ns
Predicted Routing Delays[2]								
t_{RD1}	FO = 1 Routing Delay		1.7		2.0		2.3	ns
t_{RD2}	FO = 2 Routing Delay		2.5		2.8		3.3	ns
t_{RD3}	FO = 3 Routing Delay		3.0		3.4		4.0	ns
t_{RD4}	FO = 4 Routing Delay		3.7		4.2		4.9	ns
t_{RD8}	FO = 8 Routing Delay		6.7		7.5		8.8	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.5		6.0		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Clock Asynchronous Pulse Width	5.5		6.0		7.0		ns
t_A	Flip-Flop Clock Input Period	11.7		13.3		18.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		85.0		75.0		50.0	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$—whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A1280A Timing Characteristics (continued)

Table 2-19 • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays			–2 Speed		–1 Speed		Std. Speed		Units
Parameter/Description			Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Pad to Y High			2.9		3.3		3.8	ns
t_{INYL}	Pad to Y Low			2.7		3.0		3.5	ns
t_{INGH}	G to Y High			5.0		5.7		6.6	ns
t_{INGL}	G to Y Low			4.8		5.4		6.3	ns
Input Module Predicted Input Routing Delays*									
t_{IRD1}	FO = 1 Routing Delay			4.6		5.1		6.0	ns
t_{IRD2}	FO = 2 Routing Delay			5.2		5.9		6.9	ns
t_{IRD3}	FO = 3 Routing Delay			5.6		6.3		7.4	ns
t_{IRD4}	FO = 4 Routing Delay			6.5		7.3		8.6	ns
t_{IRD8}	FO = 8 Routing Delay			9.4		10.5		12.4	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.1		14.6		17.2	
t_{CKL}	Input High to Low	FO = 32		10.2		11.0		12.8	ns
		FO = 256		13.3		14.9		17.5	
t_{PWH}	Minimum Pulse Width High	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t_{PWL}	Minimum Pulse Width Low	FO = 32	5.0		5.5		6.6		ns
		FO = 256	5.8		6.4		7.6		
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 256		2.5		2.5		2.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t_P	Minimum Period	FO = 32	9.6		11.2		13.3		ns
		FO = 256	10.6		12.6		15.3		
f_{MAX}	Maximum Frequency	FO = 32		105.0		90.0		75.0	ns
		FO = 256		95.0		80.0		65.0	

Note: **These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1280A Timing Characteristics (continued)