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Precision, High Speed, Hall-Effect Angle Sensor IC with Integrated Diagnostics for Safety-Critical Applications

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position, rotational speed, and direction measurement
  - □ Capable of sensing magnet rotational speeds targeting 12b effective resolution with 900 G field
  - □ Circular Vertical Hall (CVH) technology provides a single channel sensor system supporting operation across a wide range of air gaps
- Developed in accordance with ISO 26262:2011 requirements for hardware product development for use in safety-critical applications (pending assessment)
  - □ Single die version designed to meet ASIL B requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A1333 Safety Manual
  - □ Dual die version designed to meet ASIL D requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A1333 Safety Manual
- High diagnostic coverage
  - □ On-chip diagnostics include logic built-in self-test (LBIST), signal path diagnostics, and watchdogs to support safety-critical (ASIL) applications
  - □ 4-bit CRC on SPI
- On-chip EEPROM for storing factory and customer calibration parameters
  - □ Single-bit error correction, dual-bit error detection through the use of error correction control (ECC)

Continued on next page...

DESCRIPTION

The A1333 is a 360° angle sensor IC that provides contactless high-resolution angular position information based on magnetic Circular Vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing, and motor commutation (UVW) or encoder outputs (A, B, I). It also includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible end-of-line programming of calibration parameters. The A1333 is ideal for automotive applications requiring 0° to 360° angle measurements, such as electronic power steering (EPS), rotary PRNDLs, and throttle systems.

The A1333 supports customer integration into safety-critical applications.

The A1333 is available in a dual-die 24-pin eTSSOP and a single-die 14-pin TSSOP package. The packages are lead (Pb) free with 100% matte-tin leadframe plating.

PACKAGES:

24-pin eTSSOP (Suffix LP) | 14-pin TSSOP (Suffix LE)

Not to scale

Dual Independent SoCs | Single SoC

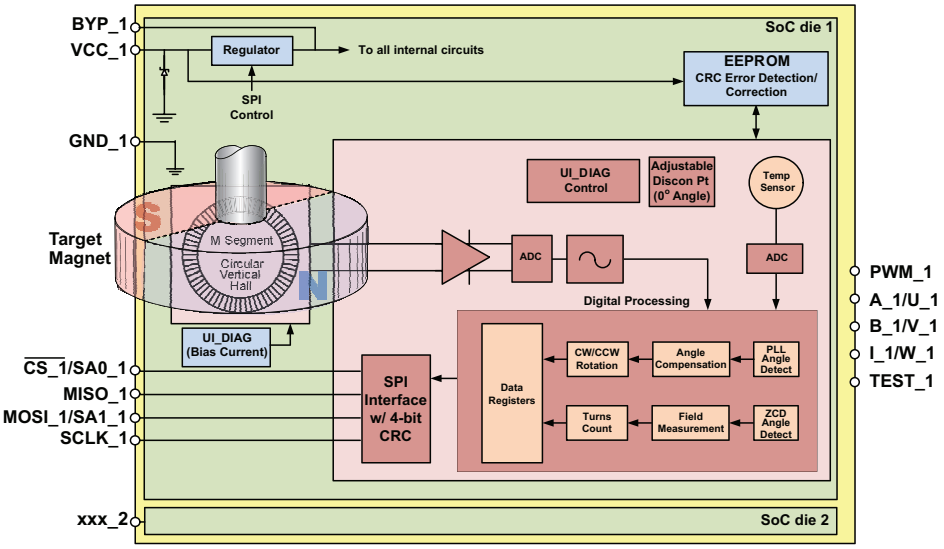

Figure 1: A1333 Magnetic Circuit and IC Diagram

FEATURES AND BENEFITS (continued)

- Supports harsh operating conditions required for automotive and industrial applications, including direct connection to 12 V battery
  - □ Operating temperature range from –40°C to 150°C
  - □ Operating supply voltage range from 4.0 to 16.5 V
    - ♦ Can support ISO 7637-2 Pulse 5b up to 39 V
- Multiple output formats supported for ease of system integration
  - □ ABI/UVW output provides high resolution, low latency, and PWM for initial position
  - □ 10 MHz SPI for low latency angle and diagnostic information; enables multiple independent ICs to be connected to the same bus
  - □ Output resolution on ABI and UVW are selectable
- Multiple programming / configuration formats supported
  - □ The system can be completely controlled and programmed over SPI, including EEPROM writes
  - □ For system with limited pins available, writing and reading can be performed over VCC and PWM pins. This allows configuring the EEPROM in production line for a device with only ABI/UVW and PWM pins connected.
- Stacked dual die construction to improve die-to-die matching for systems that require redundant sensors
- Reduces magnet misalignment impact on die-to-die matching for a given magnet diameter, relative to “side-by-side” dual die orientation

SELECTION GUIDE

Part Number	System Die	Package	Packing	Interface Voltage
A1333LLPTR-DD-T	Dual	24-pin eTSSOP	4000 pieces per 13-in. reel	3.3 V
A1333LLETR-T	Single	14-pin TSSOP	4000 pieces per 13-in. reel	3.3 V
A1333LLETR-5-T	Single	14-pin TSSOP	4000 pieces per 13-in. reel	5 V

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles	26.5	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	18	V
All Other Pins Forward Voltage	V_{IN}		5.5	V
All Other Pins Reverse Voltage	V_R		0.5	V
Operating Ambient Temperature [1]	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		170	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[1] Maximum operational voltage is reduced at high ambient temperatures (T_A). See Operating Characteristics, footnote 2.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LP-24 package	69	°C/W
		LE-14 package	82	°C/W

[2] Additional thermal information available on the Allegro website.

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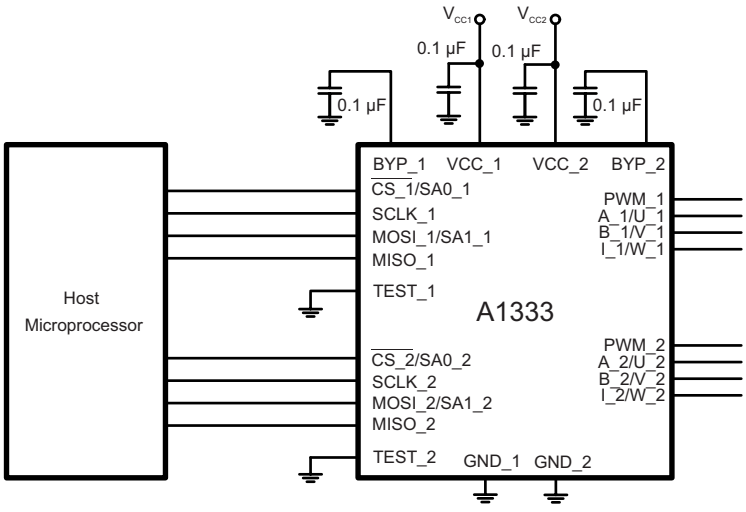


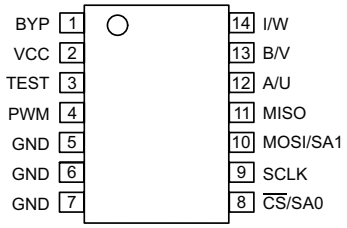
Figure 2: Typical Application Circuit

Both die are electrically separate, and may be operated simultaneously using different Power/GND sources.

PINOUT DIAGRAMS AND TERMINAL LIST TABLES

Pinout Diagram

LE 14-Pin TSSOP

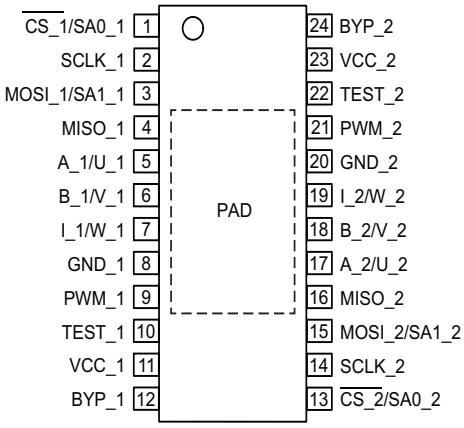


LE 14-Pin TSSOP Terminal List Table

Pin Name	Pin Number	Function
BYP	1	External bypass capacitor terminal for internal regulator
VCC	2	Power Supply / Manchester Input
TEST	3	Test pin; bring to GND
PWM	4	PWM Angle Output / Manchester Output
GND	5, 6, 7	Device ground terminal
$\overline{CS}$ /SA0	8	SPI: Chip Select terminal, active low input Manchester: LSB of ID value. Tie to BYP for “1”, GND for “0”
SCLK	9	SPI Clock terminal input
MOSI/SA1	10	SPI: Master Output, Slave Input Manchester: MSB of ID value. Tie to BYP for “1”, GND for “0”
MISO	11	SPI Master Input / Slave Output
A/U	12	Option 1: Quadrature A output signal Option 2: U (phase 1) output signal
B/V	13	Option 1: Quadrature B output signal Option 2: V (phase 2) output signal
I/W	14	Option 1: Quadrature I (index) output signal Option 2: W (phase 3) output signal

Pinout Diagram

LP 24-Pin eTSSOP



LP 24-Pin eTSSOP Terminal List Table

Pin Name	Pin Number	Function
CS_1 /SA0_1	1	SPI: Chip Select terminal, active low input (die 1) Manchester: LSB of ID value for die 1. Tie to BYP_1 for “1”, GND_1 for “0”
SCLK_1	2	SPI Clock terminal input (die 1)
MOSI_1/SA1_1	3	SPI: Master Output, Slave Input (die 1) Manchester: MSB of ID value for die 1. Tie to BYP_1 for “1”, GND_1 for “0”
MISO_1	4	SPI Master Input / Slave Output (die 1)
A_1/U_1	5	Option 1: Quadrature A output signal signal (die 1) Option 2: U (phase 1) output signal (die 1)
B_1/V_1	6	Option 1: Quadrature B output signal (die 1) Option 2: V (phase 2) output signal (die 1)
I_1/W_1	7	Option 1: Quadrature I (index) output signal (die 1) Option 2: W (phase 3) output signal (die 1)
GND_1	8	Device ground terminal (die 1)
PWM_1	9	PWM Angle Output / Manchester Output (die 1)
TEST_1	10	Test pin; bring to GND (die 1)
VCC_1	11	Power Supply / Manchester Input (die 1)
BYP_1	12	External bypass capacitor terminal for internal regulator (die 1)
CS_2/SA0_2	13	SPI: Chip Select terminal, active low input (die 2) Manchester: LSB of ID value for die 2. Tie to BYP_2 for “1”, GND_2 for “0”
SCLK_2	14	SPI Clock terminal input (die 2)
MOSI_2/SA1_2	15	SPI: Master Output, Slave Input (die 2) Manchester: MSB of ID value for die 2. Tie to BYP_2 for “1”, GND_2 for “0”
MISO_2	16	SPI Master Input / Slave Output (die 2)
A_2/U_2	17	Option 1: Quadrature A output signal (die 2) Option 2: U (phase 1) output signal (die 2)
B_2/V_2	18	Option 1: Quadrature B output signal (die 2) Option 2: V (phase 2) output signal (die 2)
I_2/W_2	19	Option 1: Quadrature I (index) output signal (die 2) Option 2: W (phase 3) output signal (die 2)
GND_2	20	Device ground terminal (die 2)
PWM_2	21	PWM Angle Output / Manchester Output (die 2)
TEST_2	22	Test pin; bring to GND (die 2)
VCC_2	23	Power Supply / Manchester Input (die 2)
BYP_2	24	External bypass capacitor terminal for internal regulator (die 2)
PAD	PAD	Exposed pad for thermal dissipation

OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage [2]	V_{CC}	Customer supply	4.0	–	16.5	V
Supply Current	I_{CC}	One die, sampling angles	–	17	19	mA
Undervoltage Flag Threshold [3]	V_{UVD}	dV/dt = 1 V/ms, A1333 sampling enabled, T_A = 25°C	3.6	–	3.9	V
Supply Zener Clamp Voltage	V_{ZSUP}	I_{CC} = I_{CC} + 3 mA, T_A = 25°C	26.5	–	–	V
Reverse Battery Current	I_{RCC}	V_{RCC} = 18 V, T_A = 25°C	–	–	5	mA
Power-On Time [4]	t_{PO}	Power-on diagnostics disabled	–	15	–	ms
	t_{PO_D}	Power-on time; CVH self-test and LBIST enabled	–	45	–	ms
Bypass Pin Output Voltage [5]	V_{BYP}	T_A = 25°C, C_{BYP} = 0.1 µF, 3.3 V interface	2.97	3.3	3.63	V
		T_A = 25°C, C_{BYP} = 0.1 µF, 5.0 V interface enabled and V_{CC} ≥ 5.0 V	4.0	5.0	5.5	V
SPI AND ABI (UVW) ELECTRICAL SPECIFICATIONS (3.3 V INTERFACE)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Output High Voltage	V_{OH}	MISO, ABI/UVW pins, C_L = 20 pF	2.93	3.3	3.63	V
Output Low Voltage	V_{OL}	MISO, ABI/UVW pins, C_L = 20 pF	–	0.3	–	V
SPI AND ABI (UVW) ELECTRICAL SPECIFICATIONS (5.0 V INTERFACE)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Output High Voltage	V_{OH}	MISO, ABI/UVW pins, C_L = 20 pF, V_{CC} ≥ 5.0 V	4	5	5.5	V
Output Low Voltage	V_{OL}	MISO, ABI/UVW pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency [6]	f_{SCLK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [6]	D_{fSCLK}	SPI_{CLKDC}	40	-	60	%
SPI Frame Rate [6]	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge [6]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [6]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [6]	t_{DAV}	Data output valid after SCLK falling edge	–	30	–	ns
MOSI Setup Time [6]	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time [6]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time [6]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [6]	C_L	Loading on digital output (MISO) pin	–	–	20	pF

Continued on the next page…

OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

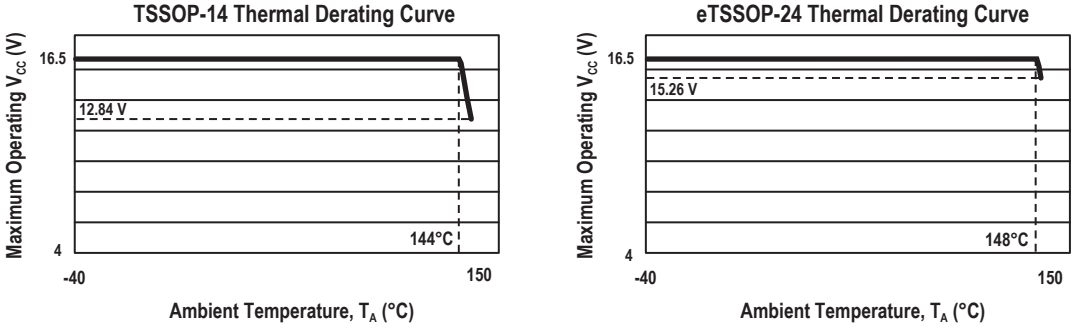
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency	f_{PWM}	PWM Frequency Min Setting	–	98	–	Hz
		PWM Programmable Options (7 bits)	–	128	–	options
		PWM Frequency Max Setting	–	3.125	–	kHz
PWM Output Low Clamp	$D_{PWM(min)}$	Corresponding to digital angle of 0x000	–	5	–	%
PWM Output High Clamp	$D_{PWM(max)}$	Corresponding to digital angle of 0xFFF	–	95	–	%
INCREMENTAL OUTPUT, ABI (UVW) SPECIFICATIONS						
ABI and UVW Output Angular Hysteresis [6]	hys_{ANG}	Programmable via EEPROM (6 bits)	0	–	1.38	degrees
AB Channel Resolution [6]	RES_{AB}	Programmable via EEPROM, 4 bit field. Specified in pulses per revolution, PPR	1	–	2048	PPR
AB Quadrature Resolution [6]	RES_{AB_INT}	Equal to 4 × RES_{AB}, specified in counts per revolution, CPR	4	–	8192	CPR
UVW Pole Pairs [6]	N_{pole}	DC commutation signals. Programmable via EEPROM, 4-bit field.	1	–	16	pole pairs
MANCHESTER INTERFACE SPECIFICATIONS						
Manchester High Voltage	$V_{MAN(H)}$	Applied to VCC line	7.3	8	$V_{CC(max)}$	V
Manchester Low Voltage	$V_{MAN(L)}$	Applied to VCC line	$V_{CC(min)}$	5	5.7	V
Manchester Bit Rate	f_{MAN}	Line state changes once or twice per bit; maximum speed is usually limited by VCC line capacitance	2.2	–	100	kbit/s
BUILT-IN SELF TEST						
Logic BIST Time	t_{LBIST}	Configurable to run on power-up or on user request. Runs in parallel with CVH self-test (if enabled).	–	30	–	ms
Circular Vertical Hall Self-Test Time	t_{CVHST}	Configurable to run on power-up or on user request. Runs in parallel with LBIST (if enabled).	–	30	–	ms

Continued on the next page…

OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
MAGNETIC CHARACTERISTICS						
Magnetic Field	B	Range of input field	–	–	1200	G
ANGLE CHARACTERISTICS						
Output [7]	RES_{ANGLE}	Both 12 and 15 bit angle values are available via SPI	–	12/15	–	bit
Angle Refresh Rate [8]	t_{ANG}	ORATE = 0	–	1.0	–	µs
Response Time [6]	$t_{RESPONSE}$	Angular Latency; valid for ABI or UVW interface; ORATE = 0	–	10	–	µs
Angle Error	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.0	±0.4	+1.0	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.3	±0.6	+1.3	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 150°C, B = 300 G, angle change from 25°C	–1.4	–	1.4	degrees
		T_A = –40°C, B = 300 G, angle change from 25°C	–	0.9	–	degrees
Angle Noise [9]	N_{ANG}	T_A = 25°C, B = 300 G, no internal filtering, target rpm = 0, 3 sigma noise	–	±0.19	–	degrees
		T_A = 150°C, no internal filtering, B = 300 G, target rpm = 0, 3 sigma noise	–	±0.25	–	degrees
Effective Resolution [10]		B = 300 G, T_A = 25°C	–	12.5	–	bits
Angle Drift Over Lifetime [11]	$ANGLE_{Drift\_Life}$	B = 300 G, average maximum drift observed following AEC-Q100 qualification testing	–	0.5	–	degrees

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Maximum operational voltage is reduced at high ambient temperatures (T_A). See plots below.



[3] Undervoltage flag indicates V_{CC} level below expected operational range. Degraded sensor accuracy may result.
[4] During the power-on phase, the A1333 SPI transactions will be valid within ≈ 300 µs of power on (with no self-tests). Angle reading requires full t_{PO} to stabilize.
[5] The output voltage specification is to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during normal operation.
[6] Parameter is not guaranteed at final test. Determined by design.
[7] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.
[8] The rate at which a new angle reading will be ready.
[9] This value represents 3-sigma or three times the standard deviation of the measured samples.
[10] Effective Resolution is calculated using the formula below:

$$log_2(360) - log_2\left(\frac{1}{n}\sum_{i=1}^{n}\sigma_i\right)$$

where σ is the Standard Deviation based on thirty averaged measurements taken at each of the 32 angular positions, I = 11.25, 22.5, … 360.
[11] Maximum observed angle drift following AEC-Q100 stress was 1.37 degrees.

TYPICAL PERFORMANCE CHARACTERISTICS

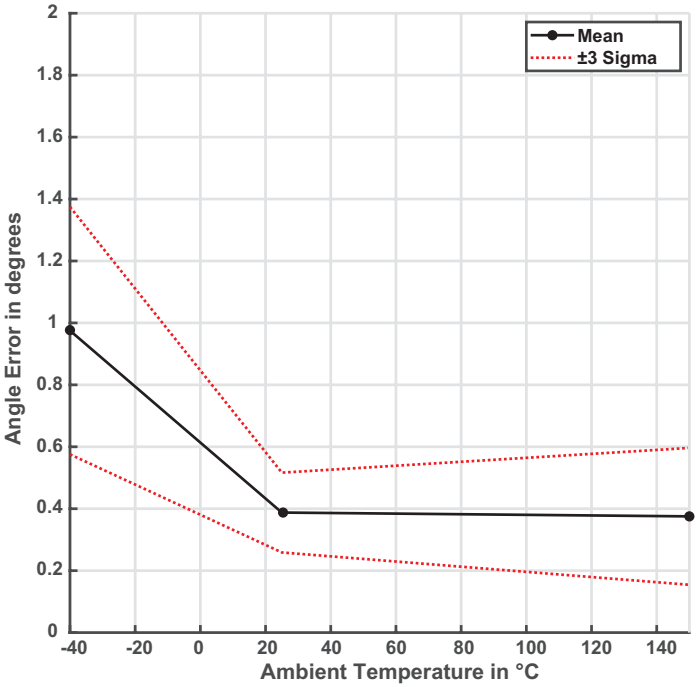


Figure 3: Peak Angle Error over Temperature (300 G)

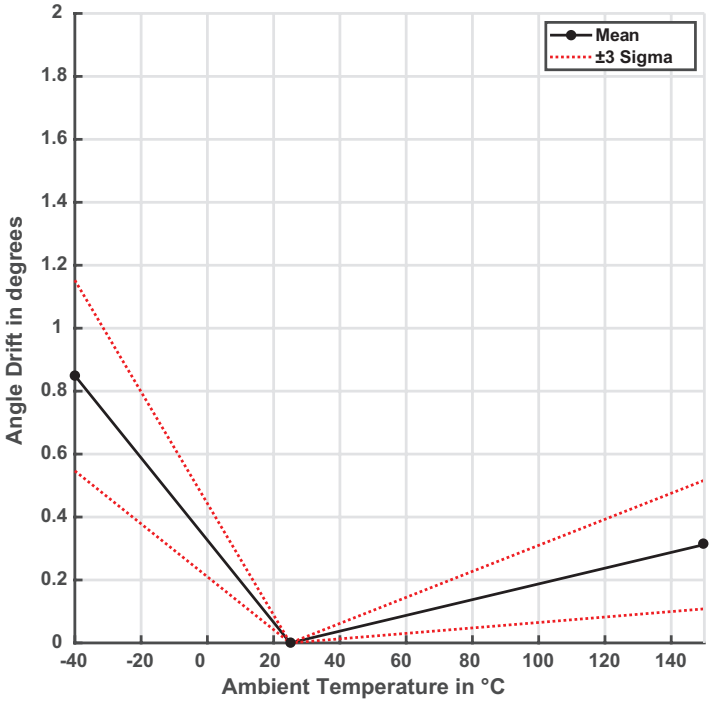


Figure 4: Maximum Absolute Drift from 25°C Reading (300 G)

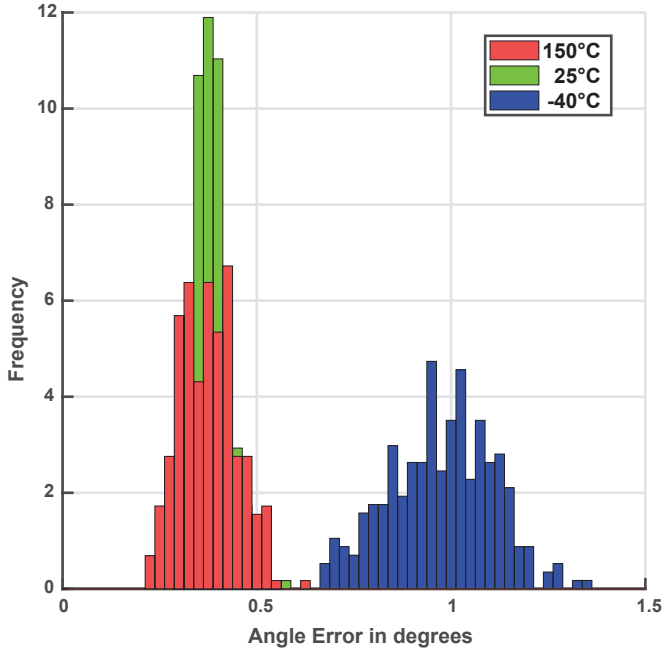


Figure 5: Peak Angle Error Distributions over Temperature (300 G)

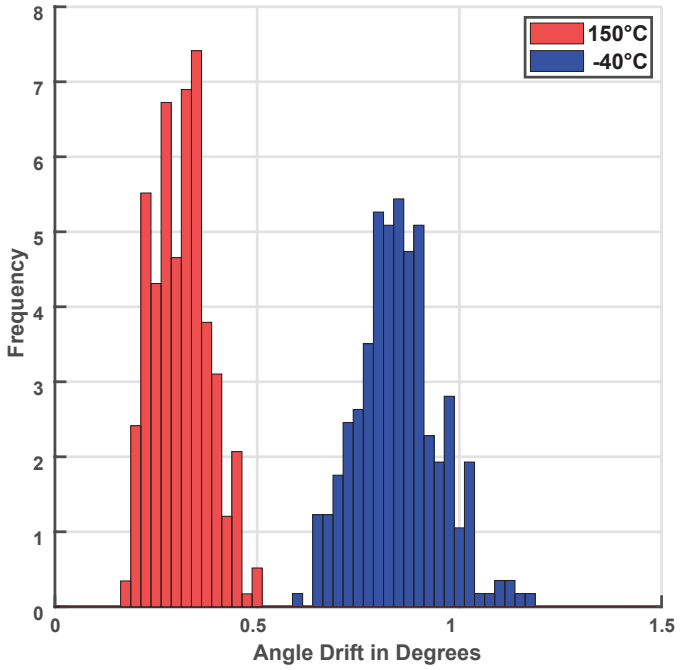


Figure 6: Angle Drift from 25°C (300 G)

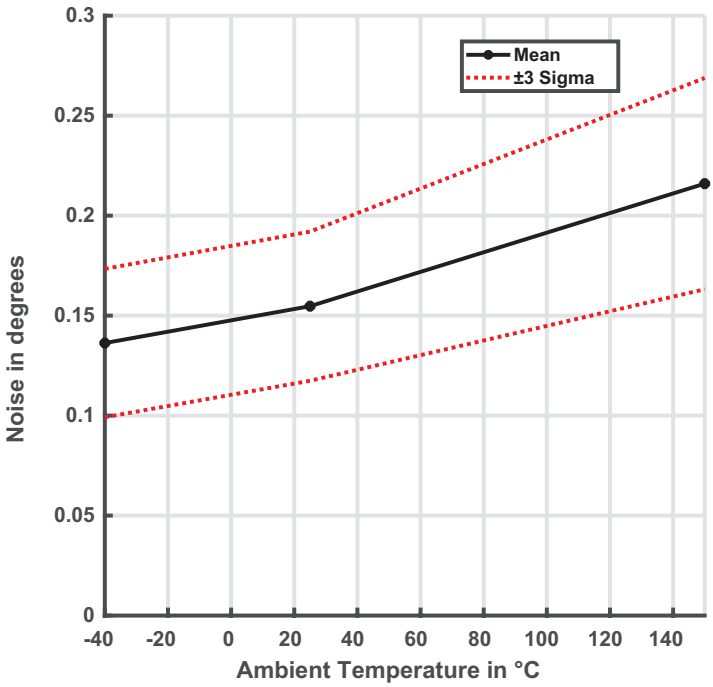


Figure 7: Noise Performance over Temperature (3 Sigma, 300 G)

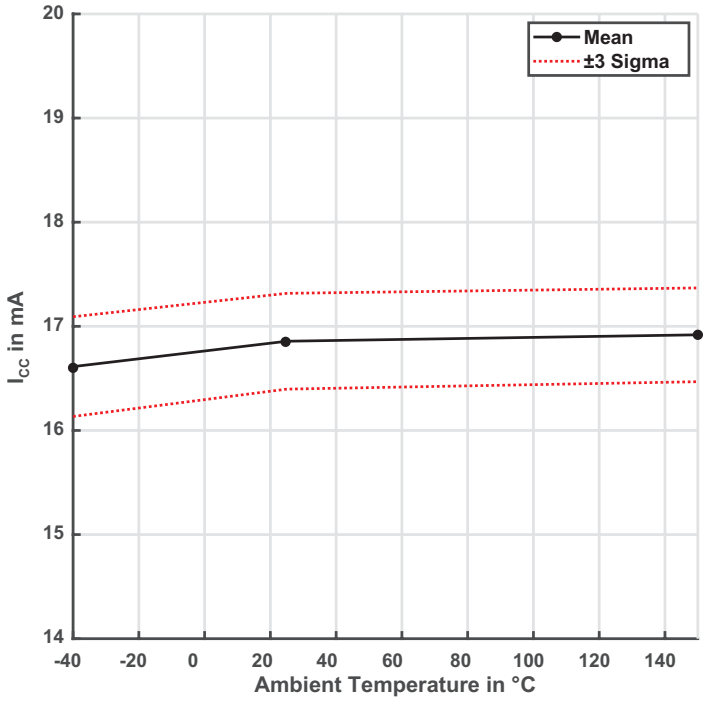


Figure 8: I_{CC} over Temperature (V_{CC} = 16.0 V)

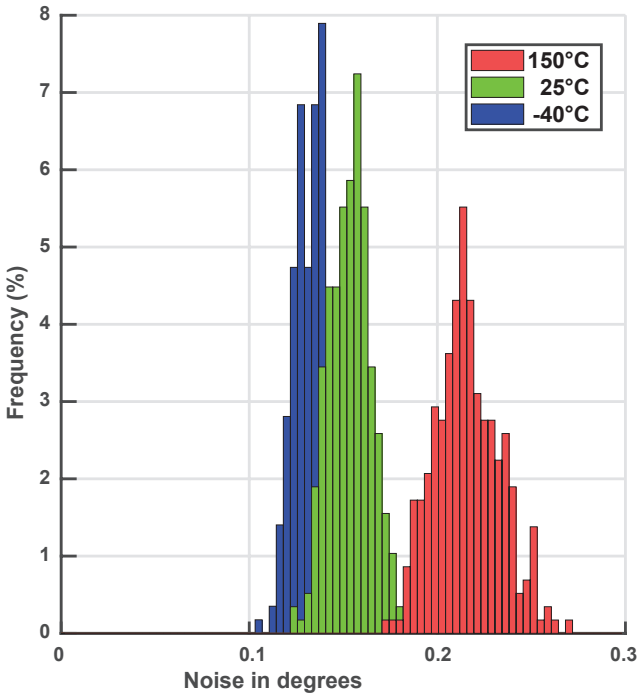


Figure 9: Noise Distribution over Temperature (3 Sigma, 300 G)

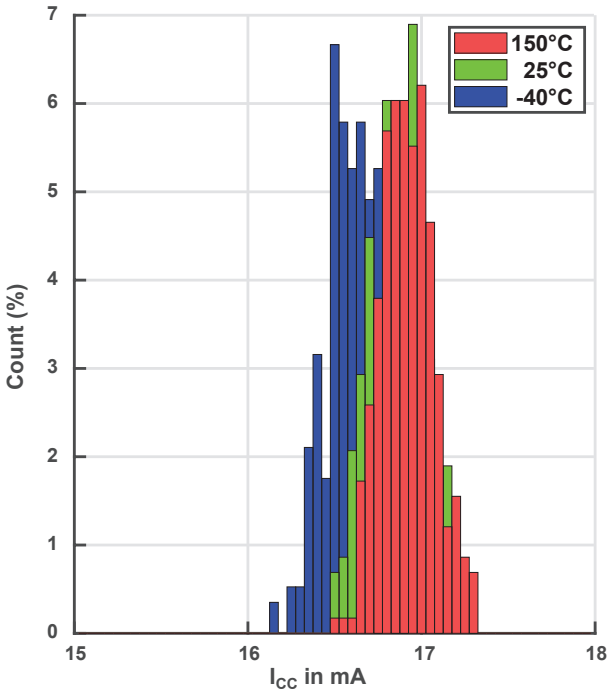


Figure 10: I_{CC} Distribution over Temperature (V_{CC} = 16.0 V)

FUNCTIONAL DESCRIPTION

Overview

The A1333 is a rotary position Hall-sensor-based device in a surface-mount package, providing solid-state consistency, reliability, and supporting a wide variety of automotive applications. The Hall-sensor-based device measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device) and computes an angle measurement based on the actual physical reading, as well as any internal parameters that have been set by the user. The output is used by the host microcontroller to provide a single channel of target data.

This device is an advanced, programmable system-on-chip (SoC). Each integrated circuit includes a Circular Vertical Hall (CVH) analog front end, a high-speed sampling A-to-D converter, digital filtering, digital signal processing (which includes two separate signal paths), SPI, PWM, motor commutation outputs (UVW), and encoder outputs (A, B, I).

Offset, filtering, and diagnostic adjustment options are available in the A1333. These options can be configured in onboard EEPROM, providing a wide range of sensing solutions in the same device. Device performance can be optimized by enabling individual functions or disabling them in EEPROM to minimize latency.

Angle Measurement

The IC features two digital signal paths. The main signal path uses a PLL to generate high resolution, low latency angle readings. A secondary, lower power signal path (referred to as the "ZCD path") is used for turns counting, magnetic field measurement, and diagnostic comparison.

The A1333 can monitor the angular position of a rotating magnet at speeds ranging from 0 to more than 15,000 rpm.

The A1333 has a typical refresh rate of 1 MHz.

Angle is represented as either a 12- or 15-bit value, based on the register address accessed.

12 Bit Angle Value; Serial register 0x20

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	EF	UV	P	angle(11:0)											

15 Bit Angle Value; Serial Register 0x32

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	angle(14:0)														

When reading the 12-bit angle value, 3 additional status bits are provided with each packet: a general error flag (EF), undervoltage flag (UV), and a parity bit (P).

PWM output is always resolved to a 12-bit angle value. ABI/UVW operates on a 15-bit angle representation.

The zero degree position may be adjusted by writing to EEPROM.

The sensor readout is processed in various steps. These are detailed in Figure 13.

System Level Timing

Internal registers are updated with a new angle value every t_{ANG}. Due to signal path delay, the angle is $t_{RESPONSE}$ old at each update. In other words, $t_{RESPONSE}$ is the delay from time of magnet sampling until generation of a processed angle value. SPI, which is asynchronously clocked, results in a varying latency depending on sampling frequency and SCLK speed. The values which are presented to the user are latched on the first SCLK edge of the SPI response frame. This results in a variable age of the angle data, ranging from $t_{RESPONSE} + t_{SPI}$ to $t_{RESPONSE} + t_{ANG} + t_{SPI}$, where t_{SPI} is the length of a read response packet, and t_{ANG} is the update rate of the angle register.

Similar to SPI, when using the PWM output, the output packet is not synchronized with the internal update rate of the sensor. The angle is latched at the beginning of the carrier frequency period (effectively at the rising edge of the PWM output). Because of this, the age of the angle value, once read by the system microcontroller, may be up to $t_{RESPONSE} + t_{ANG} + 1/f_{PWM}$.

Figure 12 shows the update rate and the signal delay of the different angle output paths depending on sensor settings.

The value of the "angle_zcd" (ZCD signal path) register is updated approximately every 32 µs. The field strength reading (register 0x2A) is updated approximately every 128 µs.

Impact of High Speed Sensing

Due to signal path latency, the angle information is delayed by $t_{RESPONSE}$. This delay equates to a greater angle value as the rotational velocity increases (i.e. a magnet rotating at 20,000 rpm traverses twice as much angular distance in a fixed time period as a magnet rotating at 10,000 rpm), and is referred to as angular lag.

The lag is directly proportional to rpm, and may be compensated for externally, if the velocity is known.

Angular lag can be expressed using the following equation:

$$Ang\_Lag = \frac{rpm \times 6}{1{,}000{,}000} \times t_{RESPONSE}$$

where *rpm* represents the rotational velocity of the magnet, *Angle_Lag* is expressed in degrees, and $t_{RESPONSE}$ is in µs.

Figure 11 depicts the typical angular lag over rpm.

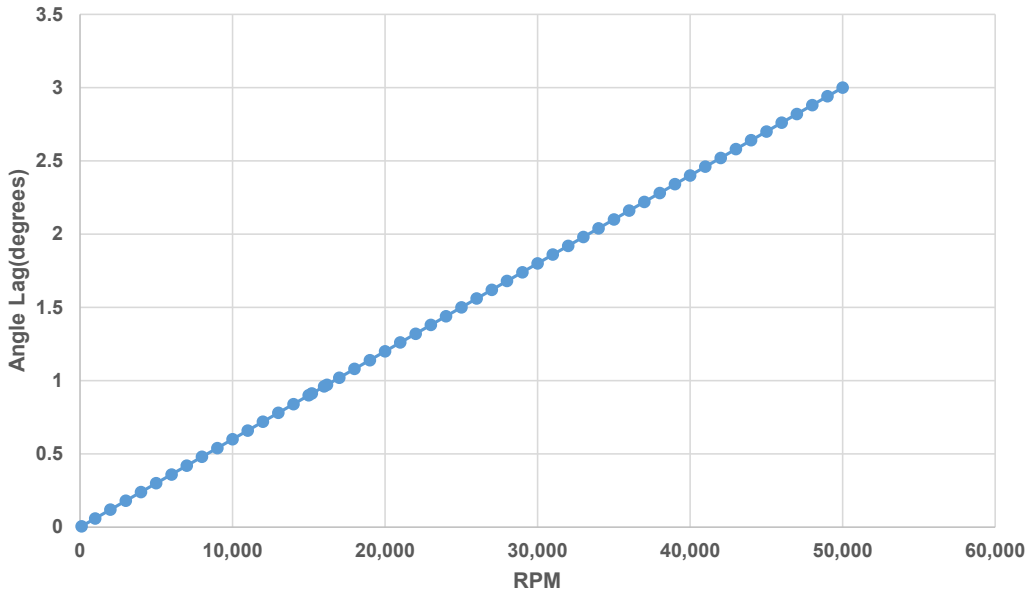


Figure 11: Angle Lag vs. RPM (10 µs Response Time)

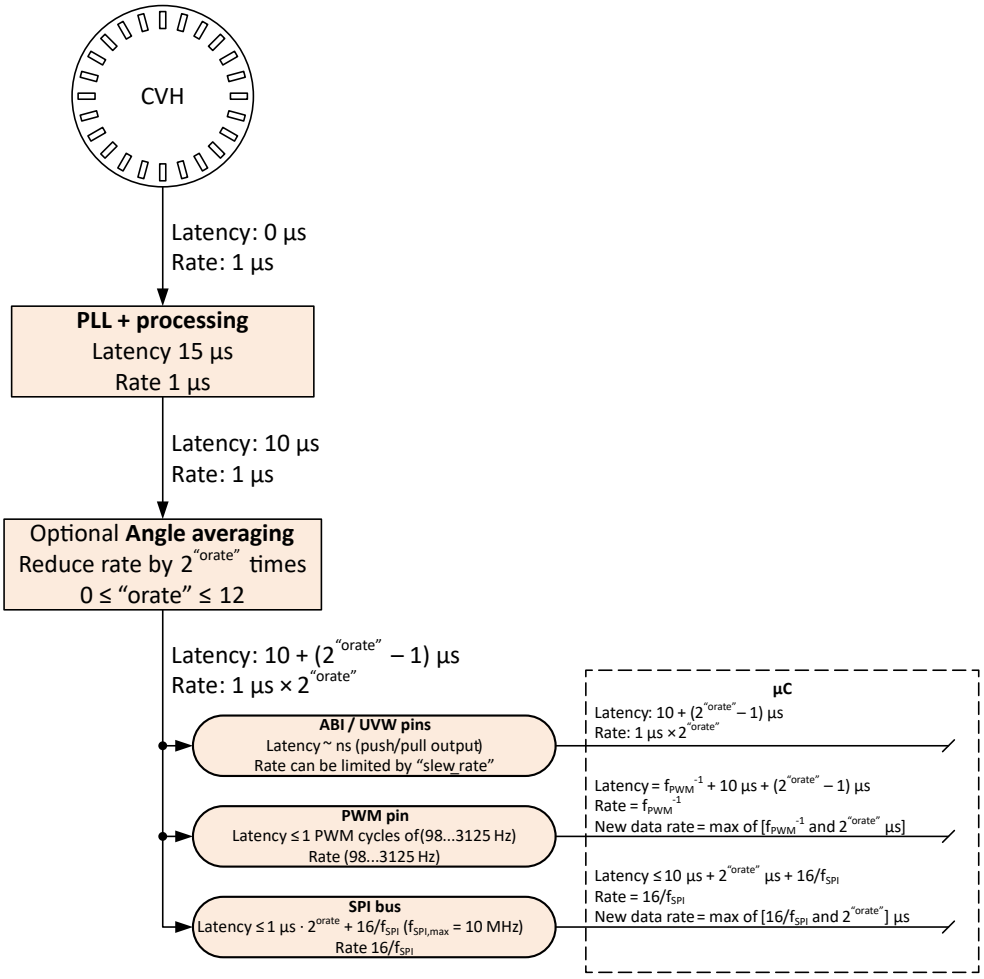


Figure 12: Update Rate and Signal Delay

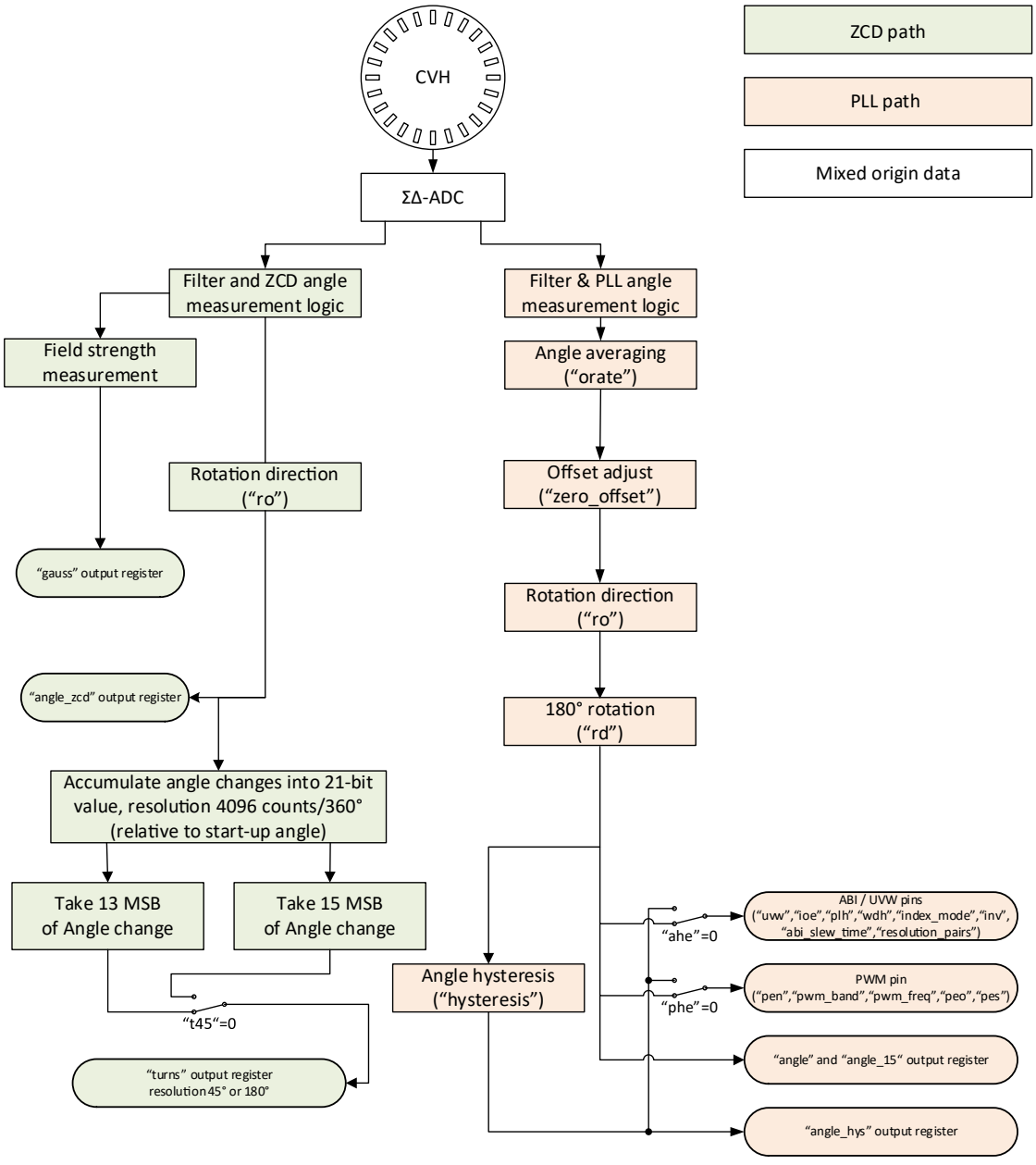


Figure 13: Angle Measurement – Sensor Readout Steps

Names in quotes correspond to EEPROM or serial register fields.

Power-Up

Upon applying power to the A1333, the device automatically runs through an initialization routine. The purpose of this initialization is to ensure that the device comes up in the same predictable operating condition every power cycle. This initialization routine takes time to complete, which is referred to as Power-On Time, t_{PO}. Regardless of the state of the device before a power cycle, the device will re-power with the shadow memory contents copied from the EEPROM anew, and serial registers in their default states. For example, on every power-up, the device will power with the "zero_offset" that was stored in the EEPROM. The extended write access field "write_adr" will be set back to its default value, zero.

PWM Output

The A1333 provides a pulse-width-modulated open-drain output, with the duty cycle (DC) proportional to measured angle. The PWM duty cycle is clamped at 5% and 95% for diagnostics purposes. A 5% DC corresponds to 0°; a 95% DC corresponds to 360°.

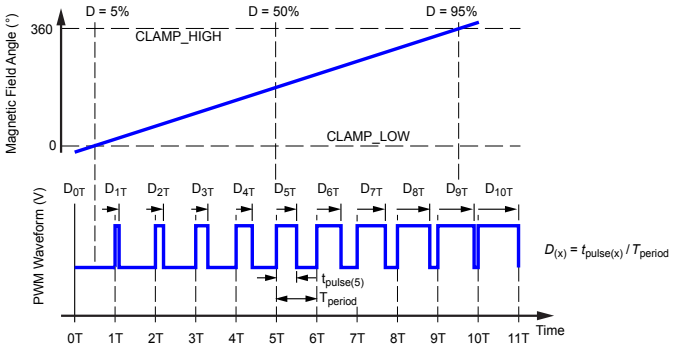


Figure 14: PWM Mode Outputs a Duty-Cycle Proportional To Sensed Angle

Within each cycle, the output is high for the first 5% and low for the last 5% of the period. The middle 90% of the period is a linear interpolation of the angle as sampled the start of the PWM period.

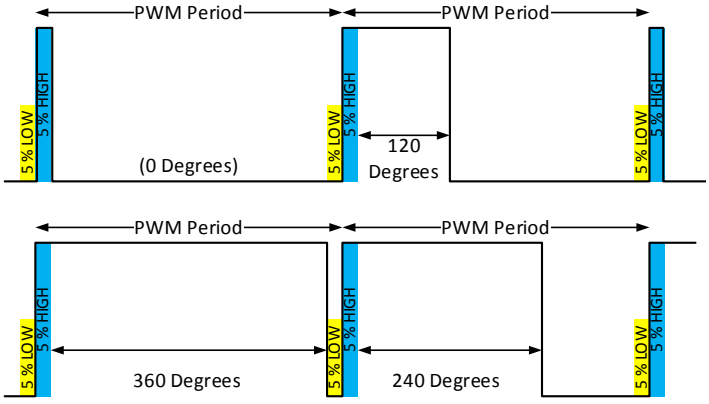


Figure 15: Pulse-Width Modulation (PWM) Examples

The angle is represented in 12-bit resolution and can never reach 360°. The maximum duty cycle high period is:

$$\text{DutyCycleMax (\%)} = (4095 / 4096) \times 90 + 5 \ .$$

PWM CARRIER FREQUENCY

The PWM carrier frequency is controlled via two EEPROM fields, both of which are found in the PWS row.

- PWM_FREQ
- PWM_BAND

Together, these two fields allow 128 different PWM carrier frequencies to be selected.

Table 1: PWM Carrier Frequencies in Hz

		PWM_BAND							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PWM_FREQ	**0**	3125	2778	2273	1667	1087	641	352	185
	1	3101	2740	2222	1613	1042	610	333	175
	2	3077	2703	2174	1563	1000	581	316	166
	3	3053	2667	2128	1515	962	556	301	157
	4	3030	2632	2083	1471	926	532	287	150
	5	3008	2597	2041	1429	893	510	275	143
	6	2985	2564	2000	1389	862	490	263	137
	7	2963	2532	1961	1351	833	472	253	131
	8	2941	2500	1923	1316	806	455	243	126
	9	2920	2469	1887	1282	781	439	234	121
	10	2899	2439	1852	1250	758	424	225	116
	11	2878	2410	1818	1220	735	410	217	112
	12	2857	2381	1786	1190	714	397	210	108
	13	2837	2353	1754	1163	694	385	203	105
	14	2817	2326	1724	1136	676	373	197	101
	15	2797	2299	1695	1111	658	362	191	98

Incremental Output Interface (ABI)

The A1333 offers an incremental output mode in the form of quadrature A/B and Index outputs to emulate an optical or mechanical encoder. The A and B signals toggle with a 50% duty cycle (relative to angular distance, not necessarily time) at a frequency of 2^N cycles per magnetic revolution, giving a cycle resolution of $(360 / 2^N)$ degrees per cycle. B is offset from A by ¼ of the cycle period. The "I" signal is an index pulse that occurs once per revolution to mark the zero (0) angle position. One revolution is shown below:

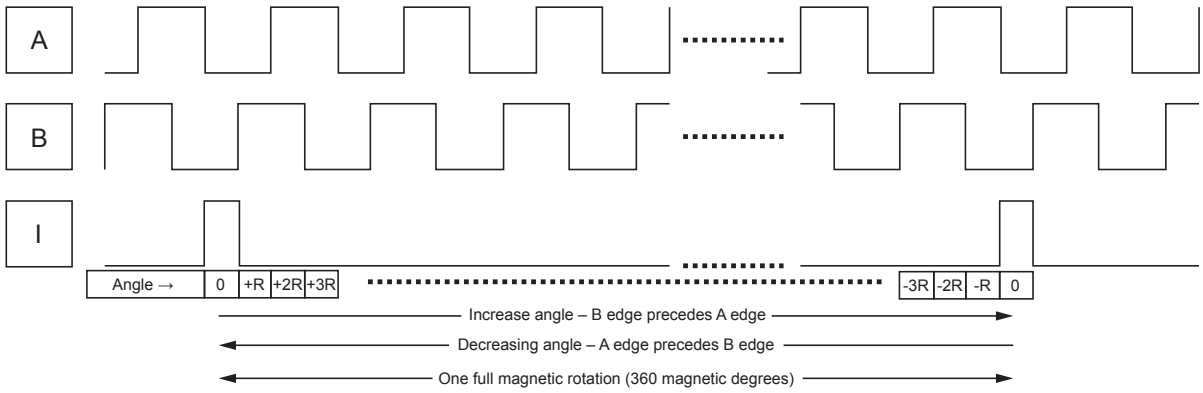


Figure 16: One Full Magnetic Revolution

Since A and B are offset by ¼ of a cycle, they are in *quadrature* and together have four unique states per cycle. Each state represents $R = [360 \div (4 \times 2^N)]$ degrees of the full revolution. This angular distance is the quadrature resolution of the encoder. The order in which the states change, or the order of the edge transitions from A to B, allow the direction of rotation to be determined. If a given B edge (rising/falling) precedes the following A edge, the angle is increasing from the perspective of the electrical (sensor) angle and the angle position should be incremented by the quadrature resolution (R) at each state transition. Conversely, if a given A edge precedes the following B edge, the angle is decreasing from the perspective of the electrical (sensor) angle and the angle position should be decremented by the quadrature resolution (R) at each state transition. The angle position accumulator wraps each revolution back to 0.

The quadrature states are designated as Q1 through Q4 in the following diagrams, and are defined as follows:

State Name	A	B
Q1	0	0
Q2	0	1
Q3	1	1
Q4	1	0

Note that the A/B progression is a grey coding sequence where only one signal transitions at a time. The state progression must be as follows to be valid:

Increasing angle: Q1 → Q2 → Q3 → Q4 → Q1 → Q2 → Q3 → Q4

Decreasing angle: Q4 → Q3 → Q2 → Q1 → Q4 → Q3 → Q2 → Q1

The duration of one cycle is referred to as 360 *electrical degrees*, or 360e. One half of a cycle is therefore 180e and one quarter of a cycle (one quadrature state, or R degrees) is 90e. This is the terminology used to express variance from perfect signal behavior. Ideally the A and B cycle would be as shown below for a constant velocity:

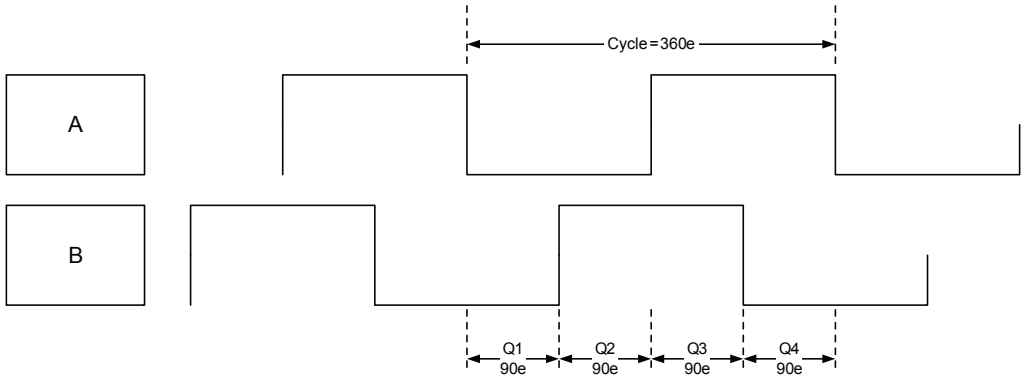


Figure 17: Electrical Cycle

In reality, the edge rate of the A and B signals, and the switching threshold of the receiver I/Os, will affect the quadrature periods:

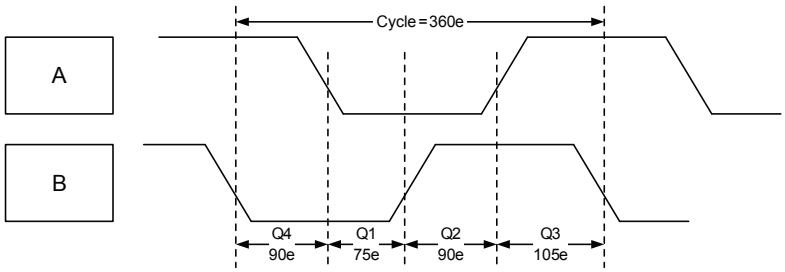


Figure 18: Electrical Cycle

Here, an exaggeration of the switching thresholds shows that Q4 and Q2, which are fall-fall and rise-rise, have the expected 90e period, whereas Q1 is less than expected and Q3 is greater than expected due to imbalance in switching thresholds.

ABI RESOLUTION

The A1333 supports the following ABI output resolutions. This is set via the "resolution_pairs" field in EEPROM and shadow (EEPROM 0x19, bits 3:0).

ABI INVERSION

The logic levels of the ABI pins may inverted by setting the ABI.inv bit within EEPROM. This also applies if using the UVW output logic.

Table 2: ABI Output Resolution

EEPROM Resolution Field	Cycle Resolution (Bits = N)	Quadrature Resolution (Bits = 4 × N)	Cycles per Revolution (A or B)	Quadrature States per Revolution	Cycle Resolution (Degrees)	Quadrature Resolution (R) (Degrees)
0	Factory Use Only					
1	Factory Use Only					
2	Factory Use Only					
3	11	13	2048	8192	0.176	0.044
4	10	12	1024	4096	0.352	0.088
5	9	11	512	2048	0.703	0.176
6	8	10	256	1024	1.406	0.352
7	7	9	128	512	2.813	0.703
8	6	8	64	256	5.625	1.406
9	5	7	32	128	11.250	2.813
10	4	6	16	64	22.500	5.625
11	3	5	8	32	45.000	11.250
12	2	4	4	16	90.000	22.5
13	1	3	2	8	180.0	45.0
14	0	2	1	4	360.0	90.0
15	n/a	n/a	n/a	n/a	n/a	n/a

INDEX PULSE

The index pulse I (or Z in some descriptions) marks the absolute zero (0) position of the encoder. Under rotation, this allows the receiver to synchronize to a known mechanical/magnetic position, and then use the incremental A/B signals to keep track of the absolute position. To support a range of ABI receivers, the 'I' pulse has four widths, defined by the INDEX_MODE EEPROM field, as shown below:

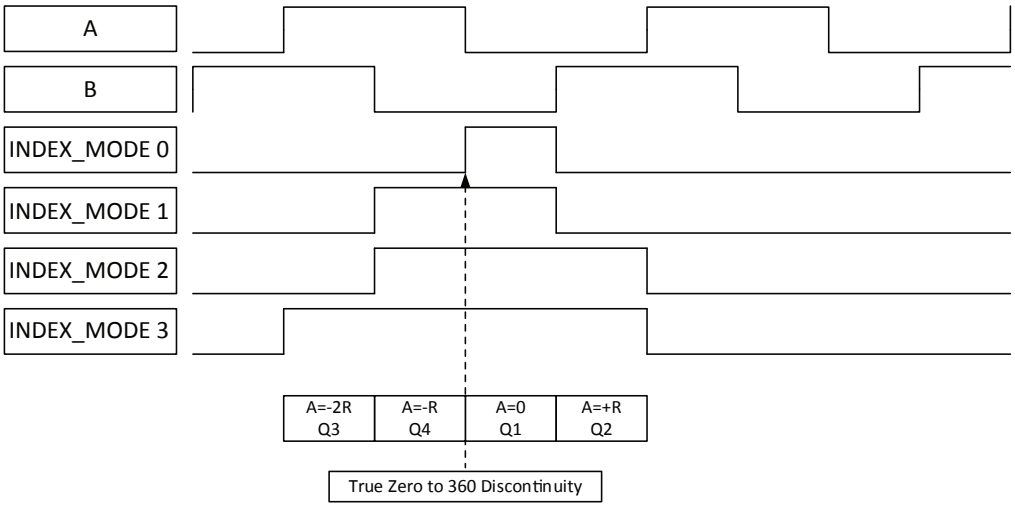


Figure 19: Index Pulse

The edge of the index pulse corresponding to the "Zero" position, as observed by the sensor, will change based on rotation direction, as shown in Figure 20.

With the magnet rotating such that the observed angle is increasing, the 0° position will be indicated by the rising edge of the Index pulse. If the magnet is rotated in the opposite direction (or the RO bit is changed in EEPROM) to produce a decreasing angle value, the 0° position will be represented by the falling edge of the Index pulse.

The ABI resolution and I pulse mode selection (described above) determine the width of the Index pulse and the corresponding shift in zero position indication.

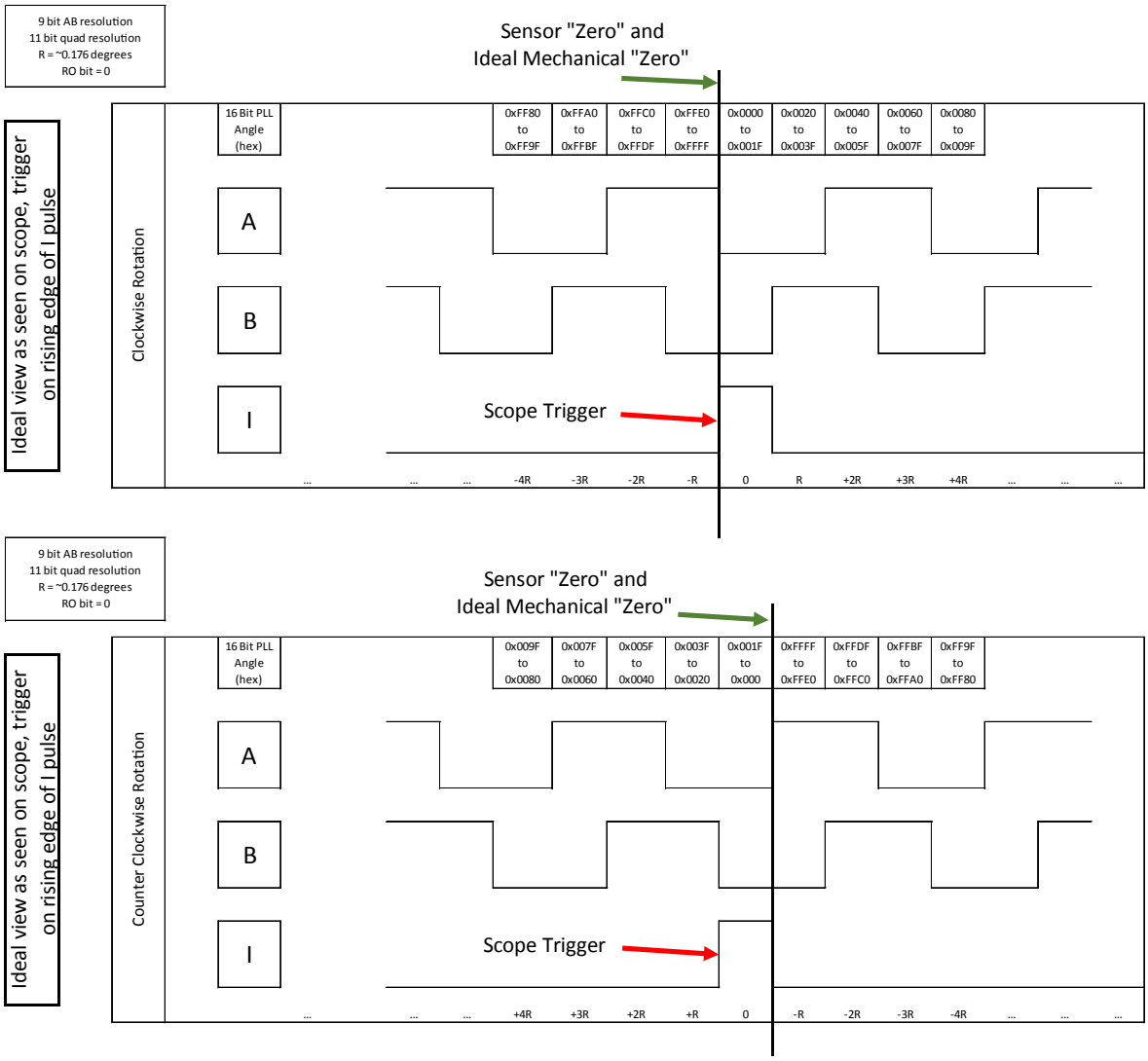


Figure 20: Index Pulse Corresponding to "Zero" Position

SLEW RATE LIMITING FOR ABI

Slew rate limiting is enabled when the "abi_slew_limit" field is non-zero. This option separates the sample update rate from the ABI output rate, and can be used to control two circumstances:

- The angle sample does not monotonically increase or decrease at the quadrature resolution, thereby "skipping" one or more quadrature states. In this case, the slew rate limiting logic transitions the ABI signals in the required valid sequence, at the slew rate, until the ABI output "catches up" with the angle samples, at which point the normal sample rate output resumes. This skipping will most likely occur either at very low velocities, if the noise is high, or at very high velocities when the angle changes more than the quadrature resolution in one angle sample period.
- The ABI receiver at the host end cannot reliably detect edge transitions that are spaced at the sample rate of 1 µs. The slew limit time can be set greater than the nominal angle sample update period, providing the velocity of the angle rotation would not on average require ABI transitions greater than the angle sample rate.

In both cases, the ABI output will correctly track the rotation position; however, the speed of the ABI edges will be accomplished at the slew rate limit set in EEPROM. Whenever slew rate limiting occurs, the SRW flag in the WARN serial register will assert informing the system of the occurrence.

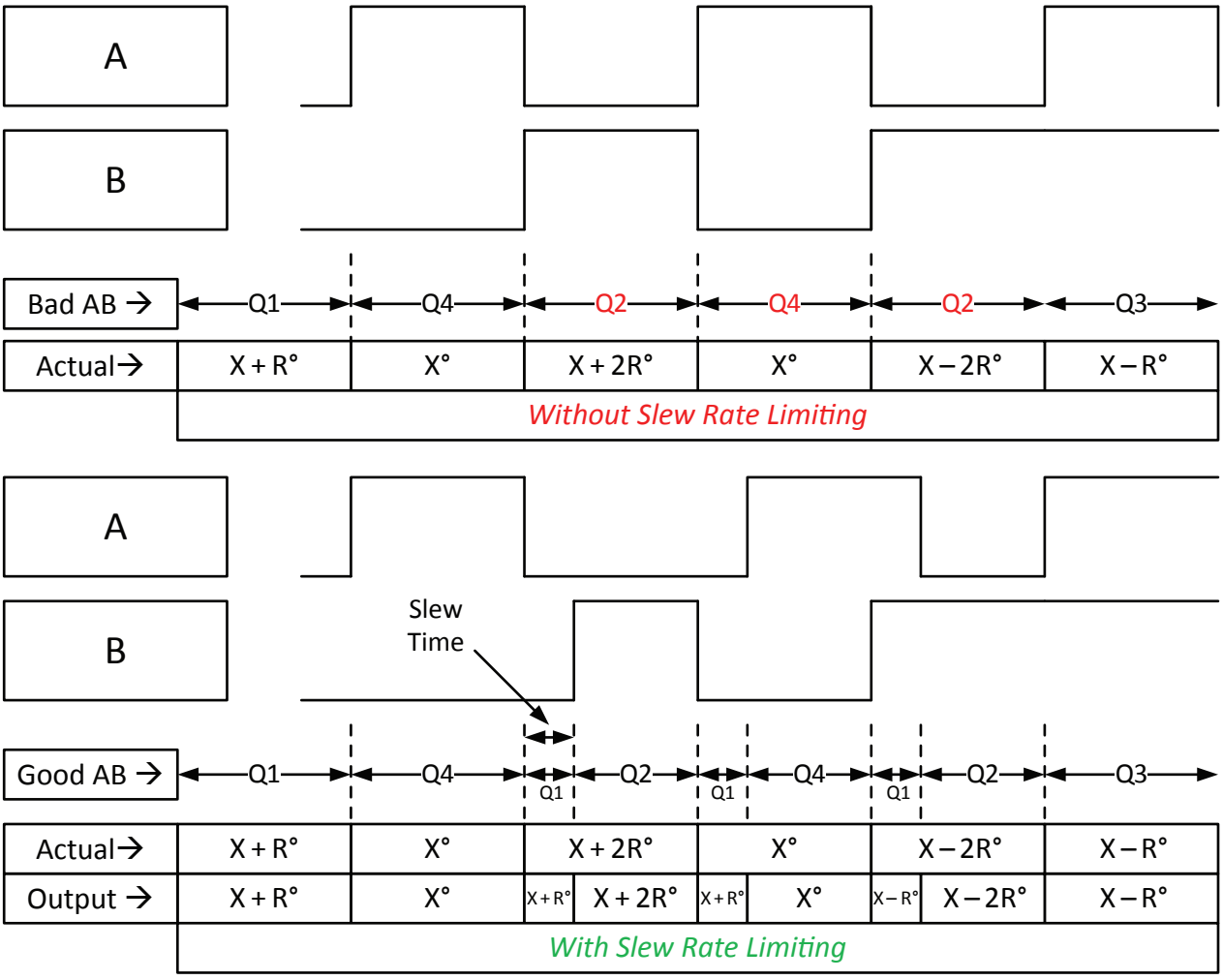


Figure 21: Slew Rate Limiting

Brushless DC Motor Output (UVW)

The A1333 offers U, V, and W signals for stator commutation of brushless DC (BLDC) motors. The device is mode-selectable for 1 to 16 pole-pairs. The BLDC signals (U, V, and W), are generated based on the quantity of pole-pairs and on angle information from the angle sensor. The U, V, and W outputs switch when the measured mechanical angle crosses the value where a change should occur. If hysteresis is used, then the output update method is different. The output behavior when hysteresis is enabled is described in the Angle Hysteresis section. Figure 22 and Figure 23 below show the UVW waveforms for three and five pole-pair BLDC motors.

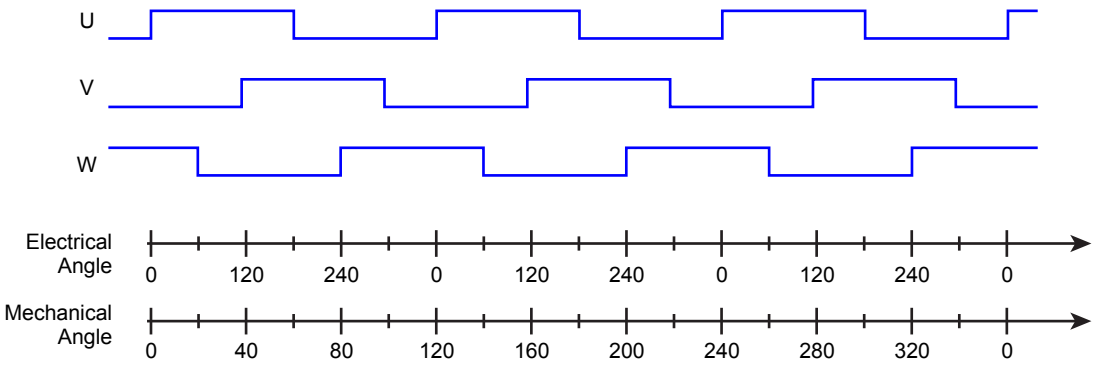


Figure 22: U, V, W Outputs for Three Pole-Pair BLDC Motor

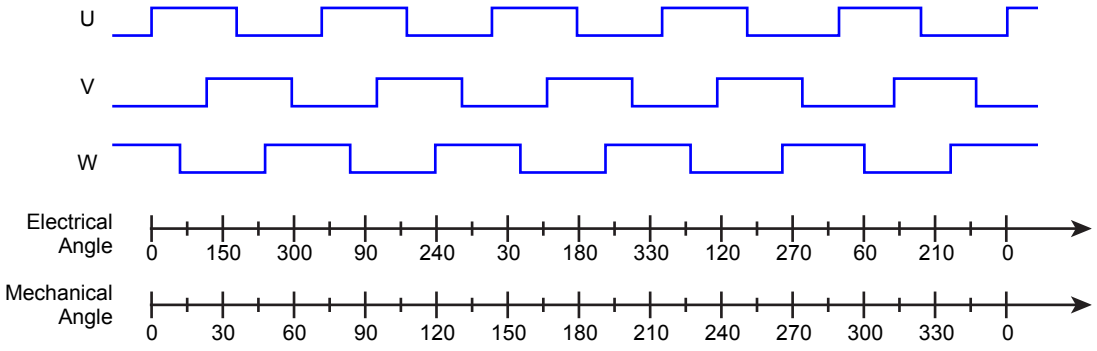


Figure 23: U, V, W Outputs for Five Pole-Pair BLDC Motor

Table 3: UVW Pole Pair Settings

Quantity of Poles ("resolution_pairs")	Quantity of Pole-Pairs	Conversion from Electrical Degrees to Mechanical Degrees	
		Electrical (°)	Mechanical (°)
0000	1	90	90
0001	2	90	45
0010	3	90	30
0011	4	90	22.5
0100	5	90	18
0101	6	90	15
0110	7	90	12.857…
0111	8	90	11.25
1000	9	90	10
1001	10	90	9
1010	11	90	8.1818…
1011	12	90	7.5
1100	13	90	6.9231…
1101	14	90	6.4286…
1110	15	90	6
1111	16	90	5.625

Angle Hysteresis

Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. In the A1333, the hysteresis field (ANG.hysteresis) defines the width of an angle window at 14-bit resolution. Mathematically, the width of this window is:

$$HYSTERESIS \times (360 / 16384) \text{ degrees} \quad ,$$

HYSTERESIS is a 6-bit wide EEPROM field, allowing a range of 0 to 1.384 degrees of hysteresis to be applied.

The hysteresis-compensated angle can be routed to the ABI or UVW interface by setting the AHE bit in EEPROM to a 1 (bit 12 of address 0x19). On the SPI or Manchester interface, the hysteresis-compensated angle can be read via an alternate register (HANG.angle_hys) at 12-bit resolution.

The effect of the hysteresis is shown in Figure 24. The current angle position as measured by the sensor is at the "head" of the hysteresis window. As long as the sensor (electrical) angle advances in the same direction of rotation, the output angle will be the sensor angle, minimizing latency. If the sensor angle reverses direction, the output angle is held static until the sensor angle exits the hysteresis window in either direction. If the exit is in the opposite direction of rotation where the "head" was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. The current direction of rotation, or "head" for the purposes of hysteresis, is viewable via the STA.rot bit, where 0 is increasing angle direction and 1 is in decreasing angle direction.

This behavior has the following consequences:

1. If the hysteresis window is greater than the output resolution, the output angle will skip consecutive resolution steps.
2. If there is jitter due to noise or mechanical vibration, especially at a static angle position or very slow rotation, the angle will tend to bias to one side of the window, depending on the direction of rotation as the angular velocity approaches zero (i.e., towards the current "head") rather than to the average position of the jitter.

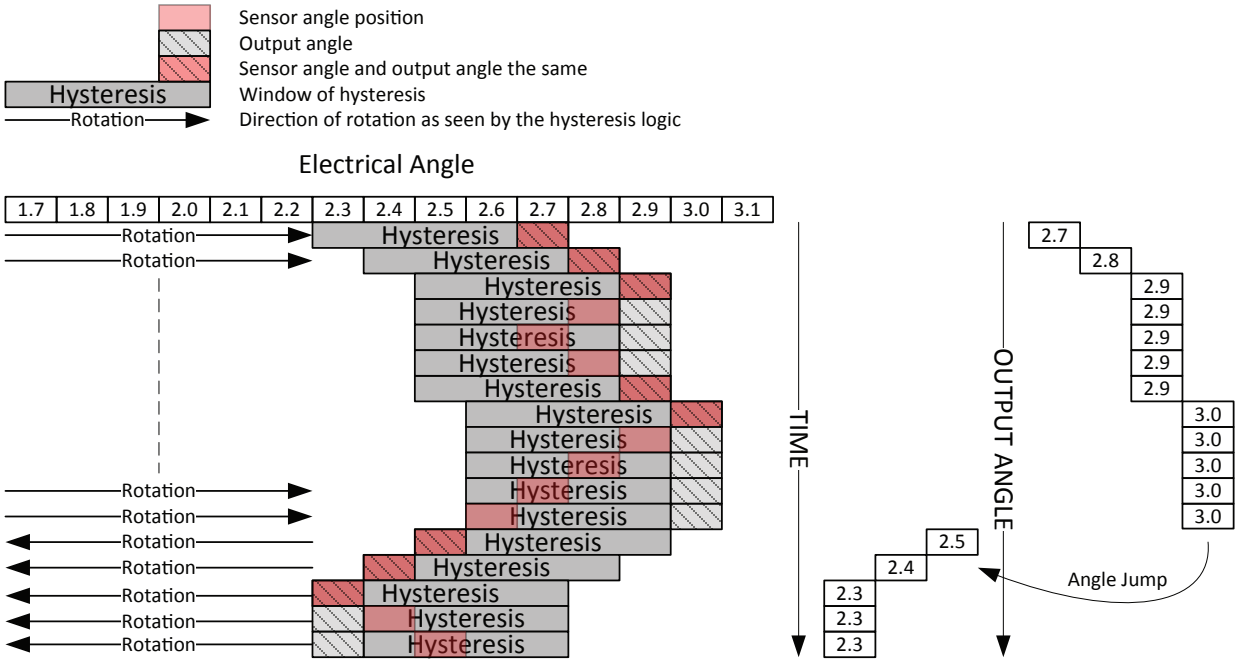


Figure 24: Effect of Hysteresis

Note: The rotation direction resets to 0, or increasing angle direction. At power-up or after LBIST, the hysteresis window will always be behind the initial angle position, so if hysteresis is enabled a decreasing angle direction of rotation will not register until the hysteresis window is past.

Turns Counting

The A1333 uses a secondary, lower power signal path (called the "ZCD" path) to track rotation turns. The turns counter logic tracks the turns in either 45 or 180 degree increments, based on the T45 register field. The signal path which tracks total turns does not implement the same angle compensation as the primary signal path. Because of this, the turns count value will not precisely match the primary angle output.

The turns counter saturates at +2047 and –2048 in the 45-degree mode and +511 and –512 in the 180-degree mode. If this happens, the Turns Count Warning Flag (bit 0 of serial register 0x26) will assert and stay asserted until the turns counter is reset via the Control register (serial register 0x1E). (see Primary Serial Interface Registers Reference section).

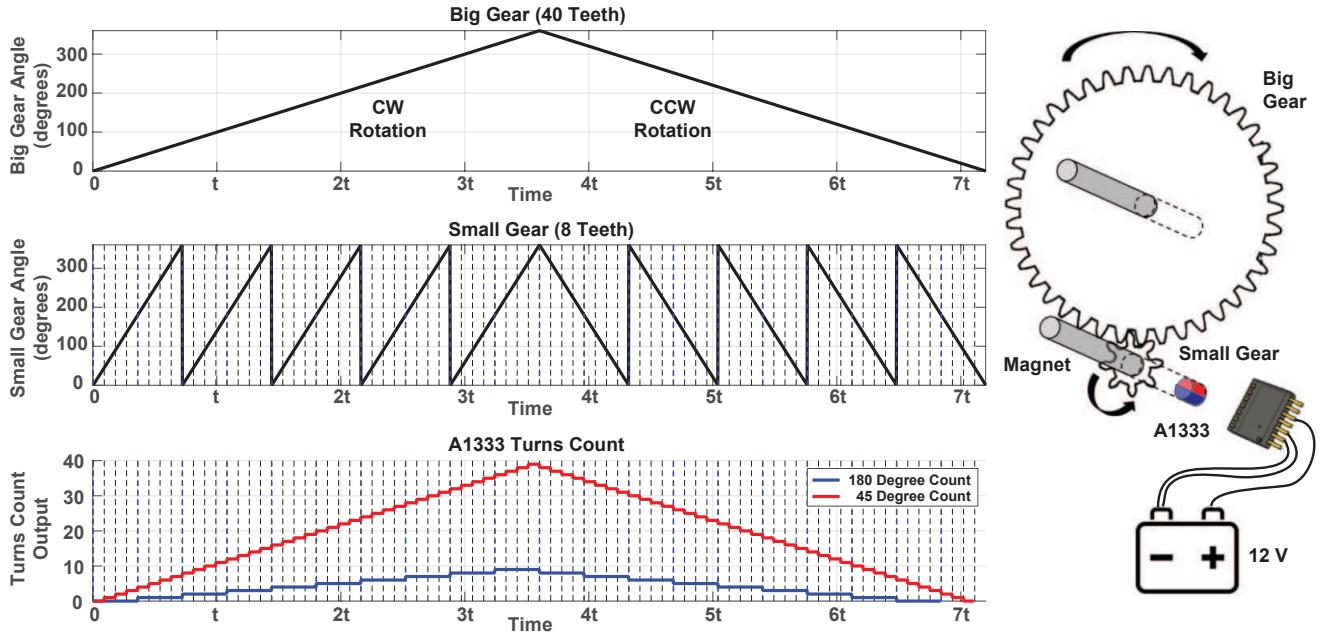


Figure 25: Example of a Turns Counting Application

INVOKING A TURNS COUNTER RESET

Resetting the turns counter is a command invoked using the "special" field of the CTRL register (Register address 0x1E, see Primary Serial Interface Reference). Following a reset, turns are tracked relative to that point, as measured by the signal path (ZCD).