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Dual-Die Programmable Linear Hall IC with Advanced Diagnostics for Safety-Critical Applications

FEATURES AND BENEFITS

- Two electrically isolated die in one package for the most safety-critical applications
  - □ In the event of a die failure, self-diagnostics allow the controller to discern which die to continue to trust
  - □ For diagnostics that impact response, these diagnostics can be run on each die while the other is fully operational
  - □ For all features below, these refer to each of the two die in the package
- High-speed analog, A-to-D converter (ADC), and digital architectures, enabling user-selectable bandwidth for speed-sensitive applications
  - □ 4-phase chopper stabilization, which minimizes offset drift across temperature range
  - □ 16-bit, high update rate ADC
- Exceptional stability throughout lifetime and across temperature changes
  - □ Factory-configured using multisegment temperature compensation to give a flat baseline across operating temperature range

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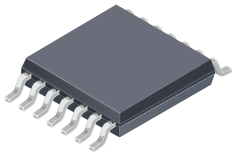
Package:

14-pin TSSOP (suffix LE)

Not to scale



DESCRIPTION

The A1346 is the ideal solution for safety-critical applications. It incorporates full die redundancy with the added benefits of advanced diagnostics. The combination of these two features allow for a higher level of diagnostics without interruption to the application (where diagnostics would otherwise render a die temporarily nonresponsive). This combination also allows the controller to know which die to trust when the output of the die do not agree.

The A1346 device has dual high-precision, programmable Hall-effect linear sensor integrated circuits (IC) with open-drain outputs, for both automotive and nonautomotive applications. The signal paths of the A1346 provides flexibility through external programming that allows the generation of accurate and customized outputs from an input magnetic signal. The A1346 is an especially configurable and robust solution for the most demanding linear field sensor applications.

The BiCMOS, monolithic integrated circuits incorporate on each SoC: a Hall sensing element, precision temperature-compensating circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element, a small-signal high-gain amplifier, proprietary dynamic offset cancellation circuits, advanced output linearization circuitry, and advanced diagnostic detection. The A1346 provides an unmatched level of customer reprogrammable options.

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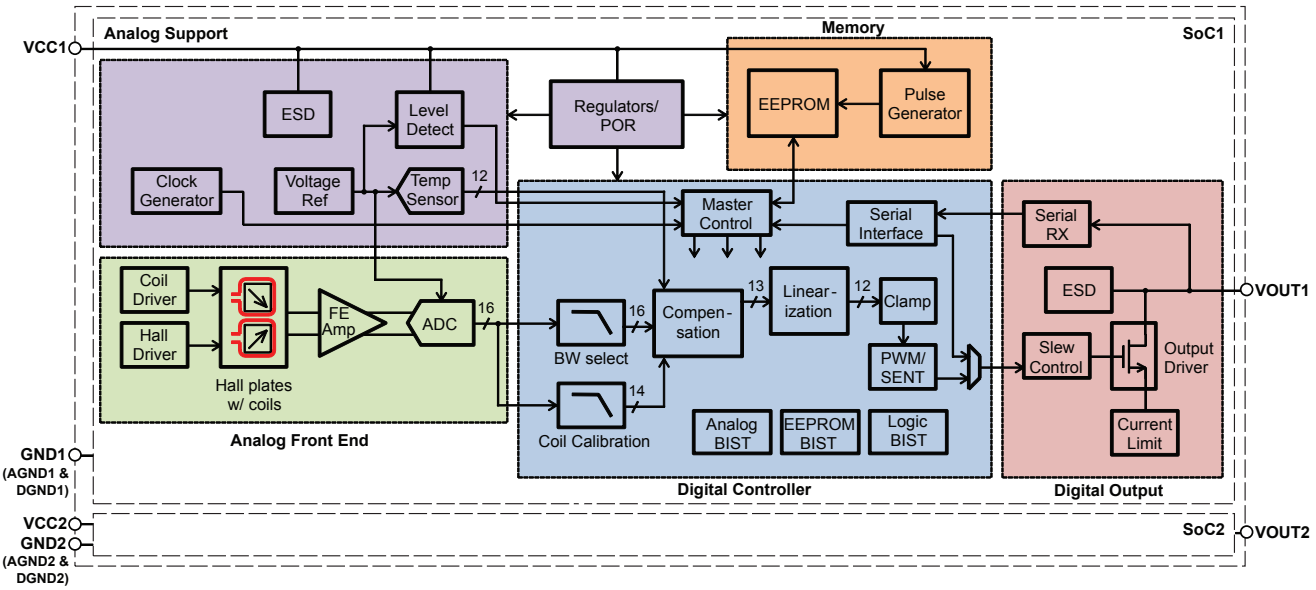


Functional Block Diagram

FEATURES AND BENEFITS (continued)

- □ Customer configurability for 1st and 2nd order sensitivity and 1st order offset compensation across temperature range
- □ Integrated feedback coil compensates for drift throughout product lifetime

- Wide operating flexibility to meet any application:
  - □ Field range from ±40 to ±1800 gauss
  - □ Rail to negative rail offset configurability
  - □ High-precision, full output range high and low clamps
  - □ Integrated linearization allows for flexible output waveform translation and compensation for nonlinear magnetic inputs
- Advanced diagnostic-focused features enabling easier system-level ASIL compliance
  - □ Full data path validation through active front-end stimulation with internal magnetic coil; this method validates all relevant transistors for device operation
  - □ Logic Built-In Self Test (LBIST) on-demand to validate the digital subsystem
  - □ Large suite of configurable fault monitors provide system level fault detection, including:
    - ♦ Overvoltage or undervoltage
    - ♦ Overtemperature
    - ♦ Magnetic Field Out of Range detection
    - ♦ Broken wire detection
- Flexible output protocols with up to 12-bit resolution and configurable error notifications
  - □ Digital open-drain output allows for flexible output voltage levels
  - □ PWM (Pulse-Width-Modulated) output with diagnostic output mode to identify fault conditions
  - □ SENT (Single Edge Nibble Transmission) compliant output with configurable reporting of error conditions and other diagnostic information
  - □ Proprietary Fast SENT provides increased data rates to support high-bandwidth applications
  - □ Device-shared SENT protocol as SSENT (Sequential SENT) and ASENT (Addressable SENT) allows user to connect up to 4 devices on the same output line for faster communication.
  - □ Enhanced EMC tuning through programmable fall-time configurability
- Integrated EEPROM enables a high level of configurability and product traceability
  - □ Customer-reserved area allows on-board storage of unique lot and date code information
  - □ Robust EEPROM with Single Error Correction and Double Error Detection (SECDED), capability
  - □ Integrated charge pump allows in-application programming without any requirement for high voltages to be supplied to the device during programming

DESCRIPTION (continued)

A key feature of the A1346 is its ability to produce a highly linear device output for nonlinear input magnetic fields. To achieve this, the device features 16-segment customer programmable linearization, where a unique linearization coefficient factor is applied to each segment. Linearization coefficients are stored in a lookup table in EEPROM.

The A1346 contains two proprietary SENT protocols in addition to SAEJ2716: SSENT and ASENT. Both protocols enable the user to attach up to 4 devices on one SENT line to reduce system costs. SSENT provides sequential access to the sensors connected to the same line. SSENT provides a very low overhead method to maximize the sensor bandwidth on this single SENT line, minimizing impact on system performance. ASENT provides random access to all the sensors on the common SENT line. Both protocols allow individual sensors on the same line to enter diagnostic mode while the other sensors continue to respond to queries, allowing for the highest diagnostic coverage while maintaining 100% availability of the sensor solution.

The A1346 is available in a surface-mount, lead (Pb) free 14-pin TSSOP package (LE suffix), with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Packing*
A1346LLETR-T	4000 pieces per 13-in. reel

*Contact Allegro™ for additional packing options

Table of Contents

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

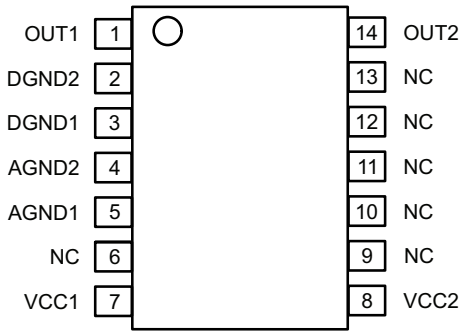
Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		20	V
Reverse Supply Voltage	V_{RCC}		–16	V
Forward Supply Current	I_{CC}		30	mA
Reverse Supply Current	I_{RCC}		–30	mA
Forward Output Voltage	V_{OUT}		20	V
Reverse Output Voltage	V_{ROUT}		–1	V
Output Short-Circuit Current	$I_{OUTSC(SINK)}$	V_{CC} to V_{OUT}, 4.5 V < V_{CC} < 5.5 V	–20	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	174	°C/W

*Additional thermal information available on the Allegro website.

PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LE, 14-Pin TSSOP Pinout Diagram

Terminal List Table

Number	Name	Function
1	OUT1	Output signal, die 1
2	DGND2	Ground, die 2, must be connected to pin 4
3	DGND1	Ground, die 1, must be connected to pin 5
4	AGND2	Ground, die 2, must be connected to pin 2
5	AGND1	Ground, die 1, must be connected to pin 3
6, 9, 10, 11, 12, 13	NC	No connection; recommend to connect to GND for best EMC performance
7	VCC1	Input power supply, die 1
8	VCC2	Input power supply, die 2
14	OUT2	Output signal, die 2

OPERATING CHARACTERISTICS: Valid T_A and V_{CC}, unless otherwise specified (specifications relate to one die in the package)

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS							
Supply Voltage	V_{CC}			4.5	5	5.5	V
Supply Current	I_{CC}	Compensation coil off		–	–	10	mA
Peak Supply Current	$I_{CC(pk)}$	Compensation coil on		–	–	16	mA
Reverse Supply Current	I_{RCC}	V_{CC} = –16 V, T_A = 25°C		–3	–	–	mA
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	I_{CC} = 14 mA, compensation coil off, T_A = 25°C		20	–	–	V
Chopping Frequency	f_C	T_A = 25°C, compensation coil off		–	128	–	kHz
		T_A = 25°C, compensation coil on		–	64	–	kHz
Oscillator Frequency	f_{OSC}	T_A = 25°C		6963	8192	9421	kHz
Undervoltage Detection Threshold	$V_{CC(UV)LOW}$	V_{CC} falling, see Figure 1		4	–	4.35	V
	$V_{CC(UV)HIGH}$	V_{CC} rising, see Figure 1		4.05	–	4.4	V
Power-On-Reset Threshold	$V_{CC(POR)LOW}$	V_{CC} falling, see Figure 1		3.4	–	3.8	V
	$V_{CC(POR)HIGH}$	V_{CC} rising, see Figure 1		3.5	–	3.9	V
Overvoltage Detection Threshold	$V_{CC(OV)LOW}$	V_{CC} falling, see Figure 1		6.6	–	7.4	V
	$V_{CC(OV)HIGH}$	V_{CC} rising, see Figure 1		6.7	–	7.6	V
High-Voltage Threshold	$V_{CC(HV)LOW}$	V_{CC} falling, see Figure 1		15	–	–	V
	$V_{CC(HV)HIGH}$	V_{CC} rising, see Figure 1		–	–	17	V
OUTPUT CHARACTERISTICS							
Noise (Peak-to-Peak) [1]	$OUT_{N(PK)}$	bw_sel_c = 0	coil_freq = 0, coil_comp_dis = 0, bw_sel_comp_c = 0, T_A = 25°C	–	0.32	–	G
		bw_sel_c = 1		–	0.5	–	G
		bw_sel_c = 2		–	0.93	–	G
		bw_sel_c = 3		–	1.74	–	G
		bw_sel_c = 4-7		–	2.85	–	G
Output Leakage Current	I_{OUT}	Output voltage ≤ 5.5 V, output FET off		–	–	100	µA
Output Load Resistance	$R_{L(PULLUP)}$	Output current ≥ –10 mA		1.2	–	–	kΩ
Output Saturation Voltage	$V_{OUT(Sat)}$ LOW	Output current = –4.7 mA, V_{CC} = 5 V, output FET on		–	–	0.35	V
Output Current Limit	I_{LIMIT}	Output FET on, T_A = 25°C		20	30	50	mA
Output Zener Clamp Voltage	V_{ZOUT}	T_A = 25°C, I_{OUT} = –3 mA		20	–	–	V
External Load Capacitor	C_{LX}			–	–	4.7	nF

Continued on the next page…

OPERATING CHARACTERISTICS (continued): Valid T_A and V_{CC}, unless otherwise specified (specifications relate to one die in the package)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Response Time[2]	t_{resp}	bw_sel_c = 4-7	–	0.15	–	ms
		bw_sel_c = 3	–	0.25	–	ms
		bw_sel_c = 2	–	0.69	–	ms
		bw_sel_c = 1	–	2.4	–	ms
		bw_sel_c = 0	–	9.3	–	ms
Power-On Time[2]	t_{PO}	bw_sel_c = 4-7	–	0.6	–	ms
		bw_sel_c = 3	–	0.75	–	ms
		bw_sel_c = 2	–	1.25	–	ms
		bw_sel_c = 1	–	3.7	–	ms
		bw_sel_c = 0	–	13	–	ms
Output Jitter, PWM[3]	PWM_{JIT}	outmsg_mode = 0, SENT_PWM_RATE < 2 kHz	–1	–	1	LSB
		outmsg_mode = 0, SENT_PWM_RATE ≥ 2 kHz	–3	–	3	LSB
Output, Integral Nonlinearity	INL	outmsg_mode = 0, SENT_PWM_RATE < 2 kHz	–	±0.5	–	%FSO
Maximum Output Resolution[4]	OUT_{RES}	T_A = 25°C, outmsg_mode = 1-5	–	12	–	bit
		T_A = 25°C, outmsg_mode = 0, SENT_PWM_RATE ≤ 2 kHz	–	12	–	bit
PWM Carrier Frequency[5]	f_{PWM}		–15	–	15	%

[1] Noise (Peak-to-Peak) calculated as 6 sigma (6 standard deviations) from characterization of a small sample of devices with a 0.01 µF bypass capacitor. Measurements were made at Sensitivity ≈ 4.5 LSB/G. Conversion of noise from gauss to LSB can be done by: Noise (G) × Sensitivity (LSB/G) = Noise (LSB).
[2] Defined as time before magnetic data is 90% of the settled value.
[3] Determined from design characterization; not tested in production.
[4] When outmsg_mode = 0, the maximum output resolution decreases to 11 – n (bits) for SENT_PWM_RATE = 2 kHz × 2^n.
[5] PWM carrier frequency accuracy is % of the programming target.

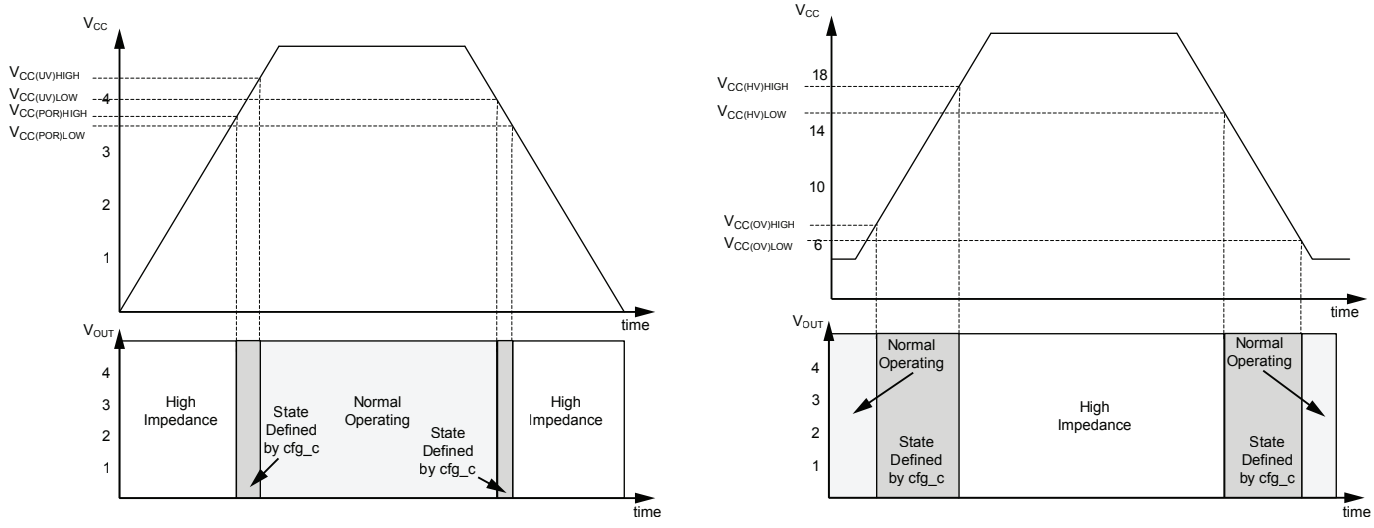


Figure 1: V_{CC} Thresholds and Resultant Output States

MAGNETIC CHARACTERISTICS: Valid at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1,2]
Input Field Range	B_{IN}		–1800	–	1800	G
Initial Sensitivity	$SENS_{INIT}$		–	0.0278	–	%FSO/G
Initial Quiescent Output	QO_{INIT}		–	50	–	%FSO
Initial Output Clamp	$OUT_{CLP(L)INIT}$	CLAMPL = 0, outmsg_mode = 1-5	–	0	–	LSB
		CLAMPL = 0, outmsg_mode = 0	–	2	–	%D
	$OUT_{CLP(H)INIT}$	CLAMPH = 0, outmsg_mode = 1-5	–	4095	–	LSB
		CLAMPH = 0, outmsg_mode = 0	–	98	–	%D

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] *FSO* means Full Scale Output. See Definitions of Terms section.

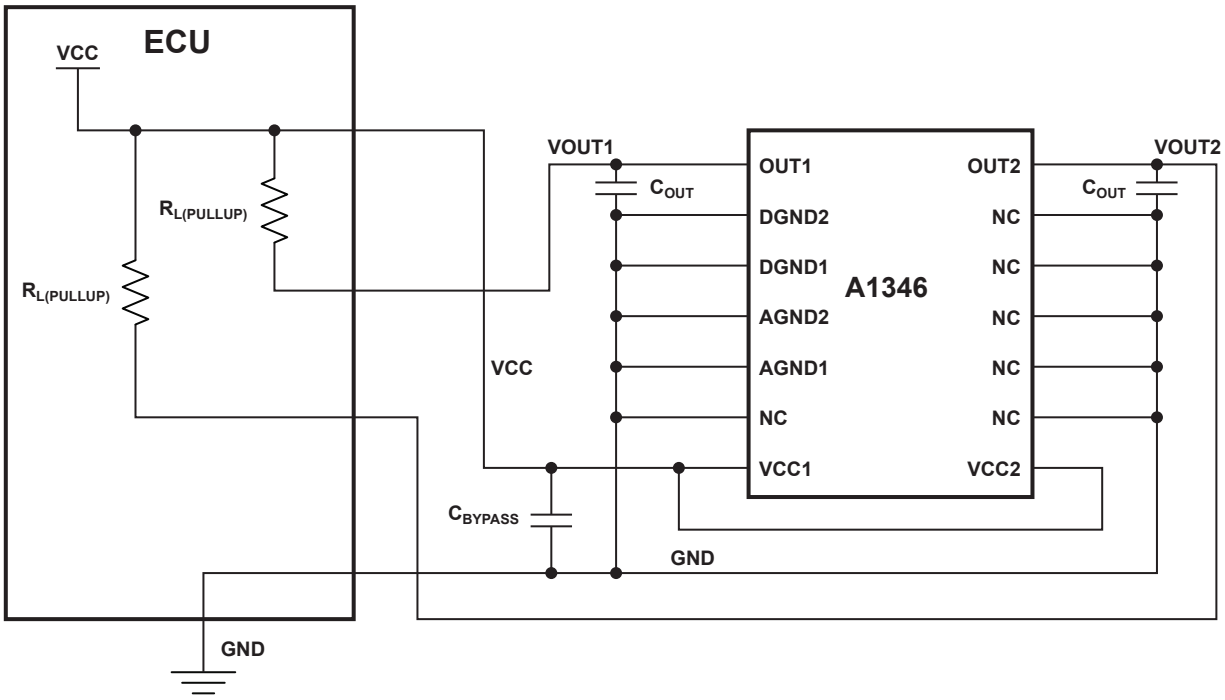


Figure 2: Typical Application Circuit
Typical C_{BYPASS} = 0.01 µF and C_{OUT} = 1.5 nF

ACCURACY CHARACTERISTICS: Valid at T_A and V_{CC}, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Lifetime Sensitivity Drift	$\Delta SENS_{LIFE}$	Variation on final programmed Sensitivity value; T_A = 25°C, shift after AEC-Q100 grade 0 qualification testing; measured at T_A = 25°C, Compensation Coil On	–	<±1	–	%
		Variation on final programmed Sensitivity value; TA = 25°C, shift after AEC-Q100 grade 0 qualification testing; measured at T_A = 25°C, Compensation Coil Off	–	<±2	–	%
Package Hysteresis	$\Delta SENS_{PKG}$	Variation on final programmed Sensitivity value; measured at T_A = 25°C after temperature cycling from 25°C, Compensation Coil On	–	<±0.5	–	%
		Variation on final programmed Sensitivity value; measured at T_A = 25°C after temperature cycling from 25°C, Compensation Coil Off	–	<±2	–	%
Quiescent Output Drift[2]	ΔQO	SENS = $SENS_{INIT}$	–1.32	–	1.32	G
Sensitivity Drift Over Temperature[3]	$\Delta SENS_{INIT}$	25°C ≤ T_A ≤ 150°C, Compensation Coil On	–1.5	–	1.5	%
		25°C ≤ T_A ≤ 150°C, Compensation Coil Off	–1	–	1	%
		–40°C ≤ T_A ≤ 25°C, Compensation Coil On	–2	–	2	%
		–40°C ≤ T_A ≤ 25°C, Compensation Coil Off	–1.5	–	1.5	%

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Quiescent Output Drift scales with Sensitivity.
[3] Does not include drift over lifetime and package hysteresis.

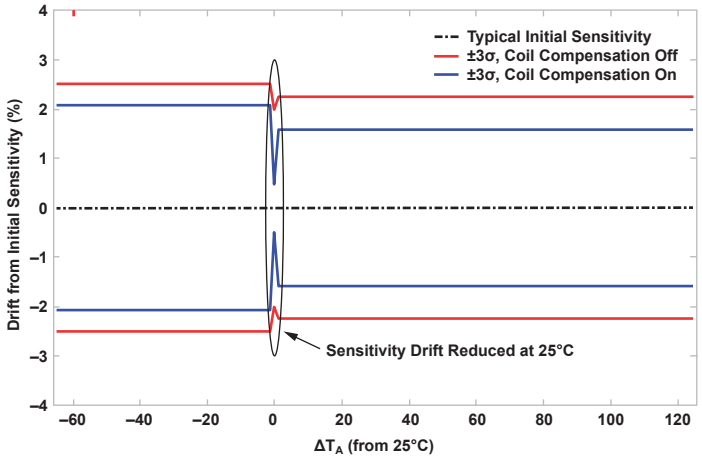


Figure 3: Typical Initial Sensitivity Drift Due To Temperature and Package Hysteresis and SENSTC1 = SENSTC2 = 0%/°C; Does Not Include Lifetime Sensitivity Drift

PROGRAMMABLE CHARACTERISTICS: Valid at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
SENSITIVITY						
Output Sensitivity Range	SENS		0.0278	–	1.3	%FSO / G
			1.138	–	53	LSB / G
Bits Sensitivity Trim, Coarse	Bit (SENSM_C)		–	3	–	bit
Sensitivity Coarse Trim Range[2]	SENSM_C		1	–	32	–
Bits Sensitivity Trim, Fine	Bit (SENS_C)		–	11	–	bit
Sensitivity Fine Trim Range[3]	SENS_C		0.5	–	1.5	–
Bits Sensitivity Polarity	Bit (POL)		–	1	–	bit
OFFSET (QUIESCENT OUTPUT)						
Bits Quiescent Output Trim, Fine	Bit (QO_C)		–	16	–	bit
Customer Quiescent Output Fine Trim Range	QO_C		–32768	–	32767	LSB
CLAMPS (HIGH AND LOW OUTPUT CLAMPS)						
Bits Output Low Clamp	Bit ($OUT_{CLP(LOW)}$)		–	12	–	bit
Output Low Clamp Range	$OUT_{CLP(LOW)}$		0	–	4095	LSB
Bits Output High Clamp	Bit ($OUT_{CLP(HIGH)}$)		–	12	–	bit
Output High Clamp Range	$OUT_{CLP(HIGH)}$		0	–	4095	LSB
TEMPERATURE COMPENSATION						
Bits 1st Order Sensitivity TC	Bit (SENSTC1)	senstc1_hot_c, senstc1_cld_c	–	11	–	bit
1st Order Sensitivity TC Range	SENSTC1	25°C < T_A ≤ 150°C	–0.391	–	0.391	% / °C
		–40°C ≤ T_A < 25°C	–0.781	–	0.781	% / °C
Bits 2nd Order Sensitivity TC	Bit (SENSTC2)	senstc2_hot_c, senstc2_cld_c	–	10	–	bit
2nd Order Sensitivity TC Range	SENSTC2	25°C < T_A ≤ 150°C	–1.5	–	1.5	m% / °C^2
		–40°C ≤ T_A < 25°C	–6	–	6	m% / °C^2
Bits 1st Order Offset TC	Bit (QOTC)	qotc_hot_c, qotc_cld_c	–	12	–	bit
1st Order Offset TC Range	QOTC	25°C < T_A ≤ 150°C	–32	–	31.98	LSB / °C
		–40°C ≤ T_A < 25°C	–64	–	63.97	LSB / °C

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PROGRAMMABLE CHARACTERISTICS (continued): Valid at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
LINEARIZATION						
Linearization Positions			–	17	–	data point
Bits Linearization Coefficients	Bits (LIN_{COEF})		–	12	–	bit
Bits Post Linearization Sensitivity Trim	Bits (PLIN_SENS)		–	12	–	bit
Post Linearization Sensitivity Trim Range	PLIN_SENS (RANGE)		–	±1	–	–
Bits Post Linearization Offset Trim	Bits (PLIN_QVO)		–	12	–	bit
Post Linearization Offset Trim Range	PLIN_QVO (RANGE)		–2048	–	2047	LSB
Bit Linearization Output Polarity	Bits (POLOUT)		–	1	–	bit
Bit Linearization Input Polarity	Bits (POLIN)		–	1	–	bit

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Sensitivity Coarse Trim is a multiplier to the initial Sensitivity with step sizes defined by the sensm parameter. Refer to the Programmable Parameter Reference section for more information.
[3] Sensitivity Fine Trim is a multiplier applied to the initial Sensitivity after the Sensitivity Coarse Trim with step sizes defined by the sens_c parameter. Refer to the Programmable Parameter Reference section for more information.

APPLICATION INFORMATION

Signal Path

Each die in the A1346 contains a Hall-effect transducer that produces a signal proportional to the magnetic flux density perpendicular to the face of the package, referred as the applied magnetic flux density. The output of the Hall transducer is then amplified and digitized. The resulting signal is a signed digital value that can be scaled, offset, and compensated to achieve a desired output. The advanced digital parameters allow for a large range of input signals to be adjusted for the application. This results in the A1346 being highly flexible and accurate for applications with challenging sensing requirements. The following sections give an overview of digital signal path blocks and the corresponding transfer functions.

COMPENSATION BLOCK

The compensation block contains adjustments to the Sensitivity and Offset. This includes compensation for input signal changes over the operating temperature range. First, the Sensitivity Trim Block multiplies the signal by a temperature-dependant gain (or attenuation) factor. The correction is segmented into two regions: hot and cold, where hot indicates ambient temperatures greater or equal to 25°C, and cold indicates ambient temperatures lesser or equal to 25°C. Each segmented region also contains 1st and 2nd order Sensitivity temperature compensation.

Note:
The hot Sensitivity temperature compensation is independent of the cold region.

Equations 1 and 2 show the transfer function of the Sensitivity Trim Block.

$$Y_1 = B_{IN} \bullet SENS_{INIT} \bullet POL\_C \bullet SENSM\_C \bullet SENS\_C \bullet \left[1 + \left(\left(\frac{SENSTC2\_HOT\_C}{1000}\right) \bullet \Delta T_A + SENSTC1\_HOT\_C\right) \bullet \frac{\Delta T_A}{100}\right] \quad (1)$$

$$Y_1 = B_{IN} \bullet SENS_{INIT} \bullet POL\_C \bullet SENSM\_C \bullet SENS\_C \bullet \left[1 + \left(\left(\frac{SENSTC2\_CLD\_C}{1000}\right) \bullet \Delta T_A + SENSTC1\_CLD\_C\right) \bullet \frac{\Delta T_A}{100}\right] \quad (2)$$

NOTE:
Included in the transfer function shown in Equations 1 and 2 is the conversion from the applied magnetic input to a digital value, $B_{IN} \times SENS_{INIT}$.

The output of the Sensitivity Trim Block, Y_1, is a 17-bit signed integer.

The Offset Trim Block adds a temperature-dependent factor to the input signal. The offset factor is segmented into two region: hot and cold, as defined in the Sensitivity Trim Block. Each segment contains 1st order Offset temperature compensation. Equations 3 and 4 show the transfer functions of the Offset Trim Block. The output, Y_2, is a 13-bit signed integer and is the value passed out of the Compensation Block.

$$Y_2 = Y_1 + QO\_C + QOTC\_HOT\_C \times \Delta T_A \quad (3)$$

$$Y_2 = Y_1 + QO\_C + QOTC\_CLD\_C \times \Delta T_A \quad (4)$$

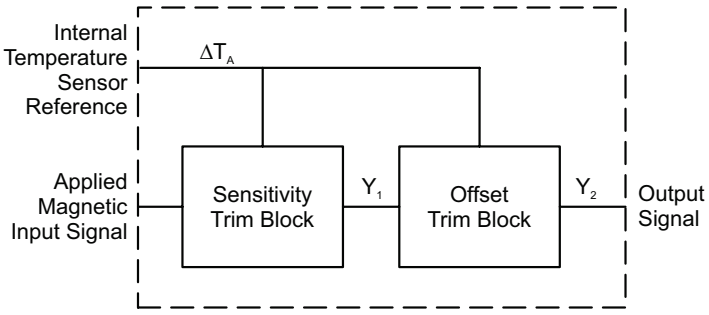

Figure 4: Compensation Block

Table 1: Compensation Block Parameters

Variable	Description	Programmable Parameter (Memory Location)	Units
POL_C	Determines the sensitivity polarity. The default polarity is increasing with output with increasing applied south magnetic flux density.	pol_c (Register sens_trim_c 0x3 [15])	NA
SENSM_C	Coarse Sensitivity multiplier	sensm_c (Register sens_trim_c 0x3 [14:12])	NA
SENS_C	Fine Sensitivity multiplier	sens_c (Register sens_trim_c 0x3 [10:0])	NA
SENSTC2_HOT_C	2nd order Sensitivity temperature compensation for $T_A \geq 25°C$	senstc2_hot_c (Register senstc2_c 0x5 [9:0])	m%/°C^2
SENSTC1_HOT_C	1st order Sensitivity temperature compensation for $T_A \geq 25°C$	senstc1_hot_c (Register senstc1_c 0x4 [10:0])	%/°C
SENSTC2_CLD_C	2nd order Sensitivity temperature compensation for $T_A \leq 25°C$	senstc2_cld_c (Register senstc2_c 0x5 [21:12])	m%/°C^2
SENSTC1_CLD_C	1st order Sensitivity temperature compensation for $T_A \leq 25°C$	senstc1_cld_c (Register senstc1_c 0x4 [22:12])	%/°C
ΔT_A	Change in ambient temperature, equal the ambient temperature, T_A, minus 25°C.	NA	°C
QO_C	Fine quiescent output adjustment	qo_c (Register qo_trim_c 0x6 [15:0])	LSB
QOTC_HOT_C	1st order quiescent output temperature drift compensation for $T_A \geq 25°C$.	qotc_hot_c (Register qotc_c 0x7 [11:0])	LSB/°C
QOTC_CLD_C	1st order quiescent output temperature drift compensation for $T_A \leq 25°C$.	qotc_cld_c (Register qotc_c 0x7 [23:12])	LSB/°C
$SENS_{INIT}$	Initial Sensitivity	NA	LSB/G
B_{IN}	Applied magnetic flux density	NA	G

LINEARIZATION

The Linearization block passes the output from the compensation block through a piecewise-linear transfer described by 17 points, which define 16 line segments. The *x*-coordinates of these points are programmable and are stored as 12-bit words in a table in memory, LIN_C. Corresponding y-coordinates are fixed and are equally spaced over the output range. For proper operation, table increasing entries, i.e., $x_0 \leq x_1 \leq x_2 \leq ... \leq x_{16}$ should be satisfied. If not satisfied, the output is undefined. Adjacent table entries can be equal. The linearization algorithm will not produce output values in between the *y*-coordinates that correspond to identical adjacent table entries; these output values are skipped. Thus jumps in the transfer function can be realized. Additionally, two more segments are implemented above and below the normal 12-bit output range to facilitate use of all 16 linearization segments without output clipping. Output points in these two segments are linearly extrapolated from the two points nearest each end of the linearization table.

The linearization algorithm incorporates two modes, linearization mode (Lin Mode) and binning mode (Bin Mode).

Linearization Mode (Lin Mode)

Figure 4 shows an example transfer function which is monotonically increasing. Adjacent points form line segments; input values between are linearly interpolated to find intermediate values. Input values smaller than the first table entry are extrapolated using the points (x_0,−2048) and (x_1, −1792), down to a minimum output value of −2304. Input values larger than the last table entry are extrapolated using the points (x_{15},+1792) and (x_{16},+2048), up to a maximum output value of +2304. The output of the Linearization Algorithm Block, Y_3, is a 13-bit signed integer.

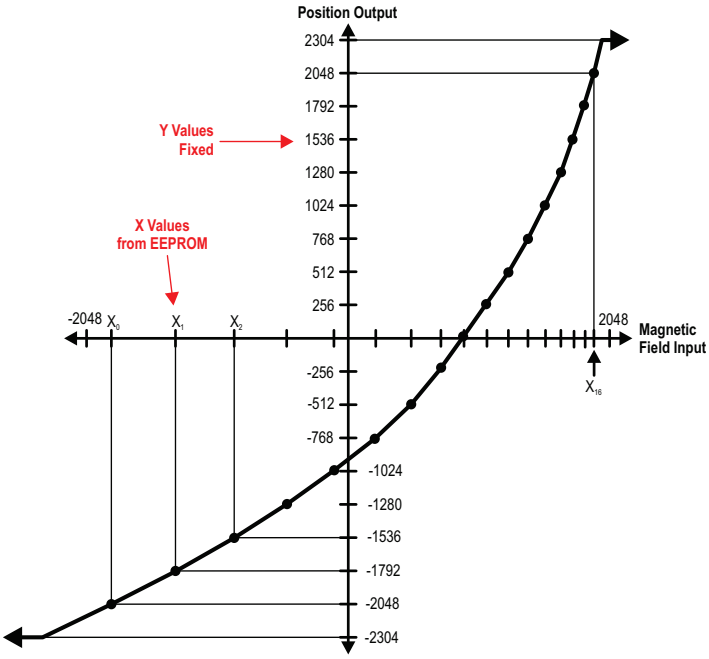

Figure 5: Monotonically Increasing Linearization Transfer Function

Linearization Binning Mode (Bin Mode)

When the bin_mode_c parameter, address lin8_c 0x12 [13], is set, the linearization algorithm does not interpolate between points, but instead produces the output corresponding to the nearest linearization table entry less than or equal to the input value. This transfer function is useful for applications that require distinguishing between several different input ranges. For example, see Figure 5, because $x_2 = x_3 = x_4$ and corresponding output points are −1536, −1280 and −1024 respectively, input values just below $x_2 = x_3 = x_4$ produce an output of −1792 (output corresponding to x_1) and inputs just above or equal to $x_2 = x_3 = x_4$ produce an output of −1024. Intermediate values are skipped. Thus the linearization table functions like a series of comparators with 12-bit programmable thresholds.

Note:
The input values below the lowest table entry produce an output value of −2304, while input values above the highest table entry produce an output value of +2048.

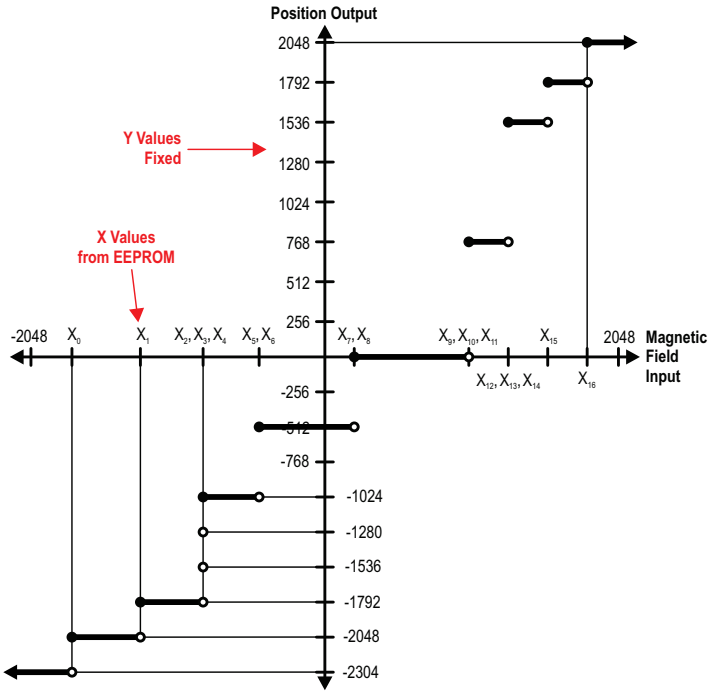

Figure 6: Bin Mode Transfer Function Containing Jumps (Identical Adjacent Table Entries)

The Linearization coefficients and corresponding parameters are stored in following memory locations.

Table 2: Linearization Algorithm Block Parameters

Coefficient/Parameter	Description	Memory Location	Units
x_0, x_2,…x_{14}, x_{16}	Even Linearization Coefficients	lin0_c … lin8_c	LSB
x_1, x_3,…x_{13}, x_{15}	Odd Linearization Coefficients	lin0_c … lin7_c	LSB
lint_e	Set to logic 1 to enable the Linearization table.	lin8_c 0x12 [12]	NA
lint_bin_e	Set to logic 1 to enable linearization binning mode.	lin8_c 0x12 [13]	NA
lint_out_inv	Set to logic 1 to Invert output of linearization block	lin8_c 0x12 [14]	NA
lint_in_inv	Set to logic 1 to Invert input of linearization block	lin8_c 0x12 [15]	NA

POST-LINEARIZATION TRIM

An additional gain and offset trim stage is available in the linearization block. This can be used to attenuate and gain the signal to maintain usage of all 17 linearization points when using an output range that is not full-scale. Equation 5 shows the transfer function for the Post Linearization. The output of the Post Linearization Block, Y_4, is a 12-bit signed integer and is the output of the Linearization Block.

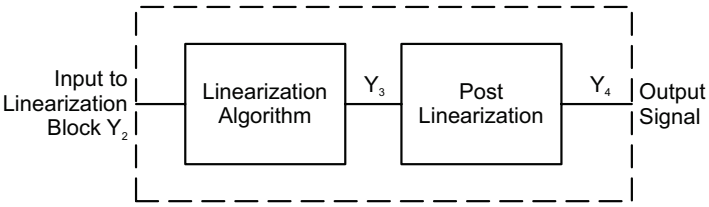

Figure 7: Linearization Block

$$Y_4 = Y_3 \times (1 + PLIN\_SENS) + PLIN\_QVO \qquad (5)$$

CLAMP

The clamp block limits the output to a programmable range set by the parameters clamph and clamp, register clamp_c 0x8. Clamps are programmable throughout the full output range. If the input to the clamp block is greater than the value set by clamph the output is limited to the upper clamp value. Similarly, if the input to the clamp block is less than the value set by clampl the output is limited to the lower clamp value. If the lower clamp exceeds the upper clamp the output is undefined.

Note:
The input to the clamp block is a 12 bit signed value (-2048 to +2047) and is changed to a 12 bit unsigned value (0 to 4095) before comparing to the upper and lower clamp values.

Equations 6 and 7 show the transfer functions for the clamp block. The output of the Clamp Comparison is a 12-bit unsigned integer and is passed to the output block at a fixed frequency of 16 kHz.

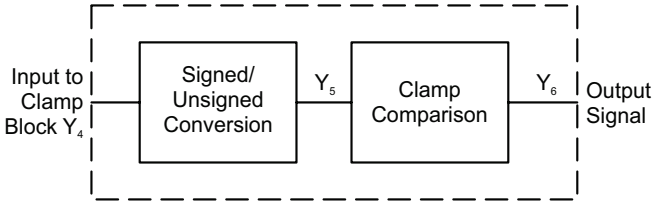

Figure 8: Clamp Block

$$Y_5 = Y_4 + 2048$$

$$(conversion\ from\ signed\ to\ unsigned) \qquad (6)$$

$$if\ (Y_5 > OUTCLP(HIGH)),\ then\ Y_6 = OUTCLP(HIGH)$$

$$else\ if\ (Y_5 < OUTCLP(LOW)),\ Y_6 = OUTCLP(LOW)$$

$$else\ Y_6 = Y_5 \qquad (7)$$

Table 3: Post-Linearization Trim Memory Parameters

Variable	Step Size	Min.	Max.	Description	Parameter (Memory Location)	Units
PLIN_SENS	2^{-11}	−1	+1	Customer post-linearization sensitivity adjustment	plin_sens, (post_lin_c 0x13 [11:0])	NA
PLIN_QVO	1	−2048	+2047	Customer post-linearization offset adjustment	plin_qvo, (post_lin_c 0x13 [23:12])	LSB

Table 4: Clamp Block Parameters

Variable	Description	Programmable Parameter (Memory Location)	Units
CLAMPH	Determines the upper clamp value	clamph (Register clamp_c 0x8 [11:0])	LSB
CLAMPL	Determines the lower clamp value	clampl (Register clamp_c 0x8 [23:12])	LSB

Diagnostic Conditions

DIAGNOSTIC MODES

Each die in the A1346 contains features specifically designed to reduce nondetectable fault conditions and improve system-level ASIL (Automotive Safety Integrity Level) performance. The diagnostic features provide ability to diagnose errors of the main signal path, including the analog signal path (Hall sensor and amplifiers), the ADC, and the digital processing. The A1346 also contains features to diagnose broken wire or open circuit conditions. A description of the broken wire fault conditions are listed in Table 5.

DIAGNOSTIC CONFIGURATION

Each die in the A1346 contains EEPROM parameters to configure the diagnostic modes and output behavior. The EEPROM register, cfg_c, contains configurable parameters to enable or disable the Overvoltage Detection, Undervoltage Detection, BIST Error, Signal Out of Range, and Analog Signal Path Error (CoilBIST). In addition the output behavior in response to the error conditions is configurable. By default the device outputs a diagnostic error signal that is decoded by either the PWM or SENT message. Alternatively the output behavior in response to the error conditions can be set to a high-impedance state.

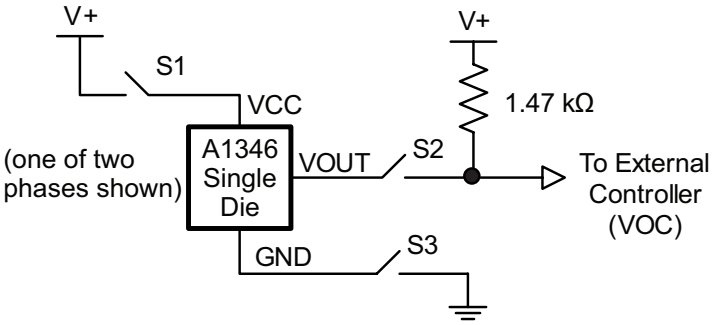

Figure 9: Diagnostic Application Circuit

ANALOG SIGNAL PATH

Errors in the analog signal path are diagnosed using an integrated active coil compensation circuit, CoilBIST. When enabled (coil_freq < 3), an active coil provides a known diagnostic input magnetic field to the Hall sensor circuit. The diagnostic input runs passively during normal operation and does not interfere with the response to external magnetic input. The analog signal path is time-shared between the diagnostic input and the external input at a rate of approximately 128 kHz. The CoilBIST signal detection circuit monitors the signal path at rate of approximately 8 kHz by comparing the diagnostic signal to an internal reference. In the event the analog signal path deviates by more than 10%, V_{OUT} is forced to a state defined by the EEPROM register cfg_c. Setting the parameter coilbist_dis = 1 prevents the analog signal path monitoring from reporting detected errors on the output.

The active coil also provides compensation to reduce Sensitivity drift from lifetime and package stress influences. This feature results in a highly stable Sensitivity over multiple temperature excursions. A programmable bit, coilcomp_dis, is available to disable the compensation while retaining the diagnostic features.

The active coil compensation feature requires an increase of the supply current, I_{CC}, to generate the internal diagnostic magnetic input. The coil compensation on-time is fixed at approximately 16 ms, while the off-time is determined by the EEPROM parameter coil_freq. When the coil compensation is on, the supply current increases by approximately 4 mA. See Table 6 for available coil compensation off time settings. Note, setting coil_freq to a value of 1 or 2 may increase noise. Setting coil_freq to a value of 3 disables the active coil compensation and diagnostic features during normal operation, while this may reduce noise.

Table 5: Broken Wire Detection Conditions

Description	Circuit	S1	S2	S3	VOUT	VOC
Broken VCC	Figure 9	OPEN	CLOSED	CLOSED	High Impedance	VCC
Broken VOUT	Figure 9	CLOSED	OPEN	CLOSED	Low Impedance	VCC
Broken Ground	Figure 9	CLOSED	CLOSED	OPEN	High Impedance	VCC

NOTE: For proper diagnostic detection the device output clamps should be programmed to appropriate levels. Typical levels are 10% FSO for clamp low and 90% FSO for clamp high.

Table 6: Coil Compensation On/Off Time

coil_freq [1] (0x09 bits 14:13)	Coil Compensation On-Time (ms)	Coil Compensation Off-Time (ms)	Average I_{CC} Increase Due to Coil Compensation (mA)	CoilBIST Response Time (ms)
0	16	0	4	10
1	16	16	2	26
2	16	4080	0.015625	4090
3	0	16	NA	After BIST request

[1] Setting coil_freq = 1 or 2 may increase noise. Setting coil_freq = 3 may decrease noise but increase Lifetime Sensitivity Drift.

BIST

Each die in the A1346 also has a BIST (Built-In Self Test) feature to check for logic errors in the digital processing circuitry. The BIST feature is configurable with options to disable or enable on request. The options are configured by customer programmable EEPROM bits in the cfg_c register. When set for enable on request, the BIST runs in response to a request by an external controller. Diagnostic request will be different based on the output protocol. When the output protocol is PWM or SENT, the controller must hold the output low for two consecutive messages to trigger a BIST. In the case when output protocol is TSENT, to request the device perform a BIST, the external controller must hold the output low for a period of time, t_{dreq}, during the Data Nibbles of the output after the SCN nibble (see Table 8, Figure 11, and Figure 15), and then release the output to a high impedance state. For SSENT and ASENT, the F_DIAG function pulse should be used to trigger a BIST request.

Alternatively, the BIST can execute in response to a write command from the serial communication interface. To request the device perform a BIST using the serial communication interface, a write command is used to set parameter lbist_run = 1 in register lbist_crtl_c (see Figure 28). The LBIST test takes approximately 10 ms to complete.

After the BIST request is received, the Output remains in a high-impedance state while the internal BIST executes. If the parameter lbist_ack is set, the first output message contains a BIST signature value (LBIST Ack) indicating whether or not an error is detected during the digital logic test. If the parameter abist_ack is set, the first output message contains the coil diagnostic signature (ABIST Ack) from the CoilBIST. If both lbist_ack and abist_ack are set, the first output message is the LBIST Ack followed by the second output message ABIST Ack. The ABIST Ack message is only valid when coil_freq = 3. For more information on CoilBIST when using coil_freq < 3, see Diagnostic Conditions: Analog Signal Path. If there are no errors detected, the next output message after the acknowledge messages contains the normal output response. Should an error be detected, the output remains in a high-impedance state after the acknowledge messages are transmitted. See Table 7, Diagnostic Summary Table, for more information on the output in response to a diagnosed error.

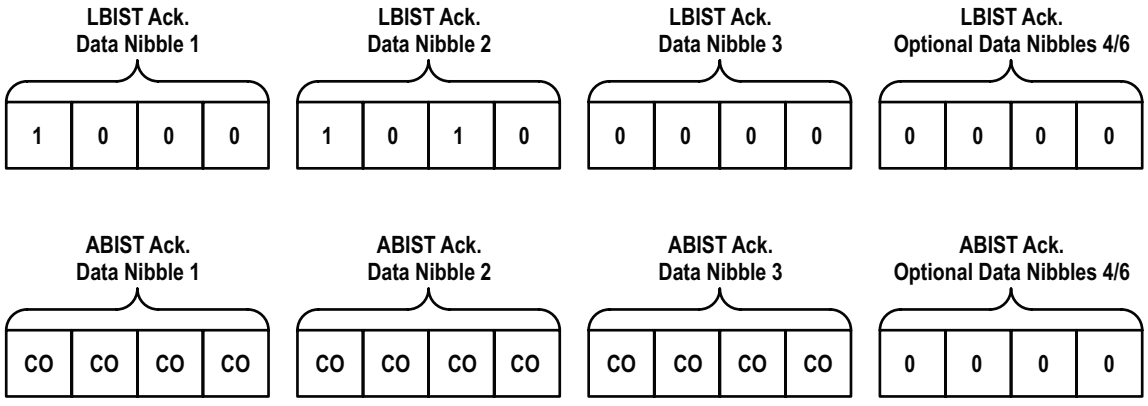

Figure 10: Acknowledgment Signatures for BIST (no errors detected)

(CO = Calibrated Output, valid when coil_freq = 3)

SIGNAL OUT OF RANGE

Included in each of the A1346 die is a diagnostic feature, Signal Out of Range, to detect erroneous clamping of digital signal path as a result of external magnetic input signals. This feature also checks that the magnetic input does not exceed internal ADC range. The output responds to a Signal Out of Range diagnostic according to the settings in the EEPROM register, cfg_c and Table 7.

UNDERVOLTAGE DETECTION AND RESET

The A1346 contains circuitry to detect a condition when the supply voltage drops below the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{CC(UV)HIGH} - V_{CC(UV)LOW}$. As an example, initially V_{CC} and V_{OUT} are within the normal operating range. If V_{CC} drops below $V_{CC(UV)LOW}$, VOUT is forced to a state defined by the EEPROM register, cfg_c. When V_{CC} returns above $V_{CC(UV)HIGH}$, VOUT returns to its normal operating state. If V_{CC} drops below the internal reset level, $V_{CC(POR)LOW}$, the output is forced to a high-impedance state. When V_{CC} returns above the rising reset level, $V_{CC(POR)HIGH}$, the output responds according the undervoltage detection. The output will not respond with normal data until a delay of t_{PO} after a reset event.

OVERVOLTAGE DETECTION

The A1346 contains circuitry to detect a condition when the supply voltage rises above the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{CC(OV)HIGH} - V_{CC(OV)LOW}$. As an example, initially V_{CC} and V_{OUT} are within the normal operating range. If V_{CC} rises above $V_{CC(OV)HIGH}$, V_{OUT} is forced to a state defined by the EEPROM register, cfg_c. When V_{CC} returns below $V_{CC(OV)LOW}$, V_{OUT} returns to its normal operating state. The overvoltage detection is only enabled when the EEPROM lock bit is set. If the EEPROM lock bit is not set, and V_{CC} increases above $V_{CC(OV)HIGH}$, the device will enter programming mode and the output is forced to a high-impedance state. If V_{CC} rises above the high-voltage threshold, $V_{CC(HV)HIGH}$, the output is forced to a high-impedance state.

OVERTEMPERATURE DETECTION

The A1346 contains circuitry to detect a condition when the ambient temperature is greater than 160°C, which is outside of the operating range of the part. This will cause the output to respond according to the settings in the EEPROM register, cfg_c and Table 8.

BROKEN GROUND DETECTION

The A1346 contains circuitry to detect a condition when the ground connection is disconnected. When the ground connection is severed, the digital output driver turns off, forcing the output to a high-impedance state. See Table 5: Broken Wire Detection Conditions for more information.

EEPROM DIAGNOSTICS

The A1346 contains EEPROM with error checking and correction, ECC. The ECC corrects for a single EEPROM bit error without effecting device performance. The ECC also detects a dual bit EEPROM error and triggers an internal fault signal and forces the output to a state defined by the EEPROM register cfg_c.

Table 7: Diagnostic Summary Table

Diagnostic Detection	Conditions	V_{OUT} (PWM) diag_mode = 0	V_{OUT} (SENT) diag_mode = 0	V_{OUT} (SENT or PWM) diag_mode = 1	diag_reg_c (binary)	SENT Data Nibble #4 and #5 (sent_data_cfg = 1) (binary)
Overvoltage Condition	Overvoltage detection is enabled, diagnostic output is set for advanced output flag, and device lock is set, ovd_dis = 0, dev_lock = 3, 5, or 6.	½ carrier frequency 60% DC	See SENT, SCN nibble bit 1 = 1	High impedance	XXX1 XXXX	XXXX 1XXX
Undervoltage Condition	Undervoltage detection is enabled, and diagnostic output is set for advanced output flag, uvd_dis = 0.	½ carrier frequency 40% DC	See SENT, SCN nibble bit 1 = 1	High impedance	XXXX 1XXX	XXX1 XXXX
CoilBIST (Analog Signal Path) Error	CoilBIST enabled, and diagnostic output is set for advanced output flag, coilbist_dis = 0, coil_freq < 3.	½ carrier frequency 30% DC	See SENT, SCN nibble bit 0 = 1	High impedance	XXXX X1XX	XX1X XXXX
BIST Error (LBIST)	lbist_dis = 0	High impedance	High impedance	High impedance	XXXX XX1X	NA (High Impedance)
Overtemperature Condition	Overtemperature detection is enabled and diagnostic output is set for advanced output flag, otmp_dis = 0.	½ carrier frequency 70% DC	See SENT, SCN nibble bit 1 = 1	High impedance	XX1X XXXX	XXXX X1XX
Signal Out of Range, Low	Signal Out of Range detection is enabled, and diagnostic output is set for advanced output flag, oor_dis = 0.	½ carrier frequency 80% DC	See SENT, SCN nibble bit 1 = 1	High impedance	X1XX XXXX	XXXX XX1X
Signal Out of Range, High	Signal Out of Range detection is enabled, and diagnostic output is set for advanced output flag, oor_dis = 0.	½ carrier frequency 90% DC	See SENT, SCN nibble bit 1 = 1	High impedance	1XXX XXXX	XXXX XXX1
EEPROM Fault (2 bit error detection)		High impedance	High impedance	High impedance	XXXX XXX1	NA (High Impedance)

Linear Output Protocols

The A1346 operating output is a digital voltage signal that transfers information proportionally to the applied magnetic input signal. Few customer-selectable options are provided for output signal formatting: pulse-width-modulated (PWM), and variations of single-edge nibble transmission encoding scheme (SENT, SAEJ2716).

Note:

The device response to the applied magnetic field is on the OUT pin. However, that pin is also used to transmit and receive data in response to a serial programming commands, during which the normal output operation is suppressed. Refer to the Programming Serial Interface section for more information. The EEPROM is described in the EEPROM Structure section. The output falling edge slew rate is adjustable using the outdrv_sel parameter. Adjusting this can improve EMC performance by reducing high-frequency currents. This parameter can also increase the output fall time and result in longer minimum pulse durations for serial communication or SENT transmission.

PWM OUTPUT MODE (outmsg_mode = 0000)

PWM involves converting the output voltage amplitude to a series of constant-frequency binary pulses, with the percentage of the of high portion of the pulse varied in direct proportion to the applied magnetic field.

The PWM output mode is configured by setting the following parameters in EEPROM:

- PWM option is EEPROM programmable (for programming parameters, see EEPROM Structure section)
- sent_pwm_rate sets the PWM carrier frequency based on the values in Table 14

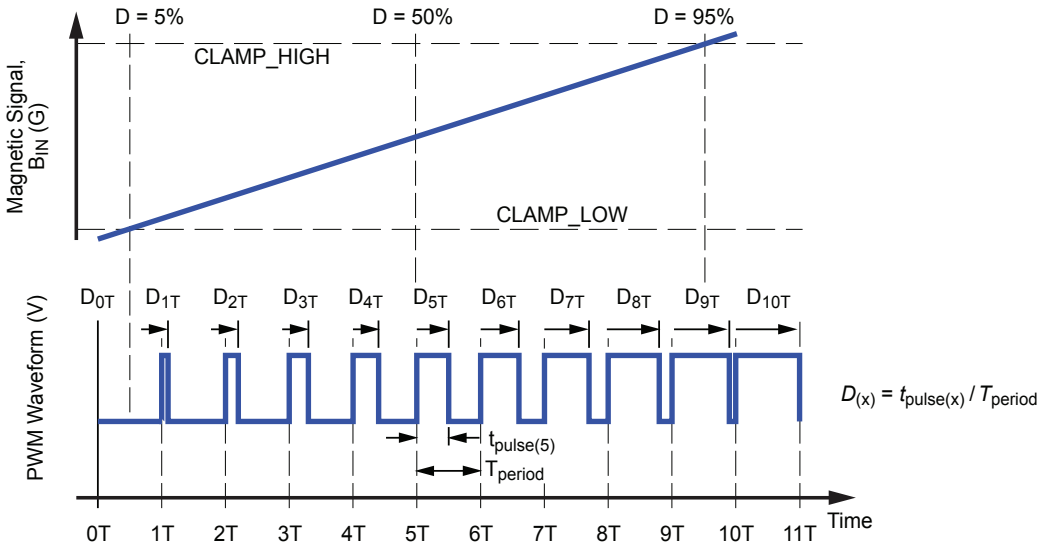

Figure 11: PWM Mode Duty-Cycle-Based Waveform

PWM mode outputs a duty-cycle-based waveform that can be read by the external controller as a cumulatively changing continuous voltage.

Initiation of the BIST is done through the external controller request and explained in Table 8 and Figure 12.

Table 8: External BIST Request and SENT Trigger Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Trigger Pulse Width	t_{trg}	Trigger Pulse for TSENT operation. See SSENT and ASENT sections for F_OUTPUT pulse durations.	1.8	–	–	µs
Synchronization Pulse Delay[1]	t_{dsync}		7	–	524	tick
External BIST Request Pulse Width	t_{dreq}	PWM	2	–	–	frame rate[2]
		SENT Modes	15	–	–	tick
BIST Delay	t_{diag}	Delay for device to execute internal BIST	10	–	20	ms

[1] t_{dsync} can increase from 7 ticks to preserve a minimum time of approximately 70 µs from the falling edge of the trigger to the start of the SCN nibble.
[2] The frame rate is determined by the sent_pwm_rate parameter.
[3] When in Trigger SENT Output mode the external controller must pull the output low after tdsync and before the first data nibble in the SENT frame, for a time of t_{dreq}, to initiate a BIST request.

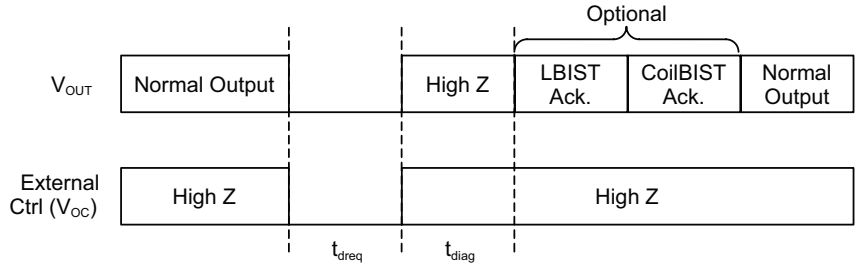

Figure 12: External BIST Request with PWM or Synchronous SENT Output Mode

SENT OUTPUT MODES

The SENT output mode converts the input magnetic signal to a binary value mapped to the Full Scale Output, FSO, range of 0 to 4095, shown in Figure 13. This data is inserted into a binary pulse message, referred to as a frame, that conforms to the SENT data transmission specification (SAEJ2716 JAN2010). Certain parameters for configuration of the SENT messages can be set in EEPROM.

The SENT output modes are selected by setting the following parameters in EEPROM:

- SAE J2716 SENT with enhancement options (outmsg_mode = 1)
- Triggered SENT – TSENT (outmsg_mode = 2) – User defines sampling and data retrieving.
- Sequential SENT – SSENT – User requests data from multiple devices on the SENT line in sequential order (outmsg_mode = 4 for short_trigger and outmsg_mode = 3 for long_trigger). Short and long trigger modes can be differentiated on the length and number of host function/request pulses.
- Addressable SENT – ASENT – User requests data from any device on the SENT line in any order. (outmsg_mode = 5-7)
- Additional configuration parameters in register 0x14, out_cfg_c.

MESSAGE STRUCTURE

A SENT message is a series of nibbles, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval
- The low interval, SENT_FIXED, is defined as 5 SENT ticks. The high interval contains information and is variable in duration to indicate the data payload of the nibble.

The duration of a nibble is denominated in clock ticks. The period of a tick is set by sent_pwm_rate parameter as in Table 14. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The nibbles of a SENT message are arranged in the following required sequence (see Figure 14):

1. Synchronization and Calibration: flags the start of the SENT message
2. Status and Communication: provides A1346 status and the format of the data
3. Data: magnetic field and optional data
4. CRC: error checking
5. Pause Pulse: sets timing relative to A1346 updates

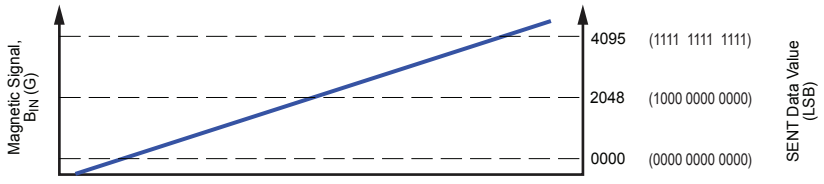

Figure 13: SENT Mode Output

SENT mode outputs a digital value that can be read by the external controller

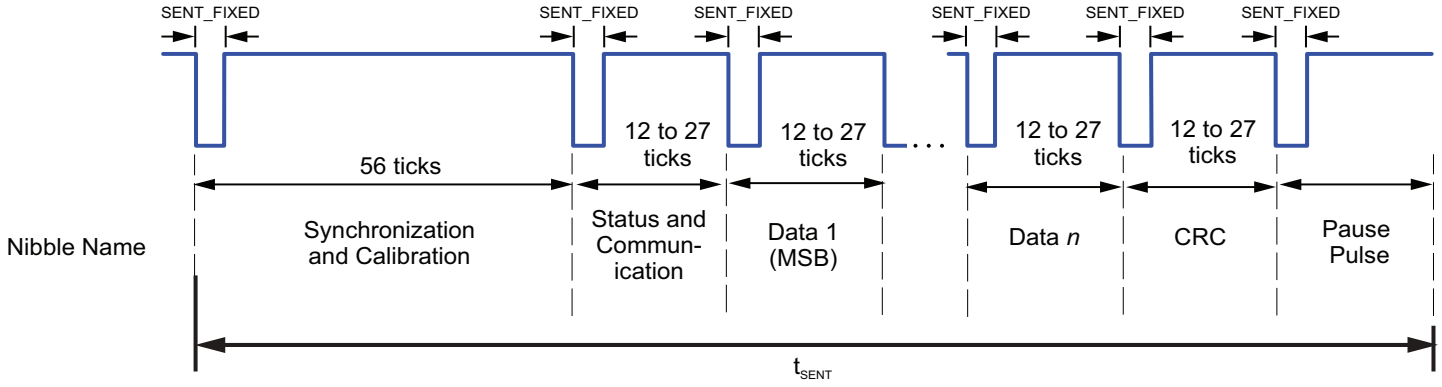

Figure 14: General Format for SENT Message Frame

OPTIONAL SHORT SERIAL MESSAGE

The A1346 SENT output supports an optional mode to transmit additional data. The slow serial mode, enables transmission of additional data by encoding information in the Status and Communication (SCN) nibbles. The encoded data is captured over several transmissions and is then decoded to indicate additional short serial message data. For more details on the short serial message please refer to the SENT SAEJ2716 specification. The slow serial mode is enabled when the EEPROM parameter sent_slow_ser_dis = 0. Following a reset, the first message transmitted is 0, following in order of the message ID until message 4, and then repeating. Table 10 identifies the data sent with each message ID. The CRC for the Short Serial Message is derived for the Message ID and data, and is the same checksum algorithm used for the SENT CRC.

Table 9: Short Serial Message Format in SENT Status and Communication Nibble

SCN Bit when sent_slow_ser_dis = 0	Nibble #															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Bit 3 (Start Bit)	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 2 (Serial Data)	Message ID				Data								CRC			
Bit 1 (Soft Error Diagnostic Bit)	See Table 7: Diagnostic Summary Table {Overvoltage, Undervoltage, Overtemperature, and Signal Out of Range Error Reporting}															
Bit 0 (Hard Error Diagnostic Bit)	See Table 7: Diagnostic Summary Table {CoilBIST Error}															

Table 10: SENT Slow Serial Data

Message ID	Data
0	Error status from the parameter diag_reg_c located in register err_status_c, 0x45 bits [23:16]. {EEPROM DBE, LBIST, Coil Measurement Monitor, Undervoltage, Overvoltage, Overtemperature, Signal out of range low, Signal out of range high}
1	8-bit temperature value from internal temperature sensor. Values are saturated to ±128°C, and 3 LSBs are rounded to nearest degree
2	id_c[7:0] (Customer ID, EEPROM 0x2)
3	id_c[15:8] (Customer ID, EEPROM 0x2)
4	id_c[23:16] (Customer ID, EEPROM 0x2)

In the case of SSENT and ASENT mode, SCN bits 2 and 3 can be selected to label the address of the sensor on the shared SENT line (sen_no_smsg =1, gives ID in SCN when the Short Serial Message is disabled by sent_slow_ser_dis = 1).

DATA NIBBLE FORMAT

The A1346 SENT output supports options for the message data nibble format. The data nibble format is determined by the EEPROM parameter sent_data_cfg. The options for either a minimum 3 or maximum 6 nibbles of data is defined in Table 11. Where:

- magout[11:0]: 12-bit magnetic output data.
- count[11:0]: SENT frame count. The counter increments once for every frame that is sent up to the maximum count. At the next count, after the maximum, the counter starts again at 0. The maximum count is 15 and 4095 for sent_data_cfg = 1 and sent_data_cfg = 2 respectively.
- temp_out[11:0]: 12-bit signed output from the internal temperature sensor. Ambient temperature (°C) = 12-bit signed temperature value / 8 (LSB / °C) + 25.
- diag[7:0] Diagnostic flags, EEPROM, LBIST, CoilBIST, Undervoltage, Overvoltage, Overtemperature, Signal out of range low, and Signal out of range high.

Table 11: SENT Data

sent_data_cfg	Data Nibble #1	Data Nibble #2	Data Nibble #3	Data Nibble #4	Data Nibble #5	Data Nibble #6	# of Nibbles
0	mag_out [11:8]	mag_out[7:4]	mag_out[3:0]	–	–	–	3
1	mag_out [11:8]	mag_out[7:4]	mag_out[3:0]	diag[7:4]	diag[3:0]	count[3:0]	6
2	mag_out[11:8]	mag_out[7:4]	mag_out[3:0]	count[11:8]	count[7:4]	count[3:0]	6
3	mag_out[11:8]	mag_out[7:4]	mag_out[3:0]	temp_out [11:8]	temp_out [7:4]	temp_out [3:0]	6

CHECKSUM (CRC) NIBBLE

The CRC consists of 4 bits derived from the data nibbles only. The CRC is calculated using the polynomial $x^4 + x^3 + x^2 + 1$ with a seed of 4'b0101. There is an option that SCN is included into the CRC nibble (sen_crc_has_scn = 1, includes SCN into CRC).

OUTPUT DRIVER FALL TIME SELECTION

User is allowed to change the fall time of the output digital signal using the EEPROM parameter outdrv_sel. See Table 12 below.

Table 12: Code vs C_{LOAD} for outdrv_sel

Function	Output Signal Configuration Sets configuration of the output signal slew-rate control. Sets the ramp rate on the gate of the output driver, thereby changing slew rate at the output.		
Syntax	Field width: 3 bits		
Related Commands	–		
Values	Code	Fall Time (Typical) (µs)	
		C_{LOAD} = 100 pF	C_{LOAD} = 1 nF
	0 (Default)	0.04	0.12
	1	0.10	0.17
	2	0.18	0.25
	3	0.26	0.33
	4	0.67	0.70
	5	1.35	1.29
	6	2.80	2.58
	7	4.02	3.73
Options	Values calculated from a small number of samples with a capacitor from output to ground to simulate load capacitance. $R_{L(PULLUP)}$ = 1.2 kΩ was used.		
Examples	–		

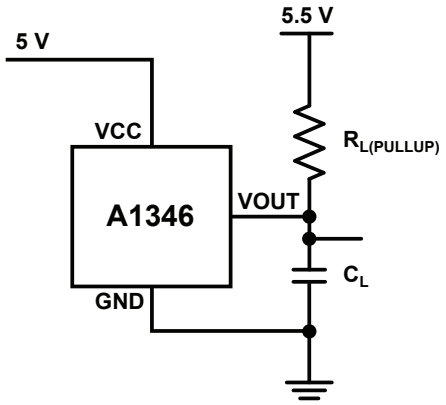

Figure 15: Fall Time Test Circuit

Table 13: Message Frame Section Definitions

Section	Description
SYNCHRONIZATION AND CALIBRATION	
Function	Provide the external controller with a detectable start of the message frame. The large quantity of ticks distinguishes this section, for ease of distinction by the external controller.
Syntax	Nibbles: 1 Quantity of ticks: 56 Quantity of bits: 1
STATUS AND COMMUNICATION	
Function	Provides the external controller with the status of the A1346 and indicates the format and contents of the Data section.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 Quantity of bits: 4 1:0 Device status (see Table 7) 3:2 Message serial data protocol (sent_slow_ser_dis)
DATA	
Function	Provides the external controller with data selected by the sent_data_cfg parameter.
Syntax	Nibbles: 3 to 6 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4 (each nibble)
CRC	
Function	Provides the external controller with cyclic redundancy check (CRC) data for certain error detection routines applied to the Data nibbles and to the Status information.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4
PAUSE PULSE	
Function	Additional time is added at the end of a SENT message frame to ensure all message frames are of appropriate length and correlate to the internal update rate of the device.
Syntax	Nibbles: NA Quantity of ticks: Quantity of bits: NA
TRIGGER PULSE	
Function	(Optional) Allow the external controller to determine when to transmit data
Syntax	Nibbles: NA Output must be held low a minimum of 1.8 µs after the pause pulse for TSENT. Defined by F_OUTPUT duration for SSENT and ASENT.

SAEJ2716 SENT AND TSENT

The A1346 SENT output is configurable for four (4) transmission modes, Internal Synchronous Mode, External Trigger Mode (TSENT), SSENT or ASENT. The transmission modes are configured by setting the parameter outmsg_mode.

When configured for Internal Synchronous Mode, outmsg_mode = 1, the SENT output transmits continuously, while in normal operating conditions. The SENT message frame rate is correlated to the internal update rate of the device (see Figure 17). The pause pulse is extended to correlate with the next available sample.

When configured for External Trigger Mode, outmsg_mode = 2, the SENT output transmits when requested by the external controller (see Figure 18). The pause pulse is extended until the next trigger pulse.

The external controller initiates a trigger pulse by holding the output pin low. The data sample is latched at the next internal update, 128 kHz, after the falling edge of the trigger pulse. The SENT frame is transmitted when external controller releases the output, the rising edge of the trigger pulse. After the rising edge of the trigger pulse the output remains high for minimum of seven SENT tick times before going low to initiate the start of the SENT synchronization pulse. For the fastest SENT rates, the start of the SENT synchronization pulse may be delayed longer than seven ticks to allow enough time for signal processing of the latched data. This is done to preserve a minimum time of 70.4 µs from the falling edge of the trigger pulse to end of the sync pulse, required for internal signal processing.

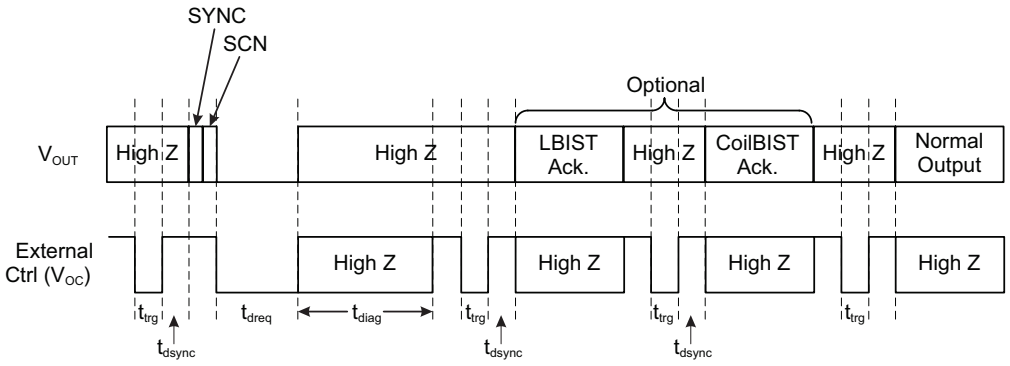

Figure 16: External BIST Request with Triggered SENT Output Mode

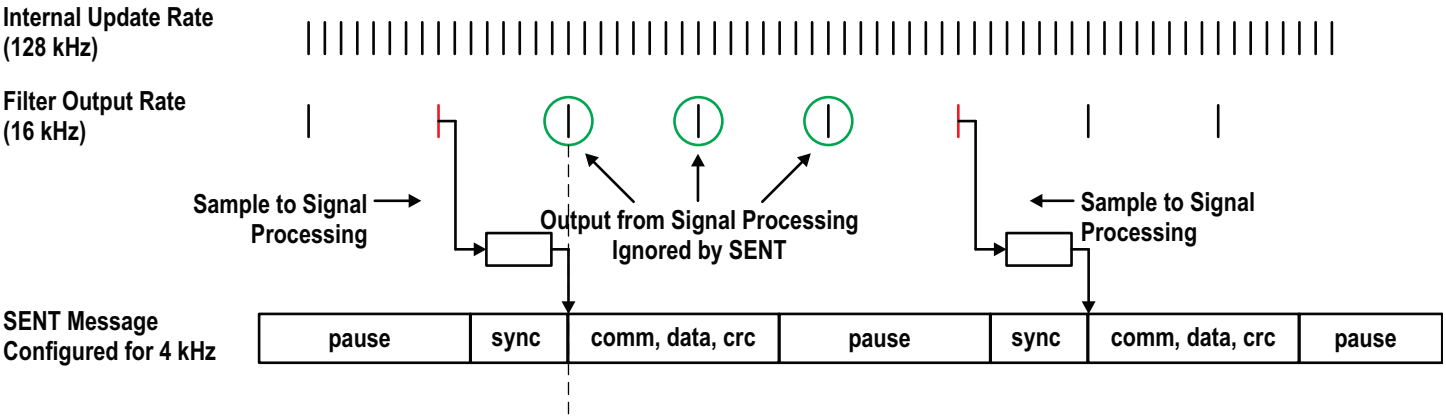

Figure 17: SENT Synchonization with Output Data and Internal Synchonous Mode

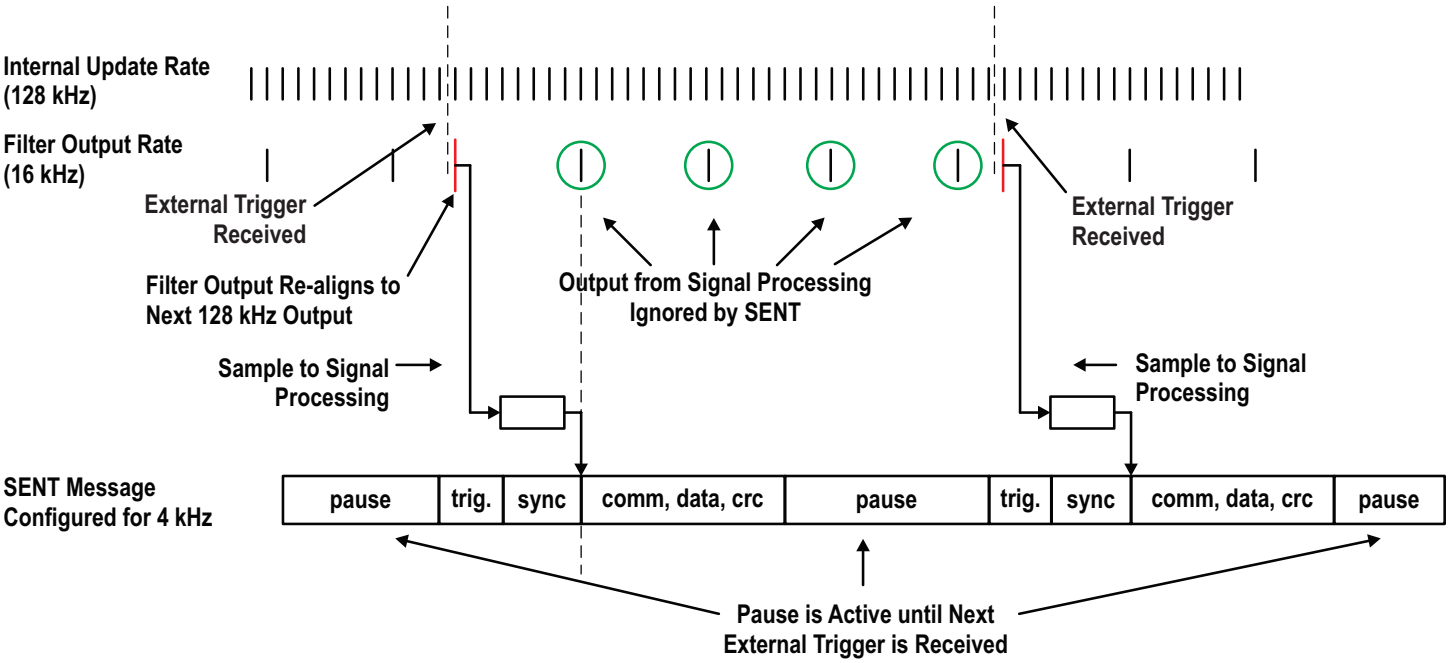

Figure 18: SENT Synchonization with Output Data and External Trigger Mode