
Chipsmall
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采购部

Low Noise, High Precision, Programmable Linear Hall Effect Sensor IC With Advanced Temperature Compensation and High Bandwidth (120 kHz) Analog Output

FEATURES AND BENEFITS

- Proprietary segmented linear interpolated temperature compensation (TC) technology provides a typical accuracy of 1% across the full operating temperature range
- Customer programmable, high resolution offset and sensitivity trim
- Factory programmed sensitivity and quiescent output voltage TC with extremely stable temperature performance
- High sensitivity Hall element for maximum accuracy
- Extremely low noise and high resolution achieved via proprietary Hall element and low noise amplifier circuits
- 120 kHz nominal bandwidth achieved via proprietary packaging and chopper stabilization techniques
- Patented circuits suppress IC output spiking during fast current step inputs

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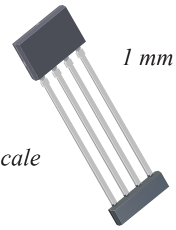
Package: 4-pin SIP (suffix KT)



1 mm case thickness

Not to scale

DESCRIPTION

The Allegro™ A1363 programmable linear Hall-effect current sensor IC has been designed to achieve high accuracy and resolution without compromising bandwidth. The goal is achieved through new proprietary linearly interpolated temperature compensation technology that is programmed at the Allegro factory and provides sensitivity and offset that are virtually flat across the full operating temperature range. Temperature compensation is done in the digital domain with integrated EEPROM technology, without sacrificing the analog signal path 120 kHz bandwidth, making this device ideal for HEV inverter, DC-to-DC converter, and electric power steering (EPS) applications.

This ratiometric Hall-effect sensor IC provides a voltage output that is proportional to the applied magnetic field. The customer can conFigure the sensitivity and quiescent (zero field) output voltage through programming on the VCC and output pins, to optimize performance in the end application. The quiescent output voltage is user-adjustable around 50% of the supply voltage, V_{CC}, and the output sensitivity is adjustable within the range of 0.6 to 14 mV/G.

The sensor IC incorporates a highly sensitive Hall element with a BiCMOS interface integrated circuit that employs a low noise small-signal high-gain amplifier, a clamped low-impedance

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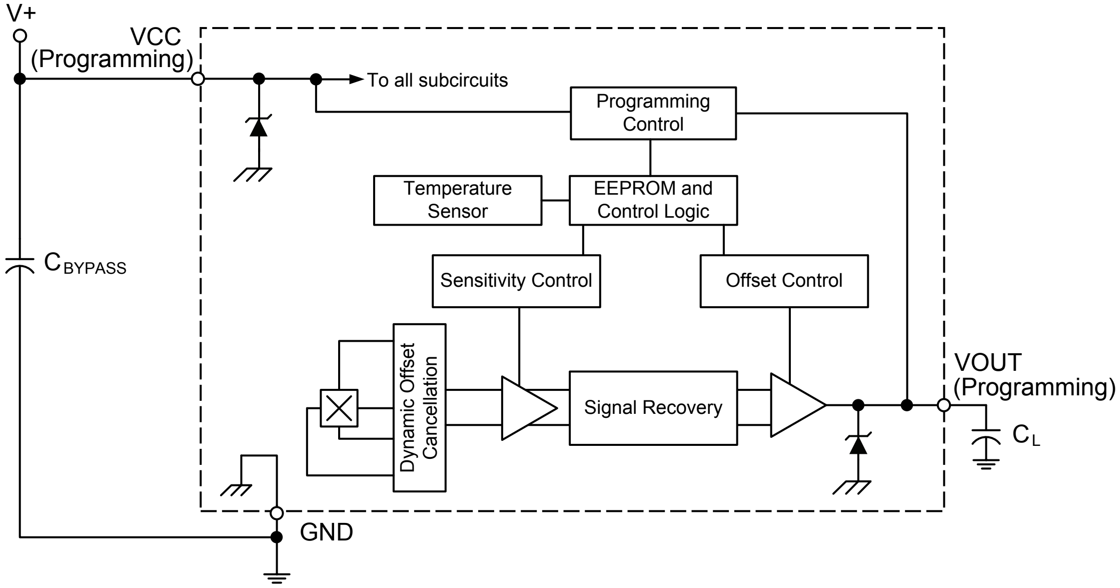


Functional Block Diagram

Features and Benefits (continued)

- Open circuit detection on ground pin (broken wire)
- Undervoltage lockout for V_{CC} below specification
- Selectable sensitivity range between 0.6 and 14 mV/G through use of coarse sensitivity programming bits
- Ratiometric sensitivity, quiescent voltage output, and clamps for interfacing with application A-to-D converter (ADC)
- Precise recoverability after temperature cycling
- Output voltage clamps provide short circuit diagnostic capabilities
- Wide ambient temperature range: –40°C to 150°C
- Immune to mechanical stress
- Extremely thin package: 1 mm case thickness
- AEC Q-100 automotive qualified

Description (continued)

output stage, and a proprietary, high bandwidth dynamic offset cancellation technique. These advances in Hall-effect technology work together to provide an industry leading sensing resolution at the full 120 kHz bandwidth. Broken ground wire detection as well as user-selectable output voltage clamps also are built into this device, for high reliability in automotive applications.

Device parameters are specified across an extended ambient temperature range: –40°C to 150°C. The A1363 sensor IC is provided in an extremely thin case (1 mm thick), 4-pin SIP (single in-line package, suffix KT) that is lead (Pb) free, with 100% matte tin lead frame plating.

Selection Guide

Part Number	Packing[1]	Sensitivity Range[2] (mV/G)
A1363LKTTN-1-T	4000 pieces per 13-in. reel	SENS_COARSE 00: 0.6 to 1.3
A1363LKTTN-2-T	4000 pieces per 13-in. reel	SENS_COARSE 01: 1.3 to 2.9
A1363LKTTN-5-T	4000 pieces per 13-in. reel	SENS_COARSE 10: 2.9 to 6.4
A1363LKTTN-10-T	4000 pieces per 13-in. reel	SENS_COARSE 11: 6.4 to 14

[1] Contact Allegro for additional packing options

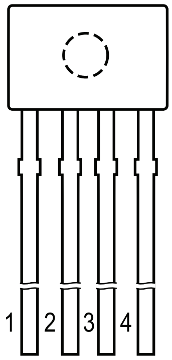
[2] Allegro recommends against changing Coarse Sensitivity settings when programming devices that will be used in production. Each A1363 has been Factory Temperature Compensated at a specific Sensitivity Range and changing coarse bits setting could cause sensitivity drift through temperature range ,$\Delta Sens_{TC}$, to exceed specified limits..

Table of Contents

SPECIFICATIONS

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		6	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}		25	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Output Source Current	$I_{OUT(source)}$	VOUT to GND	10	mA
Output Sink Current	$I_{OUT(sink)}$	VCC to VOUT	10	mA
Maximum Number of EEPROM Write Cycles	$EEPROM_W(max)$		100	cycle
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	ºC
Storage Temperature	T_{stg}		–65 to 165	ºC
Maximum Junction Temperature	$T_J(max)$		165	ºC



Pin-out Diagram
(Ejector pin mark on opposite side)

Terminal List Table

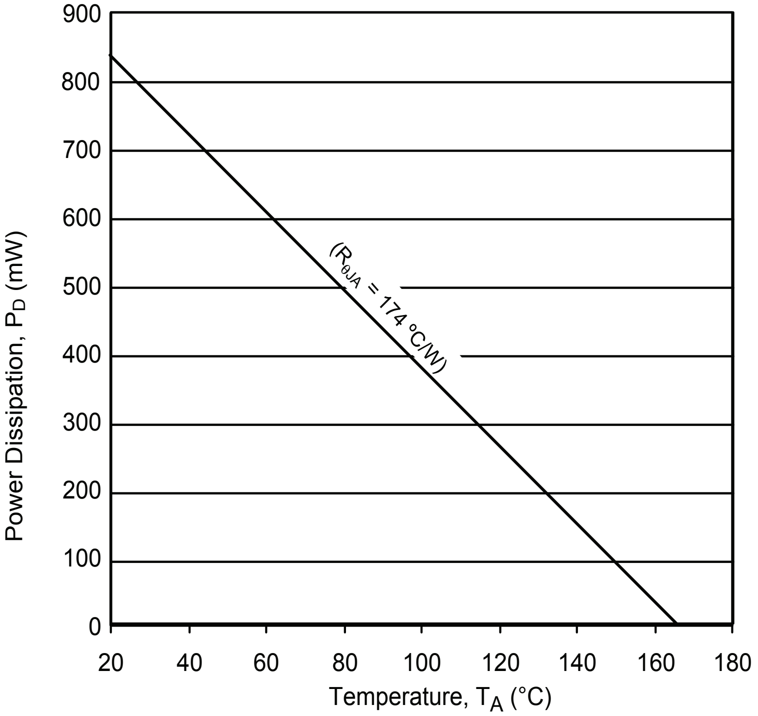
Number	Name	Function
1	VCC	Input power supply, use bypass capacitor to connect to ground; also used for programming
2	VOUT	Output signal, also used for programming
3	NC	No connection; connect to GND for optimal ESD performance
4	GND	Ground

Thermal Characteristics **may require derating at maximum conditions, see application information**

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 1-layer PCB with exposed copper limited to solder pads	174	ºC/W

*Additional thermal information available on the Allegro website

Power Dissipation versus Ambient Temperature



OPERATING CHARACTERISTICS: valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Electrical Characteristics						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	No load on VOUT	–	10	15	mA
Power-On Time[2]	t_{PO}	T_A = 25°C, C_{BYPASS} = Open, C_L = 1 nF, Sens = 2 mV/G, constant magnetic field of 400 G	–	78	–	µs
Temperature Compensation Power-On Time[2]	t_{TC}	T_A = 150°C, C_{BYPASS} = Open, C_L= 1 nF, Sens = 2 mV/G, constant magnetic field of 400 G	–	30	–	µs
Undervoltage Lockout (UVLO) Threshold[2]	V_{UVLOH}	T_A = 25°C, V_{CC} rising and device function enabled	–	4	–	V
	V_{UVLOL}	T_A = 25°C, V_{CC} falling and device function disabled	–	3.5	–	V
UVLO Enable/Disable Delay Time[2]	t_{UVLOE}	T_A = 25°C, C_{BYPASS} = Open, C_L = 1 nF, Sens = 2 mV/G, V_{CC} Fall Time (5 V to 3 V) = 1.5 µs	–	64	–	µs
	t_{UVLOD}	T_A = 25°C, C_{BYPASS} = Open, C_L = 1 nF, Sens = 2 mV/G, V_{CC} Recover Time (3 V to 5 V) = 1.5 µs	–	14	–	µs
Power-On Reset Voltage[2]	V_{PORH}	T_A = 25°C, V_{CC} rising	–	2.6	–	V
	V_{PORL}	T_A = 25°C, V_{CC} falling	–	2.3	–	V
Power-On Reset Release Time[2]	t_{PORR}	T_A = 25°C, V_{CC} rising	–	64	–	µs
Supply Zener Clamp Voltage	V_z	T_A = 25°C, I_{CC} = 30 mA	6.5	7.5	–	V
Internal Bandwidth	BW_i	Small signal –3 dB, C_L = 1 nF, T_A = 25°C	–	120	–	kHz
Chopping Frequency[3]	f_C	T_A = 25°C	–	500	–	kHz
Output Characteristics						
Propagation Delay Time[2]	t_{PD}	T_A = 25°C, magnetic field step of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	2.2	–	µs
Rise Time[2]	t_R	T_A = 25°C, magnetic field step of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	3.6	–	µs
Response Time[2]	$t_{RESPONSE}$	T_A = 25°C, magnetic field step of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	3.7	–	µs
Delay to Clamp[2]	t_{CLP}	T_A = 25°C, Step magnetic field from 800 to 1200 G, C_L = 1 nF, Sens = 2 mV/G	–	10	–	µs
Output Voltage Clamp[4]	$V_{CLP(HIGH)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	4.55	–	4.85	V
	$V_{CLP(LOW)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	0.15	–	0.45	V
Output Saturation Voltage[2]	$V_{SAT(HIGH)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	4.7	–	–	V
	$V_{SAT(LOW)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	–	–	400	mV
Broken Wire Voltage[2]	$V_{BRK(HIGH)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	–	V_{CC}	–	V
	$V_{BRK(LOW)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	–	100	–	mV

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OPERATING CHARACTERISTICS (continued): valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Output Characteristics (continued)						
Noise[5]	V_N	T_A = 25°C, CL = 1 nF, BW_f = BW_i	–	1.1	–	$mG_{RMS}/\sqrt{(Hz)}$
		T_A = 25°C, CL = 1 nF, Sens = 2 mV/G, BW_f = BW_i	–	6.3	–	$mV_{p\text{-}p}$
		T_A = 25°C, CL = 1 nF, Sens = 2 mV/G, BW_f = BW_i	–	1	–	mV_{RMS}
DC Output Resistance	R_{OUT}		–	9	–	Ω
Output Load Resistance	$R_{L(PULLUP)}$	VOUT to VCC	4.7	–	–	kΩ
	$R_{L(PULLDWN)}$	VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance[6]	C_L	VOUT to GND	–	1	10	nF
Output Slew Rate[7]	SR	Sens = 2 mV/G, C_L = 1 nF	–	230	–	V/ms
Quiescent Voltage Output ($V_{OUT(Q)}$)[2]						
Initial Unprogrammed Quiescent Voltage Output[2,8]	$V_{OUT(Q)init}$	T_A = 25°C	2.4	2.5	2.6	V
Quiescent Voltage Output Programming Range[2,4,9]	$V_{OUT(Q)PR}$	T_A = 25°C	2.3	–	2.7	V
Quiescent Voltage Output Programming Bits[10]	QVO		–	9	–	bit
Average Quiescent Voltage Output Programming Step Size[2,11,12]	$Step_{VOUT(Q)}$	T_A = 25°C	1.9	2.3	2.8	mV
Quiescent Voltage Output Programming Resolution[2,13]	$Err_{PGVOUT(Q)}$	T_A = 25°C	–	±0.5 × $Step_{VOUT(Q)}$	–	mV
Sensitivity (Sens)[2]						
Initial Unprogrammed Sensitivity[8]	$Sens_{init}$	SENS_COARSE = 00, T_A = 25°C	–	1	–	mV/G
		SENS_COARSE = 01, T_A = 25°C	–	2.2	–	mV/G
		SENS_COARSE = 10, T_A = 25°C	–	4.7	–	mV/G
		SENS_COARSE = 11, T_A = 25°C	–	9.6	–	mV/G
Sensitivity Programming Range[4,9]	$Sens_{PR}$	SENS_COARSE = 00, T_A = 25°C	0.6	–	1.3	mV/G
		SENS_COARSE = 01, T_A = 25°C	1.3	–	2.9	mV/G
		SENS_COARSE = 10, T_A = 25°C	2.9	–	6.4	mV/G
		SENS_COARSE = 11, T_A = 25°C	6.4	–	14	mV/G

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OPERATING CHARACTERISTICS (continued): valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Sensitivity Programming (continued)						
Coarse Sensitivity Programming Bits[14]	SENS_ COARSE		–	2	–	bit
Fine Sensitivity Programming Bits[10]	SENS_FINE		–	9	–	bit
Average Fine Sensitivity Programming Step Size[2,11,12]	$Step_{SENS}$	SENS_COARSE = 00, T_A = 25°C	2.4	3.2	4.1	µV/G
		SENS_COARSE = 01, T_A = 25°C	5	6.6	8.5	µV/G
		SENS_COARSE = 10, T_A = 25°C	11	14.2	18	µV/G
		SENS_COARSE = 11, T_A = 25°C	22	29	38	µV/G
Sensitivity Programming Resolution[2,13]	Err_{PGSENS}	T_A = 25°C	–	±0.5 × $Step_{SENS}$	–	µV/G
Factory Programmed Sensitivity Temperature Coefficient						
Sensitivity Temperature Coefficient[2]	TC_{SENS}	T_A=150°C, T_A= –40°C, calculated relative to 25°C	–	0	–	%/°C
Sensitivity Drift Through Temperature Range[2,9,15,20]	$\Delta Sens_{TC}$	T_A = 25°C to 150°C	–2.5	–	2.5	%
		T_A = –40°C to 25°C	–3.0	–	3.0	%
Average Sensitivity Temperature Compensation Step Size	$Step_{SENSTC}$		–	< 0.3	–	%
Factory Programmed Quiescent Voltage Output Temperature Coefficient						
Quiescent Voltage Output Temperature Coefficient[2]	TC_{QVO}	T_A = 150°C, T_A = –40°C, calculated relative to 25°C	–	0	–	mV/°C
Quiescent Voltage Output Drift Through Temperature Range[2,9,15]	$\Delta V_{OUT(Q)TC}$	T_A = 25°C to 150°C	–15	–	15	mV
		T_A = –40°C to 25°C	–30	–	30	mV
Average Quiescent Voltage Output Temperature Compensation Step Size	$Step_{QVOTC}$		–	2.3	–	mV

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OPERATING CHARACTERISTICS (continued): valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Lock Bit Programming						
EEPROM Lock Bit	EELOCK		–	1	–	bit
Error Components						
Linearity Sensitivity Error[2,16]	Lin_{ERR}		–1	< ±0.25	1	%
Symmetry Sensitivity Error[2]	Sym_{ERR}		–1	< ±0.25	1	%
Ratiometry Quiescent Voltage Output Error[2,17]	$Rat_{ERRVOUT(Q)}$	Through supply voltage range (relative to V_{CC} = 5 V)	–1	0	1	%
Ratiometry Sensitivity Error[2,17]	$Rat_{ERRSens}$	Through supply voltage range (relative to V_{CC} = 5 V)	–1.5	< ±0.5	1.5	%
Ratiometry Clamp Error[2,18]	Rat_{ERRCLP}	Through supply voltage range (relative to V_{CC} = 5 V), T_A = 25°C	–	< ±1.0	–	%
Sensitivity Drift Due to Package Hysteresis[2]	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling, 25°C to 150°C and back to 25°C	–	–1.25 ± 1.25	–	%
Sensitivity Drift Over Lifetime[19]	$\Delta Sens_{LIFE}$	T_A = 25°C, shift after AEC Q100 grade 0 qualification testing	–	±1	–	%

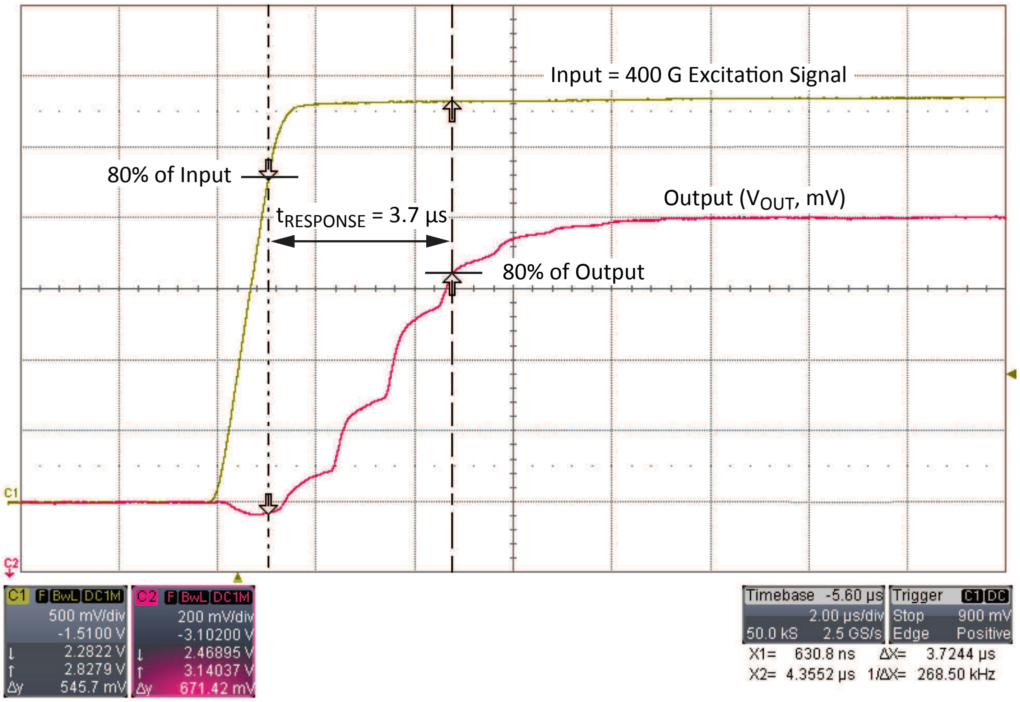
[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] See Characteristic Definitions section.
[3] f_C varies up to approximately ± 20% over the full operating ambient temperature range, T_A, and process.
[4] Sens, $V_{OUT(Q)}$, $V_{CLP(LOW)}$, and $V_{CLP(HIGH)}$ scale with V_{CC} due to ratiometry.
[5] Noise, measured in mV_{PP} and in mV_{RMS}, is dependent on the sensitivity of the device.
[6] Output stability is maintained for capacitive loads as large as 10 nF.
[7] High-to-low transition of output voltage is a function of external load components and device sensitivity.
[8] Raw device characteristic values before any programming.
[9] Exceeding the specified ranges will cause sensitivity and Quiescent Voltage Output drift through the temperature range to deteriorate beyond the specified values.
[10] Refer to Functional Description section.
[11] Step size is larger than required, in order to provide for manufacturing spread. See Characteristic Definitions section.
[12] Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{VOUT(Q)}$ or $Step_{SENS}$.
[13] Overall programming value accuracy. See Characteristic Definitions section.
[14] Each A1363 part number is factory programmed and temperature compensated at a different coarse sensitivity setting. Changing coarse bits setting could cause sensitivity drift through temperature range ,$\Delta Sens_{TC}$, to exceed specified limits.
[15] Allegro will be testing and temperature compensating each device at 150°C. Allegro will not be testing devices at –40°C. Temperature compensation codes will be applied based on characterization data.
[16] Linearity applies to output voltage ranges of ±2 V from the quiescent output for bidirectional devices.
[17] Percent change from actual value at V_{CC} = 5 V, for a given temperature, through the supply voltage operating range.
[18] Percent change from actual value at V_{CC} = 5 V, T_A = 25°C, through the supply voltage operating range.
[19] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits. Can not be guaranteed. Drift is a function of customer application conditions. Please contact Allegro MicroSystems for further information.
[20] Includes sensitivity drift due to package hysteresis observed during factory testing.

CHARACTERISTIC PERFORMANCE DATA

Response Time ($t_{RESPONSE}$)

400 G excitation signal with 10%-90% rise time = 1 µs

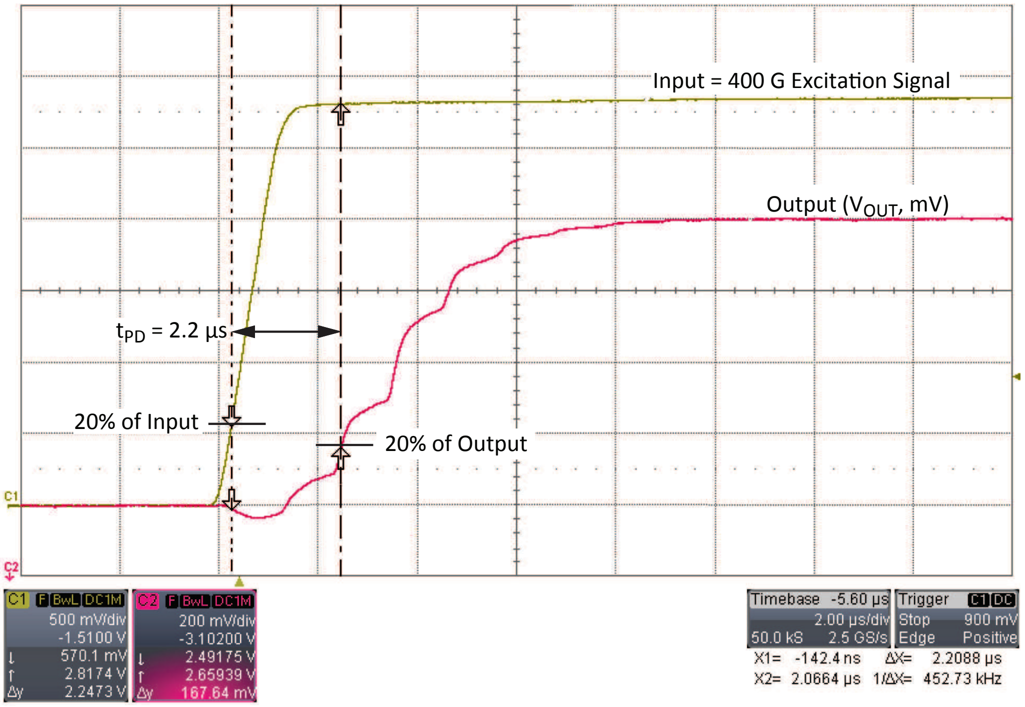
Sensitivity = 2 mV/G, C_{BYPASS}=0.1 µF, C_L=1 nF



Propagation Delay (t_{PD})

400 G excitation signal with 10%-90% rise time = 1 µs

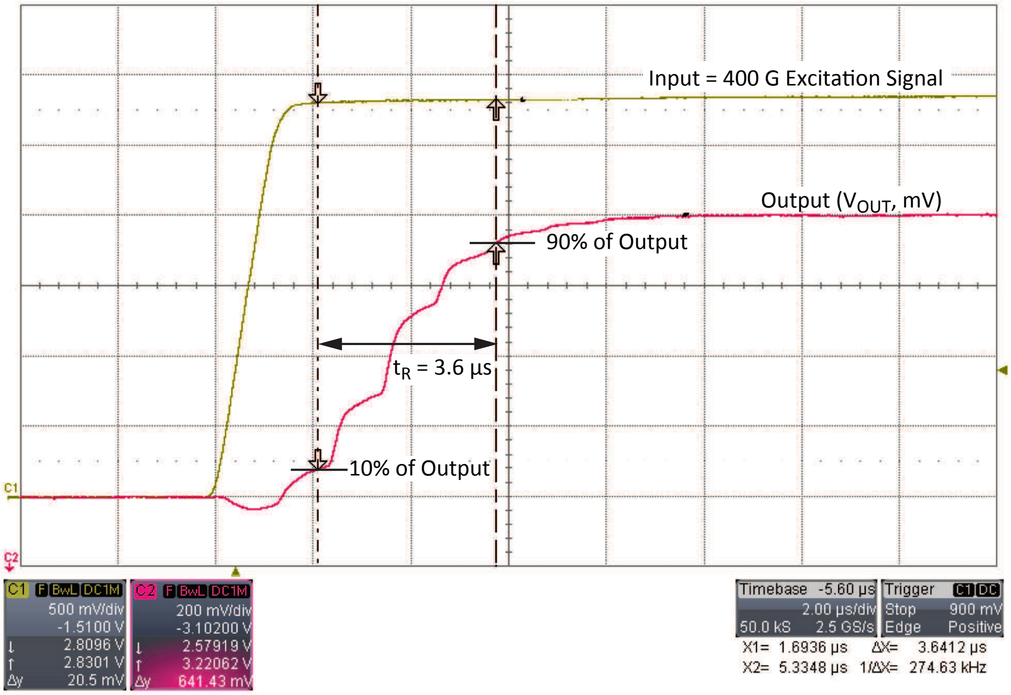
Sensitivity = 2 mV/G, C_{BYPASS}=0.1 µF, C_L=1 nF



Rise Time (t_R)

400 G excitation signal with 10%-90% rise time = 1 µs

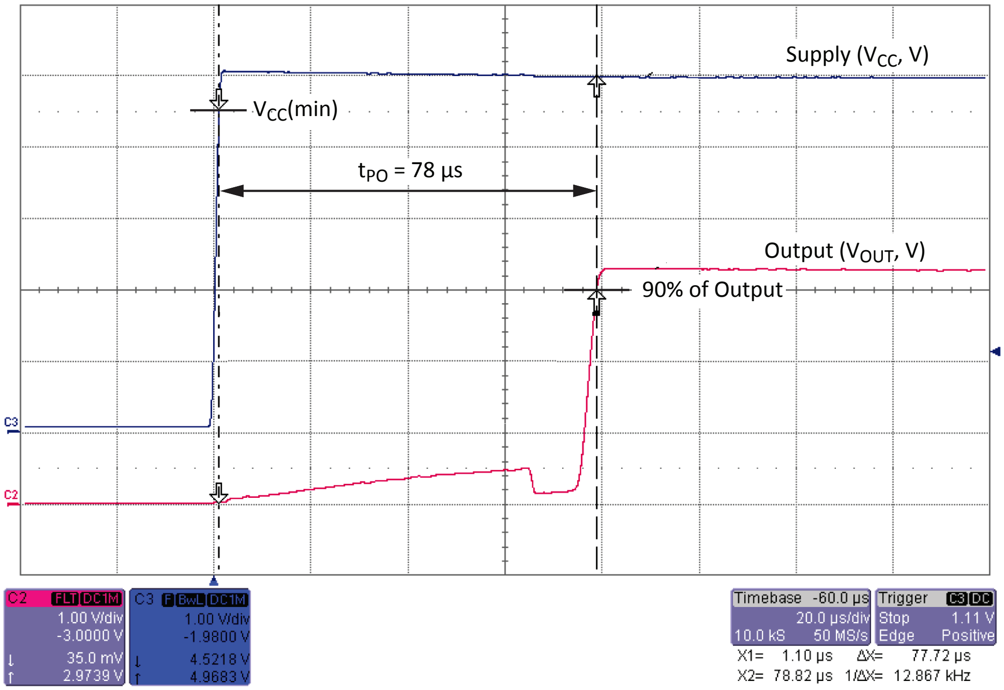
Sensitivity = 2 mV/G, C_{BYPASS}=0.1 µF, C_L=1 nF



Power-On Time (t_{PO})

400 G constant excitation signal, with V_{CC} 10%-90% rise time = 1.5 µs

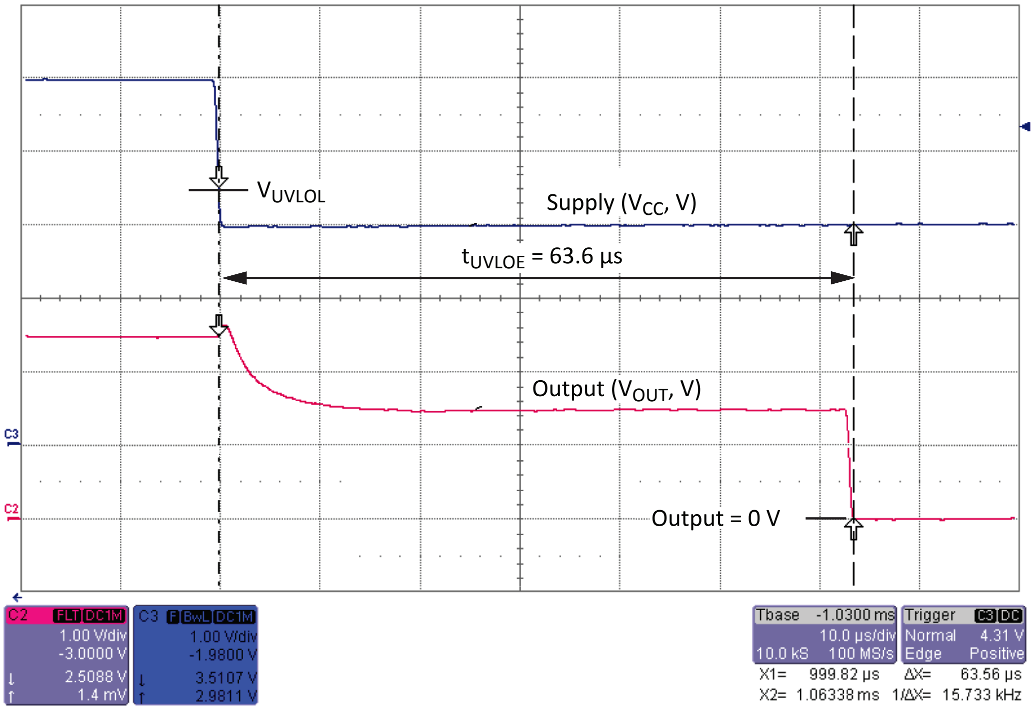
Sensitivity = 2 mV/G, C_{BYPASS}= Open, C_L=1 nF



UVLO Enable Time (t_{UVLOE})

V_{CC} 5 V-3 V fall time = 1.5 µs

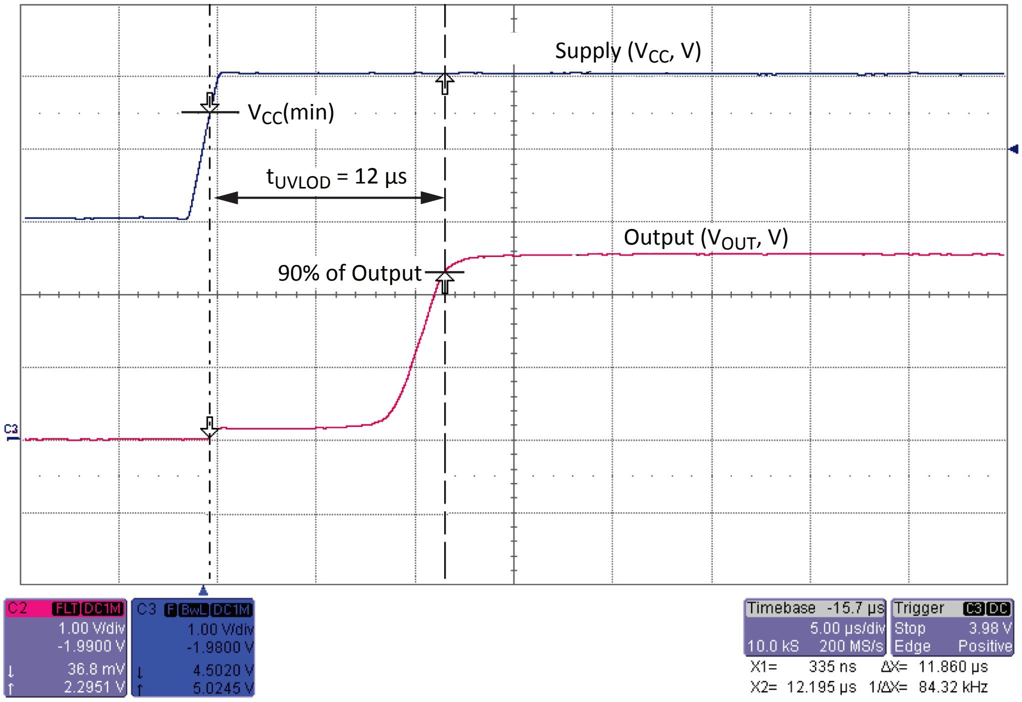
Sensitivity = 2 mV/G, C_{BYPASS}= Open, C_L=1 nF

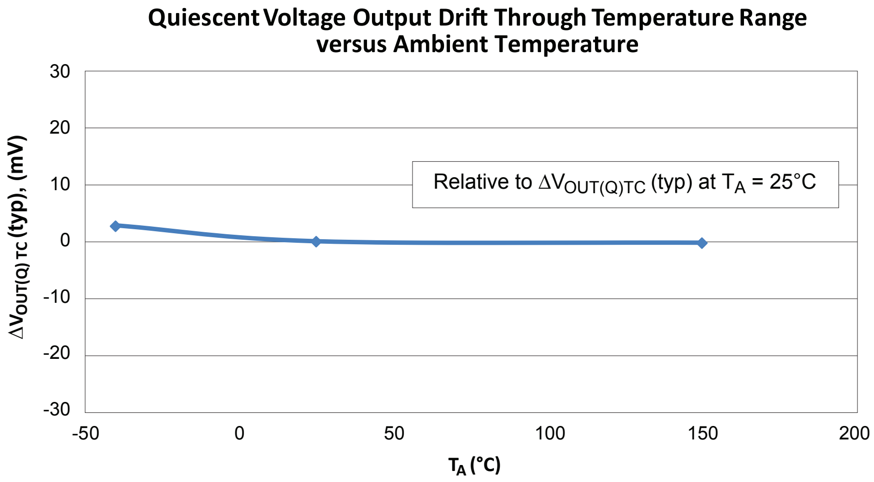


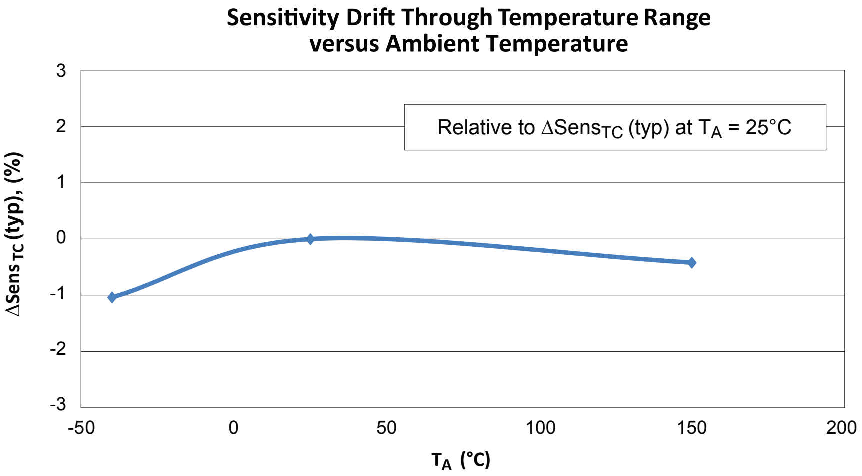
UVLO Disable Time (t_{UVLOD})

V_{CC} 3 V-5 V recovery time = 1.5 µs

Sensitivity = 2 mV/G, C_{BYPASS}= Open, C_L=1 nF




Quiescent Voltage Output Drift Through Temperature Range versus Ambient Temperature
30
20
10
0
-10
-20
-30
-50
0
50
100
150
200
ΔVOUT(Q)TC (typ), (mV)
TA (°C)
Relative to ΔVOUT(Q)TC (typ) at TA = 25°C


Sensitivity Drift Through Temperature Range versus Ambient Temperature
3
2
1
0
-1
-2
-3
-50
0
50
100
150
200
ΔSensTC (typ), (%)
TA (°C)
Relative to ΔSensTC (typ) at TA = 25°C

CHARACTERISTIC DEFINITIONS

Power-On Time (t_{PO})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Time, t_{PO}, is defined as: the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in Figure 1.

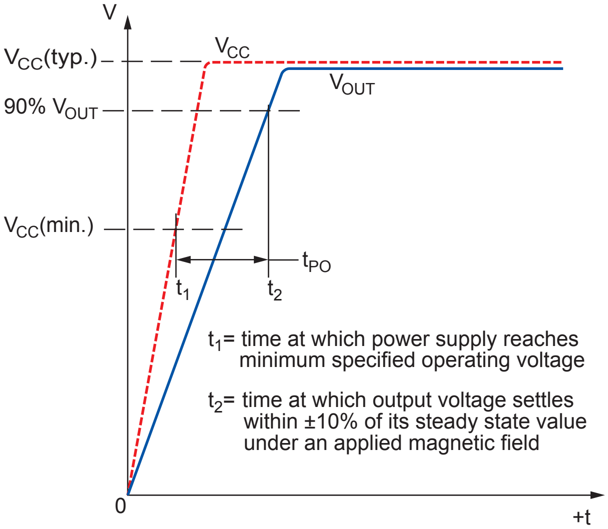


Figure 1. Power-on Time Definition

Temperature Compensation Power-On Time (t_{TC})

After Power-On Time, t_{PO}, elapses t_{TC} is also required before a valid temperature compensated output.

Propagation Delay (t_{PD})

The time interval between a) when the applied magnetic field reaches 20% of its final value, and b) when the output reaches 20% of its final value (see Figure 2).

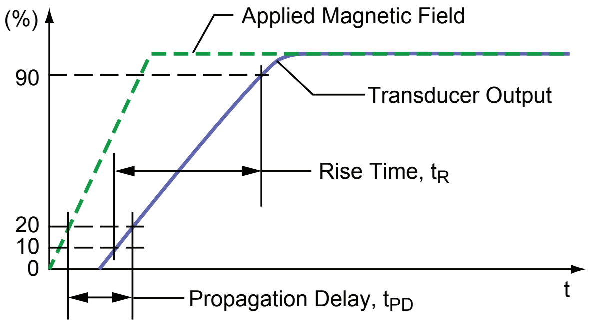


Figure 2: Propagation Delay and Rise Time Definitions

Rise Time (t_R)

The time interval between a) when the sensor IC reaches 10% of its final value, and b) when it reaches 90% of its final value (see Figure 2). Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

Response Time ($t_{RESPONSE}$)

The time interval between a) when the applied magnetic field reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied magnetic field (see Figure 3).

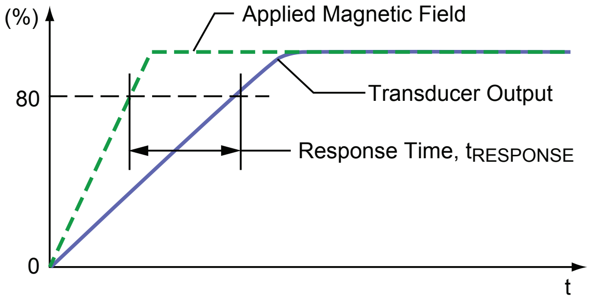


Figure 3: Response Time Definition

Delay to Clamp (t_{CLP})

A large magnetic input step may cause the clamp to overshoot its steady state value. The Delay to Clamp, t_{CLP}, is defined as: the time it takes for the output voltage to settle within ±1% of its steady state value, after initially passing through its steady state voltage, as shown in Figure 4.

Quiescent Voltage Output ($V_{OUT(Q)}$)

In the quiescent state (no significant magnetic field: B = 0 G), the output, $V_{OUT(Q)}$, has a constant ratio to the supply voltage, V_{CC}, throughout the entire operating ranges of V_{CC} and ambient temperature, T_A.

Initial Unprogrammed Quiescent Voltage Output ($V_{OUT(Q)init}$)

Before any programming, the Quiescent Voltage Output, $V_{OUT(Q)}$, has a nominal value of $V_{CC}/2$, as shown in Figure 5.

Quiescent Voltage Output Programming Range ($V_{OUT(Q)PR}$)

The Quiescent Voltage Output, $V_{OUT(Q)}$, can be programmed within the Quiescent Voltage Output Range limits: $V_{OUT(Q)PR}$ (min) and $V_{OUT(Q)PR}$ (max). Exceeding the specified Quiescent Voltage Output Range will cause Quiescent Voltage Output Drift Through Temperature Range $\Delta V_{OUT(Q)TC}$ to deteriorate beyond the specified values, as shown in Figure 5.

Average Quiescent Voltage Output Programming Step Size ($Step_{VOUT(Q)}$)

The Average Quiescent Voltage Output Progamming Step Size, $Step_{VOUT(Q)}$, is determined using the following calculation:

$$Step_{VOUT(Q)} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)mincode}}{2^{n}-1} \quad , \qquad (1)$$

where n is the number of available programming bits in the trim range, 9 bits, $V_{OUT(Q)maxcode}$ is at decimal code 255, and $V_{OUT(Q)mincode}$ is at decimal code 256.

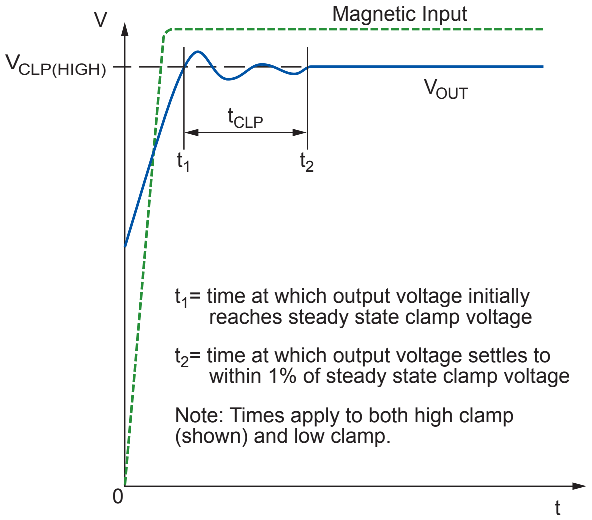


Figure 4: Delay to Clamp Definition

Quiescent Voltage Output Programming Resolution ($Err_{PGVOUT(Q)}$)

The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$Err_{PGVOUT(Q)}(typ) = 0.5 \times Step_{VOUT(Q)}(typ) \qquad (2)$$

Quiescent Voltage Output Temperature Coefficient (TC_{QVO})

Device $V_{OUT(Q)}$ changes as temperature changes, with respect to its programmed Quiescent Voltage Output Temperature Coefficient, TC_{QVO}. TC_{QVO} is programmed at 150°C, and calculated relative to the nominal $V_{OUT(Q)}$ programming temperature of 25°C. TC_{QVO} (mV/°C) is defined as:

$$TC_{QVO} = [V_{OUT(Q)T2} - V_{OUT(Q)T1}][1/(T2-T1)] \qquad (3)$$

where T1 is the nominal $V_{OUT(Q)}$ programming temperature of 25°C, and T2 is the TC_{QVO} programming temperature of 150°C. The expected $V_{OUT(Q)}$ through the full ambient temperature range, $V_{OUT(Q)EXPECTED(TA)}$, is defined as:

$$V_{OUT(Q)EXPECTED(TA)} = V_{OUT(Q)T1} + TC_{QVO}(T_A - T1) \qquad (4)$$

$V_{OUT(Q)EXPECTED(TA)}$ should be calculated using the actual measured values of $V_{OUTQ)T1}$ and TC_{QVO} rather than programming target values.

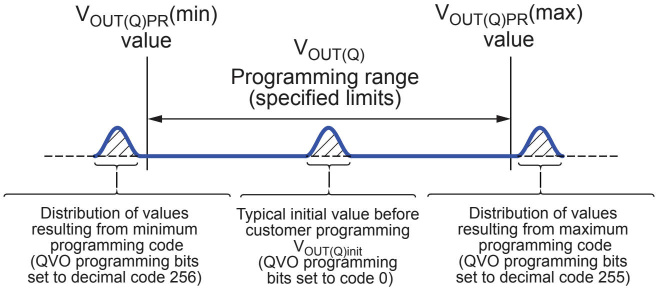


Figure 5: Quiescent Voltage Output Range Definition

Quiescent Voltage Output Drift Through Temperature Range ($\Delta V_{OUT(Q)TC}$)

Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output, $V_{OUT(Q)}$, may drift from its nominal value through the operating ambient temperature, T_A. The Quiescent Voltage Output Drift Through Temperature Range, $\Delta_{VOUT(Q)TC}$, is defined as:

$$\Delta V_{OUT(Q)TC} = V_{OUT(Q)(TA)} - V_{OUT(Q)EXPECTED(TA)} \qquad (5)$$

$\Delta V_{OUT(Q)TC}$ should be calculated using the actual measured values of $\Delta V_{OUT(Q)(TA)}$ and $\Delta V_{OUT(Q)EXPECTED(TA)}$ rather than programming target values.

Sensitivity (Sens)

The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.

Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mv/G), of the device, and it is defined as:

$$\text{Sens} = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{\text{BPOS} - \text{BNEG}} \,, \qquad (6)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

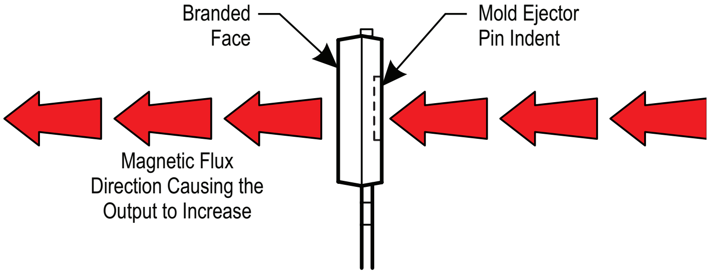


Figure 6: Magnetic Flux Direction

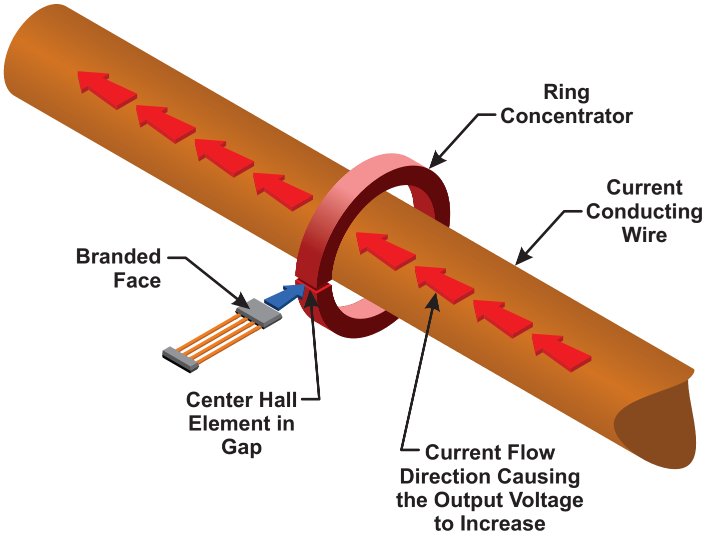


Figure 7: KT Sensor in Ring Concentrator

Initial Unprogrammed Sensitivity ($Sens_{init}$)

Before any programming, Sensitivity has a nominal value that depends on the SENS_COARSE bits setting. Each A1363 variant has a different SENS_COARSE setting.

Sensitivity Programming Range ($Sens_{PR}$)

The magnetic sensitivity, Sens, can be programmed around its initial value within the sensitivity range limits: $Sens_{PR}$(min) and $Sens_{PR}$(max). Exceeding the specified Sensitivity Range will cause Sensitivity Drift Through Temperature Range $\Delta Sens_{TC}$ to deteriorate beyond the specified values. Refer to the Quiescent Voltage Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Fine Sensitivity Programming Step Size ($Step_{SENS}$)

Refer to the Average Quiescent Voltage Output Programming Step Size section for a conceptual explanation.

Sensitivity Programming Resolution (Err_{PGSENS})

Refer to the Quiescent Voltage Output Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient (TC_{SENS})

Device sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, TC_{SENS}.

$\mathrm{TC_{SENS}}$ is programmed at 150°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. $\mathrm{TC_{SENS}}$ (%/°C) is defined as:

$$\mathrm{TC_{SENS}} = \left(\frac{\mathrm{Sens_{T2}} - \mathrm{Sens_{T1}}}{\mathrm{Sens_{T1}}} \times 100\%\right)\left(\frac{1}{T2-T1}\right) \quad , \qquad (7)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the $\mathrm{TC_{SENS}}$ programming temperature of 150°C. The expected value of Sens over the full ambient temperature range, $\mathrm{Sens_{EXPECTED(TA)}}$, is defined as:

$$\mathrm{Sens_{EXPECTED(TA)}} = \mathrm{Sens_{T1}} \times [100\% + \mathrm{TC_{SENS}}\,(T_A - T1)]\,. \qquad (8)$$

$\mathrm{Sens_{EXPECTED(TA)}}$ should be calculated using the actual measured values of $\mathrm{Sens_{T1}}$ and $\mathrm{TC_{SENS}}$ rather than programming target values.

Sensitivity Drift Through Temperature Range ($\Delta\mathrm{Sens_{TC}}$)

Second order sensitivity temperature coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range, T_A. The Sensitivity Drift Through Temperature Range, $\Delta\mathrm{Sens_{TC}}$, is defined as:

$$\Delta\mathrm{Sens_{TC}} = \frac{\mathrm{Sens_{TA}} - \mathrm{Sens_{EXPECTED(TA)}}}{\mathrm{Sens_{EXPECTED(TA)}}} \times 100\% \quad . \qquad (9)$$

Sensitivity Drift Due to Package Hysteresis ($\Delta\mathrm{Sens_{PKG}}$)

Package stress and relaxation can cause the device sensitivity at T_A = 25°C to change during and after temperature cycling. The sensitivity drift due to package hysteresis, $\Delta\mathrm{Sens_{PKG}}$, is defined as:

$$\Delta\mathrm{Sens_{PKG}} = \frac{\mathrm{Sens_{(25°C)2}} - \mathrm{Sens_{(25°C)1}}}{\mathrm{Sens_{(25°C)1}}} \times 100\% \quad , \qquad (10)$$

where $\mathrm{Sens_{(25°C)1}}$ is the programmed value of sensitivity at T_A = 25°C, and $\mathrm{Sens_{(25°C)2}}$ is the value of sensitivity at T_A = 25°C, after temperature cycling T_A up to 150°C and back to 25°C.

Linearity Sensitivity Error ($\mathrm{Lin_{ERR}}$)

The A1363 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error

Linearity Error is calculated separately for the positive ($\mathrm{Lin_{ERRPOS}}$) and negative ($\mathrm{Lin_{ERRNEG}}$) applied magnetic fields. Linearity Error (%) is measured and defined as:

$$\mathrm{Lin_{ERRPOS}} = \left(1 - \frac{\mathrm{Sens_{BPOS2}}}{\mathrm{Sens_{BPOS1}}}\right) \times 100\% \quad ,$$

$$\mathrm{Lin_{ERRNEG}} = \left(1 - \frac{\mathrm{Sens_{BNEG2}}}{\mathrm{Sens_{BNEG1}}}\right) \times 100\% \quad , \qquad (11)$$

where:

$$\mathrm{Sens}_{Bx} = \frac{|V_{\mathrm{OUT}(Bx)} - V_{\mathrm{OUT(Q)}}|}{B_x} \quad , \qquad (12)$$

and BPOSx and BNEGx are positive and negative magnetic fields, with respect to the quiescent voltage output such that |BPOS2| = 2 × |BPOS1| and |BNEG2| = 2 × |BNEG1|.

Then:

$$\mathrm{Lin_{ERR}} = \max(\mathrm{Lin_{ERRPOS}}\,,\, \mathrm{Lin_{ERRNEG}}) \quad . \qquad (13)$$

Symmetry Sensitivity Error ($\mathrm{Sym_{ERR}}$)

The magnetic sensitivity of an A1363 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry Error, $\mathrm{Sym_{ERR}}$ (%), is measured and defined as:

$$\mathrm{Sym_{ERR}} = \left(1 - \frac{\mathrm{Sens_{BPOS}}}{\mathrm{Sens_{BNEG}}}\right) \times 100\% \quad , \qquad (14)$$

where $\mathrm{Sens_{Bx}}$ is as defined in equation 12, and BPOSx and BNEGx are positive and negative magnetic fields such that |BPOSx| = |BNEGx|.

Ratiometry Error ($\mathrm{Rat_{ERR}}$)

The A1363 device features ratiometric output. This means that the Quiescent Voltage Output, $V_{\mathrm{OUT(Q)}}$, magnetic sensitivity, Sens, and Output Voltage Clamp, $V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$, are proportional to the Supply Voltage, V_{CC}. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in Quiescent Voltage Output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRVOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(5V)}}{V_{CC} / 5\text{ V}}\right) \times 100\% \quad (15)$$

The ratiometric error in magnetic sensitivity, $Rat_{ERRSens}$ (%), for a given Supply Voltage, V_{CC}, is defined as:

$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\text{ V}}\right) \times 100\% \quad . \quad (16)$$

The ratiometric error in the clamp voltages, Rat_{ERRCLP} (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRCLP} = \left(1 - \frac{V_{CLP(VCC)} / V_{CLP(5V)}}{V_{CC} / 5\text{ V}}\right) \times 100\% \quad , \quad (17)$$

where V_{CLP} is either $V_{CLP(HIGH)}$ or $V_{CLP(LOW)}$.

Power-On Reset Voltage (V_{POR})

On power-up, to initialize to a known state and avoid current spikes, the A1363 is held in Reset state. The Reset signal is disabled when V_{CC} reaches V_{UVLOH} and time t_{PORR} has elapsed, allowing output voltage to go from a high impedance state into normal operation. During power-down, the Reset signal is enabled when V_{CC} reaches V_{PORL}, causing output voltage to go into a high impedance state. (Note that detailed description of POR and UVLO operation can be found in the Functional Description section).

Power-On Reset Release Time (t_{PORR})

When V_{CC} rises to V_{PORH}, the Power-On Reset Counter starts. The A1363 output voltage will transition from a high impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR} and V_{CC} has exceeded V_{UVLOH}.

Undervoltage Lockout Threshold (VUVLO)

If V_{CC} drops below V_{UVLOL} output voltage will be locked to GND. If V_{CC} starts rising A1363 will come out of Lock state when V_{CC} reaches V_{UVLOH}.

UVLO Enable/Disable Delay Time (t_{UVLO})

When a falling V_{CC} reaches V_{UVLOL}, time t_{UVLOE} is required to engage Undervoltage Lockout state. When V_{CC} rises above V_{UVLOH}, time t_{UVLOD} is required to disable UVLO and have a valid output voltage.

Output Saturation Voltage (V_{SAT})

When output voltage clamps are disabled, output voltage can swing to a maximum of $V_{SAT(HIGH)}$ and to a minimum of $V_{SAT(LOW)}$.

Broken Wire Voltage (V_{BRK})

If the GND pin is disconnected (broken wire event), output voltage will go to $V_{BRK(HIGH)}$ (if a load resistor is connected to VCC) or to $V_{BRK(LOW)}$ (if a load resistor is connected to GND).

FUNCTIONAL DESCRIPTION

Programming Sensitivity and Quiescent Voltage Output

Sensitivity and $V_{OUT(Q)}$ can be adjusted by programming SENS_FINE and QVO bits, as illustrated in Figures 8 and 9.

Customers should not program sensitivity or $V_{OUT(Q)}$ beyond the maximum or minimum programming ranges specified in the Operating Characteristics table. Exceeding the specified limits will cause sensitivity and $V_{OUT(Q)}$ drift through temperature range, $\Delta Sens_{TC}$ and $\Delta V_{OUT(Q)TC}$, to deteriorate beyond the specified values.

Programming sensitivity might cause a small drift in $V_{OUT(Q)}$. As a result, Allegro recommends programming sensitivity first, then $V_{OUT(Q)}$.

Coarse Sensitivity

Each A1363 variant is programmed to a different coarse sensitivity setting. Devices are tested and temperature compensation is factory programmed under that specific coarse sensitivity setting. If the coarse sensitivity setting is changed, by programming SENS_COARSE bits, Allegro can not guarantee the specified sensitivity drift through temperature range limits, $\Delta Sens_{TC}$.

Memory Locking Mechanisms

The A1363 is equipped with two distinct memory locking mechanisms:

DEFAULT LOCK

At power-up, all registers of the A1363 are locked by default. EEPROM and volatile memory cannot be read or written. To disable Default Lock, a very specific 30 bits customer access code has to be written to address 0x24 within Access Code Time Out, t_{ACC} = 8 ms, from power-up. At this point, registers can be accessed. If VCC is power cycled, the Default Lock will automatically be re-enabled. This ensures that during normal operation, memory content will not be altered due to unwanted glitches on VCC or the output pin.

LOCK BIT

After EEPROM has been programmed by the customer, the EELOCK bit can be set high and VCC power cycled to permanently disable the ability to read or write any register. This will prevent the ability to disable Default Lock using the method described above. Please note that after EELOCK bit is set high and VCC pin power cycled, the customer will not have the ability to clear the EELOCK bit or to read/write any register.

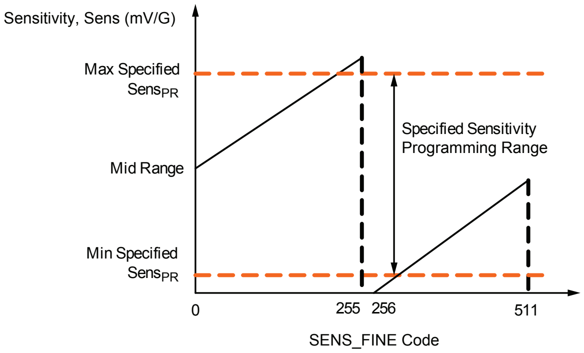


Figure 8. Device Sensitivity versus SENS_FINE Programmed Value

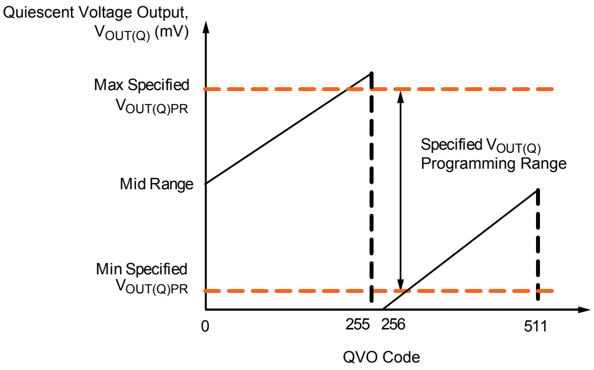


Figure 9. Device $V_{OUT(Q)}$ versus QVO Programmed Value

Power-On Reset (POR) and Undervoltage Lock-Out (UVLO) Operation

The descriptions in this section assume: temperature = 25°C, no output load (R_L, C_L), and no significant magnetic field is present.

POWER-UP

At power-up, as V_{CC} ramps up, the output is in a high impedance state. When V_{CC} crosses V_{PORH} (location [1] in Figure 10 and [1'] in Figure 11), the POR Release counter starts counting for t_{PORR}= 64 µs. At this point, if V_{CC} exceeds V_{UVLOH} = 4 V [2'], the output will go to V_{CC} / 2 after t_{UVLOD} = 14 µs [3']. If V_{CC} does not exceed V_{UVLOH} = 4 V [2], the output will stay in the high impedance state until V_{CC} reaches V_{UVLOH} = 4 V [3] and then will go to V_{CC} / 2 after t_{UVLOD} = 14 µs [4].

V_{CC} DROPS BELOW V_{CC}(MIN)= 4.5 V

If V_{CC} drops below V_{UVLOL} [4', 5], the UVLO Enable Counter starts counting. If V_{CC} is still below V_{UVLOL} when counter reaches t_{UVLOE} = 64 µs, the UVLO function will be enabled and the ouput will be pulled near GND [6]. If V_{CC} exceeds V_{UVLOL} before the UVLO Enable Counter reaches 64 µs [5'], the output will continue to be V_{CC}/2.

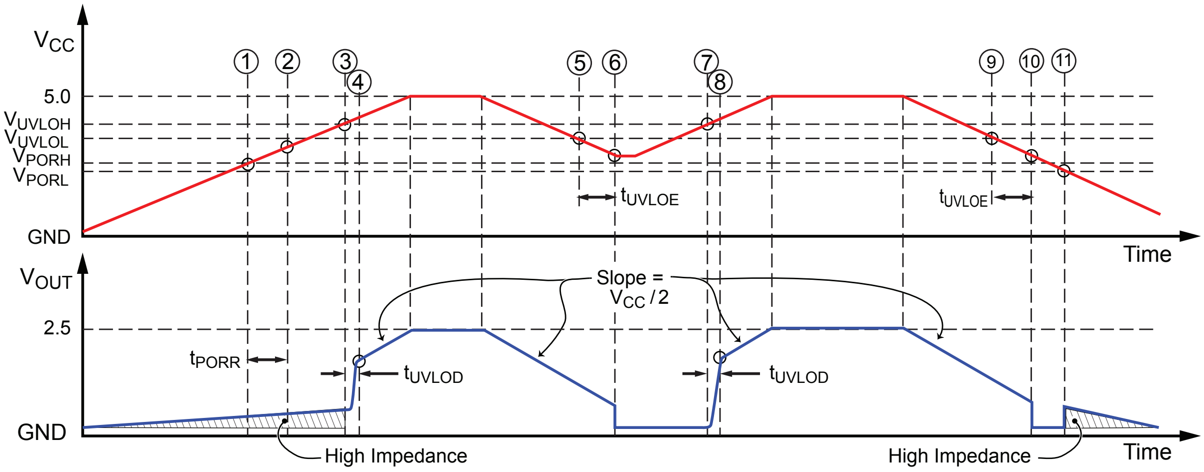


Figure 10. POR and UVLO Operation: Slow Rise Time Case

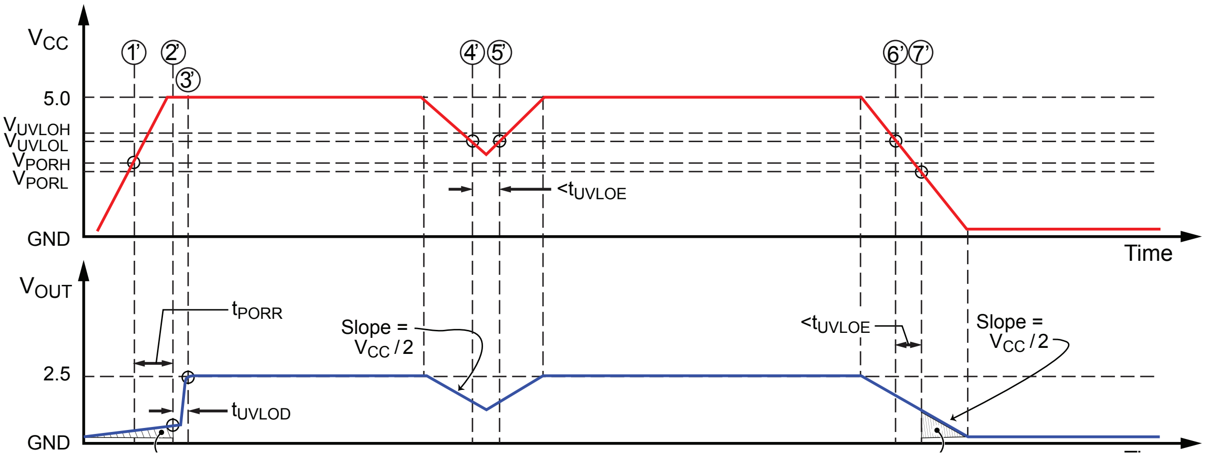


Figure 11: POR and UVLO Operation: Fast Rise Time Case

COMING OUT OF UVLO

While UVLO is enabled [6], if V_{CC} exceeds V_{UVLOH} [7], UVLO will be disabled after t_{UVLOD} =14 µs, and the output will be V_{CC} / 2 [8].

POWER-DOWN

As V_{CC} ramps down below V_{UVLOL} [6’, 9], the UVLO Enable Counter will start counting. If V_{CC} is higher than V_{PORL} = 2.3 V when the counter reaches t_{UVLOE} = 64 µs, the UVLO function will be enabled and the ouput will be pulled near GND [10]. The output will enter a high impedance state as V_{CC} goes below V_{PORL} [11]. If V_{CC} falls below V_{PORL} before the UVLO Enable Couner reaches 64 µs, the output will transition directly into a high impedance state [7'].

Detecting Broken Ground Wire

If the GND pin is disconnected, node A becoming open (figure 10), the VOUT pin will go to a high impedance state. Output voltage will go to $V_{BRK(HIGH)}$ if a load resistor $R_{L(PULLUP)}$ is connected to V_{CC} or to $V_{BRK(LOW)}$ if a load resistor $R_{L(PULLDWN)}$ is connected to GND. The device will not respond to any applied magnetic field.

If the ground wire is reconnected, A1363 will resume normal operation.

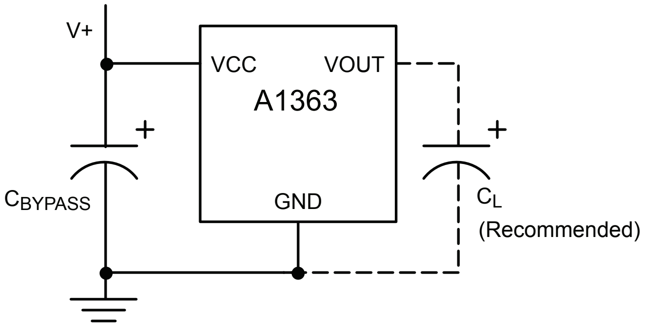
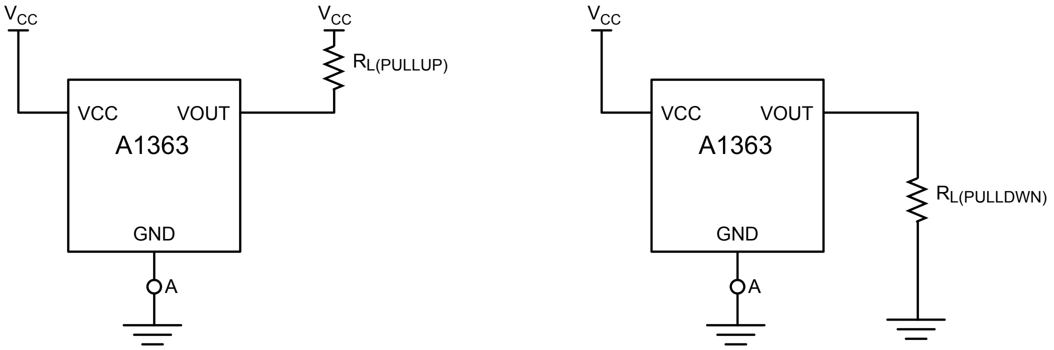


Figure 12: Typical Application Drawing



Connecting VOUT to $R_{L(PULLUP)}$

Connecting VOUT to $R_{L(PULLDWN)}$

Figure 13: Connections for Detecting Broken Ground Wire

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for total accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip.

The patented Allegro technique removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and a proprietary, dynamic notch filter. The new Allegro filtering techniques are far more effective at suppressing chopper induced signal noise compared to the previous generation of Allegro chopper stabilized devices.

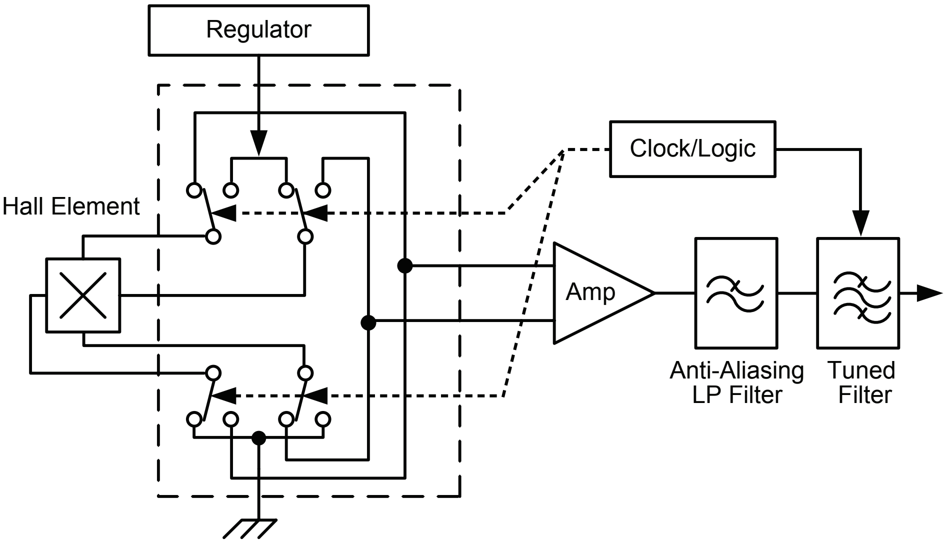


Figure 14: Concept of Chopper Stabilization

Programming Serial Interface

The A1363 incorporates a serial interface that allows an external controller to read and write registers in the EEPROM and volatile memory. The A1363 uses a point-to-point communication protocol, based on Manchester encoding per G. E. Thomas (a rising edge indicates 0 and a falling edge indicates 1), with address and data transmitted MSB first.

TRANSACTION TYPES

Each transaction is initiated by a command from the controller; the A1363 does not initiate any transactions. Three commands are recognized by the A1363: Write Access Code, Write, and Read. One response frame type is generated by the A1363, Read Acknowledge. If the command is Read, the A1363 responds by transmitting the requested data in a Read Acknowledge frame. If the command is any other type, the A1363 does not acknowledge. As shown in Figure 16, the A1363 receives all commands via the VCC pin. It responds to Read commands via the VOUT pin. This implementation of Manchester encoding requires the communication pulses be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages for the VCC line and the VOUT line. The Write command to EEPROM is supported by two high voltage pulses on the VOUT line.

WRITING THE ACCESS CODE

In order for the external controller to write or read from the A1363 memory during the current session, it must establish serial communication with the A1363 by sending a Write command including the Access Code within Access Code Time Out, t_{ACC}, from power-up. If this deadline is missed, all write and read access is disabled until the next power-up.

WRITING TO VOLATILE MEMORY

In order for the external controller to write to volatile memory, a Write command must be transmitted on the VCC pin. Successive Write commands to volatile memory must be separated by t_{WRITE}. The required sequence is shown in Figure 15.

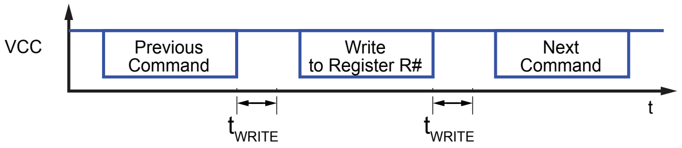


Figure 15: Writing to Volatile Memory

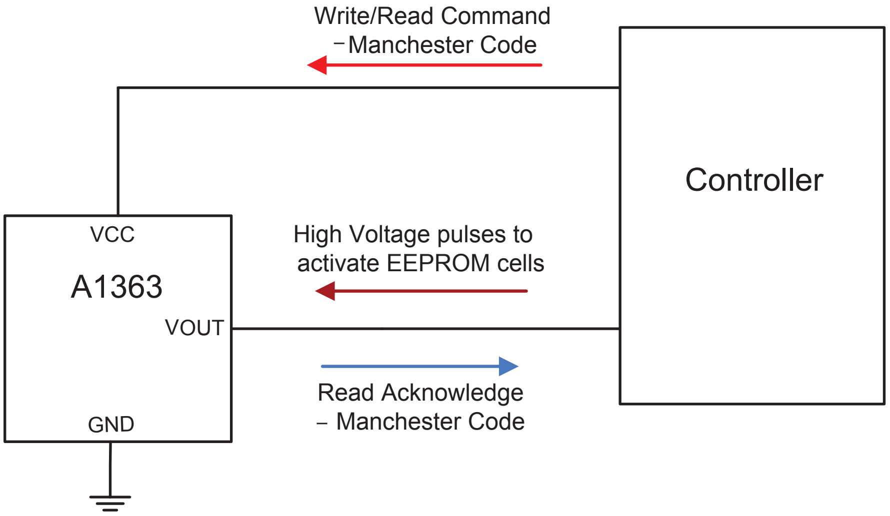


Figure 16: Top-level Programming Interface

WRITING TO EEPROM

In order for the external controller to write to non-volatile EEPROM, a Write command must be transmitted on the VCC pin. The controller must also send two Programming pulses, long high-voltage strobes, via the VOUT pin. These strobes are detected internally, allowing the A1363 to boost the voltage on the EEPROM gates. The required sequence is shown in Figures 17 and 18.

To ensure EEPROM integrity over life time, EEPROM should not be exposed to more than 100 Write cycles.

READING FROM EEPROM OR VOLATILE MEMORY

In order for the external controller to read from EEPROM or volatile memory, a Read command must be transmitted on the VCC line. Within time t_{start_read}, the VOUT line will stop responding to the magnetic field and the Read Acknowledge frame will be transmitted on the VOUT line. The Read Acknowledge frame contains Read data.

After the Read Acknowledge frame has been received from the A1363, the VOUT line resumes normal operation after time t_{READ}. The required sequence is shown in Figure 19.

ERROR CHECKING

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check). The CRC algorithm is based on the polynomial g(x) = x3 + x + 1 , and the calculation is represented graphically in Figure 20. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111. If the serial interface receives a command with a CRC error, the command is ignored.

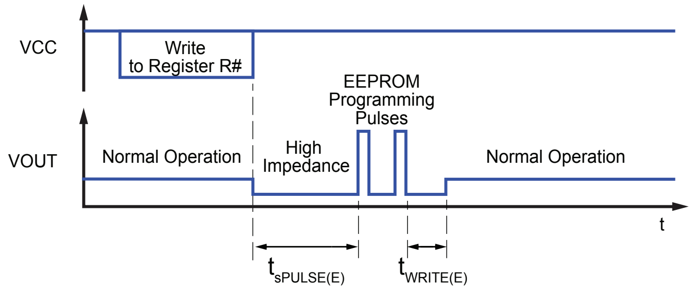


Figure 17: Writing to EEPROM

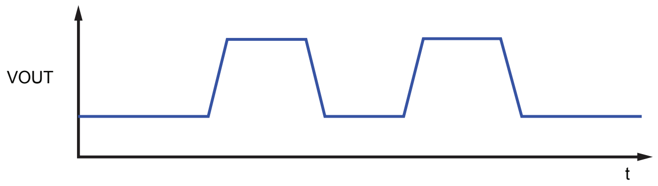


Figure 18: EEPROM Programming Pulses

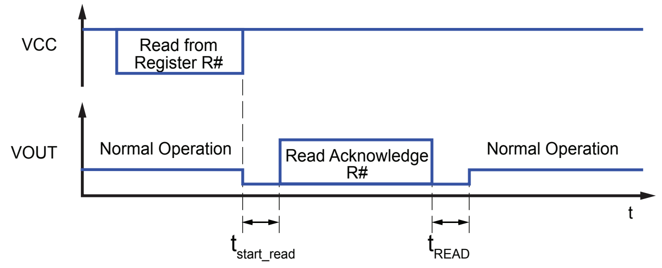


Figure 19: Reading from EEPROM or Volatile Memory

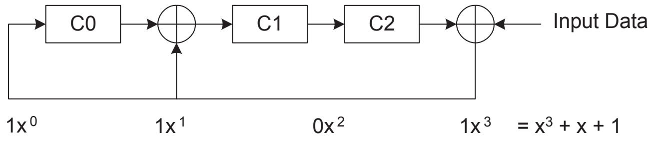


Figure 20: CRC Calculation

SERIAL INTERFACE REFERENCE

Required timing parameters for successful serial communication with A1363 device are given in table below.

Required Serial Interface Timing Parameters

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
Input/Output Signal Timing						
Access Code Time Out	t_{ACC}	Customer Access Code should be fully entered in less than t_{ACC}, measured from when V_{CC} crosses V_{UVLOH}.	–	–	8	ms
Bit Rate	t_{BITR}	Defined by the input message bit rate sent from the external controller	32	–	80	kbps
Bit Time	t_{BIT}	Data bit pulse width at 70 kbps	13.6	14.3	15	μs
Bit Time Error	err_{TBIT}	Deviation in t_{BIT} during one command frame	–11	–	+ 11	%
Volatile Memory Write Delay	t_{WRITE}	Required delay from the trailing edge of certain Write command frames to the leading edge of a following command frame	2 × t_{BIT}	–	–	μs
Non-Volatile Memory Write Delay	$t_{WRITE(E)}$	Required delay from the trailing edge of the second EEPROM Programming pulse to the leading edge of a following command frame	2 × t_{BIT}	–	–	μs
Read Acknowledge Delay	t_{READ}	Required delay from the trailing edge of a Read Acknowledge frame to the leading edge of a following command frame	2 × t_{BIT}	–	–	μs
Read Delay	t_{start_read}	Delay from the trailing edge of a Read command frame to the leading edge of the Read Acknowledge frame	25 μs – 0.25 × t_{BIT}	50 μs –0.25 × t_{BIT}	150 μs – 0.25 × t_{BIT}	μs
EEPROM Programming Pulse						
EEPROM Programming Pulse Setup Time	$t_{sPULSE(E)}$	Delay from last edge of write command to start of EEPROM programming pulse	40	–	–	μs
Input/Output Signal Voltage						
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to VCC line	5.1	–	–	V
		Read from VOUT line	V_{CC} – 0.2 V	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to VCC line	–	–	3.9	V
		Read from VOUT line	–	–	0.2	V
Manchester Level to VCC Delay	t_{MAN_VCC}		–	–	15	μs

SERIAL INTERFACE MESSAGE STRUCTURE

The general format of a command message frame is shown in Figure 21. Note that, in the Manchester coding used, a bit value of one is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.

V_{CC} LEVELS DURING MANCHESTER COMMUNICATION

For all devices with UVLO functionality, after power-up it is important that the VCC pin be held at V_{CC} until the first Synchronization pulse of a read/write transaction is sent (see Figure 22). During the transaction, the VCC pin varies between $V_{MAN(H)}$ and $V_{MAN(L)}$, but right after the last CRC bit has been sent, the controller must bring the VCC pin back to the V_{CC} level in less than t_{MAN_VCC}. This is important in order to avoid triggering the UVLO functionality during EEPROM read/write.

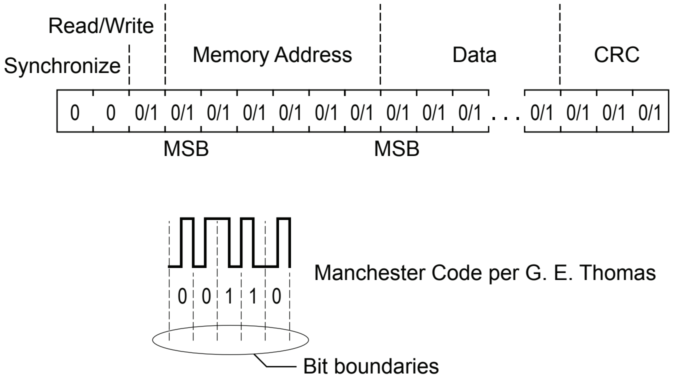


Figure 21: General Format for Serial Interface Commands

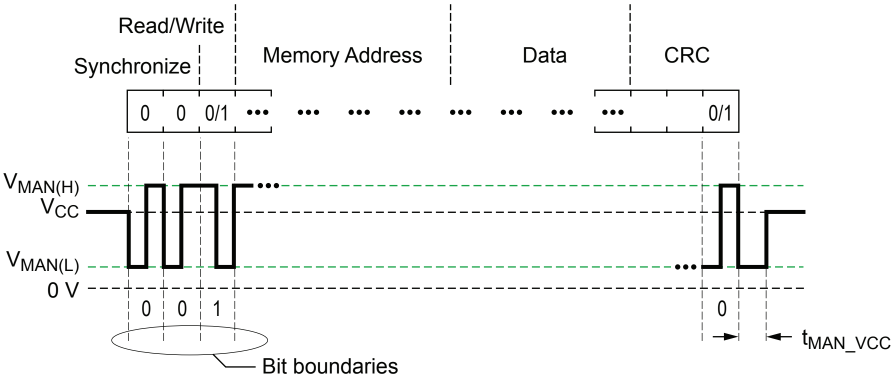


Figure 22: V_{CC} Levels During Manchester Communication

Serial Interface Command General Format

Quantity of Bits	Parameter Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
30	Data	0/1	24 data bits and 6 ECC bits
3	CRC	0/1	Incorrect value indicates errors