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Accelerator Series FPGAs – ACT 3 Family

Features

- Up to 10,000 Gate Array Equivalent Gates (up to 25,000 equivalent PLD Gates)
- Highly Predictable Performance with 100% Automatic Place-and-Route
- As Low as 9.0 ns Clock-to-Output Times (–1 Speed Grade)
- Up to 186 MHz On-Chip Performance (–1 Speed Grade)
- Up to 228 User-Programmable I/O Pins
- Four Fast, Low-Skew Clock Networks
- More than 500 Macro Functions
- Replaces up to Twenty 32 Macro-Cell CPLDs
- Replaces up to One Hundred 20-Pin PAL[®] Packages
- Up to 1,153 Dedicated Flip-Flops
- VQFP, TQFP, BGA, and PQFP Packages
- Nonvolatile, User Programmable
- Fully Tested Prior to Shipment
- 5.0 V and 3.3 V Versions
- Optimized for Logic Synthesis Methodologies
- Low Power CMOS Technology

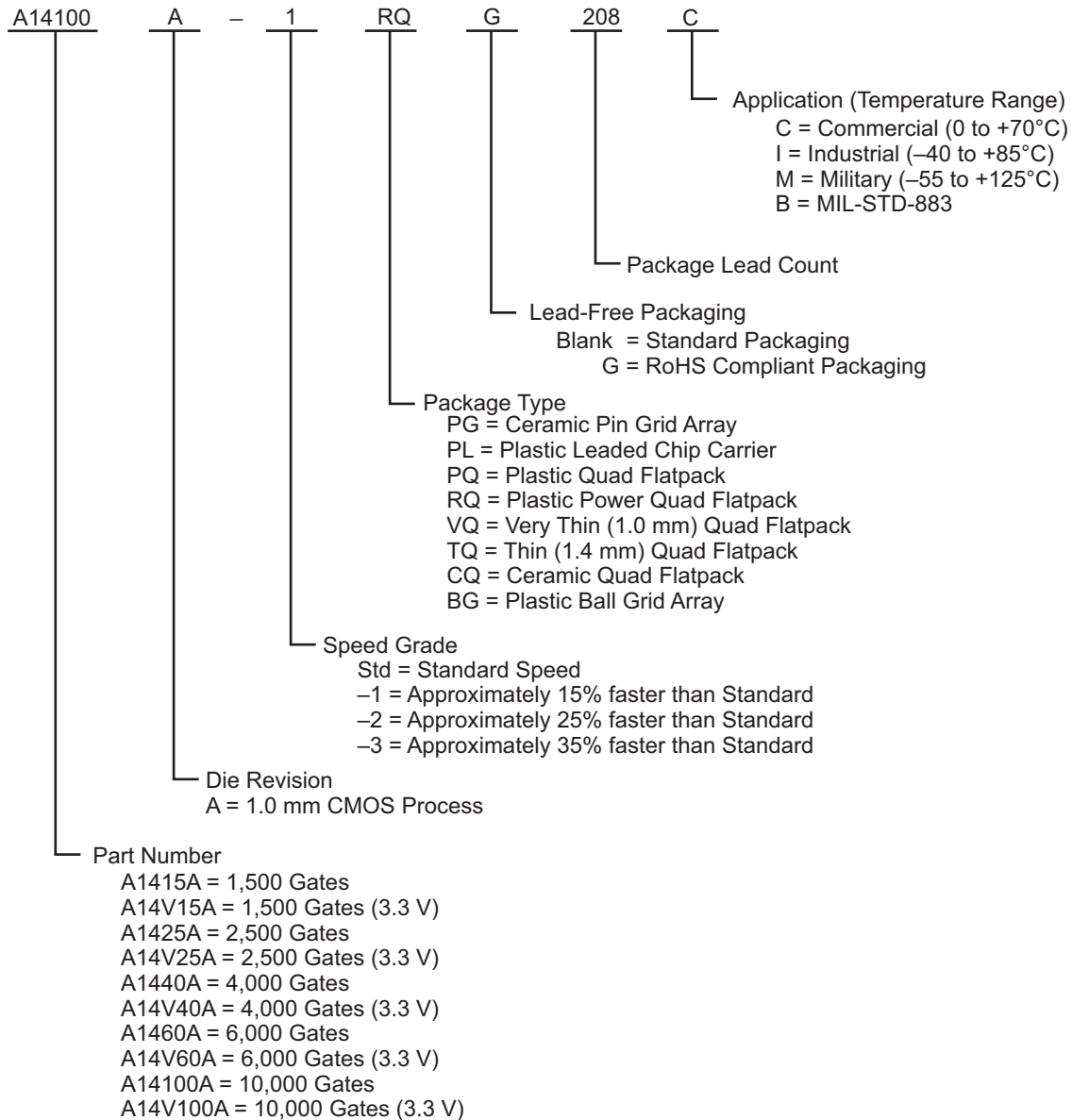
Table 1 • ACT 3 Family Product Information

Device	A1415	A1425	A1440	A1460	A14100
Capacity					
Gate Array Equivalent Gates	1,500	2,500	4,000	6,000	10,000
PLD Equivalent Gates	3,750	6,250	10,000	15,000	25,000
TTL Equivalent Package (40 gates)	40	60	100	150	250
20-Pin PAL Equivalent Packages (100 gates)	15	25	40	60	100
Logic Modules					
S-Module	104	160	288	432	697
C-Module	96	150	276	416	680
Dedicated Flip-Flops ¹	264	360	568	768	1,153
User I/Os (maximum)	80	100	140	168	228
Maximum Performance ² (worst-case commercial, –1 speed grade)					
Chip-to-Chip ³ (MHz)	80	80	80	78	76
Accumulators (16-bit, MHz)	47	47	47	47	47
Loadable Counter (16-bit, MHz)	82	82	82	82	78
Prescaled Loadable Counters (16-bit, MHz)	186	186	186	150	150
Datapath, Shift Registers (MHz)	186	186	186	150	150
Clock-to-Output (pad-to-pad, ns)	9.0	9.0	9.5	10.0	10.5
Packages ⁴ (by pin count)					
CPGA	PG100 ⁵	PG133 ⁵	PG175 ⁵	PG207	PG257
PLCC	PL84	PL84	PL84	–	–
PQFP	PQ100	PQ100, PQ160	PQ160	PQ160, PQ208	–
RQFP	–	–	–	–	RQ208
VQFP	VQ100	VQ100	VQ100	–	–
TQFP	–	–	TQ176	TQ176	–
BGA	–	–	–	BG225 ⁵	BG313
CQFP	–	CQ132	–	CQ196	CQ256

Notes:

1. One flip-flop per S0Module, two flip-flops per I/O Module.
2. Based on A1415A-1, A1425A-1, A1440A-1, A1460A-1, and A14100A-1.
3. Clock-to-Output (pad-to-pad) + assumed trace delay + setup time. Refer to the "System Performance Model" on page 1-1 and Table 1-1 on page 1-2.
4. See the "Product Plan" table on page III for package availability.
5. Discontinued device and package combination.
6. –2 and –3 speed grades have been discontinued. For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:
[PDN March 2001](#), [PDN 0104](#), [PDN 0203](#), [PDN 0604](#), [PDN 1004](#)

Ordering Information



Notes:

1. The -2 and -3 speed grades have been discontinued.
2. The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.
3. The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.
4. Military Grade devices are no longer available for the A1440A device.
5. For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:
 - [PDN March 2001](#)
 - [PDN 0104](#)
 - [PDN 0203](#)
 - [PDN 0604](#)
 - [PDN 1004](#)

Product Plan

Device/Package	Speed Grade ¹				Application ¹			
	Std.	-1	-2	-3	C	I	M	B
A1415A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	✓	-
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	✓	-
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	✓	-
100-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	-	-	-
A14V15A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	-	-	-	✓	-	-	-
100-Pin Very Thin Quad Flatpack (VQFP)	✓	-	-	-	✓	-	-	-
A1425A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓		
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	-	-
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	-	-
132-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	-	-	✓	-	✓	✓
133-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	-	D	D
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	-	-
A14V25A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	-	-	-	✓	-	-	-
100-Pin Very Thin Quad Flatpack (VQFP)	✓	-	-	-	✓	-	-	-
160-Pin Plastic Quad Flatpack (PQFP)	✓	-	-	-	✓	-	-	-
A1440A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	-	-
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	-	-
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	-	-
175-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	-	-	-
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	-	-

Notes:

- Applications:
 C = Commercial
 I = Industrial
 M = Military
 2. Commercial only

Availability:
 ✓ = Available
 P = Planned
 - = Not planned
 D = Discontinued

Speed Grade:
 -1 = Approx. 15% faster than Std.
 -2 = Approx. 25% faster than Std.
 -3 = Approx. 35% faster than Std.
 (-2 and -3 speed grades have been discontinued.)

Device/Package	Speed Grade ¹				Application ¹			
	Std.	-1	-2	-3	C	I	M	B
A14V40A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	-	-	-	✓	-	-	-
100-Pin Very Thin Quad Flatpack (VQFP)	✓	-	-	-	✓	-	-	-
160-Pin Plastic Quad Flatpack (PQFP)	✓	-	-	-	✓	-	-	-
176-Pin Thin Quad Flatpack (TQFP)	✓	-	-	-	✓	-	-	-
A1460A Device								
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	-	-
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	-	-
196-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	-	-	✓	-	✓	✓
207-Pin Ceramic Pin Grid Array (CPGA)	✓	✓	D	D	✓	-	✓	✓
208-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	-	-
225-Pin Plastic Ball Grid Array (BGA)	D	D	D	D	D	-	-	-
A14V60A Device								
160-Pin Plastic Quad Flatpack (PQFP)	✓	-	-	-	✓	-	-	-
176-Pin Thin Quad Flatpack (TQFP)	✓	-	-	-	✓	-	-	-
208-Pin Plastic Quad Flatpack (PQFP)	✓	-	-	-	✓	-	-	-
A14100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	✓	D	D	✓	✓	-	-
257-Pin Ceramic Pin Grid Array (CPGA)	✓	✓	D	D	✓	-	✓	✓
313-Pin Plastic Ball Grid Array (BGA)	✓	✓	D	D	✓	-	-	-
256-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	-	-	✓	-	✓	✓
A14V100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	-	-	-	✓	-	-	-
313-Pin Plastic Ball Grid Array (BGA)	✓	-	-	-	✓	-	-	-

Notes:

- Applications:
 C = Commercial
 I = Industrial
 M = Military
- Commercial only

Availability:
 ✓ = Available
 P = Planned
 - = Not planned
 D = Discontinued

Speed Grade:
 -1 = Approx. 15% faster than Std.
 -2 = Approx. 25% faster than Std.
 -3 = Approx. 35% faster than Std.
 (-2 and -3 speed grades have been discontinued.)

Plastic Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			PL84	PQ100	PQ160	PQ/RQ208	VQ100	TQ176	BG225*	BG313
A1415	200	1500	70	80	–	–	80	–	–	–
A1425	310	2500	70	80	100	–	83	–	–	–
A1440	564	4000	70	–	131	–	83	140	–	–
A1460	848	6000	–	–	131	167	–	151	168	–
A14100	1377	10000	–	–	–	175	–	–	–	228

Note: *Discontinued

Hermetic Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			PG100*	PG133*	PG175*	PG207	PG257	CQ132	CQ196	CQ256
A1415	200	1500	80	–	–	–	–	–	–	–
A1425	310	2500	–	100	–	–	–	100	–	–
A1440	564	4000	–	–	140	–	–	–	–	–
A1460	848	6000	–	–	–	168	–	–	168	–
A14100	1377	10000	–	–	–	–	228	–	–	228

Note: *Discontinued

Contact your local Microsemi SoC Products Group (formerly Actel) representative for device availability:

<http://www.microsemi.com/soc/contact/default.aspx>.

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1 – ACT 3 Family Overview

General Description

Microsemi's ACT 3 Accelerator Series of FPGAs offers the industry's fastest high-capacity programmable logic device. ACT 3 FPGAs offer a high performance, PCI compliant programmable solution capable of 186 MHz on-chip performance and 9.0 nanosecond clock-to-output (–1 speed grade), with capacities spanning from 1,500 to 10,000 gate array equivalent gates.

The ACT 3 family builds on the proven two-module architecture consisting of combinatorial and sequential logic modules used in Microsemi's 3200DX and 1200XL families. In addition, the ACT 3 I/O modules contain registers which deliver 9.0 nanosecond clock-to-out times (–1 speed grade). The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals such as flip-flop resets and output.

The ACT 3 family is supported by Microsemi's Designer Series Development System which offers automatic placement and routing (with automatic or fixed pin assignments), static timing analysis, user programming, and debug and diagnostic probe capabilities.

Accumulators (16-Bit)	47 MHz
Loadable Counters (16-Bit)	82 MHz
Prescaled Loadable Counters (16-Bit)	186 MHz
Shift Registers	186 MHz

Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade)

System Performance Model

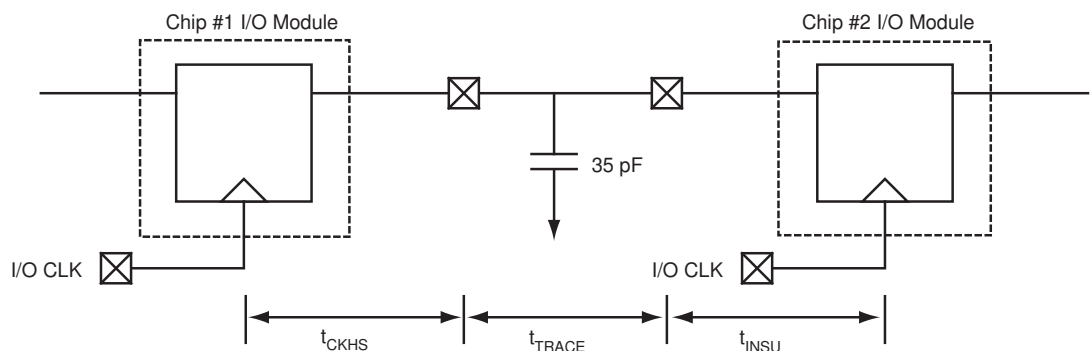


Table 1-1 • Chip-to-Chip Performance (worst-case commercial)

Device and Speed Grade	t _{CKHS} (ns)	t _{TRACE} (ns)	t _{INSU} (ns)	Total (ns)	MHz
A1425A -3	7.5	1.0	1.8	10.3	97
A1460A -3	9.0	1.0	1.3	11.3	88
A1425A -2	7.5	1.0	2.0	10.5	95
A1460A -2	9.0	1.0	1.5	11.5	87
A1425A -1	9.0	1.0	2.3	12.3	81
A1460A -1	10.0	1.0	1.8	12.8	78
A1425A STD	10.0	1.0	2.7	13.7	73
A1460A STD	11.5	1.0	2.0	14.5	69

Note: The -2 and -3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

2 – Detailed Specifications

This section of the datasheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. The on-chip circuitry required to program the devices is not covered.

Topology

The ACT 3 family architecture is composed of six key elements: Logic modules, I/O modules, I/O Pad Drivers, Routing Tracks, Clock Networks, and Programming and Test Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in [Figure 2-1](#).

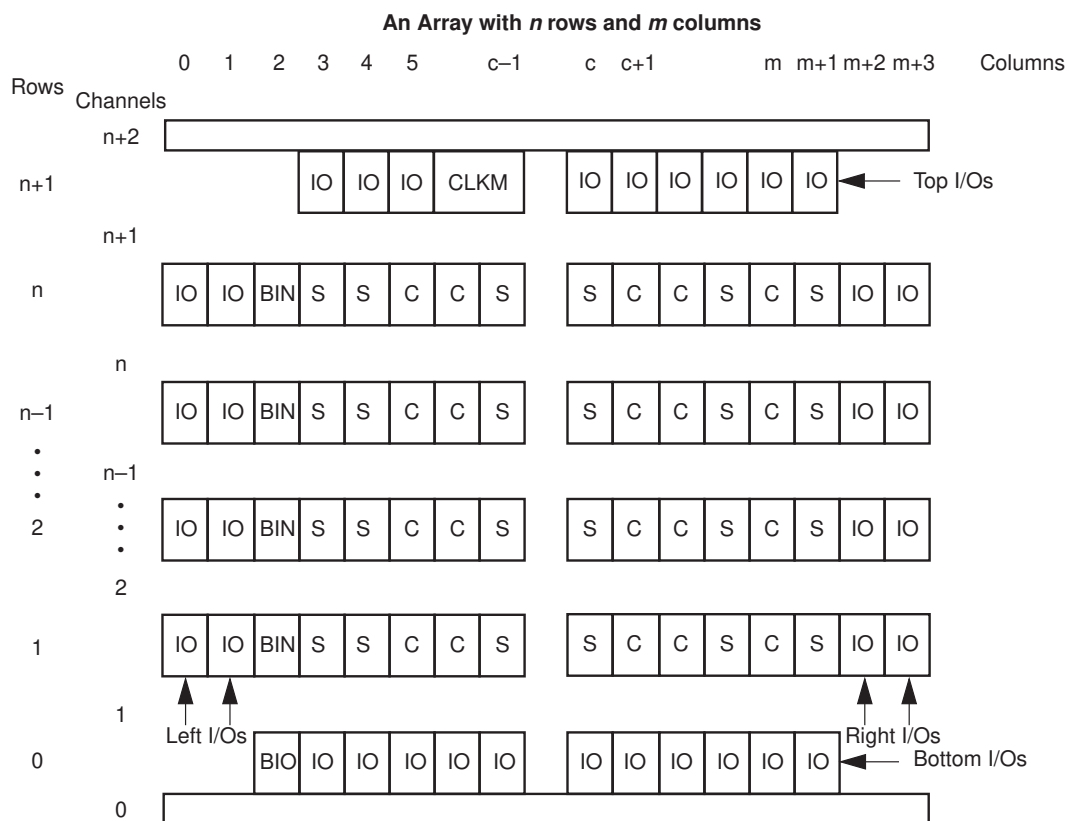


Figure 2-1 • Generalized Floor Plan of ACT 3 Device

Logic Modules

ACT 3 logic modules are enhanced versions of the 1200XL family logic modules. As in the 1200XL family, there are two types of modules: C-modules and S-modules (Figure 2-2 and Figure 2-3). The C-module is functionally equivalent to the 1200XL C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module.

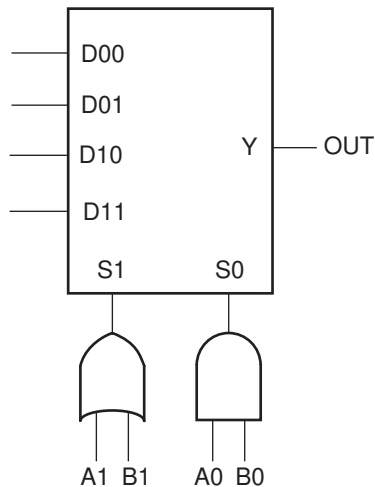


Figure 2-2 • C-Module Diagram

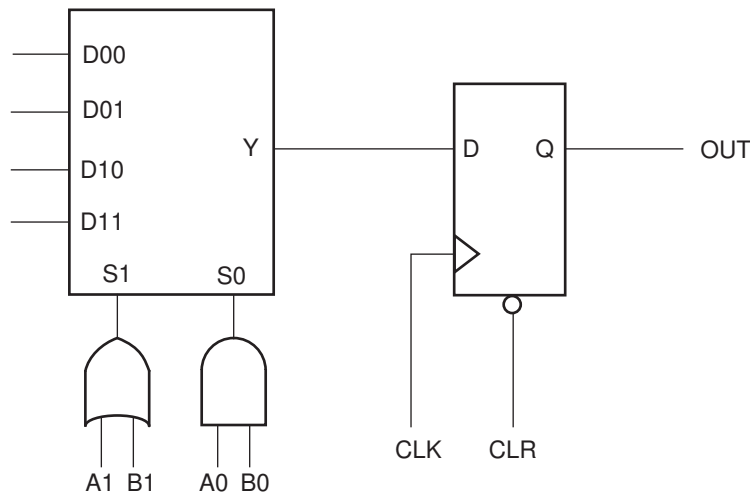


Figure 2-3 • S-Module Diagram

S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

$$Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11$$

EQ 1

where: $S0 = A0 * B0$ and $S1 = A1 + B1$

The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can therefore implement any function implemented by the C-module. This allows complex combinatorial-sequential functions to be implemented with no delay penalty. The Designer Series Development System will automatically combine any C-module macro driving an S-module macro into the S-module, thereby freeing up a logic module and eliminating a module delay.

The clear input CLR is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLKA, CLKB, or HCLK. The C-module and S-module functional descriptions are shown in [Figure 2-2](#) and [Figure 2-3](#) on page 2-2. The clock selection is determined by a multiplexer select at the clock input to the S-module.

I/Os

I/O Modules

I/O modules provide an interface between the array and the I/O Pad Drivers. I/O modules are located in the array and access the routing channels in a similar fashion to logic modules. The I/O module schematic is shown in [Figure 4](#). The signals DataIn and DataOut connect to the I/O pad driver.

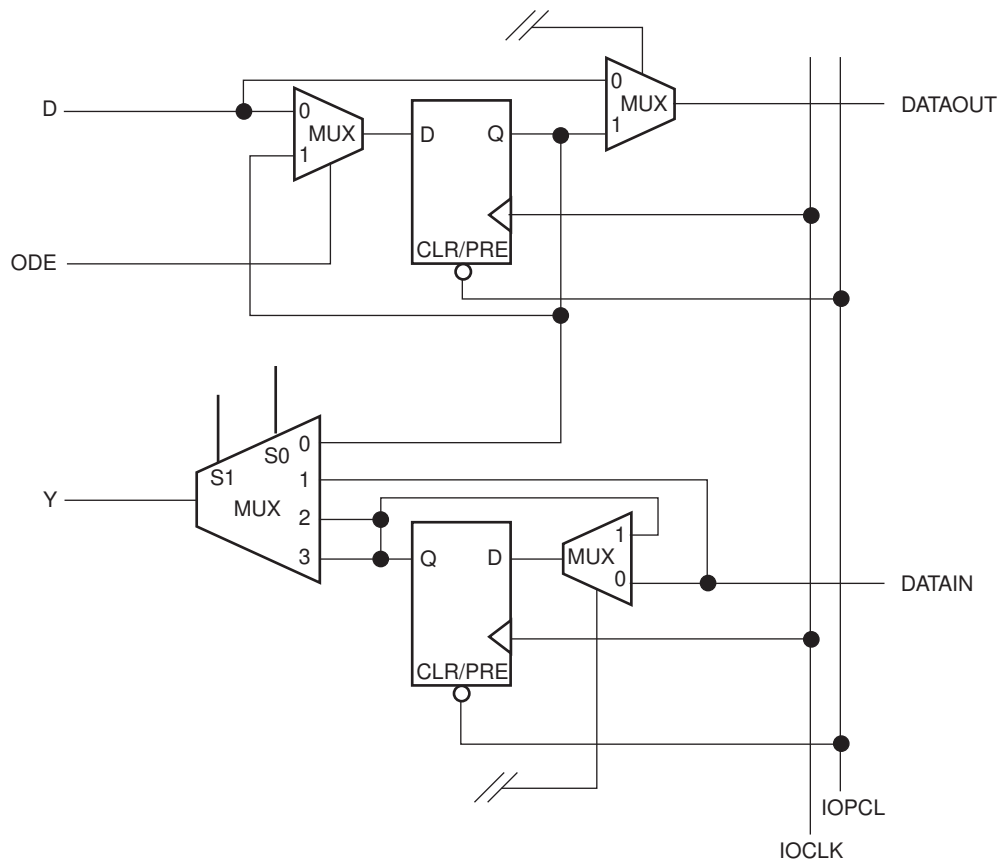


Figure 2-4 • Functional Diagram for I/O Module

Each I/O module contains two D-type flip-flops. Each flip-flop is connected to the dedicated I/O clock (IOCLK). Each flip-flop can be bypassed by nonsequential I/Os. In addition, each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O module by I/O module basis.

The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See [Figure 2-5](#).

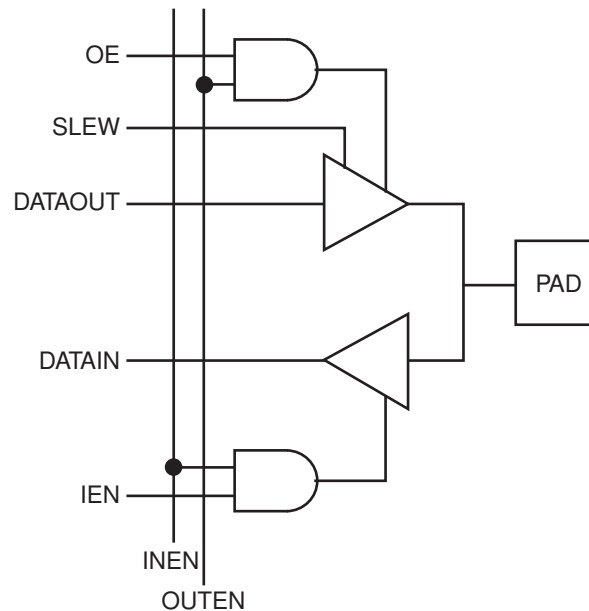


Figure 2-5 • Function Diagram for I/O Pad Driver

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

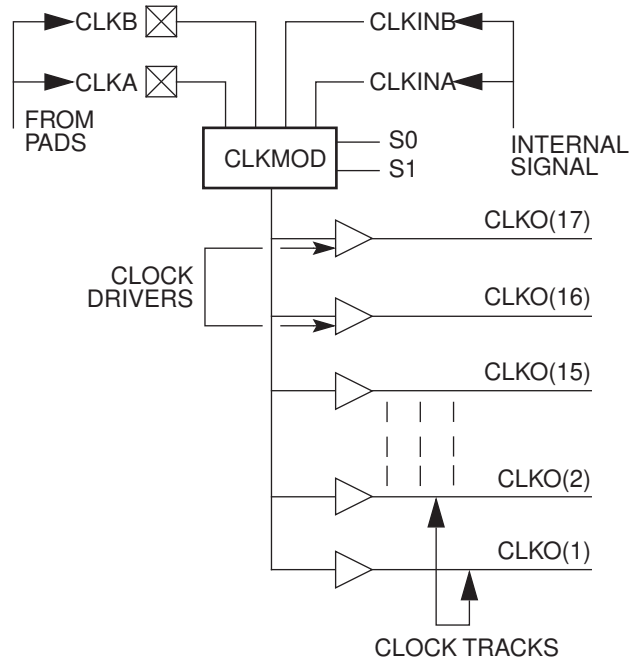


Figure 2-6 • Clock Networks

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (Figure 2-6):

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINA input
- Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

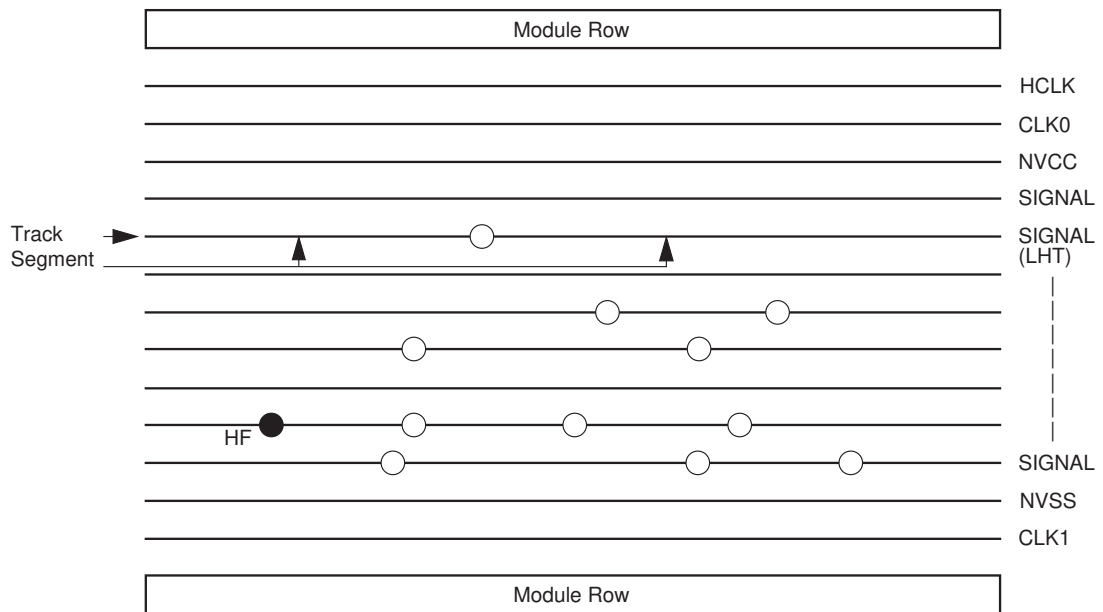


Figure 2-7 • Horizontal Routing Tracks and Segments

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.

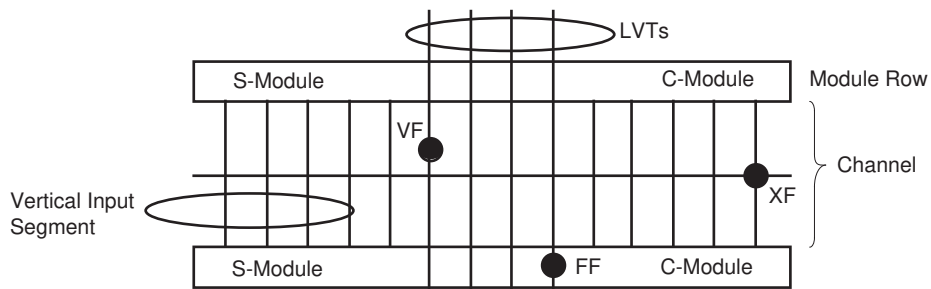


Figure 2-8 • Vertical Routing Tracks and Segments

Antifuse Connections

An antifuse is a “normally open” structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.)

Table 2-1 shows four types of antifuses.

Table 2-1 • Antifuse Types

Type	Description
XF	Horizontal-to-vertical connection
HF	Horizontal-to-horizontal connection
VF	Vertical-to-vertical connection
FF	"Fast" vertical connection

Examples of all four types of connections are shown in Figure 2-7 on page 2-6 and Figure 2-8 on page 2-6.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 2-9.

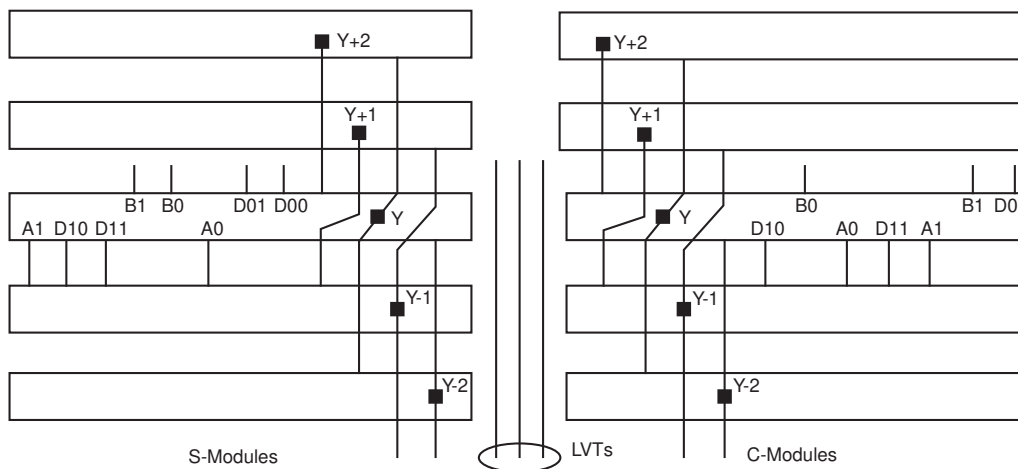


Figure 2-9 • Logic Module Routing Interface

Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

LVT Connections

Outputs may also connect to nondedicated segments called Long Vertical Tracks (LVTs). Each module pair in the array shares four LVTs that span the length of the column. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

Clock Connections

To minimize loading on the clock networks, a subset of inputs has antifuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module.

Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the temporary special I/O pins MODE, SDI, and DCLK. The function of these pins is similar to all ACT family devices. The ACT 3 family also includes support for two Actionprobe[®] circuits, allowing complete observability of any logic or I/O module in the array using the temporary special I/O pins, PRA and PRB.

5 V Operating Conditions

Table 2-2 • Absolute Maximum Ratings¹, Free Air Temperature Range

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	–0.5 to +7.0	V
VI	Input voltage	–0.5 to VCC + 0.5	V
VO	Output voltage	–0.5 to VCC + 0.5	V
IIO	I/O source sink current ²	±20	mA
T _{STG}	Storage temperature	–65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will forward bias and can draw excessive current.

Table 2-3 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	–40 to +85	–55 to +125	°C
5 V power supply tolerance	±5	±10	±10	%VCC

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Table 2-4 • Electrical Specifications

Symbol	Parameter	Test Condition	Commercial		Industrial		Military		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
VOH ^{1,2}	High level output	IOH = –4 mA (CMOS)	–	–	3.7	–	3.7	–	V
		IOH = –6 mA (CMOS)	3.84						V
		IOH = –10 mA (TTL) ³	2.40						V
VOL ^{1,2}	Low level output	IOL = +6 mA (CMOS)		0.33		0.4		0.4	V
		IOL = +12 mA (TTL) ³		0.50					
VIH	High level input	TTL inputs	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIL	Low level input	TTL inputs	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
IIN	Input leakage	VI = VCC or GND	–10	+10	–10	+10	–10	+10	µA
IOZ	3-state output leakage	VO = VCC or GND	–10	+10	–10	+10	–10	+10	µA
C _{IO}	I/O capacitance ^{3,4}			10		10		10	pF
ICC(S)	Standby VCC supply current (typical = 0.7 mA)			2		10		20	mA
ICC(D)	Dynamic VCC supply current. See the Power Dissipation section.								

Notes:

1. Microsemi devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.
2. Tested one output at a time, VCC = minimum.
3. Not tested; for information only.
4. VOUT = 0 V, f = 1 MHz
5. Typical standby current = 0.7 mA. All outputs unloaded. All inputs = VCC or GND.

3.3 V Operating Conditions

Table 2-5 • Absolute Maximum Ratings¹, Free Air Temperature Range

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	−0.5 to +7.0	V
VI	Input voltage	−0.5 to VCC + 0.5	V
VO	Output voltage	−0.5 to VCC + 0.5	V
IIO	I/O source sink current ²	±20	mA
T _{STG}	Storage temperature	−65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND −0.5 V, the internal protection diodes will forward bias and can draw excessive current.

Table 2-6 • Recommended Operating Conditions

Parameter	Commercial	Units
Temperature range*	0 to +70	°C
Power supply tolerance	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial.

Table 2-7 • Electrical Specifications

Parameter		Commercial		Units
		Min.	Max.	
VOH ¹	I _{OH} = −4 mA	2.15	–	V
	I _{OH} = −3.2 mA	2.4		V
VOL ¹	I _{OL} = 6 mA		0.4	V
VIL		−0.3	0.8	V
VIH		2.0	VCC + 0.3	V
Input transition time t _R , t _F ²	VI = VCC or GND	−10	+10	μA
C _{IO} I/O Capacitance ^{2,3}			10	pF
Standby current, I _{CC} ⁴ (typical = 0.3 mA)			0.75	mA
Leakage current ⁵		−10	10	μA

1. Only one output tested at a time. VCC = minimum.
2. Not tested; for information only.
3. Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. Typical standby current = 0.3 mA. All outputs unloaded. All inputs = VCC or GND.
5. VO, VIN = VCC or GND

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc} , and the junction to ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ °C/W}} = \frac{150\text{°C} - 70\text{°C}}{25\text{°C/W}} = 3.2 \text{ W}$$

EQ 2

Table 2-8 • Package Thermal Characteristics

Package Type*	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft./min.	Units
Ceramic Pin Grid Array	100	20	35	17	°C/W
	133	20	30	15	°C/W
	175	20	25	14	°C/W
	207	20	22	13	°C/W
	257	20	15	8	°C/W
Ceramic Quad Flatpack	132	13	55	30	°C/W
	196	13	36	24	°C/W
	256	13	30	18	°C/W
Plastic Quad Flatpack	100	13	51	40	°C/W
	160	10	33	26	°C/W
	208	10	33	26	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	11	32	25	°C/W
Power Quad Flatpack	208	0.4	17	13	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Plastic Ball Grid Array	225	10	25	19	°C/W
	313	10	23	17	°C/W

Note: Maximum power dissipation in still air:

PQ160 = 2.4 W

PQ208 = 2.4 W

PQ100 = 1.6 W

VQ100 = 1.9 W

TQ176 = 2.5 W

PL84 = 2.2 W

RQ208 = 4.7 W

BG225 = 3.2 W

BG313 = 3.5 W

Power Dissipation

$$P = [I_{CC \text{ standby}} + I_{\text{active}}] * V_{CC} * I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

EQ 3

where:

$I_{CC \text{ standby}}$ is the current flowing when no inputs or outputs are changing

I_{active} is the current flowing due to CMOS switching.

I_{OL} and I_{OH} are TTL sink/source current.

V_{OL} and V_{OH} are TTL level output voltages.

N is the number of outputs driving TTL loads to V_{OL} .

M equals the number of outputs driving TTL loads to V_{OH} .

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in [Table 2-9](#) for commercial, worst case conditions.

Table 2-9 • Standby Power Calculation

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by [EQ 4](#).

$$\text{Power } (\mu\text{W}) = C_{EQ} * V_{CC}^2 * F$$

EQ 4

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Figure 2-10.

Table 2-10 • CEQ Values for Microsemi FPGAs

Item	CEQ Value
Modules (C _{EQM})	6.7
Input Buffers (C _{EQI})	7.2
Output Buffers (C _{EQO})	10.4
Routed Array Clock Buffer Loads (C _{EQCR})	1.6
Dedicated Clock Buffer Loads (C _{EQCD})	0.7
I/O Clock Buffer Loads (C _{EQCI})	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 5 shows a piece-wise linear summation over all components.

$$\begin{aligned}
 \text{Power} = & VCC^2 * [(m * C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} \\
 & + (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} \\
 & + 0.5 * (q1 * C_{EQCR} * f_{q1})_{\text{routed_Clk1}} + (r1 * f_{q1})_{\text{routed_Clk1}} \\
 & + 0.5 * (q2 * C_{EQCR} * f_{q2})_{\text{routed_Clk2}} \\
 & + (r2 * f_{q2})_{\text{routed_Clk2}} + 0.5 * (s1 * C_{EQCD} * f_{s1})_{\text{dedicated_Clk}} \\
 & + (s2 * C_{EQCI} * f_{s2})_{\text{IO_Clk}}]
 \end{aligned}$$

EQ 5

Where:

- m = Number of logic modules switching at f_m
- n = Number of input buffers switching at f_n
- p = Number of output buffers switching at f_p
- q1 = Number of clock loads on the first routed array clock
- q2 = Number of clock loads on the second routed array clock
- r1 = Fixed capacitance due to first routed array clock
- r2 = Fixed capacitance due to second routed array clock
- s1 = Fixed number of clock loads on the dedicated array clock
- s2 = Fixed number of clock loads on the dedicated I/O clock
- C_{EQM} = Equivalent capacitance of logic modules in pF
- C_{EQI} = Equivalent capacitance of input buffers in pF
- C_{EQO} = Equivalent capacitance of output buffers in pF
- C_{EQCR} = Equivalent capacitance of routed array clock in pF
- C_{EQCD} = Equivalent capacitance of dedicated array clock in pF
- C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF
- C_L = Output lead capacitance in pF
- f_m = Average logic module switching rate in MHz
- f_n = Average input buffer switching rate in MHz
- f_p = Average output buffer switching rate in MHz
- f_{q1} = Average first routed array clock rate in MHz
- f_{q2} = Average second routed array clock rate in MHz
- f_{s1} = Average dedicated array clock rate in MHz
- f_{s2} = Average dedicated I/O clock rate in MHz

Table 2-11 • Fixed Capacitance Values for Microsemi FPGAs

Device Type	r1, routed_Clk1	r2, routed_Clk2
A1415A	60	60
A14V15A	57	57
A1425A	75	75
A14V25A	72	72
A1440A	105	105
A14V40A	100	100
A1440B	105	105
A1460A	165	165
A14V60A	157	157
A1460B	165	165
A14100A	195	195
A14V100A	185	185
A14100B	195	195

Table 2-12 • Fixed Clock Loads (s1/s2)

Device Type	s1, Clock Loads on Dedicated Array Clock	s2, Clock Loads on Dedicated I/O Clock
A1415A	104	80
A14V15A	104	80
A1425A	160	100
A14V25A	160	100
A1440A	288	140
A14V40A	288	140
A1440B	288	140
A1460A	432	168
A14V60A	432	168
A1460B	432	168
A14100A	697	228
A14V100A	697	228
A14100B	697	228

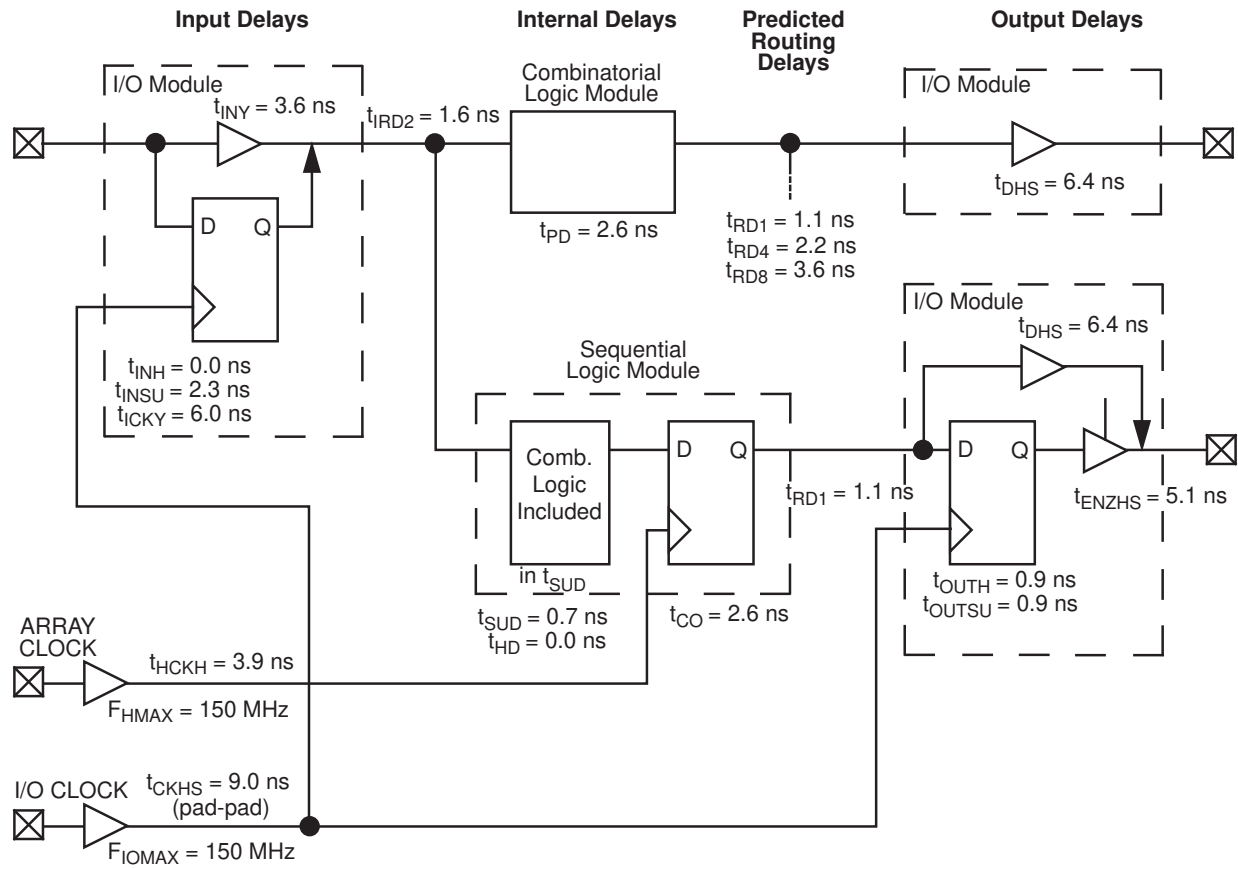
Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Table 2-13 • Guidelines for Predicting Power Dissipation

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (CL)	35 pF
Average logic module switching rate (fm)	F/10
Average input switching rate (fn)	F/5
Average output switching rate (fp)	F/10
Average first routed array clock rate (fq1)	F/2
Average second routed array clock rate (fq2)	F/2
Average dedicated array clock rate (fs1)	F
Average dedicated I/O clock rate (fs2)	F

ACT 3 Timing Model



Note: Values shown for A1425A -1 speed grade device.

Figure 2-10 • Timing Model

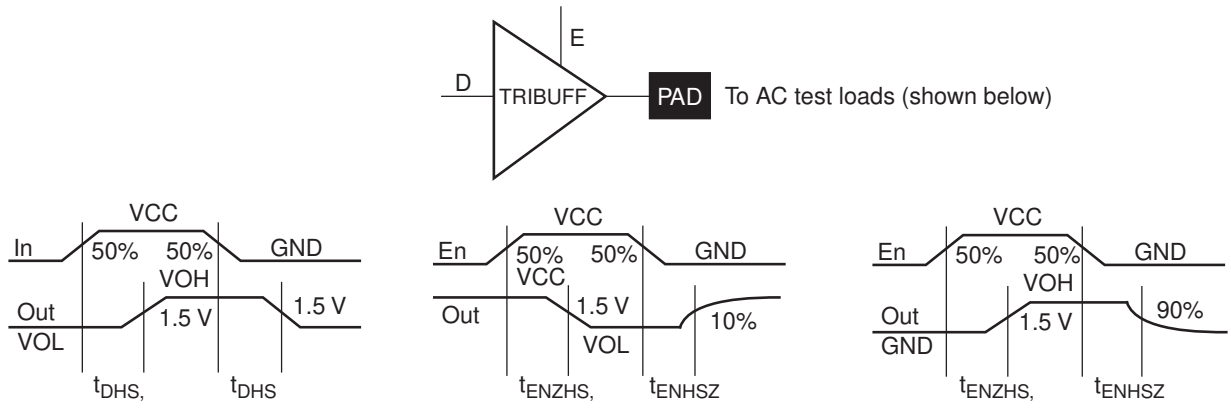


Figure 2-11 • Output Buffers

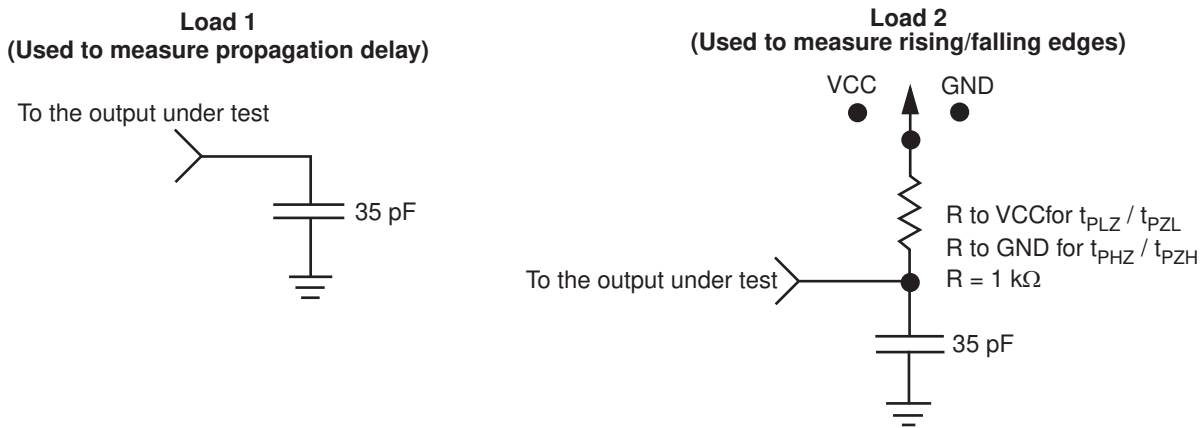


Figure 2-12 • AC Test Loads

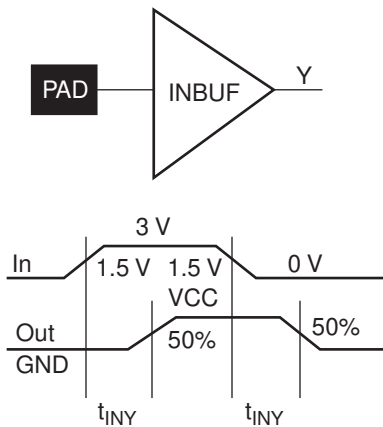


Figure 2-13 • Input Buffer Delays