Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Military Grade SmartFusion Customizable System-on-Chip (cSoC)

Product Benefits

- 100% Military Temperature Tested and Qualified from –55°C to 125°C
- Not Susceptible to Neutron-Induced Configuration Loss

Microcontroller Subsystem (MSS)

- Hard 50 MHz 32-Bit ARM® Cortex®-M3
  - Fully Tested Across Military Temperature Range (–55°C to 125°C)
  - 1.25 DMIPS/MHz Throughput from Zero Wait State Memory
  - Memory Protection Unit (MPU)
  - Single Cycle Multiplication, Hardware Divide
  - JTAG Debug (4 wires), Serial Wire Debug (SWD, 2 wires), and Single Wire Viewer (SWV) Interfaces
- Internal Memory
  - Embedded Nonvolatile Flash Memory (eNVM), 128 Kbytes to 512 Kbytes
  - Embedded High-Speed SRAM (eSRAM), 16 Kbytes to 64 Kbytes, Implemented in 2 Physical Blocks to Enable Simultaneous Access from 2 Different Masters
- Multi-Layer AHB Communications Matrix
  - Provides up to 16 Gbps of On-Chip Memory Bandwidth,[1] Allowing Multi-Master Schemes
- 10/100 Ethernet MAC with RMII Interface[2]
- Programmable External Memory Controller, Which Supports:
  - Asynchronous Memories
  - NOR Flash, SRAM, PSRAM
  - Synchronous SRAMs
- Two I^2C Peripherals
- Two 16550 Compatible UARTs
- Two SPI Peripherals
- Two 32-Bit Timers
- 32-Bit Watchdog Timer
- 8-Channel DMA Controller to Offload the Cortex-M3 processor from Data Transactions
- Clock Sources
  - 32 kHz to 20 MHz Main Oscillator
  - Battery-Backed 32 KHz Low Power Oscillator with Real-Time Counter (RTC)
  - 100 MHz Embedded RC Oscillator; Up to 3% Accurate at Military Temperature
  - Embedded Analog PLL with 4 Output Phases (0, 90, 180, 270)

High-Performance FPGA

- Based on proven ProASIC®3 FPGA Fabric
- Low Power, Firm-Error Immune 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Nonvolatile, Live at Power-Up, Retains Program When Powered Off
- 350 MHz System Performance
- Embedded SRAMs and FIFOs
  - Variable Aspect Ratio 4,608-Bit SRAM Blocks
  - x1, x2, x4, x9, and x18 Organizations
  - True Dual-Port SRAM (excluding x18)
  - Programmable Embedded FIFO Control Logic
- Secure ISP with 128-Bit AES via JTAG
- FlashLock® to Secure FPGA Contents
- Five Clock Conditioning Circuits (CCCs) with up to 2 Integrated Analog PLLs
  - Phase Shift, Multiply/Divide, and Delay Capabilities
  - Frequency: Input 1.5–350 MHz, Output 0.75 to 350 MHz

Programmable Analog

Analog Front-End (AFE)

- Up to Three 12-Bit SAR ADCs
  - 500 Ksps in 12-Bit Mode
  - 550 Ksps in 10-Bit Mode
  - 600 Ksps in 8-Bit Mode
- Internal 2.56 V Reference or Optional External Reference
- One First-Order ΣΔ DAC (sigma-delta) per ADC
  - 12-Bit 500 Ksps Update Rate
- Up to 5 High-Performance Analog Signal Conditioning Blocks (SCB) per Device, Each Including:
  - Two High-Voltage Bipolar Voltage Monitors (with 4 input ranges from ±2.5 V to –11.5/12 V) with 4% Accuracy
  - High Gain Current Monitor, Differential Gain = 50, up to 12 V Common Mode
  - Temperature Monitor (Resolution = ¼°C in 12-Bit Mode; Accurate from –55°C to 150°C)
- Up to Ten High-Speed Voltage Comparators (t_{pd} = 15 ns)

Analog Compute Engine (ACE)

- Offloads Cortex-M3–Based MSS from Analog Initialization and Processing of ADC, DAC, and SCBs
- Sample Sequence Engine for ADC and DAC Parameter Set-Up
- Post-Processing Engine for Functions such as Low-Pass Filtering and Linear Transformation
- Easily Configured via GUI in Libero® System-on-Chip (SoC) Software

I/Os and Operating Voltage

- FPGA I/Os
  - LVDS, PCI, PCI-X, up to 24 mA IOH/IOL
  - Up to 350 MHz
- MSS I/Os
  - Schmitt Trigger, up to 6 mA IOH, 8 mA IOL
  - Up to 180 MHz
- Single 3.3 V Power Supply with On-Chip 1.5 V Regulator
- External 1.5 V Is Allowed by Bypassing Regulator (digital VCC = 1.5 V for FPGA and MSS, analog VCC = 3.3 V and 1.5 V)

1 Theoretical maximum
2 A2F500 devices

© 2015 Microsemi Corporation

SmartFusion cSoC Family Product Table

<table>
<tr><th colspan="2">SmartFusion® cSoC</th><th>A2F060</th><th>A2F500</th></tr>
<tr><td rowspan="3">FPGA Fabric</td><td>System Gates</td><td>60,000</td><td>500,000</td></tr>
<tr><td>Tiles (D-flip-flops)</td><td>1,536</td><td>11,520</td></tr>
<tr><td>RAM Blocks (4,608 bits)</td><td>8</td><td>24</td></tr>
<tr><td rowspan="14">Microcontroller Subsystem (MSS)</td><td>Flash (Kbytes)</td><td>128</td><td>512</td></tr>
<tr><td>SRAM (Kbytes)</td><td>16</td><td>64</td></tr>
<tr><td>Cortex-M3 with memory protection unit (MPU)</td><td colspan="2">Yes</td></tr>
<tr><td>10/100 Ethernet MAC</td><td>No</td><td>Yes</td></tr>
<tr><td>External Memory Controller (EMC)</td><td colspan="2">24-bit address,16-bit data</td></tr>
<tr><td>DMA</td><td colspan="2">8 Ch</td></tr>
<tr><td>I^2C</td><td colspan="2">2</td></tr>
<tr><td>SPI</td><td colspan="2">2</td></tr>
<tr><td>16550 UART</td><td colspan="2">2</td></tr>
<tr><td>32-Bit Timer</td><td colspan="2">2</td></tr>
<tr><td>PLL</td><td>1</td><td>2[1]</td></tr>
<tr><td>32 KHz Low Power Oscillator</td><td colspan="2">1</td></tr>
<tr><td>100 MHz On-Chip RC Oscillator</td><td colspan="2">1</td></tr>
<tr><td>Main Oscillator (32 KHz to 20 MHz)</td><td colspan="2">1</td></tr>
<tr><td rowspan="7">Programmable Analog</td><td>ADCs (8-/10-/12-bit SAR)</td><td>1</td><td>3[3]</td></tr>
<tr><td>DACs (12-bit sigma-delta)</td><td>1</td><td>3[3]</td></tr>
<tr><td>Signal Conditioning Blocks (SCBs)</td><td>1</td><td>5[3]</td></tr>
<tr><td>Comparator[2]</td><td>2</td><td>10[3]</td></tr>
<tr><td>Current Monitors[2]</td><td>1</td><td>5[3]</td></tr>
<tr><td>Temperature Monitors[2]</td><td>1</td><td>5[3]</td></tr>
<tr><td>Bipolar High Voltage Monitors[2]</td><td>2</td><td>10[3]</td></tr>
</table>

Notes:

1. *Two PLLs are available in FG484 (one PLL in FG256).*
2. *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the SmartFusion Programmable Analog User's Guide for details.*
3. *Available on FG484 only.*

Package I/Os: MSS + FPGA I/Os

Device	A2F060	A2F500	
Package	**FG256**	**FG256**	**FG484**
Direct Analog Inputs	11	8	12
Shared Analog Inputs[1]	4	16	20
Total Analog Inputs	15	24	32
Total Analog Outputs	1	2	3
MSS I/Os[2,3]	26[4]	25	41
FPGA I/Os	66	66	128
Total I/Os	108	117	204

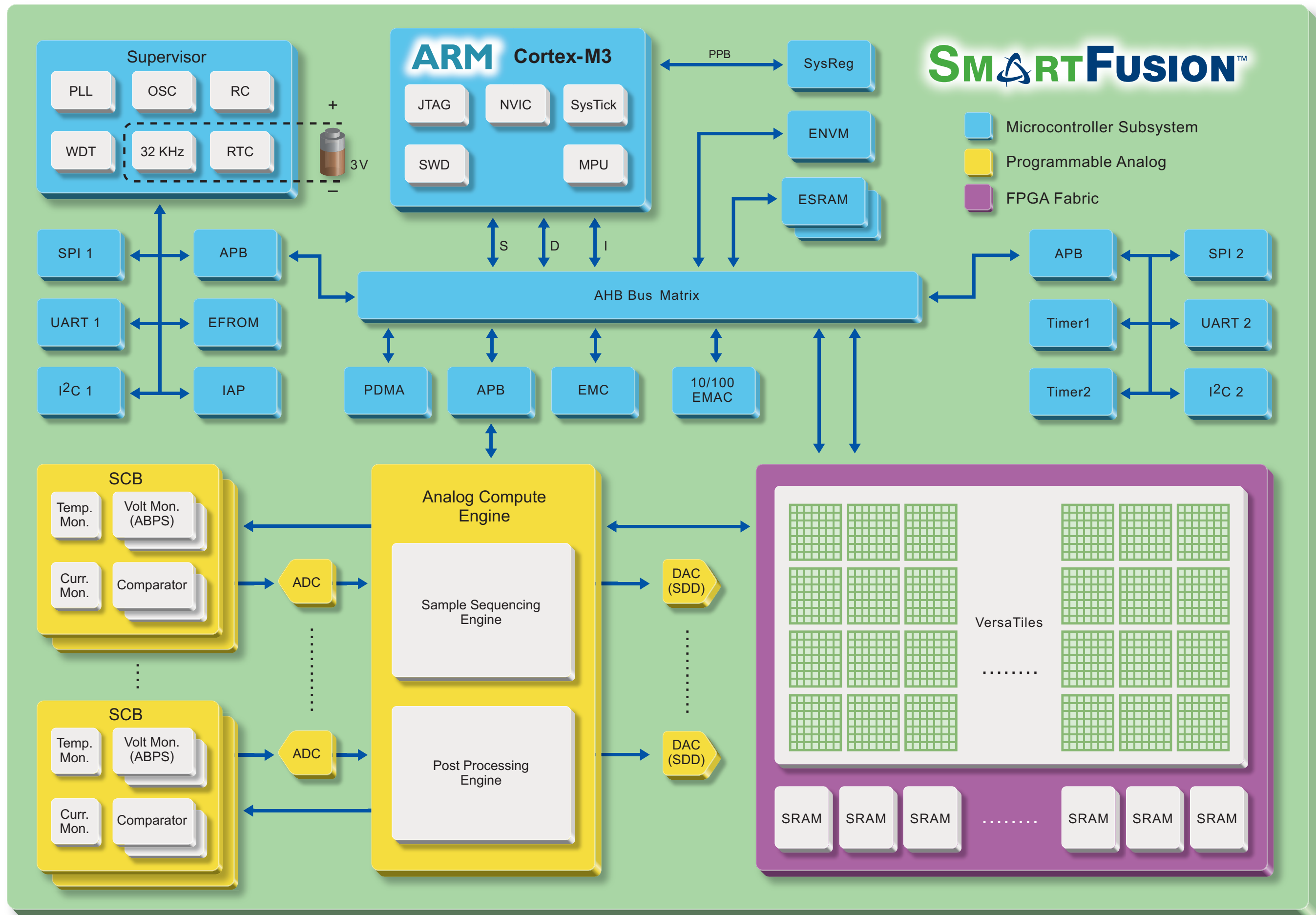
Notes:

1. *These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.*
2. *16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.*
3. *9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V standards.*
4. *10/100 Ethernet MAC is not available on A2F060.*

SmartFusion cSoC Device Status

Device	Status
A2F060	Production
A2F500	Production

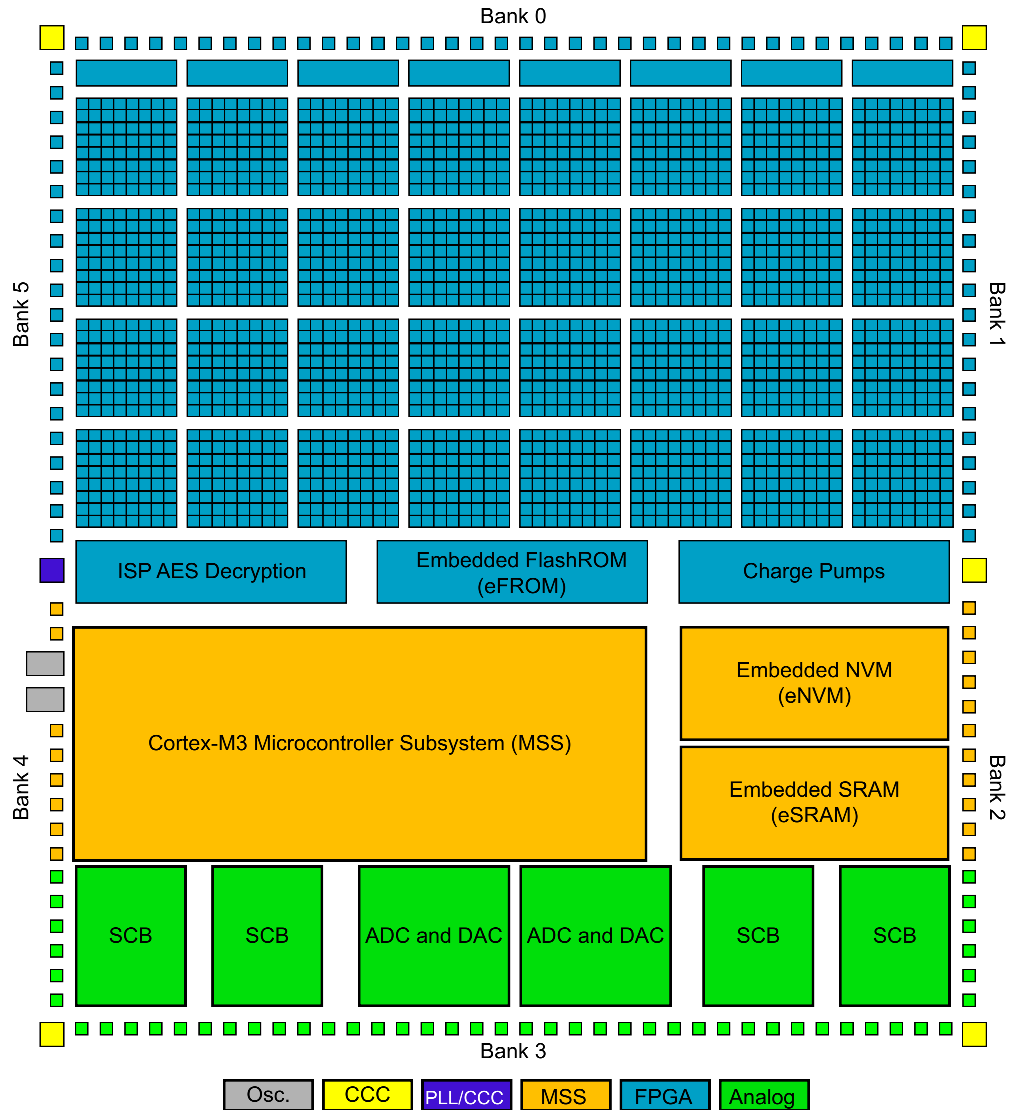
SmartFusion cSoC Block Diagram



Legend:

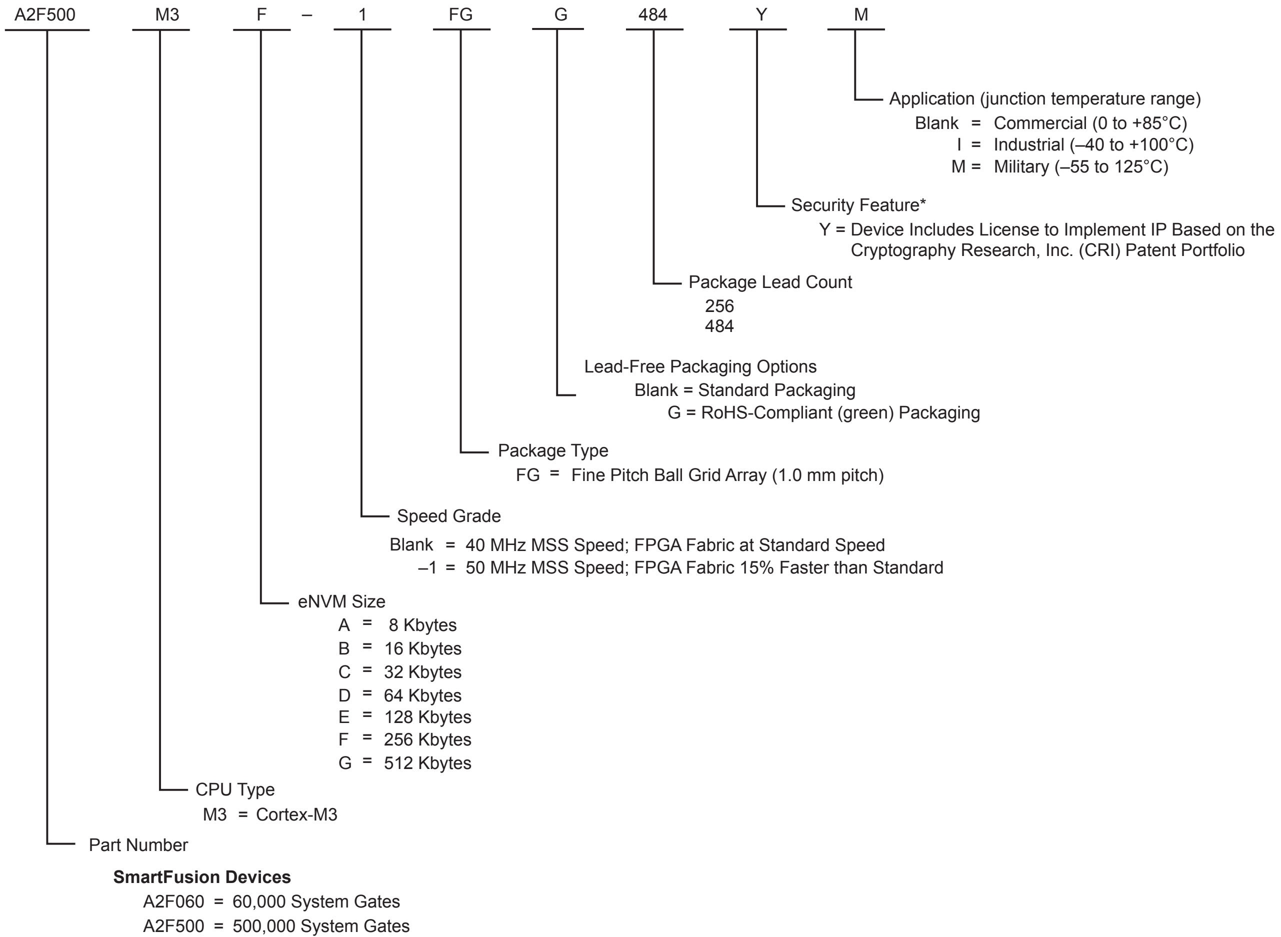
SDD – Sigma-delta DAC
SCB – Signal conditioning block
PDMA – Peripheral DMA
IAP – In-application programming
ABPS – Active bipolar prescaler
WDT – Watchdog Timer
SWD – Serial Wire Debug

SmartFusion cSoC System Architecture



Note: Generic Architecture for the SmartFusion Family

Product Ordering Codes



*Note: *Most devices in the SmartFusion cSoC family can be ordered with the Y suffix. Devices with a package size greater or equal to 5x5 mm are supported. Contact your local Microsemi SoC Products Group sales representative for more information.*

Temperature Grade Offerings

SmartFusion cSoC	A2F060	A2F500
FG256	C, I, M	C, I, M
FG484	–	C, I, M

Notes:

1. *C = Commercial Temperature Range: 0°C to 85°C Junction*
2. *I = Industrial Temperature Range: –40°C to 100°C Junction*
3. *M = Military Temperature Range: –55°C to 125°C Junction*

Table of Contents

SmartFusion Family Overview

Introduction 1-1
General Description 1-1

SmartFusion DC and Switching Characteristics

General Specifications 2-1
Calculating Power Dissipation 2-10
User I/O Characteristics 2-20
VersaTile Characteristics 2-57
Global Resource Characteristics 2-61
RC Oscillator 2-63
Main and Lower Power Crystal Oscillator 2-64
Clock Conditioning Circuits 2-65
FPGA Fabric SRAM and FIFO Characteristics 2-67
Embedded Nonvolatile Memory Block (eNVM) 2-76
Embedded FlashROM (eFROM) 2-77
JTAG 1532 Characteristics 2-77
Programmable Analog Specifications 2-78
Serial Peripheral Interface (SPI) Characteristics 2-90
Inter-Integrated Circuit (I^2C) Characteristics 2-92

SmartFusion Development Tools

Types of Design Tools 3-1
SmartFusion Ecosystem 3-3
Middleware 3-5

SmartFusion Programming

In-System Programming 4-7
In-Application Programming 4-8
Typical Programming and Erase Times 4-9
References 4-9

Pin Descriptions

Supply Pins 5-1
User-Defined Supply Pins 5-4
Global I/O Naming Conventions 5-5
User Pins 5-5
Special Function Pins 5-7
JTAG Pins 5-9
Microcontroller Subsystem (MSS) 5-11
Analog Front-End (AFE) 5-13
Analog Front-End Pin-Level Function Multiplexing 5-15
FG256 5-17
FG484 5-26

Datasheet Information

List of Changes 6-1
Microsemi SoC Products Group Safety Critical, Life Support, and High-Reliability Applications Policy 6-2

Microsemi

1 – SmartFusion Family Overview

Introduction

The SmartFusion® family of cSoCs builds on the technology first introduced with the Fusion mixed signal FPGAs. SmartFusion cSoCs are made possible by integrating FPGA technology with programmable high-performance analog and hardened ARM Cortex-M3 microcontroller blocks on a flash semiconductor process. The SmartFusion cSoC takes its name from the fact that these three discrete technologies are integrated on a single chip, enabling the lowest cost of ownership and smallest footprint solution to you.

General Description

Microcontroller Subsystem (MSS)

The MSS is composed of a 100 MHz Cortex-M3 processor and integrated peripherals, which are interconnected via a multi-layer AHB bus matrix (ABM). This matrix allows the Cortex-M3 processor, FPGA fabric master, Ethernet message authentication controller (MAC), when available, and peripheral DMA (PDMA) controller to act as masters to the integrated peripherals, FPGA fabric, embedded nonvolatile memory (eNVM), embedded synchronous RAM (eSRAM), external memory controller (EMC), and analog compute engine (ACE) blocks.

SmartFusion cSoCs of different densities offer various sets of integrated peripherals. Available peripherals include SPI, I^2C, and UART serial ports, embedded FlashROM (EFROM), 10/100 Ethernet MAC, timers, phase-locked loops (PLLs), oscillators, real-time counters (RTC), and peripheral DMA controller (PDMA).

Programmable Analog

Analog Front-End (AFE)

SmartFusion cSoCs offer an enhanced analog front-end compared to Fusion devices. The successive approximation register analog-to-digital converters (SAR ADC) are similar to those found on Fusion devices. SmartFusion cSoC also adds first order sigma-delta digital-to-analog converters (SDD DAC).

SmartFusion cSoCs can handle multiple analog signals simultaneously with its signal conditioning blocks (SCBs). SCBs are made of a combination of active bipolar prescalers (ABPS), comparators, current monitors and temperature monitors. ABPS modules allow larger bipolar voltages to be fed to the ADC. Current monitors take the voltage across an external sense resistor and convert it to a voltage suitable for the ADC input range. Similarly, the temperature monitor reads the current through an external PN-junction (diode or transistor) and converts it internally for the ADC. The SCB also includes comparators to monitor fast signal thresholds without using the ADC. The output of the comparators can be fed to the analog compute engine or the ADC.

Analog Compute Engine (ACE)

The mixed signal blocks found in SmartFusion cSoCs are controlled and connected to the rest of the system via a dedicated processor called the analog compute engine (ACE). The role of the ACE is to offload control of the analog blocks from the Cortex-M3, thus offering faster throughput or better power consumption compared to a system where the main processor is in charge of monitoring the analog resources. The ACE is built to handle sampling, sequencing, and post-processing of the ADCs, DACs, and SCBs.

ProASIC3 FPGA Fabric

The SmartFusion cSoC family, based on the proven, low power, firm-error immune ProASIC®3 flash FPGA architecture, benefits from the advantages only flash-based devices offer:

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based SmartFusion cSoCs are live at power-up and do not need to be loaded from an external boot PROM at each power-up. On-board security mechanisms prevent access to the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system programming (ISP) to support future design iterations and critical field upgrades, with confidence that valuable IP cannot be compromised or copied. Secure ISP can be performed using the industry standard AES algorithm with MAC data authentication on the device.

Low Power

Flash-based SmartFusion cSoCs exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With SmartFusion cSoCs, there is no power-on current and no high current transition, both of which are common with SRAM-based FPGAs.

SmartFusion cSoCs also have low dynamic power consumption and support very low power time-keeping mode, offering further power savings.

Security

As the nonvolatile, flash-based SmartFusion cSoC family requires no boot PROM, there is no vulnerable external bitstream. SmartFusion cSoCs incorporate FlashLock®, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only a device with nonvolatile flash programming can offer.

SmartFusion cSoCs utilize a 128-bit flash-based key lock and a separate AES key to provide security for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the AES-128 block cipher encryption standard (FIPS Publication 192).

SmartFusion cSoCs with AES-based security are designed to provide protection for remote field updates over public networks, such as the Internet, and help to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the SmartFusion cSoC family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. SmartFusion cSoCs, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry standard security measures, making remote ISP feasible. A SmartFusion cSoC provides the highest security available for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based SmartFusion cSoCs do not require system configuration components such as electrically erasable programmable read-only memories (EEPROMs) or microcontrollers to load device configuration data during power-up. This reduces bill-of-materials costs and PCB area, and increases system security and reliability.

Live at Power-Up

Flash-based SmartFusion cSoCs are live at power-up (LAPU). LAPU SmartFusion cSoCs greatly simplify total system design and reduce total system cost by eliminating the need for complex programmable logic devices (CPLDs). SmartFusion LAPU clocking (PLLs) replace off-chip clocking resources. In addition, glitches and brownouts in system power will not corrupt the SmartFusion flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout

detection devices from the PCB design. Flash-based SmartFusion cSoCs simplify total system design and reduce cost and design risk, while increasing system reliability.

Immunity to Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O configuration behavior in an unpredictable way.

Another source of radiation-induced firm errors is alpha particles. For alpha radiation to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in SmartFusion cSoCs. Once it is programmed, the flash cell configuration element of SmartFusion cSoCs cannot be altered by high energy neutrons and is therefore immune to errors from them. Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-1 on page 1-4).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

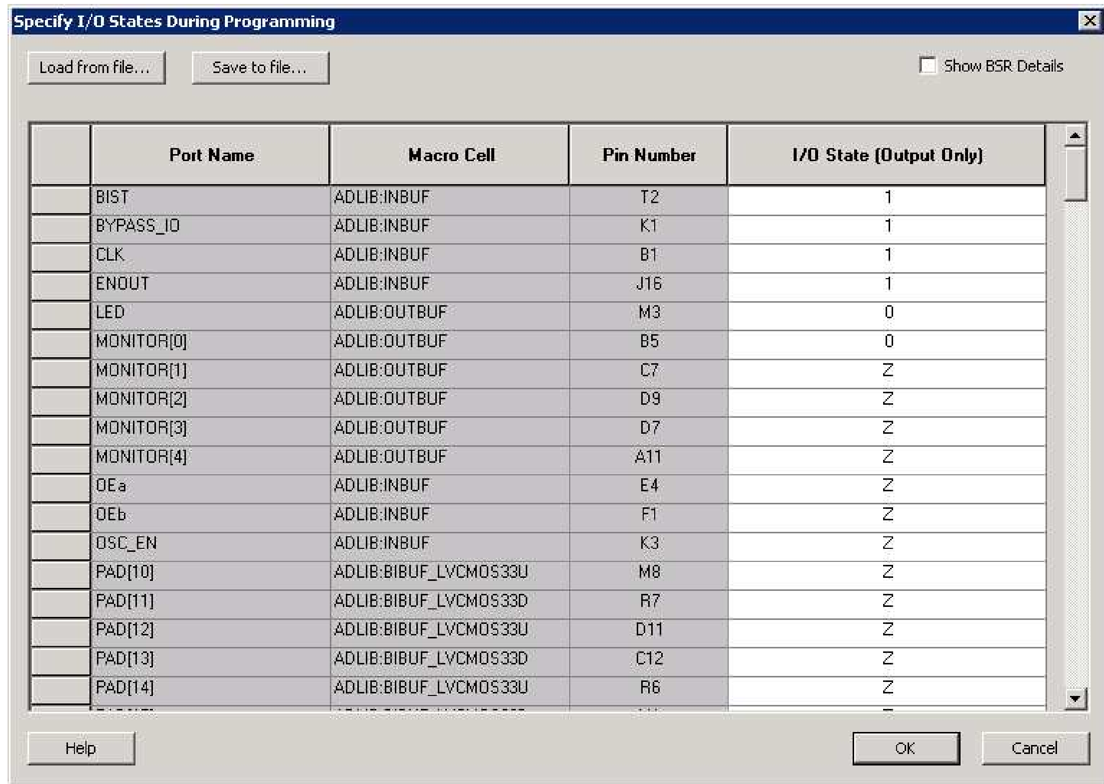


Figure 1-1 • **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

2 – SmartFusion DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond the operating conditions listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-3 on page 2-3 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPP	Programming voltage	–0.3 to 3.75	V
VCCPLLx	Analog power supply (PLL)	–0.3 to 1.65	V
VCCFPGAIOBx	DC FPGA I/O buffer supply voltage	–0.3 to 3.75	V
VCCMSSIOBx	DC MSS I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCxxxxIOBx + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
VCC33A	Analog clean 3.3 V supply to the analog circuitry	–0.3 to 3.75	V
VCC33ADCx	Analog 3.3 V supply to ADC	–0.3 to 3.75	V
VCC33AP	Analog clean 3.3 V supply to the charge pump	–0.3 to 3.75	V
VCC33SDDx	Analog 3.3 V supply to the sigma-delta DAC	–0.3 to 3.75	V
VAREFx	Voltage reference for ADC	1.0 to 3.75	V
VCCRCOSC	Analog supply to the integrated RC oscillator	–0.3 to 3.75	V
VDDBAT	External battery supply	–0.3 to 3.75	V
VCCMAINXTAL	Analog supply to the main crystal oscillator	–0.3 to 3.75	V
VCCLPXTAL	Analog supply to the low power 32 kHz crystal oscillator	–0.3 to 3.75	V
VCCENVM	Embedded nonvolatile memory supply	–0.3 to 1.65	V
VCCESRAM	Embedded SRAM supply	–0.3 to 1.65	V
VCC15A	Analog 1.5 V supply to the analog circuitry	–0.3 to 1.65	V
VCC15ADCx	Analog 1.5 V supply to the ADC	–0.3 to 1.65	V
T_{STG} [1]	Storage temperature	–65 to +150	°C
T_J [1]	Junction temperature	125	°C

Notes:

1. *For flash programming and retention maximum limits, refer to Table 2-4 on page 2-4. For recommended operating conditions, refer to Table 2-3 on page 2-3.*
2. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-5 on page 2-4.*

Table 2-2 • **Analog Maximum Ratings**

Parameter	Conditions	Min.	Max.	Units
ABPS[n] pad voltage (relative to ground)	GDEC[1:0] = 00 (±15.36 V range)			
	Absolute maximum	–11.5	12.4	V
	Recommended	–11	12	V
	GDEC[1:0] = 01 (±10.24 V range)	–11.5	12	V
	GDEC[1:0] = 10 (±5.12 V range)	–6	6	V
	GDEC[1:0] = 11 (±2.56 V range)	–3	3	V
CM[n] pad voltage relative to ground)	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 0 (comparator off, for the associated even-numbered comparator)			
	Absolute maximum	–0.3	12.4	V
	Recommended	–0.3	12	V
	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 1 (comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
TM[n] pad voltage (relative to ground)	TMB_DI_ON = 0 (ADC isolated) COMP_EN = 1(comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
ADC[n] pad voltage (relative to ground)		–0.3	3.6	V

Table 2-3 • **Recommended Operating Conditions**

Symbol	Parameter[1]		Military	Units
T_J	Junction temperature		–55 to +125	°C
VCC [2]	1.5 V DC core supply voltage		1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.425 to 3.6	V
VPP	Programming voltage	Programming mode	3.15 to 3.45	V
		Operation[3]	0 to 3.6	V
VCCPLLx	Analog power supply (PLL)		1.425 to 1.575	V
VCCFPGAIOBx/ VCCMSSIOBx[4]	1.5 V DC supply voltage		1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	V
VCC33A[5]	Analog clean 3.3 V supply to the analog circuitry		3.15 to 3.45	V
VCC33ADCx[5]	Analog 3.3 V supply to ADC		3.15 to 3.45	V
VCC33AP[5]	Analog clean 3.3 V supply to the charge pump		3.15 to 3.45	V
VCC33SDDx[5]	Analog 3.3 V supply to sigma-delta DAC		3.15 to 3.45	V
VAREFx	Voltage reference for ADC		2.527 to 3.3	V
VCCRCOSC	Analog supply to the integrated RC oscillator		3.15 to 3.45	V
VDDBAT	External battery supply		2.7 to 3.63	V
VCCMAINXTAL[5]	Analog supply to the main crystal oscillator		3.15 to 3.45	V
VCCLPXTAL[5]	Analog supply to the low power 32 KHz crystal oscillator		3.15 to 3.45	V
VCCENVM	Embedded nonvolatile memory supply		1.425 to 1.575	V
VCCESRAM	Embedded SRAM supply		1.425 to 1.575	V
VCC15A[2]	Analog 1.5 V supply to the analog circuitry		1.425 to 1.575	V
VCC15ADCx[2]	Analog 1.5 V supply to the ADC		1.425 to 1.575	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *VPP can be left floating during operation (not programming mode).*
4. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-19 on page 2-24. VCCxxxxIOBx should be at the same voltage within a given I/O bank.*
5. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*

Table 2-4 • **Embedded Flash Programming, Storage and Operating Limits**

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Military	Max. T_J = 125°C	Embedded Flash	< 1,000	6 years
			< 10,000	3 years
			< 15,000	1.5 years

Tj (°C)	HTR Lifetime (yrs)
70	102.7
85	43.8
100	20.0
105	15.6
110	12.3
115	9.7
120	7.7
125	6.2
130	5.0
135	4.0
140	3.3
145	2.7
150	2.2

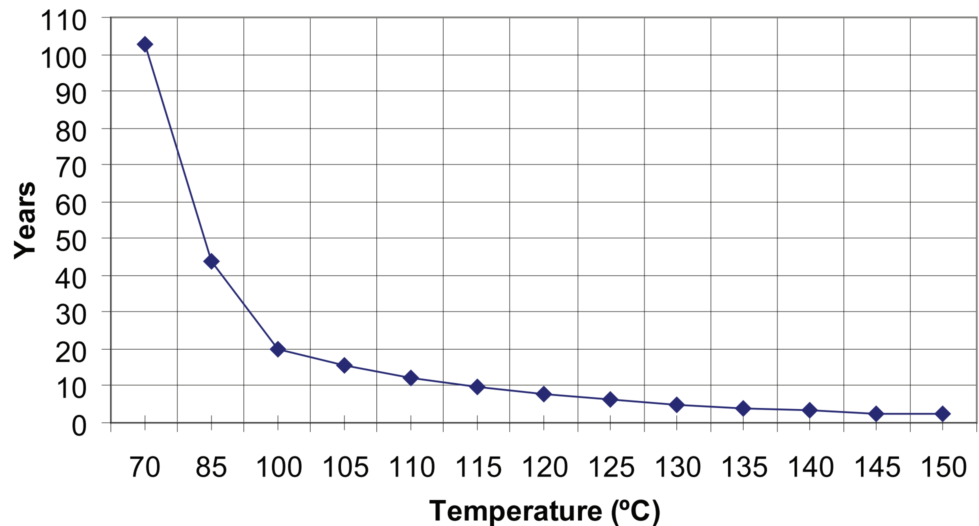


Figure 2-1 • **High Temperature Data Retention (HTR) for FPGA/FlashROM**

Table 2-5 • **Overshoot and Undershoot Limits** [1]

VCCxxxxIOBx	Average VCCxxxxIOBx–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[1]	Maximum Overshoot/ Undershoot (125°C)
2.7 V or less	10%	0.72 V
	5%	0.82 V
3 V	10%	0.72 V
	5%	0.81 V
3.3 V	10%	0.69 V
	5%	0.70 V
3.6 V	10%	–
	5%	–

Notes:

1. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
2. *This table does not provide PCI overshoot/undershoot limits.*

Power Supply Sequencing Requirement

SmartFusion cSoCs have an on-chip 1.5 V regulator, but usage of an external 1.5 V supply is also allowed while the on-chip regulator is disabled. In that case, the 3.3 V supplies (VCC33A, etc.) should be powered before 1.5 V (VCC, etc.) supplies. The 1.5 V supplies should be enabled only after 3.3 V supplies reach a value higher than 2.7 V.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Military)

Sophisticated power-up management circuitry is designed into every SmartFusion cSoC. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-2 on page 2-6.

There are five regions to consider during power-up.

SmartFusion I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCxxxxIOBx are above the minimum specified trip points (Figure 2-2 on page 2-6).
2. VCCxxxxIOBx > VCC – 0.75 V (typical)
3. Chip is in the SoC Mode.

VCCxxxxIOBx Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCxxxxIOBx ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCxxxxIOBx.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

The Microsemi SoC Products Group recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLx exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-2 on page 2-6 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

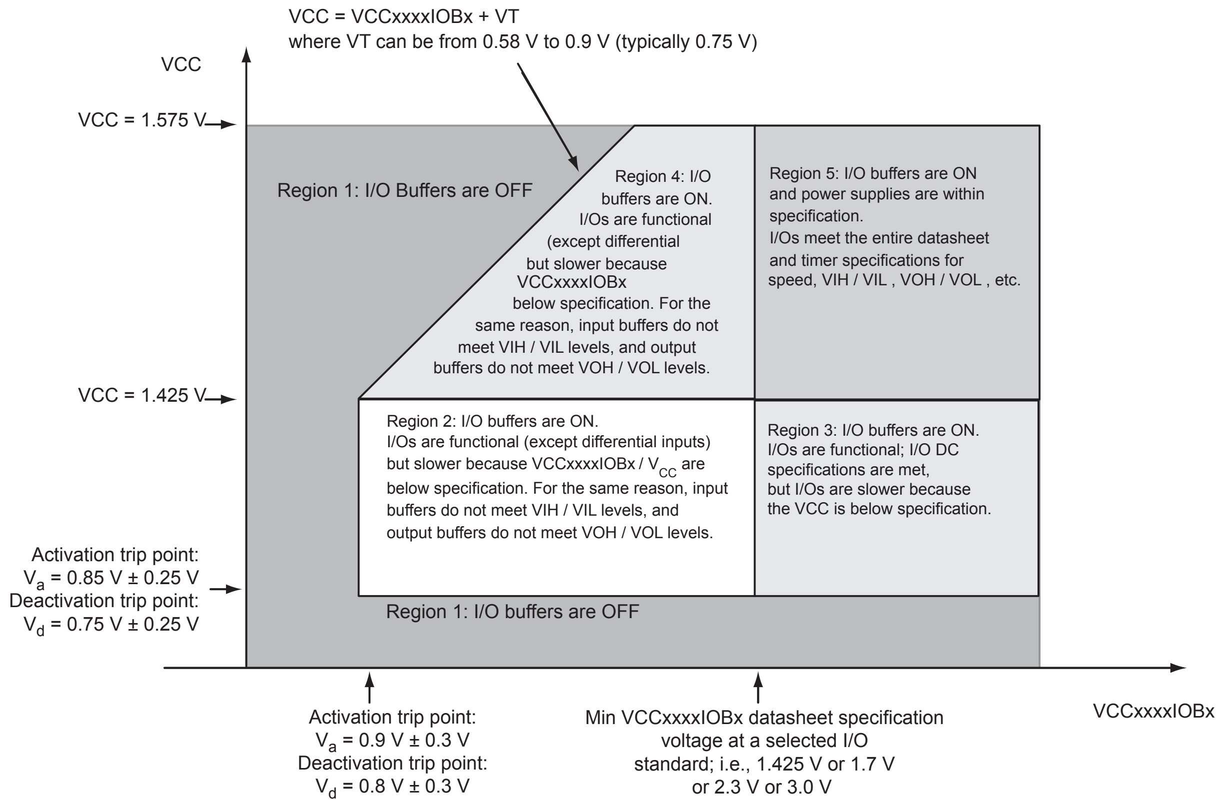


Figure 2-2 • **I/O State as a Function of VCCxxxxIOBx and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 2-6 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
A2F060-FG256	36.9	31.1	29.4	TBD	23.7	°C/W
A2F500-FG256	26.2	20.6	18.9	TBD	13.2	°C/W
A2F500-FG484	21.9	18.6	16.4	7.5	11	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the A2F500-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

θ_{JA} = 18.6°C/W (taken from Table 2-6 on page 2-7).

T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{18.6°C/W} = 1.61\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an A2F500-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 100.00°C

T_A = 70.00°C

From the datasheet:

θ_{JA} = 16.4°C/W

θ_{JC} = 7.5°C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{16.4\ W} = 1.82\ W$$

EQ 6

The 1.82 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{JA(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

θ_{JA} = 0.37°C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 10°C/W - 7.5°C/W - 0.37°C/W = 2.5°C/W$$

A heat sink with a thermal resistance of 2.5°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 125°C, worst-case VCC = 1.425 V)**

Array Voltage VCC (V)		Junction Temperature (°C)						
	–55°C	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**100°C**	**125°C**
1.425	0.81	0.82	0.87	0.89	0.94	0.96	0.97	1.00
1.500	0.76	0.78	0.82	0.84	0.89	0.91	0.92	0.95
1.575	0.73	0.75	0.79	0.81	0.86	0.87	0.89	0.91

Calculating Power Dissipation

Quiescent Supply Current

Table 2-8 • Power Supplies Configuration

Modes and Power Supplies	VCCxxxxIOBx VCCFPGAIOBx VCCMSSIOBx	VCC33A / VCC33ADCx VCC33AP / VCC33SDDx VCCMAINXTAL / VCCLPXTAL	VCC / VCC15A / VCC15ADCx VCCPLLx, VCCENVM, VCCESRAM	VDDBAT	VCCRCOSC	VJTAG	VPP	eNVM (reset/off)	LPXTAL (enable/disable)	MAINXTAL (enable/disable)
Time Keeping mode	0 V	0 V	0 V	3.3 V	0 V	0 V	0 V	Off	Enable	Disable
Standby mode	On*	3.3 V	1.5 V	N/A	3.3 V	N/A	N/A	Reset	Enable	Disable
SoC mode	On*	3.3 V	1.5 V	N/A	3.3 V	N/A	N/A	On	Enable	Enable

*Note: *On means proper voltage is applied. Refer to Table 2-3 on page 2-3 for recommended operating conditions.*

Table 2-9 • Quiescent Supply Current Characteristics

Parameter	Modes		Temperature	A2F060		A2F500	
				1.5 V Domain	3.3 V Domain	1.5 V Domain	3.3 V Domain
IDC1	SoC mode		25°C	3 mA	2 mA	16.5 mA	4 mA
		Nominal	125°C	9.2 mA	9.6 mA	47 mA	9.9 mA
		Worst case	125°C	31 mA	20.5 mA	92 mA	20.5 mA
IDC2	Standby mode		25°C	3 mA	2 mA	16.5 mA	4 mA
		Nominal	125°C	9.2 mA	9.6 mA	47 mA	9.9 mA
		Worst case	125°C	31 mA	20.5 mA	92 mA	20.5 mA
IDC3	Time Keeping mode		25°C	–	10 µA	–	10 µA
		Nominal	125°C	–	30 µA	–	30 µA
		Worst case	125°C	–	300 µA	–	300 µA

Power per I/O Pin

Table 2-10 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins**

	VCCFPGAIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.55
2.5 V LVCMOS	2.5	–	5.97
1.8 V LVCMOS	1.8	–	2.88
1.5 V LVCMOS (JESD8-11)	1.5	–	2.33
3.3 V PCI	3.3	–	19.21
3.3 V PCI-X	3.3	–	19.21
Differential			
LVDS	2.5	2.25	0.82
LVPECL	3.3	5.74	1.16

Table 2-11 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks**

	VCCMSSIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.21
3.3 V LVCMOS / 3.3 V LVCMOS – Schmitt trigger	3.3	–	20.00
2.5 V LVCMOS	2.5	–	5.55
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.03
1.8 V LVCMOS	1.8	–	2.61
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.72
1.5 V LVCMOS (JESD8-11)	1.5	–	1.98
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	1.93

Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings* Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

	C_{LOAD} (pF)	VCCFPGAIOBx (V)	Static Power PDC8 (mW)	Dynamic Power PAC10 (µW/MHz)
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	475.66
2.5 V LVCMOS	35	2.5	–	270.50
1.8 V LVCMOS	35	1.8	–	152.17
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.44
3.3 V PCI	10	3.3	–	202.69
3.3 V PCI-X	10	3.3	–	202.69
Differential				
LVDS	–	2.5	7.75	88.26
LVPECL	–	3.3	19.54	164.99

*Note: *Dynamic power consumption is given for standard load and software default drive strength and output slew.*

Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks

	C_{LOAD} (pF)	VCCMSSIOBx (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	10	3.3	–	19.67
2.5 V LVCMOS	10	2.5	–	11.23
1.8 V LVCMOS	10	1.8	–	5.82
1.5 V LVCMOS (JESD8-11)	10	1.5	–	4.07

Power Consumption of Various Internal Resources

Table 2-14 • **Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs**

Parameter	Definition	Power Supply		Device		Units
		Name	Domain	A2F060	A2F500	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	3.39	5.05	µW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	1.14	2.50	µW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	1.15	1.15	µW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.12	0.12	µW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07	0.07	µW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29	0.29	µW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29	0.29	µW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	1.04	0.79	µW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11			
PAC10	Contribution of an I/O output pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-12			
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25.00		µW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30.00		µW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.60		µW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358.00		µW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	12.88		mW
PAC17	2nd contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	4.80		µW/MHz
PAC18	Main Crystal Oscillator contribution	VCCMAINXTAL	3.3 V	1.98		mW
PAC19a	RC Oscillator contribution	VCCRCOSC	3.3 V	3.30		mW
PAC19b	RC Oscillator contribution	VCC	1.5 V	3.00		mW
PAC20a	Analog Block Dynamic Power Contribution of the ADC	VCC33ADCx	3.3 V	8.25		mW
PAC20b	Analog Block Dynamic Power Contribution of the ADC	VCC15ADCx	1.5 V	3.00		mW
PAC21	Low Power Crystal Oscillator contribution	VCCLPXTAL	3.3 V	33.00		µW
PAC22	MSS Dynamic Power Contribution – Running Drysthone at 100MHz[1]	VCC	1.5 V	67.50		mW
PAC23	Temperature Monitor Power Contribution	See Table 2-94 on page 2-79	–	1.23		mW
PAC24	Current Monitor Power Contribution	See Table 2-93 on page 2-78	–	1.03		mW