
Chipsmall
深圳市津利帝科技有限公司
Geelead Technology Limited
Chipsmall
采购部

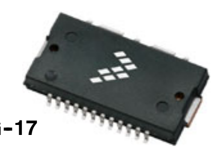
RoHS

RF LDMOS Wideband Integrated Power Amplifiers

A2I20D040NR1
A2I20D040GNR1

1400–2200 MHz, 5 W AVG., 28 V AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS

TO-270WB-17 PLASTIC A2I20D040NR1



TO-270WBG-17 PLASTIC A2I20D040GNR1

The A2I20D040N wideband integrated circuit is designed with on-chip matching that makes it usable from 1400 to 2200 MHz. This multi-stage structure is rated for 20 to 32 V operation and covers all typical cellular base station modulation formats.

1800–2200 MHz

- Typical Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 56 mA, $I_{DQ2(A+B)}$ = 220 mA, P_{out} = 5 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
1800 MHz	32.7	21.8	–43.6
1900 MHz	32.6	20.7	–44.5
2000 MHz	32.8	20.1	–44.8
2100 MHz	32.9	19.9	–44.9
2200 MHz	33.3	19.7	–44.5

1. All data measured in fixture with device soldered to heatsink.

Features

- Extremely Wide RF Bandwidth
- RF Decoupled Drain Pins Reduce Overall Board Space
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (2)

2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

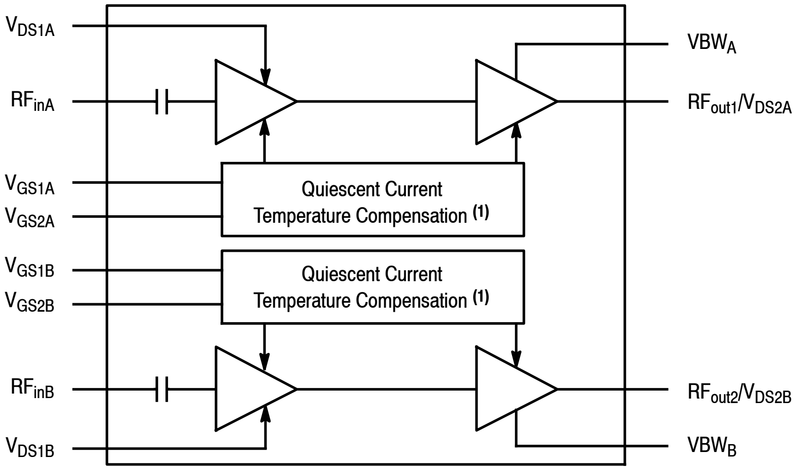
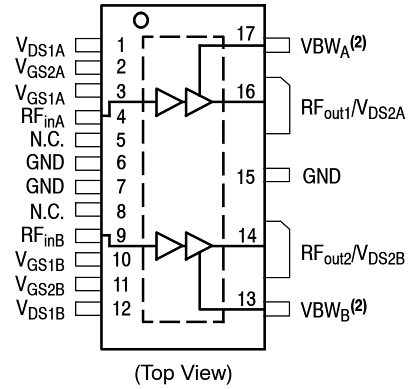


Figure 1. Functional Block Diagram



Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.
2. Device can operate with V_{DD} current supplied through pin 13 and pin 17.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (3,4)	T_J	–40 to +225	°C
Input Power	P_{in}	18	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (4,5)	Unit
Thermal Resistance, Junction to Case Case Temperature 78°C, 5 W, 1900 MHz Stage 1, 28 Vdc, $I_{DQ1(A+B)}$ = 56 mA Stage 2, 28 Vdc, $I_{DQ2(A+B)}$ = 220 mA	$R_{\theta JC}$	 4.8 1.3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	II

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

3. Continuous use at maximum temperature will affect MTTF.
4. MTTF calculator available at http://www.nxp.com/RF/calculators.
5. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 – Off Characteristics [1]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 – On Characteristics					
Gate Threshold Voltage [1] (V_{DS} = 10 Vdc, I_D = 3.5 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ1(A+B)}$ = 56 mAdc)	$V_{GS(Q)}$	—	1.9	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 56 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	6.7	7.4	8.2	Vdc
Stage 2 – Off Characteristics [1]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 – On Characteristics					
Gate Threshold Voltage [1] (V_{DS} = 10 Vdc, I_D = 22 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ2(A+B)}$ = 220 mAdc)	$V_{GS(Q)}$	—	1.8	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ2(A+B)}$ = 220 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.1	4.8	5.6	Vdc
Drain-Source On-Voltage [1] (V_{GS} = 10 Vdc, I_D = 220 mAdc)	$V_{DS(on)}$	0.1	0.3	1.5	Vdc

1. Each side of device measured separately.

(continued)

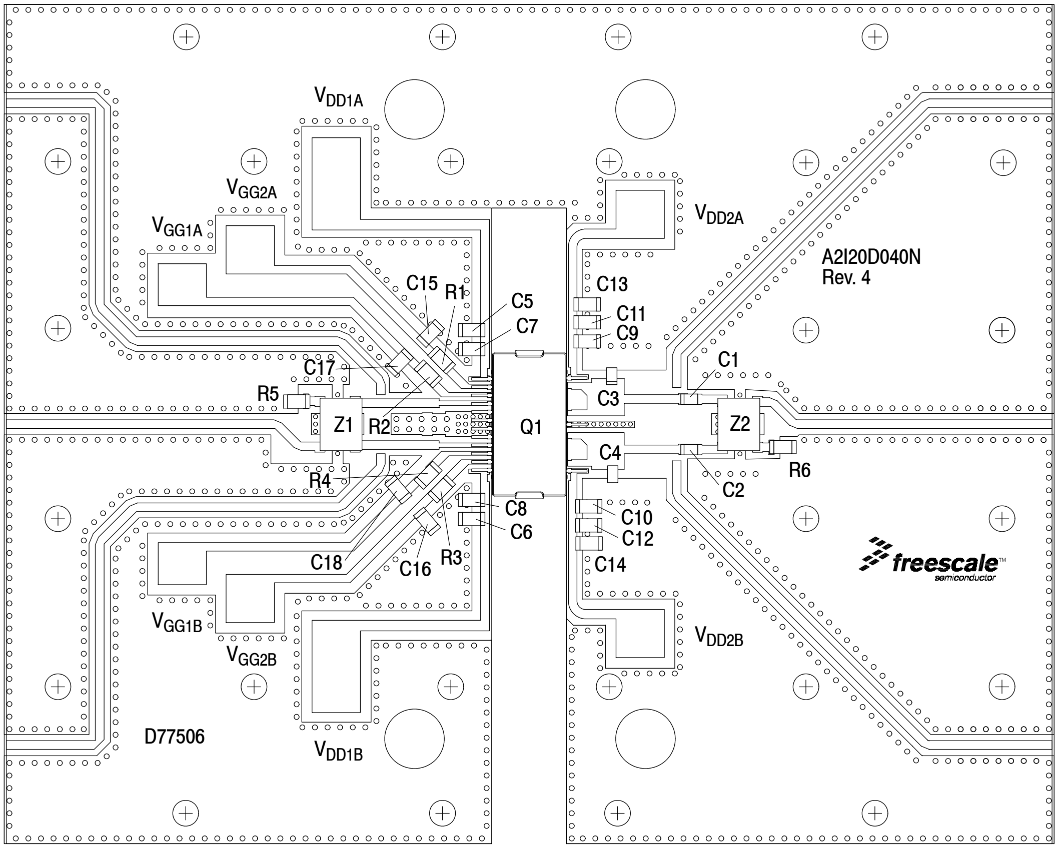
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In Freescale Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 56 mA, $I_{DQ2(A+B)}$ = 220 mA, P_{out} = 5 W Avg., f = 1900 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	31.5	32.1	35.0	dB
Power Added Efficiency	PAE	19.0	19.9	—	%
Adjacent Channel Power Ratio	ACPR	—	–44.7	–43.5	dBc
P_{out} @ 3 dB Compression Point, CW	P3dB	39.8	44.1	—	W
Load Mismatch (In Freescale Production Test Fixture, 50 ohm system) $I_{DQ1(A+B)}$ = 56 mA, $I_{DQ2(A+B)}$ = 220 mA, f = 2200 MHz					
VSWR 10:1 at 32 Vdc, 46.8 W CW Output Power (3 dB Input Overdrive from 40.7 W CW Rated Power)	No Device Degradation				
Typical Performance (3) (In Freescale Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 56 mA, $I_{DQ2(A+B)}$ = 220 mA, 1800–2200 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	36.3	—	W
P_{out} @ 3 dB Compression Point (4)	P3dB	—	44.6	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1800–2200 MHz frequency range.)	Φ	—	–11.8	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	185	—	MHz
Quiescent Current Accuracy over Temperature (5)	ΔI_{QT}				%
with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1		—	2.17	—	
with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2		—	1.70	—	
Gain Flatness in 400 MHz Bandwidth @ P_{out} = 5 W Avg.	G_F	—	0.9	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.038	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.007	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I20D040NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-Reel	TO-270WB-17
A2I20D040GNR1		TO-270WBG-17

1. Part internally input and output matched.
2. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
3. All data measured in fixture with device soldered to heatsink.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.



Note: All data measured in fixture with device soldered to heatsink. Production fixture does not include device soldered to heatsink.

Figure 3. A2I20D040NR1 Test Circuit Component Layout

Table 7. A2I20D040NR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	8.2 pF Chip Capacitors	ATC600F8R2BT250XT	ATC
C3, C4	0.3 pF Chip Capacitors	ATC600F0R3BT250XT	ATC
C5, C6, C7, C8, C9, C10, C11, C12, C13, C14	10 μF Chip Capacitors	GRM31CR61H106KA12L	Murata
C15, C16, C17, C18	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
Q1	RF LDMOS Power Amplifier	A2I20D040NR1	NXP
R1, R2, R3, R4	4.7 kΩ, 1/4 W Chip Resistors	CRCW12064K70FKEA	Vishay
R5, R6	50 Ω, 10 W Chip Resistors	060120A25Z50-2	Anaren
Z1, Z2	1700–2300 MHz, 90°, 3 dB Hybrid Couplers	X3C19P1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D77506	MTL

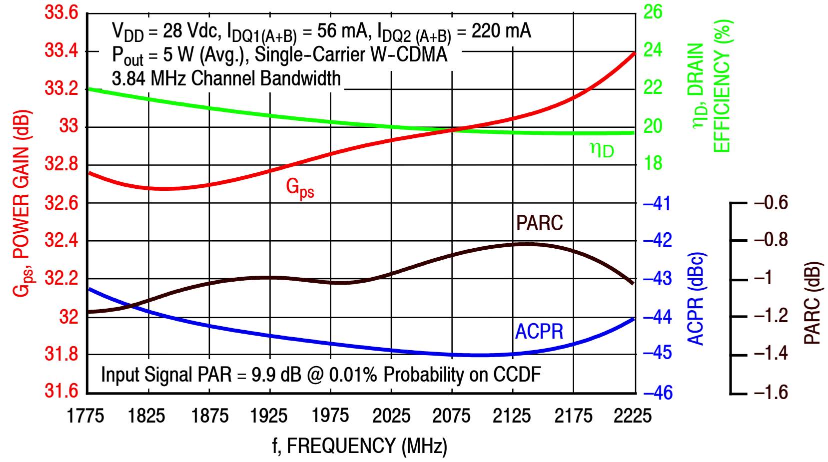


Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 5 Watts Avg.

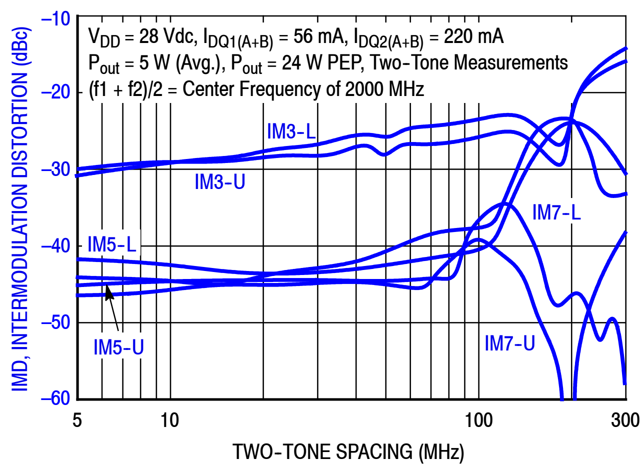


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

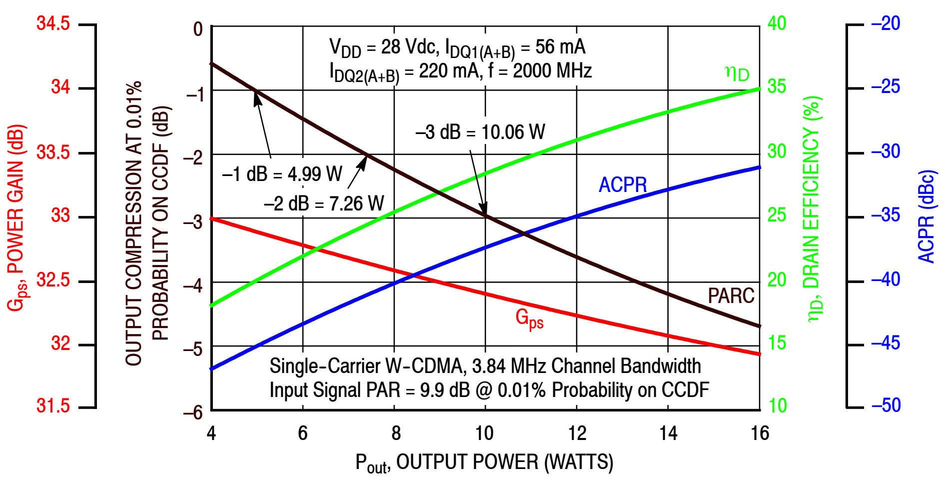


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1800–2200 MHz

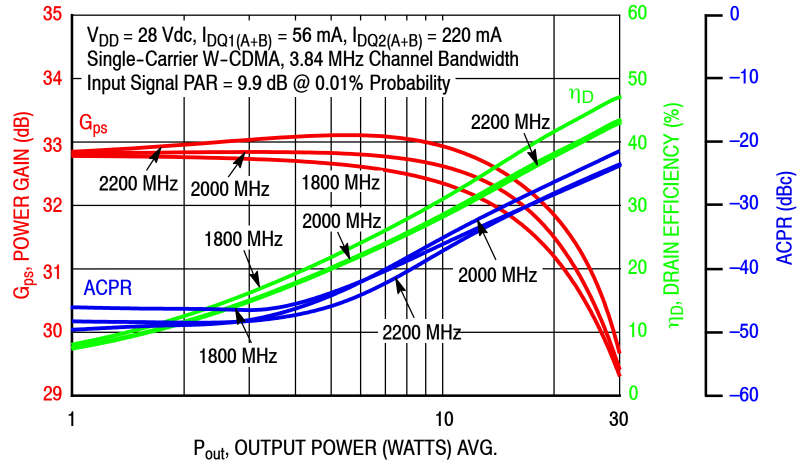


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

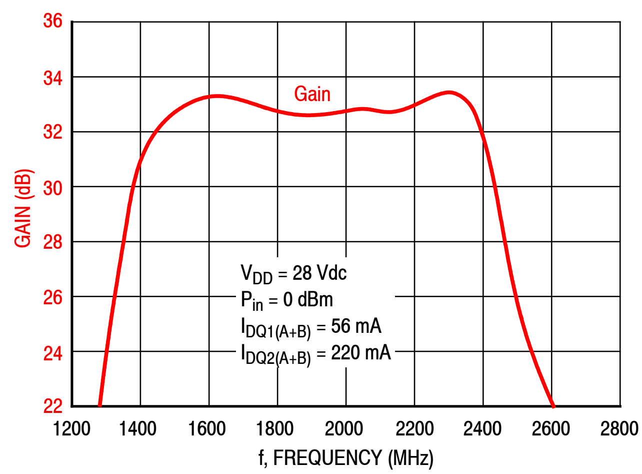


Figure 8. Broadband Frequency Response

Table 8. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 111 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	91.7 + j30.8	84.3 – j41.0	9.16 – j6.03	33.3	43.7	23	54.1	–1
1840	88.8 + j41.4	80.2 – j51.7	8.74 – j5.80	33.6	43.7	23	55.5	–1
1880	74.4 + j58.5	66.7 – j57.5	8.39 – j5.72	33.7	43.8	24	55.9	–1

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	91.7 + j30.8	82.8 – j44.5	9.20 – j6.95	31.2	44.5	28	54.9	–4
1840	88.8 + j41.4	77.1 – j54.3	8.41 – j7.17	31.3	44.5	28	54.4	–4
1880	74.4 + j58.5	63.5 – j58.4	8.39 – j7.13	31.4	44.5	28	54.5	–3

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Table 9. Load Pull Performance — Maximum Drain Efficiency Tuning

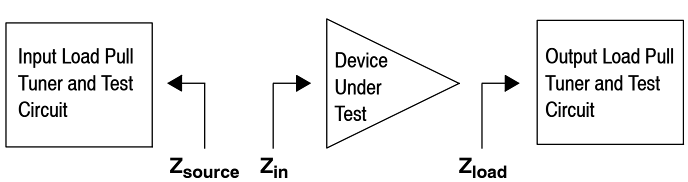
V_{DD} = 28 Vdc, I_{DQ} = 111 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	91.7 + j30.8	91.9 – j41.3	17.6 + j1.68	34.5	41.9	16	64.1	–4
1840	88.8 + j41.4	87.0 – j54.3	15.5 + j2.09	34.7	41.8	15	64.5	–5
1880	74.4 + j58.5	71.3 – j60.7	12.0 + j1.09	34.7	42.3	17	63.8	–4

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	91.7 + j30.8	89.4 – j43.8	16.5 – j0.05	32.4	43.1	20	64.4	–8
1840	88.8 + j41.4	84.7 – j55.7	14.7 + j1.27	32.6	42.8	19	64.2	–9
1880	74.4 + j58.5	70.5 – j62.2	12.0 + j2.85	32.8	42.5	18	63.2	–10

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

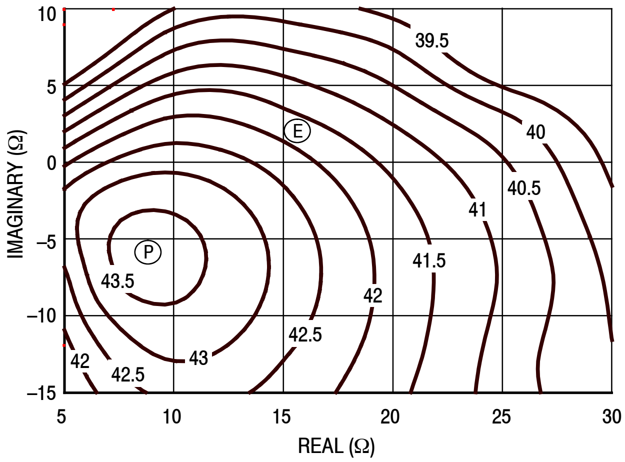


Figure 9. P1dB Load Pull Output Power Contours (dBm)

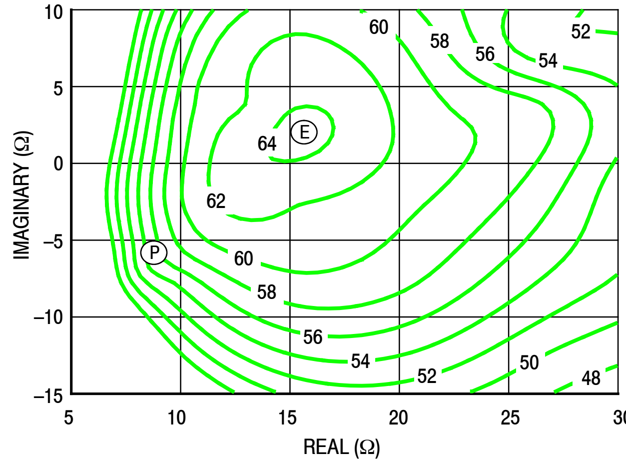


Figure 10. P1dB Load Pull Efficiency Contours (%)

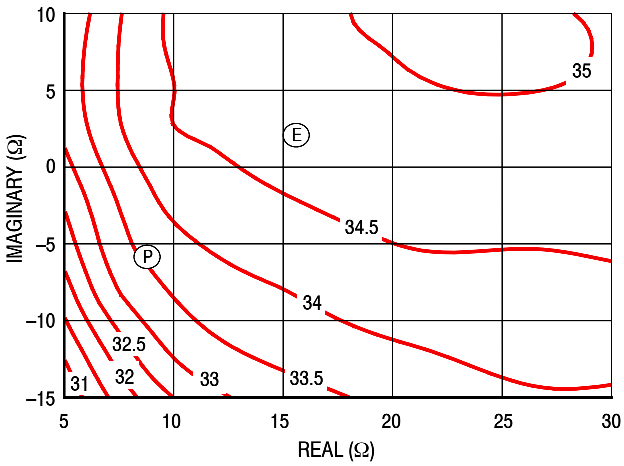


Figure 11. P1dB Load Pull Gain Contours (dB)

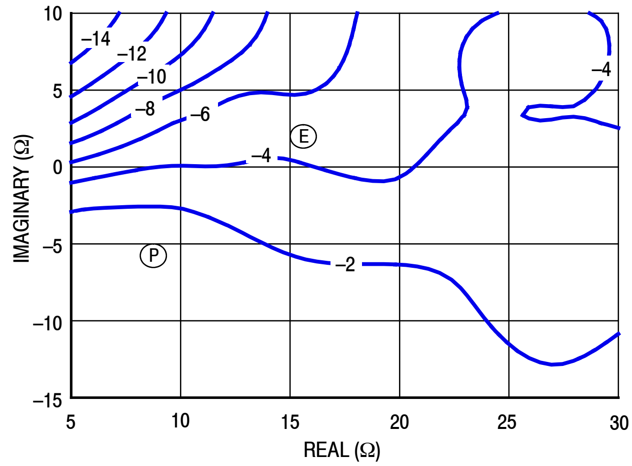


Figure 12. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

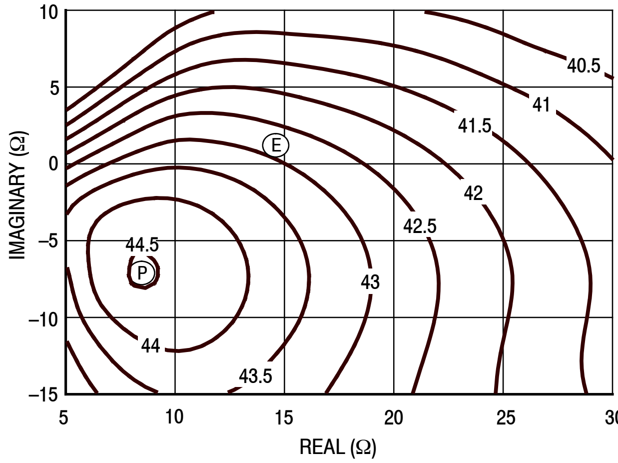


Figure 13. P3dB Load Pull Output Power Contours (dBm)

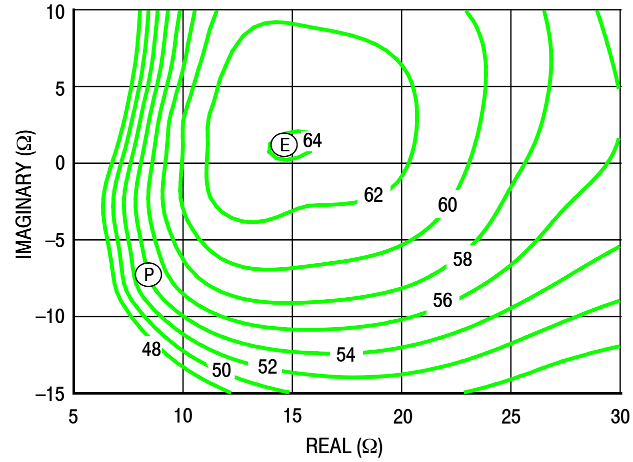


Figure 14. P3dB Load Pull Efficiency Contours (%)

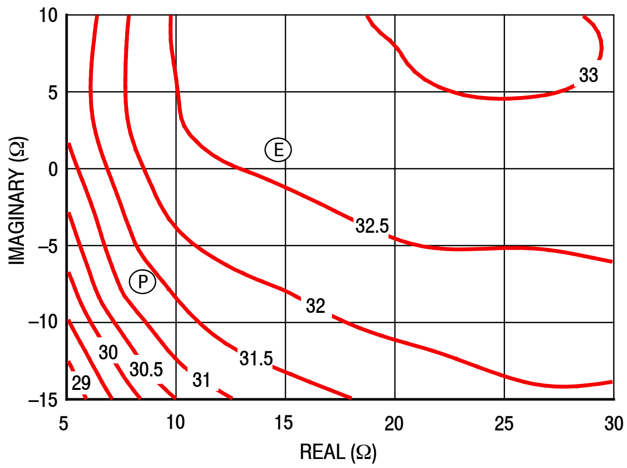


Figure 15. P3dB Load Pull Gain Contours (dB)

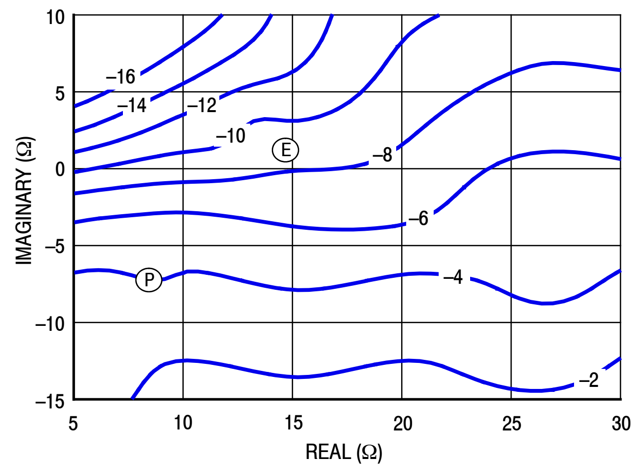


Figure 16. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

Table 10. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 111 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	33.8 + j58.4	31.3 – j52.8	8.14 – j5.05	35.1	43.9	24	53.3	–4
2140	36.0 + j56.4	32.9 – j52.4	8.52 – j4.88	35.8	43.9	24	55.6	–6
2170	38.5 + j56.7	38.3 – j50.8	9.19 – j5.96	35.9	43.8	24	56.5	–5

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	33.8 + j58.4	29.1 – j50.2	8.66 – j5.52	33.0	44.6	29	53.8	–11
2140	36.0 + j56.4	31.4 – j49.2	9.28 – j5.61	33.7	44.6	29	54.8	–14
2170	38.5 + j56.7	37.6 – j46.7	9.78 – j6.87	33.8	44.5	28	54.9	–15

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Table 11. Load Pull Performance — Maximum Drain Efficiency Tuning

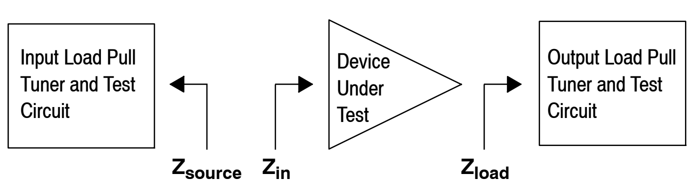
V_{DD} = 28 Vdc, I_{DQ} = 111 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	33.8 + j58.4	31.4 – j56.8	9.04 + j1.83	36.4	42.4	17	63.4	–6
2140	36.0 + j56.4	32.3 – j56.1	9.22 + j1.33	37.0	42.5	18	64.9	–7
2170	38.5 + j56.7	36.6 – j56.0	8.87 + j1.29	37.2	42.2	16	65.5	–9

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	33.8 + j58.4	29.2 – j55.5	8.71 + j1.50	34.3	43.2	21	62.3	–11
2140	36.0 + j56.4	30.2 – j55.0	8.75 + j1.82	35.1	43.0	20	63.0	–14
2170	38.5 + j56.7	34.9 – j53.0	8.38 + j0.32	35.1	43.1	20	63.6	–17

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB – TYPICAL LOAD PULL CONTOURS — 2140 MHz

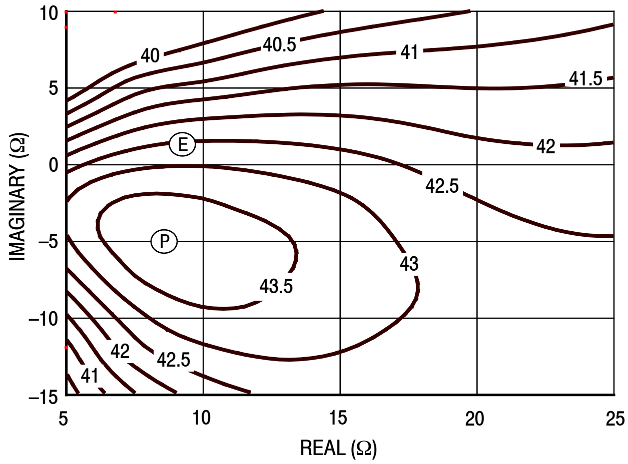


Figure 17. P1dB Load Pull Output Power Contours (dBm)

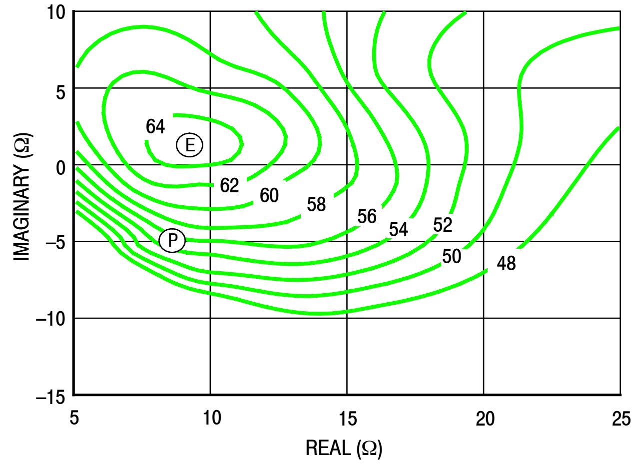


Figure 18. P1dB Load Pull Efficiency Contours (%)

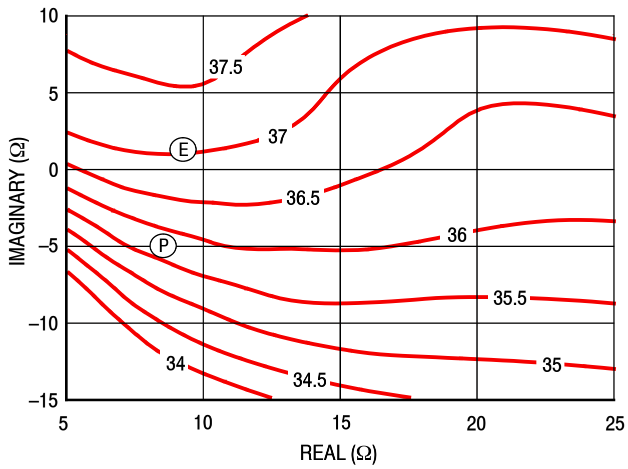


Figure 19. P1dB Load Pull Gain Contours (dB)

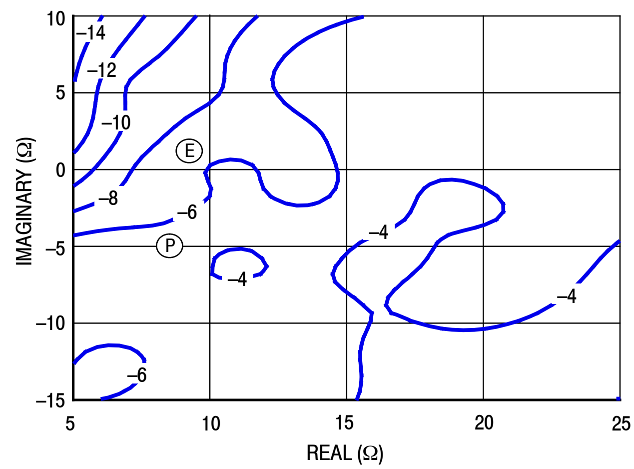


Figure 20. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 2140 MHz

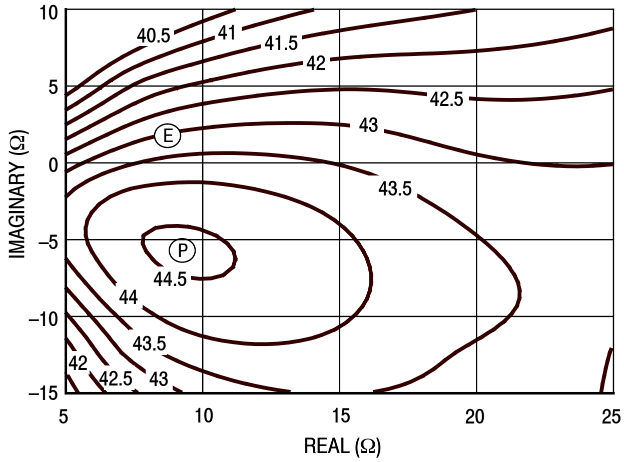


Figure 21. P3dB Load Pull Output Power Contours (dBm)

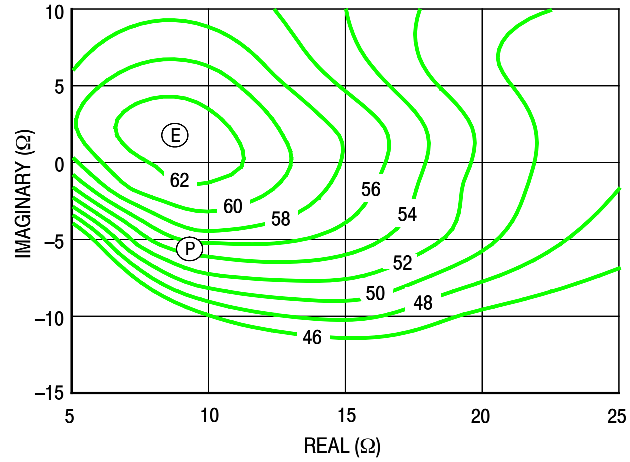


Figure 22. P3dB Load Pull Efficiency Contours (%)

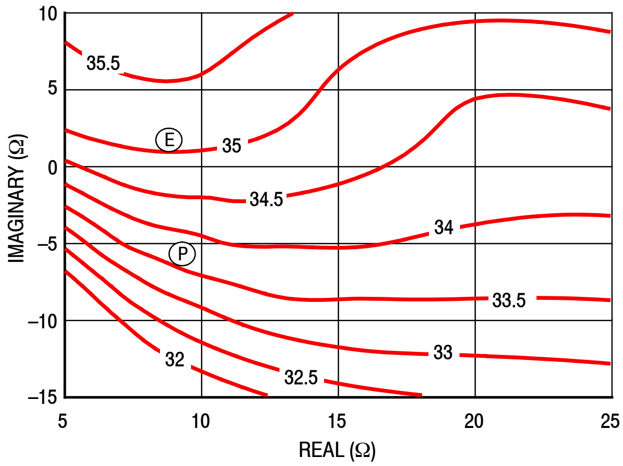


Figure 23. P3dB Load Pull Gain Contours (dB)

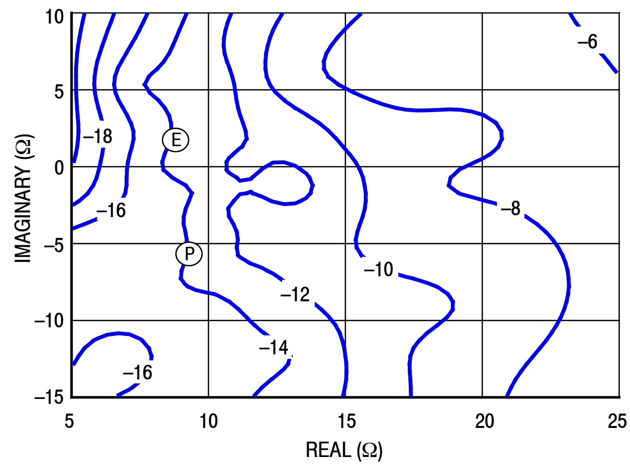


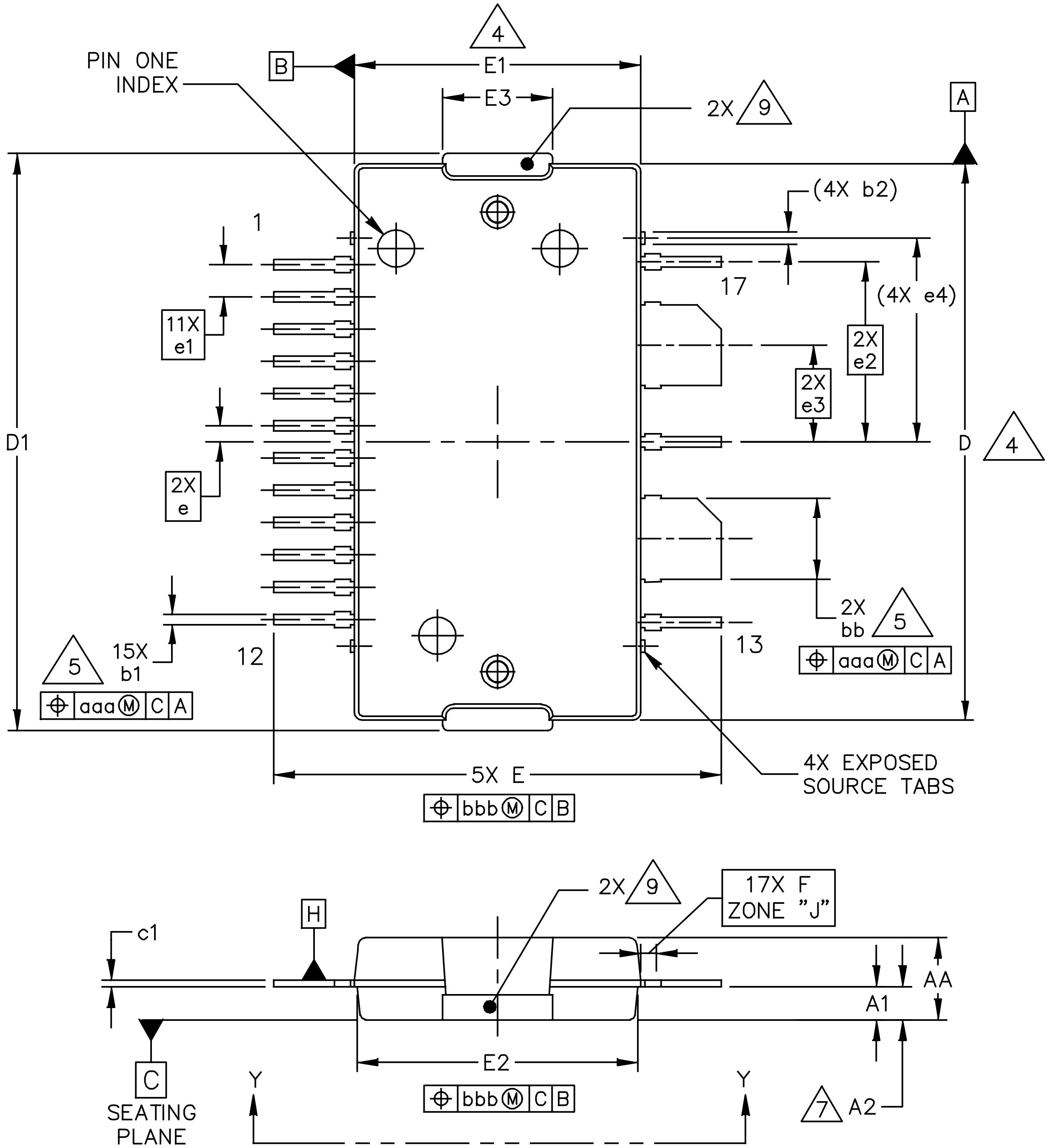
Figure 24. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

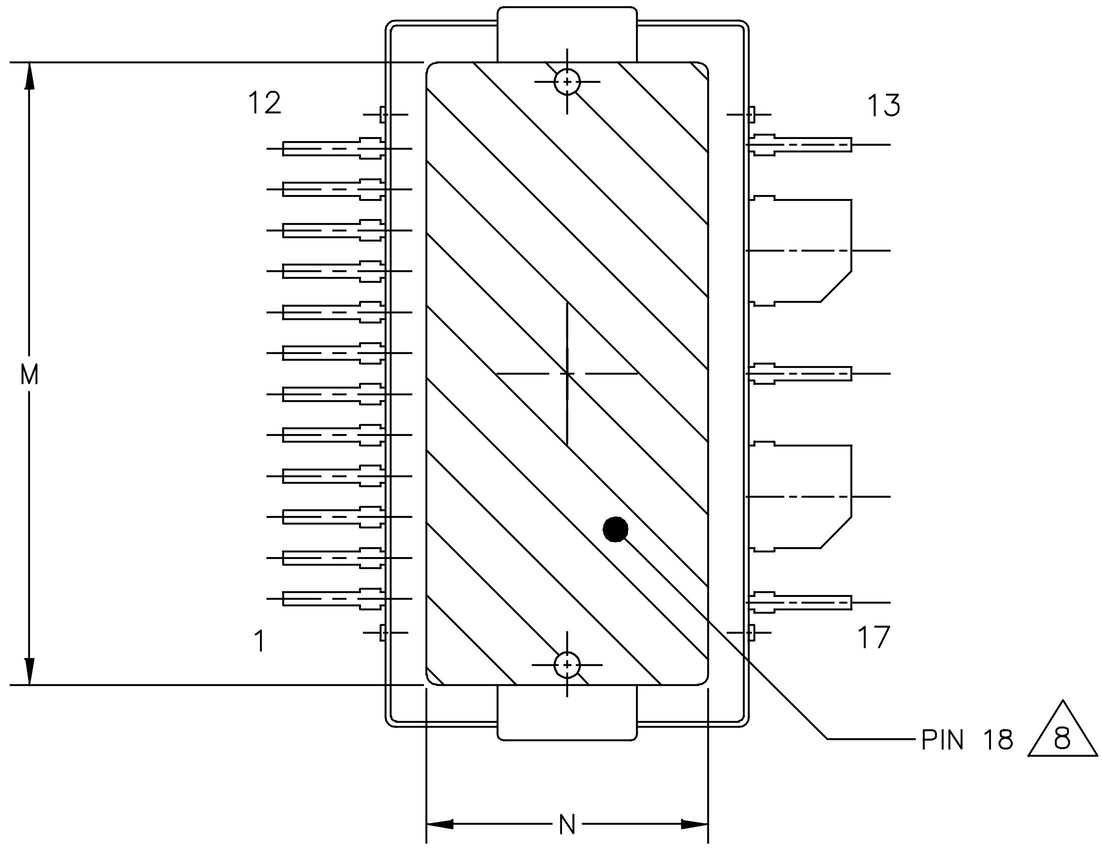
(E) = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270WB–17	DOCUMENT NO: 98ASA00583D	REV: B
	STANDARD: NON–JEDEC	
	SOT1730–1	21 JAN 2016



VIEW Y–Y

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270WB–17	DOCUMENT NO: 98ASA00583D REV: B	
	STANDARD: NON–JEDEC	
	SOT1730–1 21 JAN 2016	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

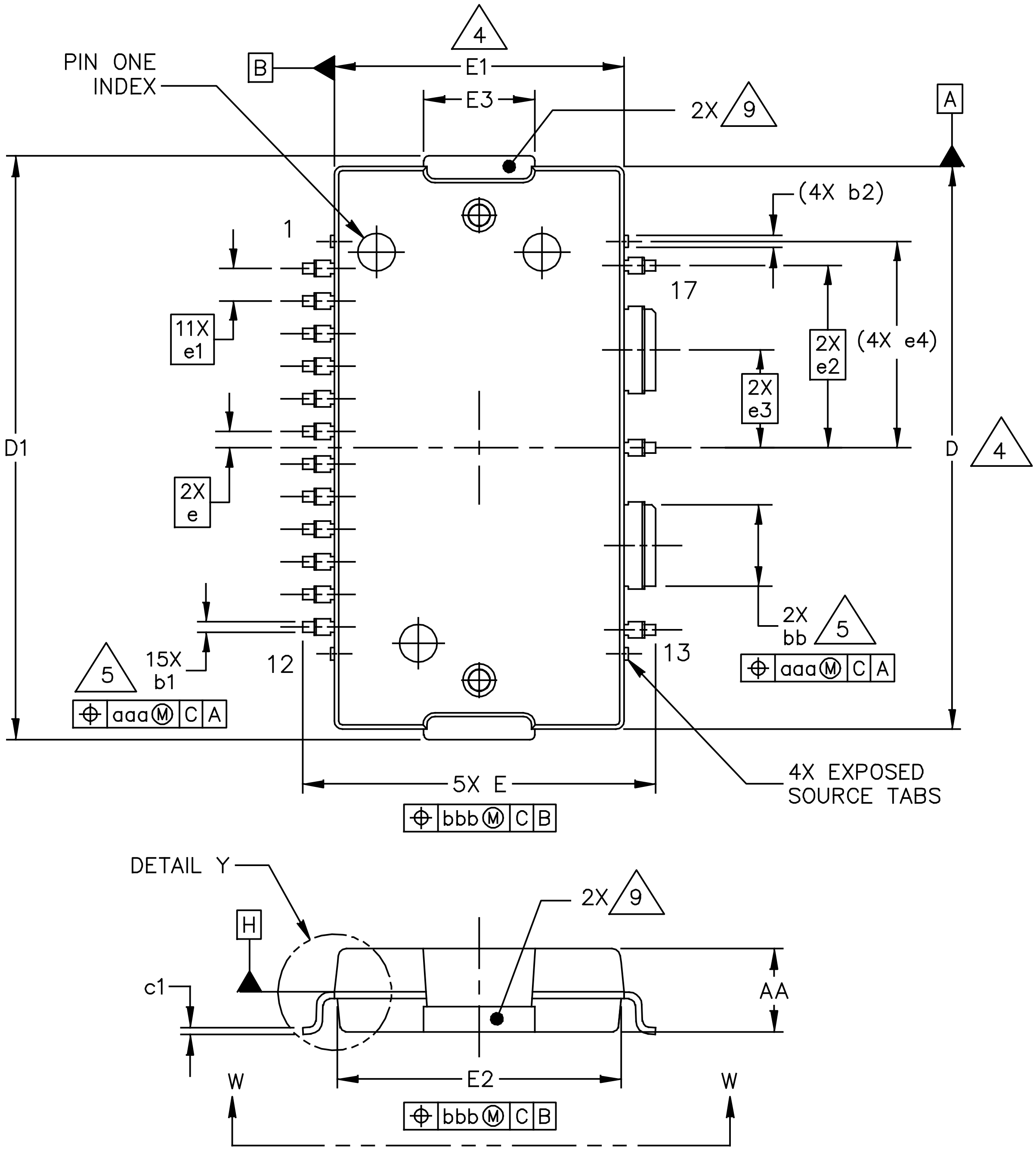
7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

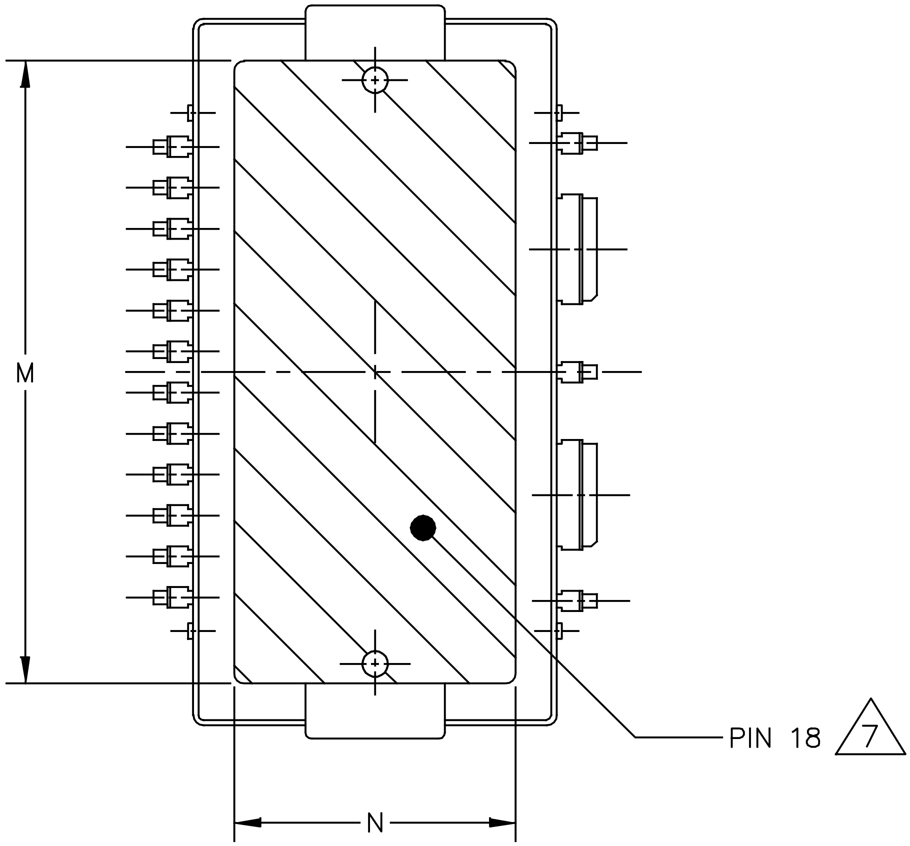
9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.551	.559	14.00	14.20	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

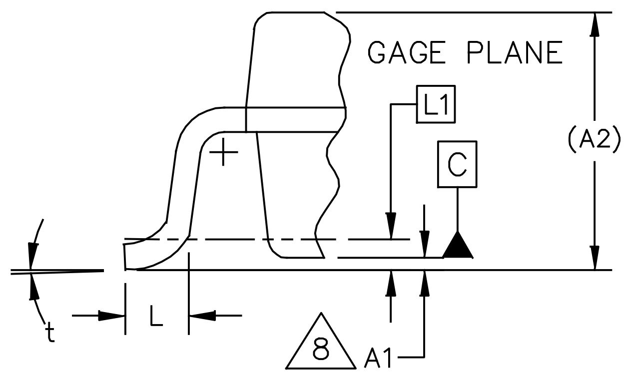
	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270WB–17	DOCUMENT NO: 98ASA00583D	REV: B
	STANDARD: NON–JEDEC	
	SOT1730–1	21 JAN 2016



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE
TITLE: TO–270WBG–17		DOCUMENT NO: 98ASA00729D	REV: B
		STANDARD: NON–JEDEC	
		SOT1730–2	12 JAN 2016



VIEW W–W



DETAIL "Y"

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270WBG–17	DOCUMENT NO: 98ASA00729D	REV: B
	STANDARD: NON–JEDEC	
	SOT1730–2	12 JAN 2016

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.001	.004	0.03	0.10	b1	.010	.016	0.25	0.41
A2	(.105)		(2.67)		b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.429	.437	10.90	11.10	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:

TO–270WBG–17

DOCUMENT NO: 98ASA00729D REV: B

STANDARD: NON–JEDEC

SOT1730–2 12 JAN 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2016	• Initial Release of Data Sheet

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: A2I20D040N
Rev. 0, 4/2016