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RoHS

RF LDMOS Wideband Integrated Power Amplifiers

A2I22D050NR1
A2I22D050GNR1

1800–2200 MHz, 5.3 W AVG., 28 V AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS

The A2I22D050N wideband integrated circuit is designed with on-chip matching that makes it usable from 1800 to 2200 MHz. This multi-stage structure is rated for 24 to 32 V operation and covers all typical cellular base station modulation formats.

2100 MHz

- Typical Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA, $I_{DQ2(A+B)}$ = 520 mA, P_{out} = 5.3 W Avg., Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.(1)

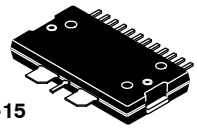
Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
2110 MHz	32.2	17.6	–48.4
2140 MHz	32.4	17.8	–48.2
2170 MHz	32.6	17.9	–47.0

1800 MHz

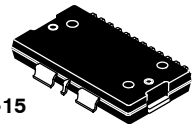
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 70 mA, $I_{DQ2(A+B)}$ = 470 mA, P_{out} = 5.3 W Avg., Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.(1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
1805 MHz	31.8	18.4	–47.5
1840 MHz	31.7	18.2	–50.6
1880 MHz	31.5	17.9	–51.8

1. All data measured in fixture with device soldered to heatsink.



TO-270WB-15
PLASTIC
A2I22D050NR1



TO-270WBG-15
PLASTIC
A2I22D050GNR1

Features

- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (2)
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications

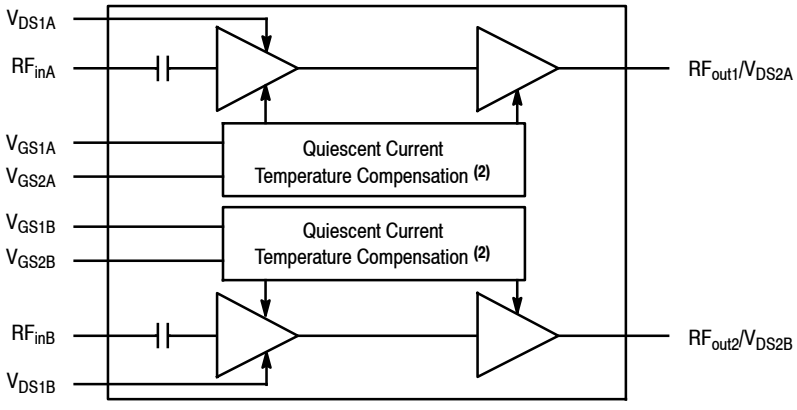
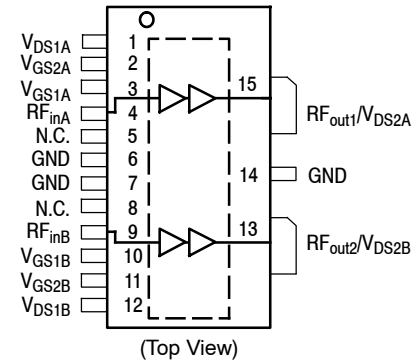


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1977 or AN1987.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
Input Power	P_{in}	28	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 5.3 W CW, 2140 MHz Stage 1, 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA Stage 2, 28 Vdc, $I_{DQ2(A+B)}$ = 520 mA	$R_{\theta JC}$	 5.1 1.1	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	II

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 - Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 - On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 12 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	6.1	6.8	7.6	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.

(continued)

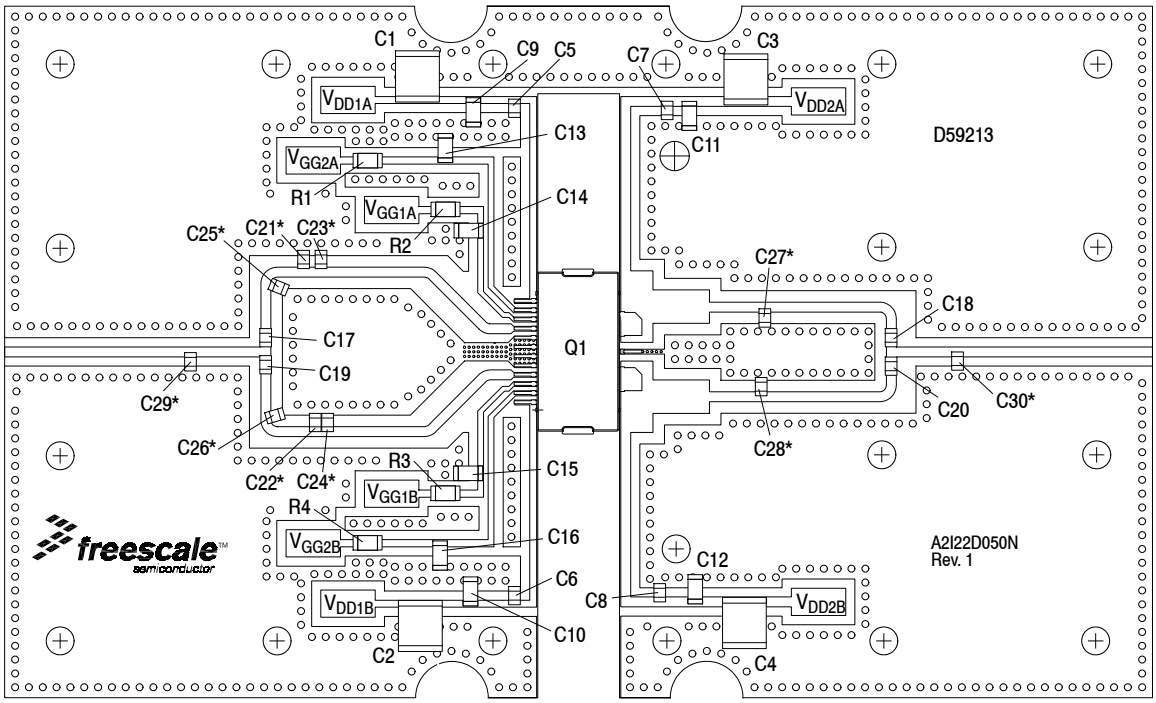
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 46 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ2(A+B)}$ = 520 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ2(A+B)}$ = 520 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	5.3	6.1	6.8	Vdc
Drain–Source On–Voltage (1) (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	0.1	0.24	1.5	Vdc
Functional Tests (2,3) (In Freescale Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA, $I_{DQ2(A+B)}$ = 520 mA, P_{out} = 5.3 W Avg., f = 2140, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	30	31.1	34.0	dB
Power Added Efficiency	PAE	16.7	18.2	—	%
Input Return Loss	IRL	—	–12	–10	dB
P_{out} @ 1 dB Compression Point, CW	P1dB	38.9	44.7	—	W
Load Mismatch (4) (In Freescale Characterization Test Fixture, 50 ohm system) $I_{DQ1(A+B)}$ = 80 mA, $I_{DQ2(A+B)}$ = 520 mA, f = 2140 MHz					
VSWR 10:1 at 32 Vdc, 63 W CW Output Power (3 dB Input Overdrive from 45 W CW Rated Power)	No Device Degradation				
Typical Performance (4) (In Freescale Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA, $I_{DQ2(A+B)}$ = 520 mA, 2110–2170 MHz Bandwidth					
P_{out} @ 3 dB Compression Point, CW (5)	P3dB	—	56	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz frequency range.)	Φ	—	–6.8	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Quiescent Current Accuracy over Temperature (6)	ΔI_{QT}				%
with 4.7 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1		—	1.5	—	
with 4.7 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2		—	5.0	—	
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 5.3 W Avg.	G_F	—	0.4	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.028	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.028	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I22D050NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13–Reel	TO–270WB–15
A2I22D050GNR1		TO–270WBG–15

1. Each side of device measured separately.
2. Part internally input matched.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
4. All data measured in fixture with device soldered to heatsink.
5. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W–CDMA single–carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
6. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf.Select Documentation/Application Notes – AN1977 or AN1987.



*C21, C22, C23, C24, C25, C26, C27, C28, C29 and C30 are mounted vertically.

Note: All data measured in fixture with device soldered to heatsink. Production fixture does not include device soldered to heatsink.

Figure 3. A2I22D050NR1 Characterization Test Circuit Component Layout — 2110–2170 MHz

Table 7. A2I22D050NR1 Characterization Test Circuit Component Designations and Values — 2110–2170 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	10 μF Chip Capacitors	GRM55DR61H106KA88L	Murata
C5, C6	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C7, C8	6.2 pF Chip Capacitors	ATC600F6R2BT250XT	ATC
C9, C10	1 μF Chip Capacitors	GRM31MR71H105KA88L	Murata
C11, C12, C13, C14, C15, C16	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
C17, C18, C19, C20	33 pF Chip Capacitors	ATC600F330JT250XT	ATC
C21, C22	0.3 pF Chip Capacitors	ATC600F0R3BT250XT	ATC
C23, C24, C25, C26, C27, C28	0.2 pF Chip Capacitors	ATC600F0R2BT250XT	ATC
C29, C30	1.1 pF Chip Capacitors	ATC600F1R1BT250XT	ATC
Q1	RF LDMOS Power Amplifier	A2I22D050NR1	Freescale
R1, R2, R3, R4	4.7 kΩ, 1/4 W Chip Resistors	CRCW12064K70FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D59213	MTL

TYPICAL CHARACTERISTICS — 2110–2170 MHz

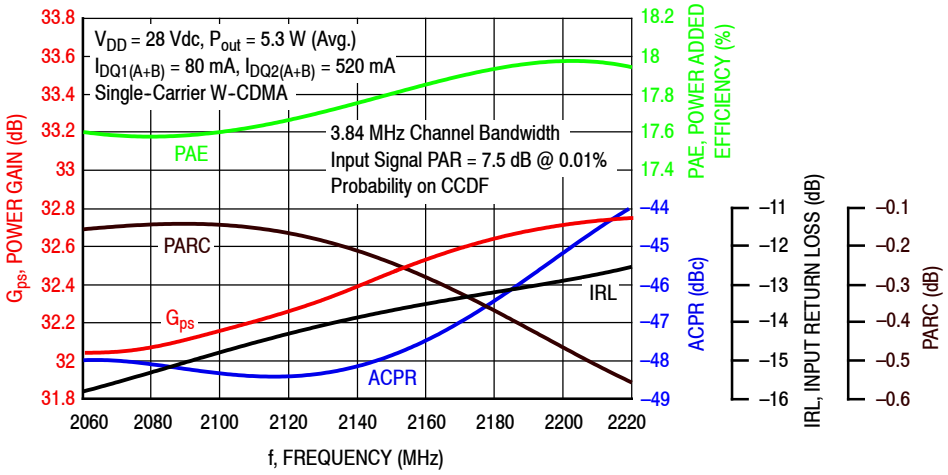


Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 5.3 Watts Avg.

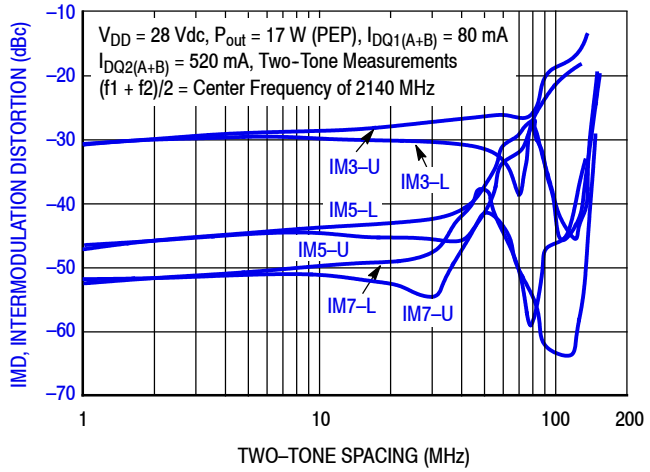


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

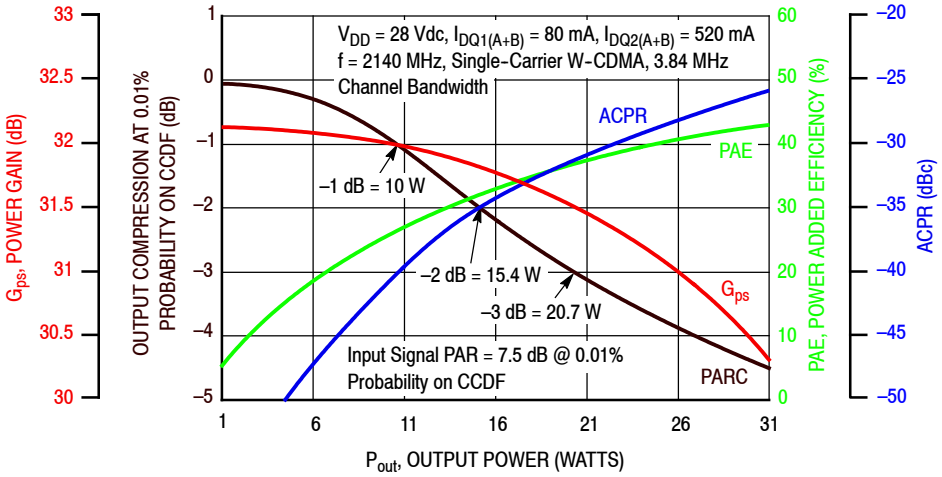


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2110–2170 MHz

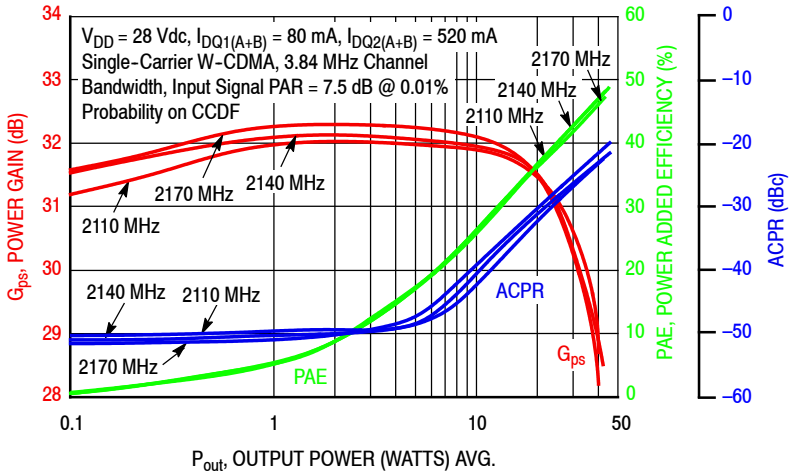


Figure 7. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

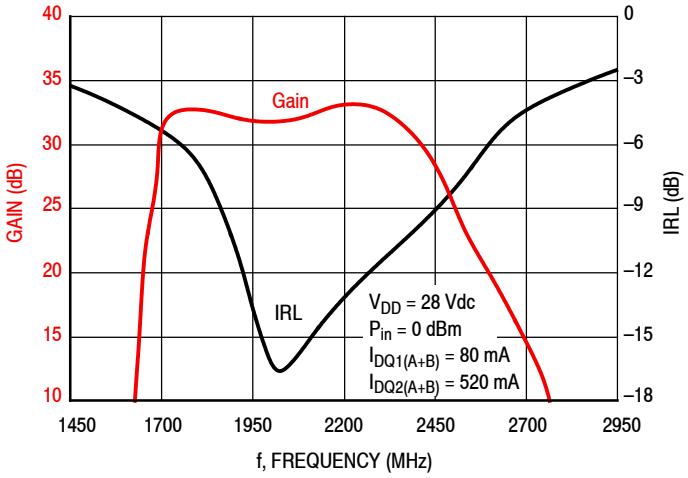


Figure 8. Broadband Frequency Response

Table 8. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 40 mA, I_{DQ2A} = 260 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2110	77.6 + j58.1	70.6 – j50.0	4.21 – j13.5	30.5	46.1	41	51.7	–3
2140	68.5 + j56.2	62.8 – j47.2	4.07 – j13.4	30.7	46.0	40	51.1	–4
2170	60.3 + j50.1	57.8 – j44.5	4.33 – j14.2	30.8	46.2	41	50.9	–4

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2110	77.6 + j58.1	67.2 – j49.6	4.06 – j13.5	28.4	46.8	47	52.1	–6
2140	68.5 + j56.2	59.3 – j45.8	4.07 – j13.7	28.5	46.7	47	51.0	–8
2170	60.3 + j50.1	55.2 – j42.0	4.25 – j14.3	28.7	46.8	48	51.8	–10

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Table 9. Load Pull Performance — Maximum Power Added Efficiency Tuning

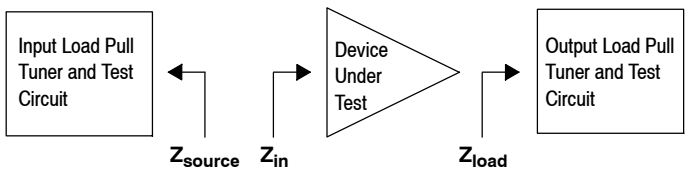
V_{DD} = 28 Vdc, I_{DQ1A} = 40 mA, I_{DQ2A} = 260 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Power Added Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2110	77.6 + j58.1	73.5 – j58.0	6.03 – j9.55	32.3	44.4	28	60.2	–8
2140	68.5 + j56.2	64.2 – j55.4	5.58 – j9.50	32.4	44.4	27	59.2	–8
2170	60.3 + j50.1	58.6 – j53.6	5.05 – j9.53	32.9	44.4	27	59.5	–8

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Power Added Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2110	77.6 + j58.1	71.8 – j57.2	4.13 – j9.91	29.9	45.2	33	60.7	–13
2140	68.5 + j56.2	60.3 – j52.1	5.22 – j10.7	30.0	45.6	37	61.2	–10
2170	60.3 + j50.1	53.7 – j47.3	6.54 – j11.8	30.1	45.8	38	60.4	–8

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB – TYPICAL LOAD PULL CONTOURS — 2140 MHz

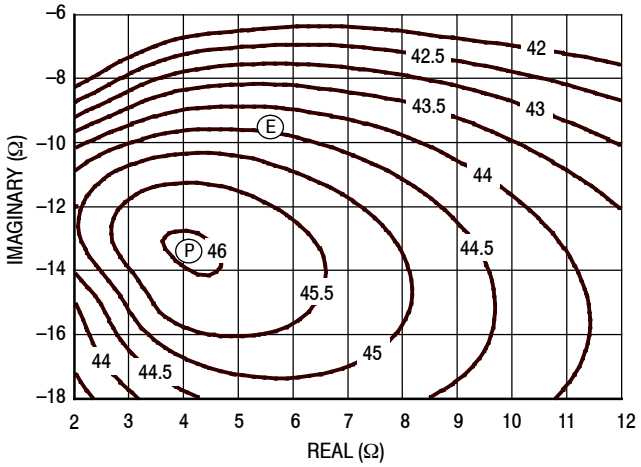


Figure 9. P1dB Load Pull Output Power Contours (dBm)

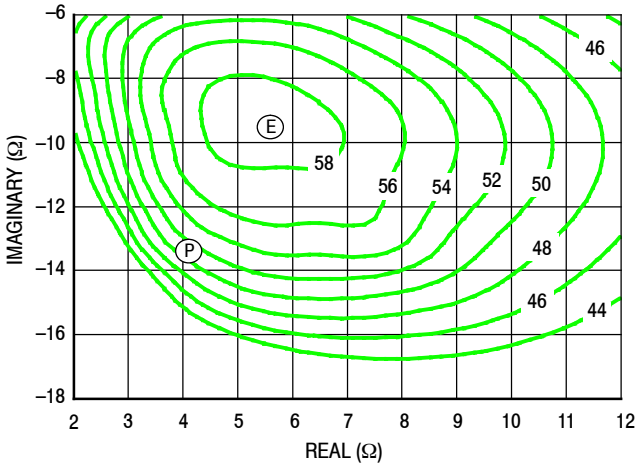


Figure 10. P1dB Load Pull Efficiency Contours (%)

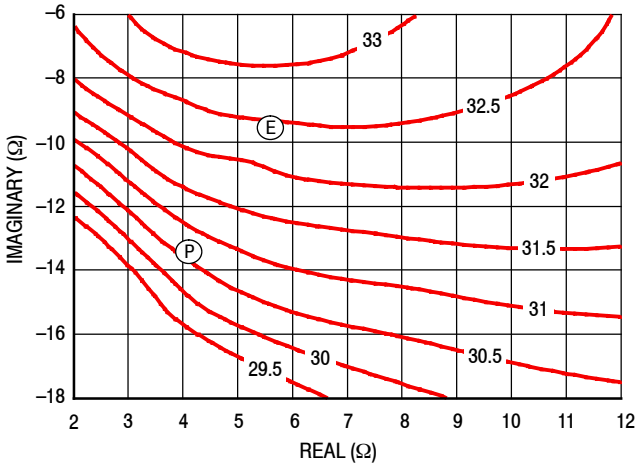


Figure 11. P1dB Load Pull Gain Contours (dB)

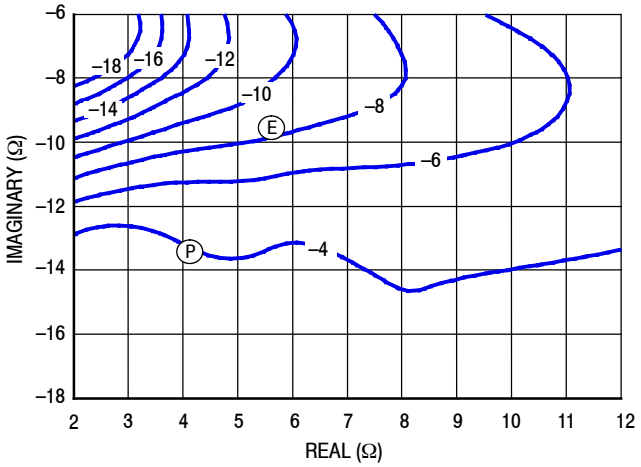


Figure 12. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Power Added Efficiency

Gain

Power Added Efficiency

Linearity

Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 2140 MHz

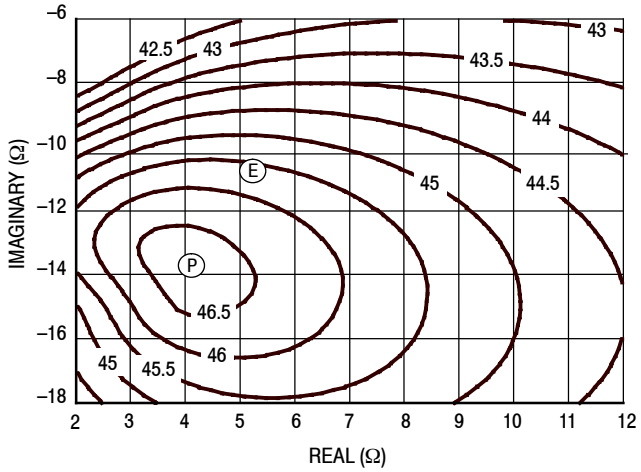


Figure 13. P3dB Load Pull Output Power Contours (dBm)

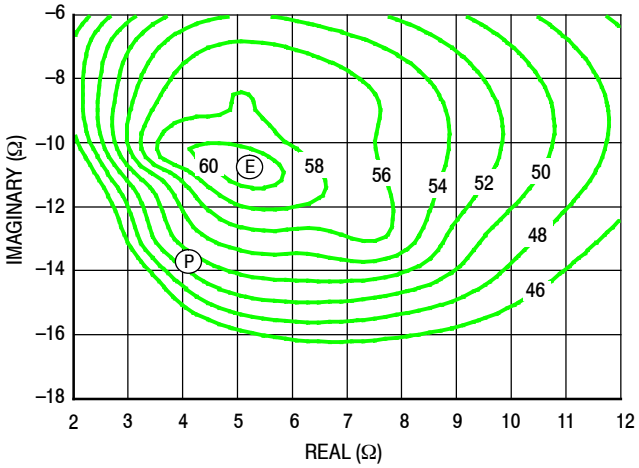


Figure 14. P3dB Load Pull Efficiency Contours (%)

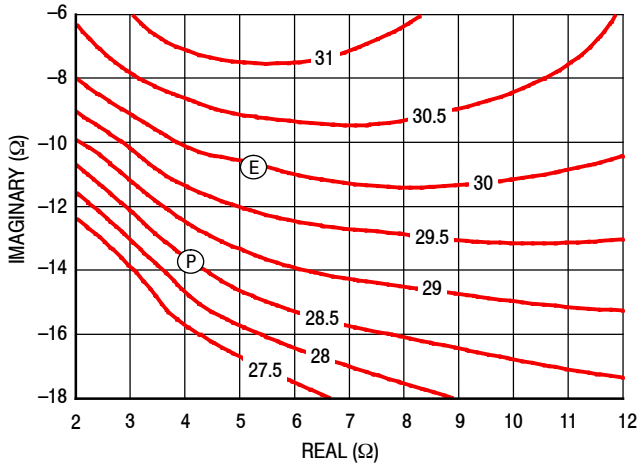


Figure 15. P3dB Load Pull Gain Contours (dB)

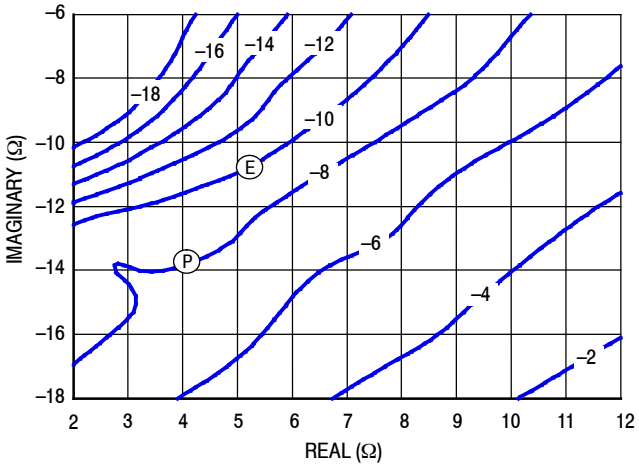


Figure 16. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

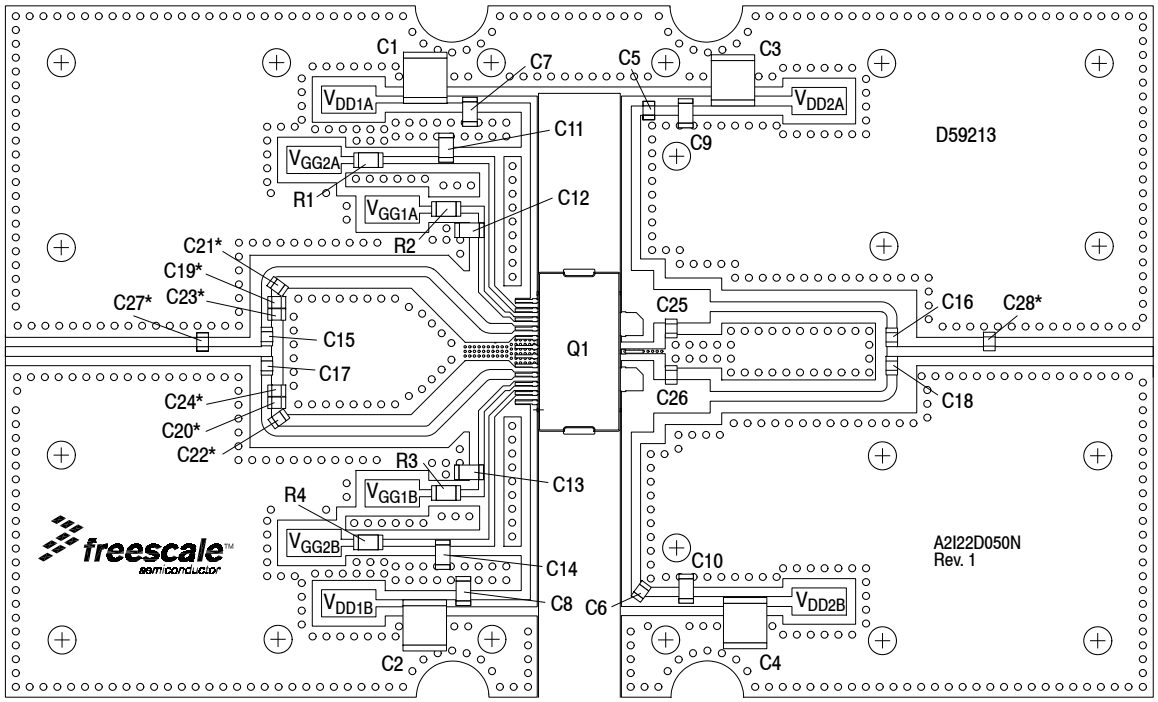
Ⓔ = Maximum Power Added Efficiency

Gain

Power Added Efficiency

Linearity

Output Power



*C19, C20, C21, C22, C23, C24, C27 and C28 are mounted vertically.
Note: All data measured in fixture with device soldered to heatsink.

Figure 17. A2I22D050NR1 Test Circuit Component Layout — 1805–1880 MHz

Table 10. A2I22D050NR1 Test Circuit Component Designations and Values — 1805–1880 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	10 μF Chip Capacitors	GRM55DR61H106KA88L	Murata
C5, C6	6.8 pF Chip Capacitors	ATC600F6R8BT250XT	ATC
C7, C8	1 μF Chip Capacitors	GRM31MR71H105KA88L	Murata
C9, C10, C11, C12, C13, C14	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
C15, C16, C17, C18	47 pF Chip Capacitors	ATC600F470JT250XT	ATC
C19, C20	0.2 pF Chip Capacitors	ATC600F0R2BT250XT	ATC
C21, C22	0.3 pF Chip Capacitors	ATC600F0R3BT250XT	ATC
C23, C24	0.9 pF Chip Capacitors	ATC600F0R9BT250XT	ATC
C25, C26	0.1 pF Chip Capacitors	ATC600F0R1BT250XT	ATC
C27, C28	1.2 pF Chip Capacitors	ATC600F1R2BT250XT	ATC
Q1	RF LDMOS Power Amplifier	A2I22D050NR1	Freescale
R1, R2, R3, R4	4.7 kΩ Chip Resistors	CRCW12064K70FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D59213	MTL

TYPICAL CHARACTERISTICS — 1805–1880 MHz

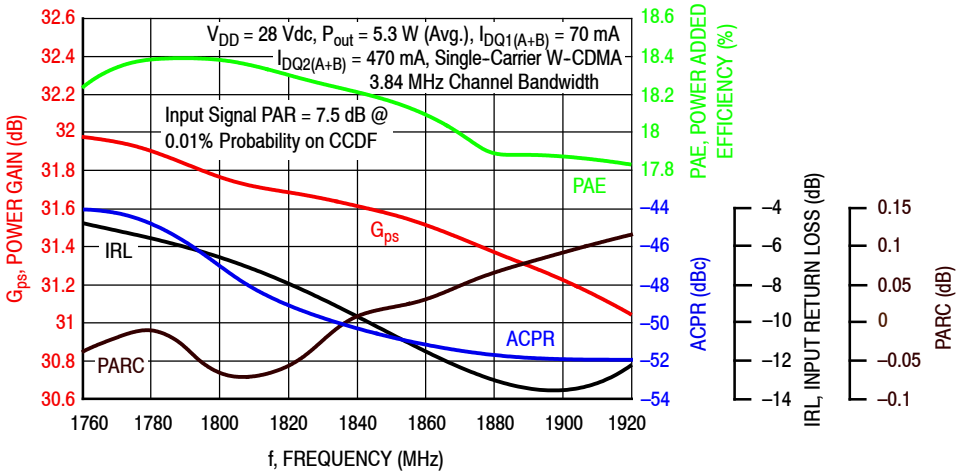


Figure 18. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 5.3 Watts Avg.

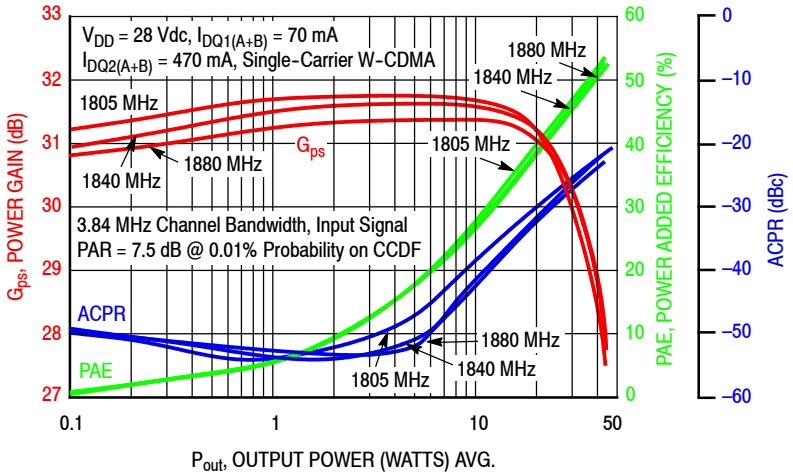


Figure 19. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

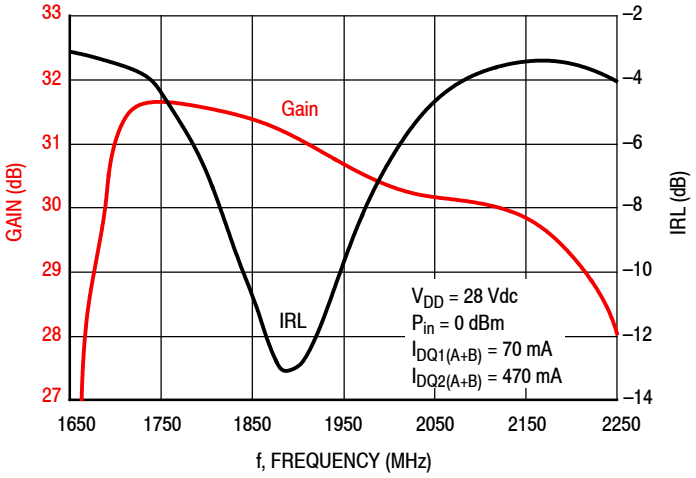


Figure 20. Broadband Frequency Response

Table 11. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 40 mA, I_{DQ2A} = 260 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
1805	69.9 – j34.3	69.7 + j22.8	6.16 – j13.2	32.2	46.0	40	55.3	–5
1840	81.4 – j33.3	82.7 + j22.2	6.22 – j12.4	32.2	46.0	40	56.0	–3
1880	109.0 – j26.4	101.0 + j12.4	5.84 – j12.6	31.6	46.1	40	56.3	–1

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
1805	69.9 – j34.3	72.0 + j22.0	5.85 – j13.2	30.0	47.0	50	58.7	–7
1840	81.4 – j33.3	84.7 + j19.7	5.75 – j12.5	30.0	46.9	49	58.0	–4
1880	109.0 – j26.4	101.0 + j9.08	5.39 – j12.6	29.4	46.9	49	57.4	–3

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Table 12. Load Pull Performance — Maximum Power Added Efficiency Tuning

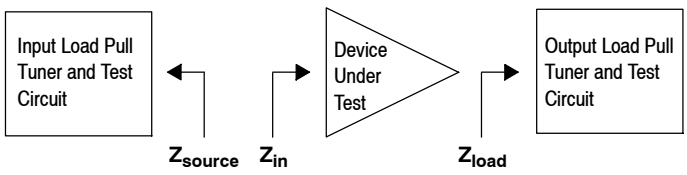
V_{DD} = 28 Vdc, I_{DQ1A} = 40 mA, I_{DQ2A} = 260 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Power Added Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
1805	69.9 – j34.3	68.6 + j30.8	12.0 – j12.8	33.9	44.6	29	62.2	–6
1840	81.4 – j33.3	86.2 + j28.8	10.6 – j11.9	33.3	44.8	31	62.3	–5
1880	109.0 – j26.4	108.0 + j18.3	10.2 – j10.9	32.8	44.7	30	62.1	–5

			Max Power Added Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
1805	69.9 – j34.3	71.2 + j25.7	8.55 – j12.8	31.1	46.5	44	68.6	–7
1840	81.4 – j33.3	88.8 + j27.6	11.6 – j11.7	31.5	45.4	34	65.5	–7
1880	109.0 – j26.4	106.0 + j13.6	8.68 – j11.3	30.5	45.9	39	65.6	–6

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

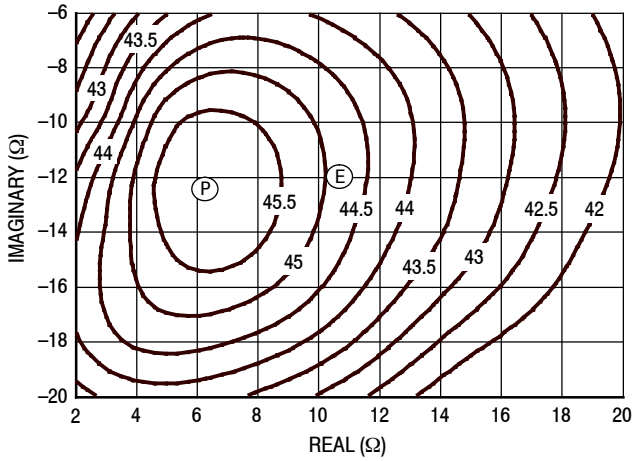


Figure 21. P1dB Load Pull Output Power Contours (dBm)

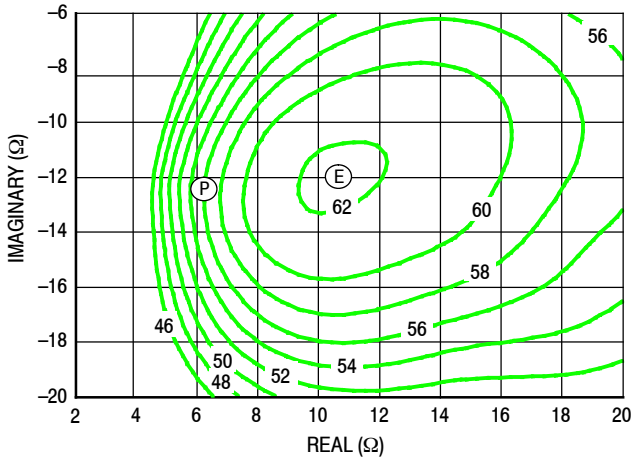


Figure 22. P1dB Load Pull Efficiency Contours (%)

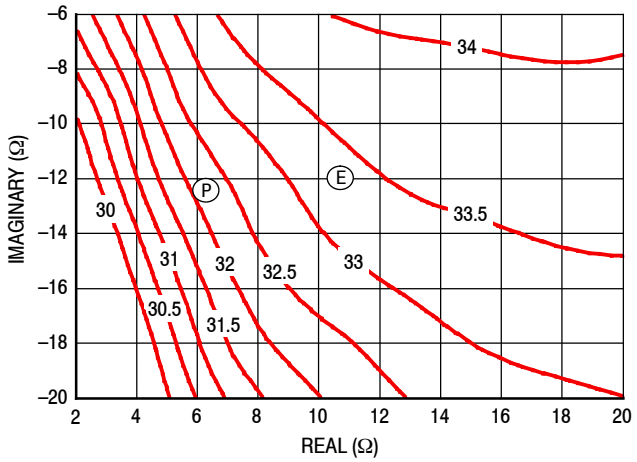


Figure 23. P1dB Load Pull Gain Contours (dB)

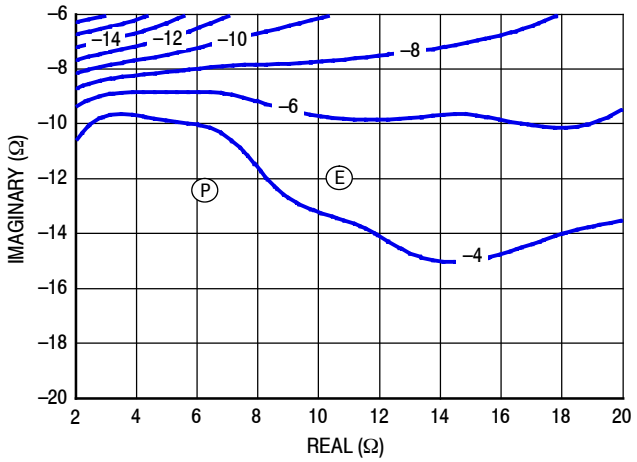


Figure 24. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Power Added Efficiency

Gain

Power Added Efficiency

Linearity

Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

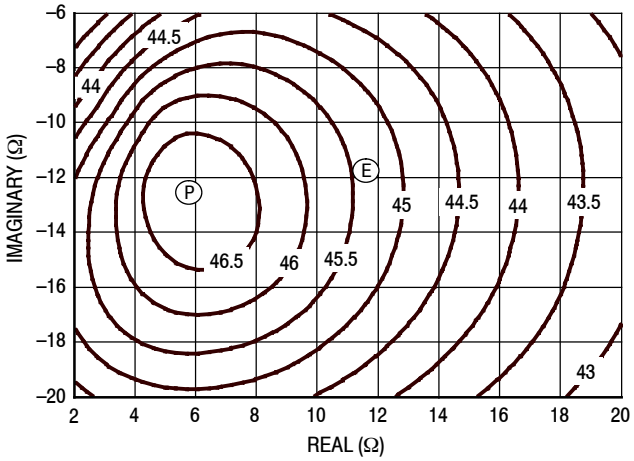


Figure 25. P3dB Load Pull Output Power Contours (dBm)

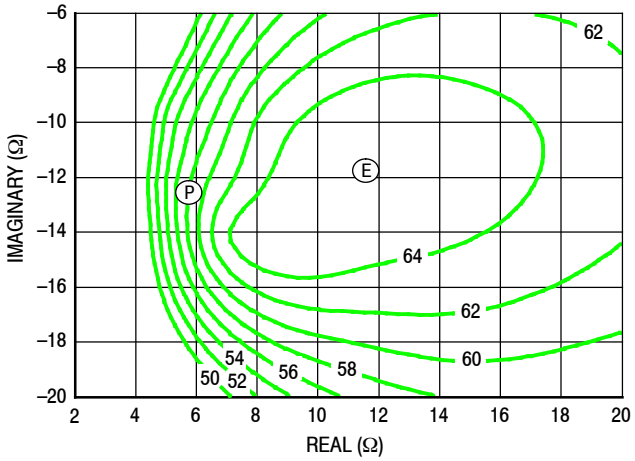


Figure 26. P3dB Load Pull Efficiency Contours (%)

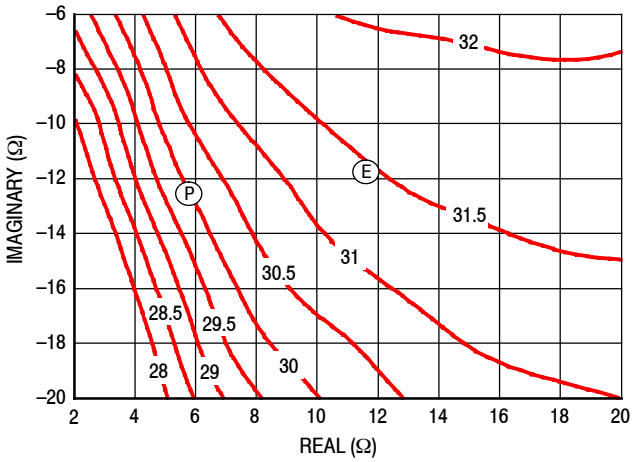


Figure 27. P3dB Load Pull Gain Contours (dB)

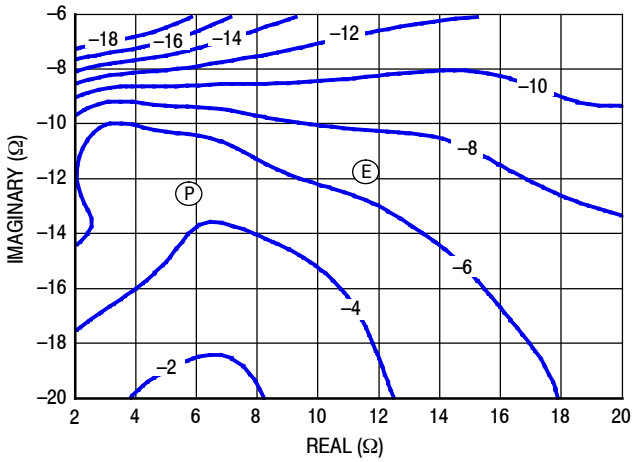


Figure 28. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Power Added Efficiency

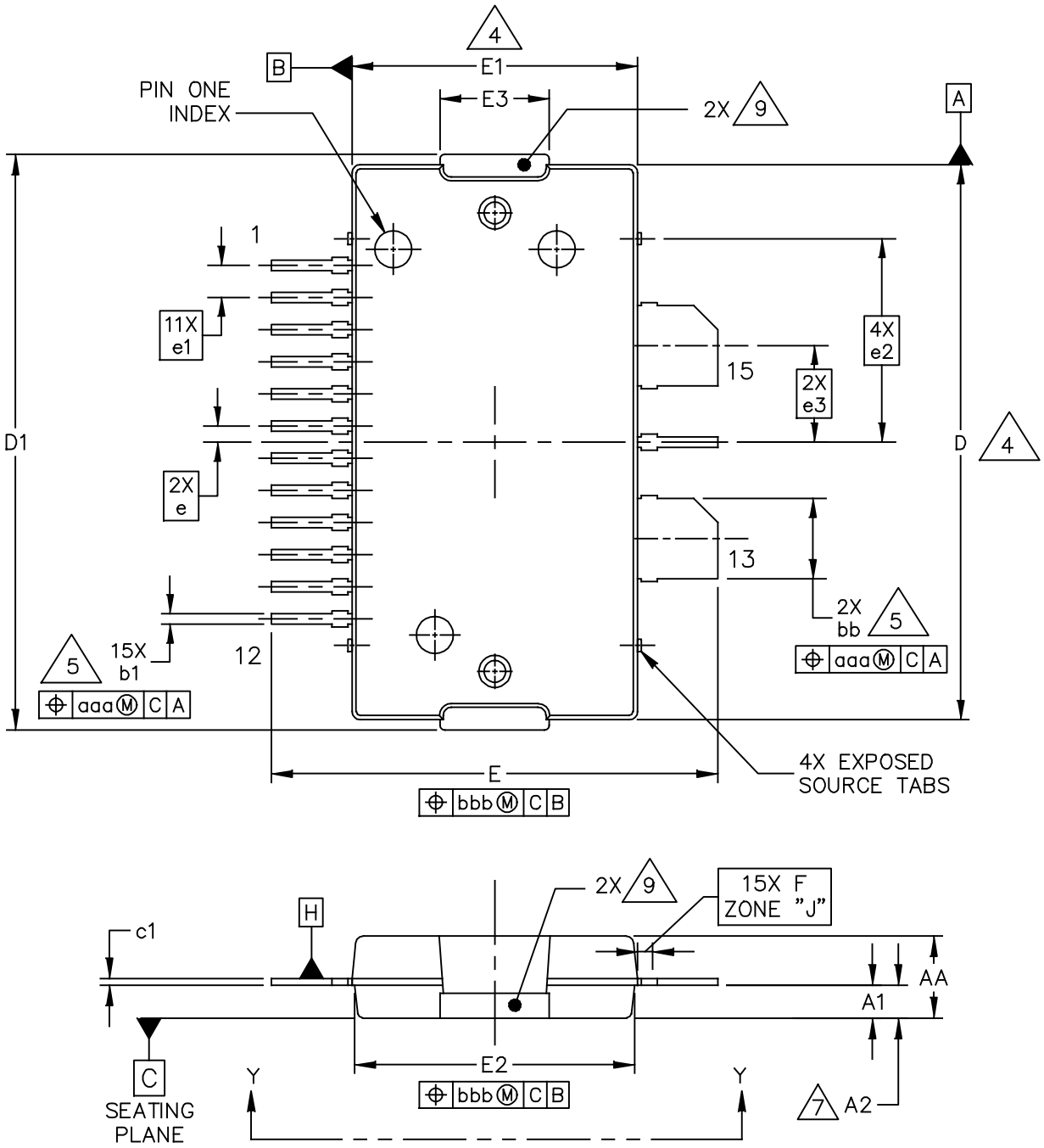
Gain

Power Added Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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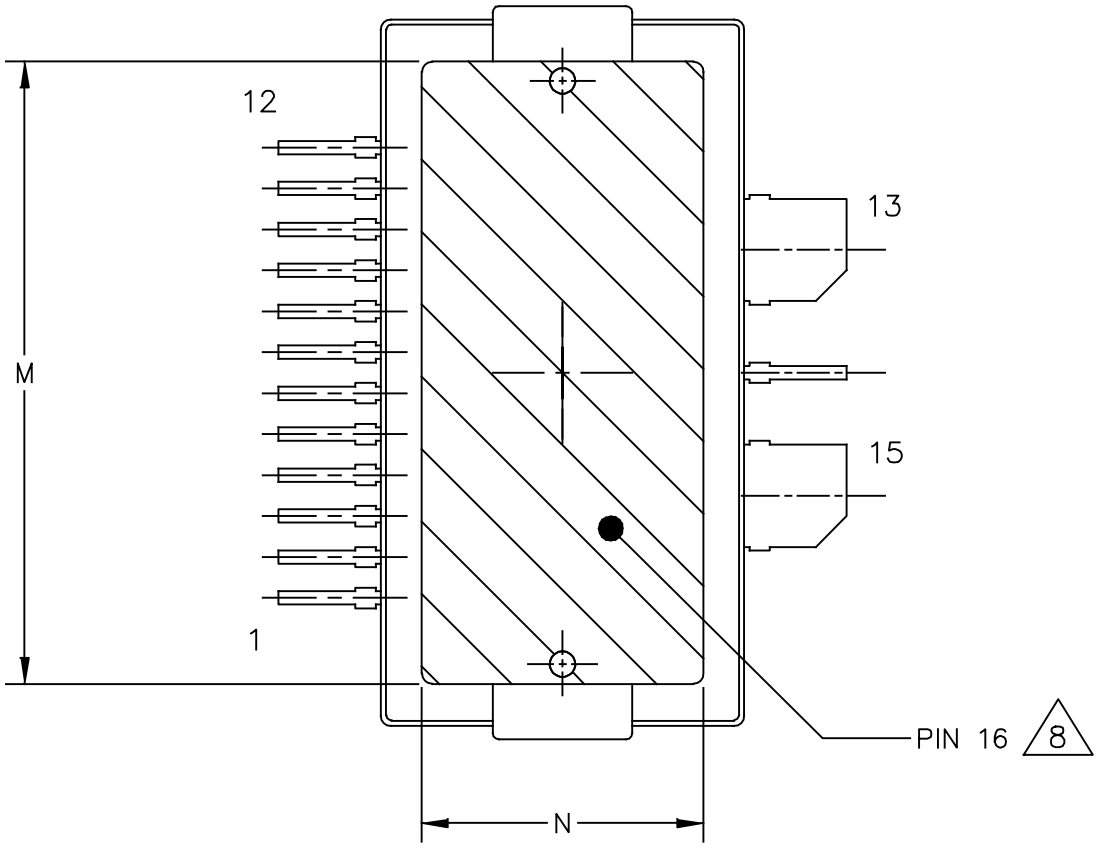

VIEW Y–Y

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.039	.043	0.99	1.09	N	.270	----	6.86	----
A2	.040	.042	1.02	1.07	bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.551	.559	14.00	14.20	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

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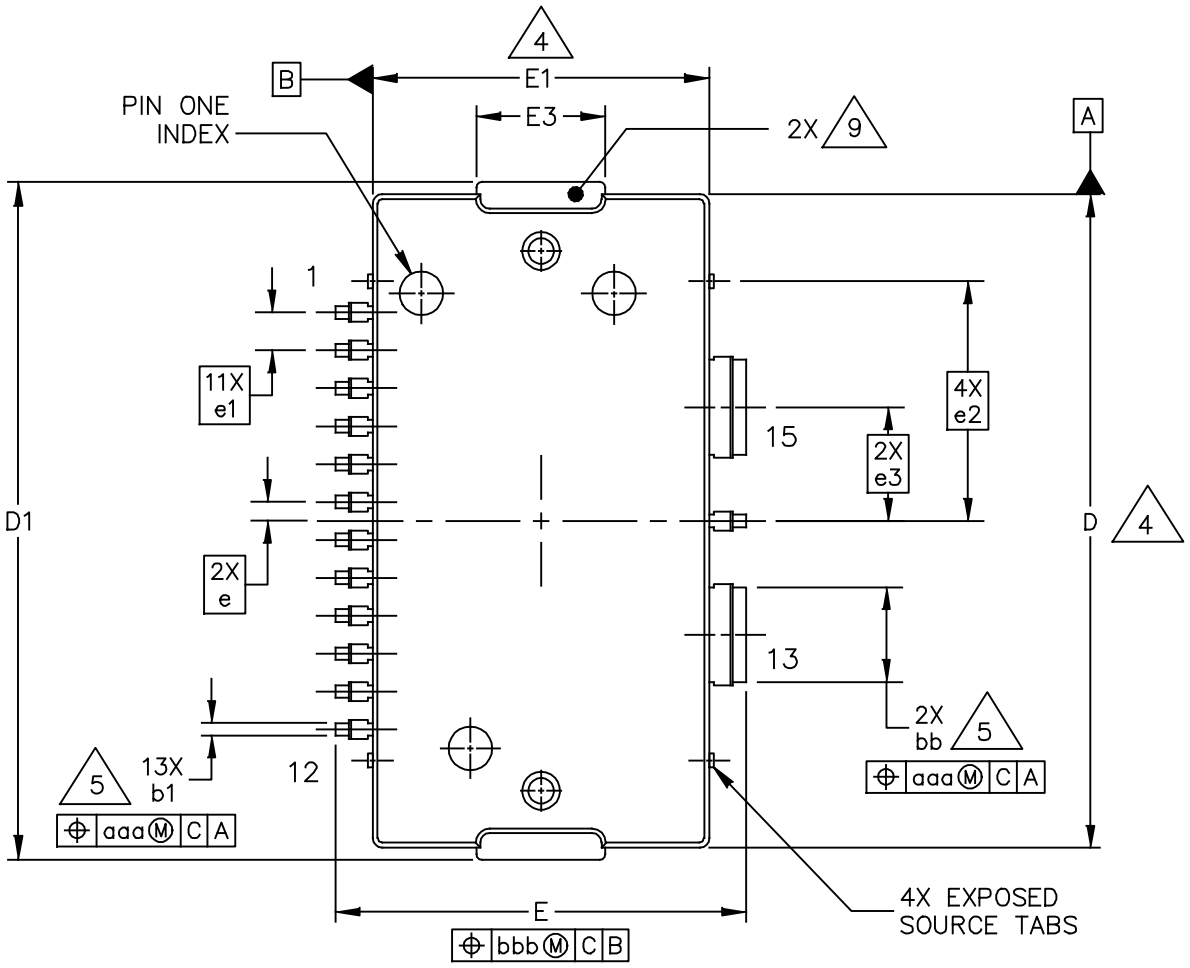

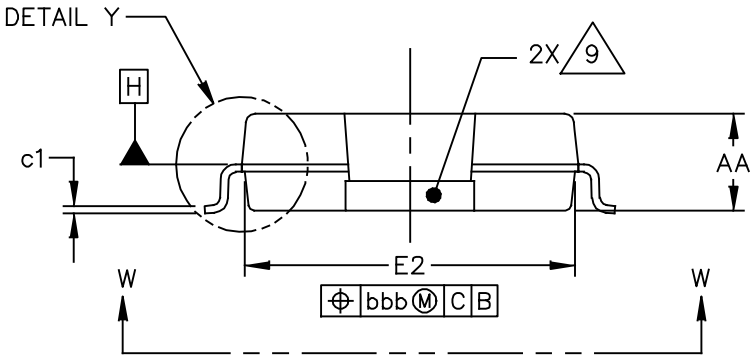

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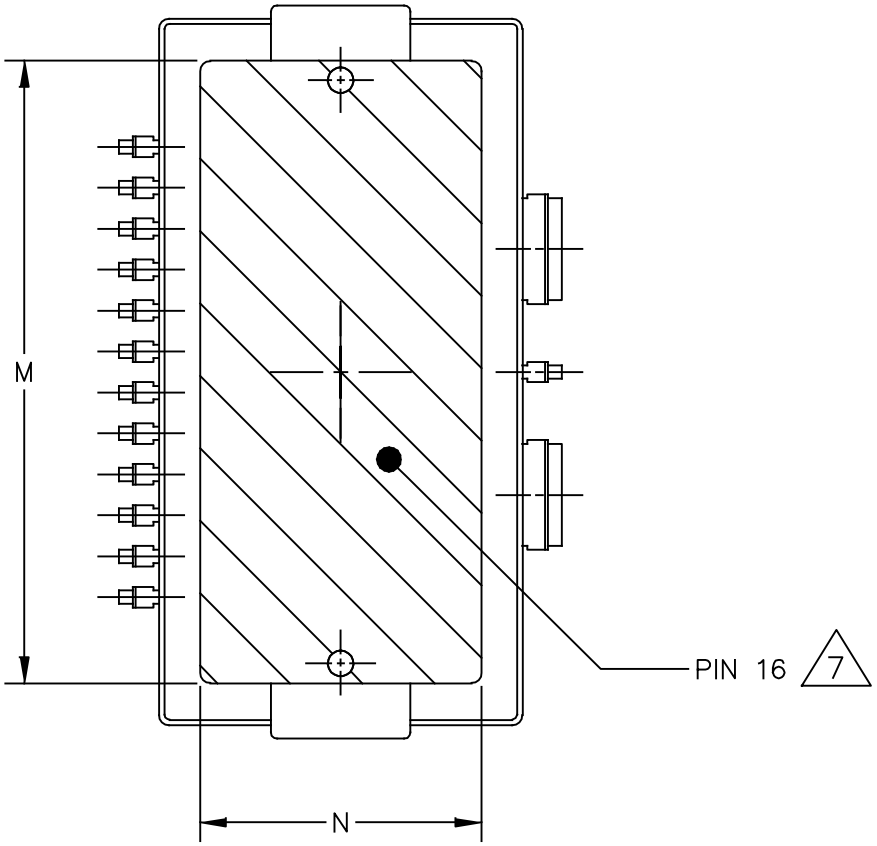
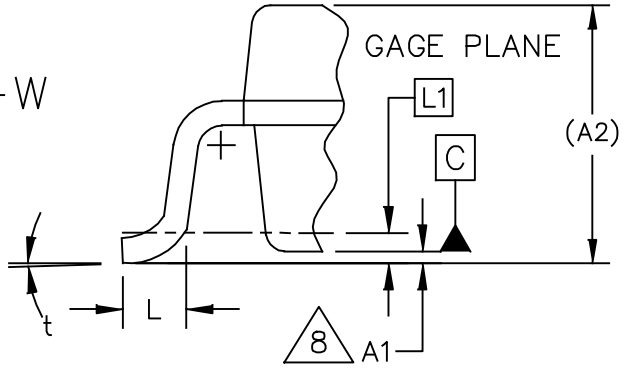


VIEW W–W



DETAIL "Y"

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6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.001	.004	0.03	0.10	N	.270	----	6.86	----
A2	(.105)		(2.67)		bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.429	.437	10.90	11.10	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins
- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software
- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools
- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2014	• Initial release of data sheet
1	Mar. 2015	• Figs. 4, 6–7 and 18–19: changed drain efficiency to power added efficiency for plots and axes labels, pp. 5–6, 11 • Tables 7–8 and 10–11: changed drain efficiency to power added efficiency, pp. 7, 12

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