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Military ProASIC3/EL Low Power Flash FPGAs
with Flash*Freeze Technology

Features and Benefits

Military Temperature Tested and Qualified
- Each Device Tested from –55°C to 125°C

Firm-Error Immune
- Not Susceptible to Neutron-Induced Configuration Loss

Low Power
- Dramatic Reduction in Dynamic and Static Power
- 1.2 V to 1.5 V Core and I/O Voltage Support for Low Power†
- Low Power Consumption in Flash*Freeze Mode Allows for Instantaneous Entry To / Exit From Low-Power Flash*Freeze Mode†
- Supports Single-Voltage System Operation
- Low-Impedance Switches

High Capacity
- 250K to 3M System Gates
- Up to 504 Kbits of True Dual-Port SRAM
- Up to 620 User I/Os

Reprogrammable Flash Technology
- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

High Performance
- 350 MHz (1.5 V systems) and 250 MHz (1.2 V systems) System Performance
- 3.3 V, 66 MHz, 64-Bit PCI (1.5 V systems) and 66 MHz, 32-Bit PCI (1.2 V systems)

In-System Programming (ISP) and Security
- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532–compliant)
- FlashLock® to Secure FPGA Contents

High-Performance Routing Hierarchy
- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Advanced and Pro (Professional) I/Os††
- 700 Mbps DDR, LVDS-Capable I/Os
- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation†
- Bank-Selectable I/O Voltages—up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input†
- Differential I/O Standards: LVPECL, LVDS, BLVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II (A3PE3000L only)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay (A3PE3000L only)
- Schmitt Trigger Option on Single-Ended Inputs (A3PE3000L)
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the Military ProASIC®3EL Family

Clock Conditioning Circuit (CCC) and PLL
- Six CCC Blocks—One Block with Integrated PLL in ProASIC3 and All Blocks with Integrated PLL in ProASIC3EL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range 1.5 MHz to 250 MHz (1.2 V systems) and 350 MHz (1.5 V systems)

SRAMs and FIFOs
- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)
- 24 SRAM and FIFO Configurations with Synchronous Operation:
  - 250 MHz: For 1.2 V Systems
  - 350 MHz: For 1.5 V Systems

ARM® Processor Support in ProASIC3/EL FPGAs
- ARM Cortex™-M1 Soft Processor Available with or without Debug

Table 1 • Military ProASIC3/EL Low-Power Devices

ProASIC3/EL Devices	A3P250	A3PE600L	A3P1000	A3PE3000L
ARM Cortex-M1 Devices[1]			**M1A3P1000**	**M1A3PE3000L**
System Gates	250,000	600,000	1M	3M
VersaTiles (D-flip-flops)	6,144	13,824	24,576	75,264
RAM kbits (1,024 bits)	36	108	144	504
4,608-Bit Blocks	8	24	32	112
FlashROM Kbits	1	1	1	1
Secure (AES) ISP[2]	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	1	6	1	6
VersaNet Globals	18	18	18	18
I/O Banks	4	8	4	8
Maximum User I/Os	68	270	154	620
Package Pins VQFP PQFP FBGA	VQ100	 FG484	 PQ208 FG144, FG256, FG484	 FG484, FG896

Notes:
1. *Refer to the Cortex-M1 product brief for more information.*
2. *AES is not available for ARM-enabled ProASIC3/EL devices.*

† A3P250 and A3P1000 support only 1.5 V core operation.
*ƒ Flash*Freeze technology is not available for A3P250 or A3P1000.*
††Pro I/Os are not available on A3P250 or A3P1000.

I/Os Per Package [1]

ProASIC3/EL Low Power Devices	A3P250		A3PE600L		A3P1000		A3PE3000L	
ARM Cortex-M1 Devices					M1A3P1000		M1A3PE3000L	
Package	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs
VQ100	68	13	–	–	–	–	–	–
PQ208	–	–	–	–	154	35	–	–
FG144	–	–	–	–	97	25	–	–
FG256	–	–	–	–	177	44	–	–
FG484	–	–	270	135	300	74	341	168
FG896	–	–	–	–	–	–	620	310

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the packaging section of the datasheet to ensure you are complying with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
3. *"G" indicates RoHS-compliant packages. Refer to "Military ProASIC3/EL Ordering Information" on page III for the location of the "G" in the part number.*
4. *For A3PE3000L devices, the usage of certain I/O standards is limited as follows:*
   – SSTL3(I) and (II): up to 40 I/Os per north or south bank
   – LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   – SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank
5. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

Military ProASIC3/EL Device Status

Military ProASIC3/EL Devices	Status	M1 Military ProASIC3/EL Devices	Status
A3P250	Production		
A3PE600L	Production		
A3P1000	Production	M1A3P1000	Production
A3PE3000L	Production	M1A3PE3000L	Production

Military ProASIC3/EL Ordering Information

A3P1000 – 1 FG G 144 Y M

Application (Temperature Range)
M = Military (–55°C to 125°C Junction Temperature)

Security Feature
Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS-Compliant (Green) Packaging

Package Type
VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
FG = Fine Pitch Ball Grid Array (1.0 mm pitch)
PQ = Plastic Quad Flat Pack (0.5 mm pitch)

Speed Grade
Blank = Standard
1 = 15% Faster than Standard
2 = 25% Faster than Standard
Note: Speed Grade –2 is available only for A3P1000 device in FG256 and FG484 packages

Part Number

Military ProASIC3/EL Devices
A3P250 = 250,000 System Gates
A3PE600L = 600,000 System Gates
A3P1000 = 1,000,000 System Gates
A3PE3000L = 3,000,000 System Gates

Military ProASIC3/EL Devices with ARM Cortex-M1
M1A3P1000 = 1,000,000 System Gates
M1A3PE3000L = 3,000,000 System Gates

Temperature Grade Offerings

Package	A3P250	A3PE600L	A3P1000	A3PE3000L
ARM Cortex-M1 Devices			**M1A3P1000**	**M1A3PE3000L**
VQ100	M	–	–	–
PQ208	–	–	M	–
FG144	–	–	M	–
FG256	–	–	M	–
FG484	–	M	M	M
FG896	–	–	–	M

Note: M = Military temperature range: –55°C to 125°C junction temperature

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1	–2[1]
M	✓	✓	✓

Notes:
1. *M1 devices are not available in -2 speed grade*
2. *M = Military temperature range: –55°C to 125°C junction temperature*

Contact your local Microsemi SoC Products Group (formerly Actel) representative for device availability: http://www.microsemi.com/contact/default.aspx.

Table of Contents

1 – Military ProASIC3/EL Device Family Overview

General Description

The military ProASIC3/EL family of flash FPGAs dramatically reduces dynamic power consumption by 40% and static power by 50%. These power savings are coupled with performance, density, true single chip, 1.2 V to 1.5 V core and I/O operation, reprogrammability, and advanced features.

Microsemi's proven Flash*Freeze technology enables military ProASIC3EL device users to shut off dynamic power instantaneously and switch the device to static mode without the need to switch off clocks or power supplies, and retaining internal states of the device. This greatly simplifies power management. In addition, optimized software tools using power-driven layout provide instant push-button power reduction.

Nonvolatile flash technology gives military ProASIC3/EL devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). Military ProASIC3/EL devices offer dramatic dynamic power savings, giving FPGA users flexibility to combine low power with high performance.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Military ProASIC3/EL devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry (CCC) based on an integrated phase-locked loop (PLL). Military ProASIC3/EL devices support devices from 250K system gates to 3 million system gates with up to 504 kbits of true dual-port SRAM and 620 user I/Os.

M1 military ProASIC3/EL devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. ARM Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low-power consumption and speed when implemented in an M1 military ProASIC3/EL device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. ARM Cortex-M1 is available at no cost from Microsemi for use in M1 military ProASIC3/EL FPGAs.

The ARM-enabled devices have ordering numbers that begin with M1 and do not support AES decryption.

Flash*Freeze Technology†

Military ProASIC3EL devices offer Flash*Freeze technology, which allows instantaneous switching from an active state to a static state. When Flash*Freeze mode is activated, military ProASIC3EL devices enter a static state while retaining the contents of registers and SRAM. Power is conserved without the need for additional external components to turn off I/Os or clocks. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of military ProASIC3EL devices to support a 1.2 V core voltage allows for an even greater reduction in power consumption, which enables low total system power.

When the military ProASIC3EL device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low-power modes, combined with a reprogrammable, single-chip, single-voltage solution, make military ProASIC3EL devices suitable for low-power data transfer and manipulation in military-temperature applications where available power may be limited (e.g., in battery-powered equipment); or where heat dissipation may be limited (e.g., in enclosures with no forced cooling).

† *Flash*Freeze technology is not supported on A3P1000.*

Flash Advantages

Low Power[f]

The military ProASIC3EL family of flash-based FPGAs provides a low-power advantage, and when coupled with high performance, enables designers to make power-smart choices using a single-chip, reprogrammable, and live-at-power-up device.

Military ProASIC3EL devices offer 40% dynamic power and 50% static power savings by reducing the core operating voltage to 1.2 V. In addition, the power-driven layout (PDL) feature in Libero®SoC offers up to 30% additional power reduction. With Flash*Freeze technology, military ProASIC3EL device is able to retain device SRAM and logic while dynamic power is reduced to a minimum, without the need to stop clock or power supplies. Combining these features provides a low-power, feature-rich, and high-performance solution.

Security

Nonvolatile, flash-based military ProASIC3/EL devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. Military ProASIC3/EL devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Military ProASIC3/EL devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in military ProASIC3/EL devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. Military ProASIC3/EL devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. Military ProASIC3/EL devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the military ProASIC3/EL family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The military ProASIC3/EL family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. A military ProASIC3/EL device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based military ProASIC3/EL FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

Flash-based military ProASIC3/EL devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based military ProASIC3/EL devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the military ProASIC3/EL device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based military ProASIC3/EL devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

ƒ A3P1000 only supports 1.5 V core operation.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based military ProASIC3/EL devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The military ProASIC3/EL family device architecture mitigates the need for ASIC migration at higher volumes. This makes the military ProASIC3/EL family a cost-effective ASIC replacement.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of military ProASIC3/EL flash-based FPGAs. Once it is programmed, the flash cell configuration element of military ProASIC3/EL FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The military ProASIC3/EL family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with 7 layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary military ProASIC3/EL architecture provides granularity comparable to standard-cell ASICs. The military ProASIC3/EL device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the military ProASIC3/EL core tile, as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable, allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

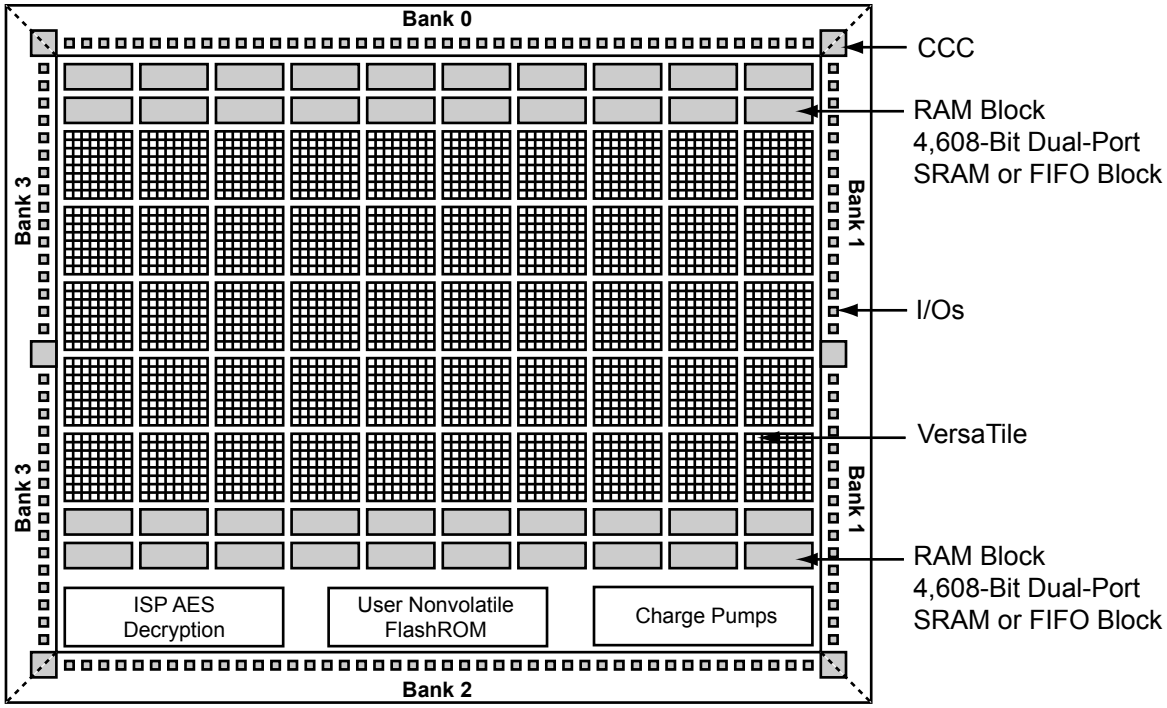

Figure 1-1 • **Military ProASIC3 Device Architecture Overview with Four I/O Banks (A3P250 and A3P1000)**

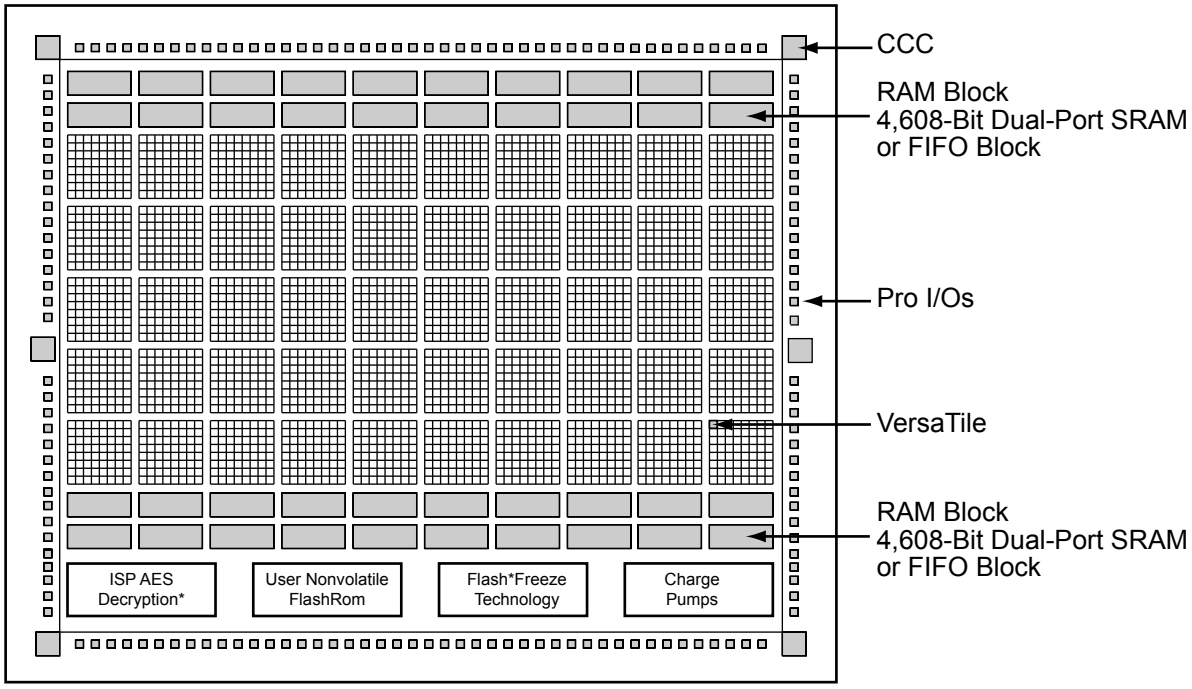

Figure 1-2 • **Military ProASIC3EL Device Architecture Overview (A3PE600L and A3PE3000L)**

Flash*Freeze Technology††

Military ProASIC3EL devices offer proven Flash*Freeze technology, which enables designers to instantaneously shut off dynamic power consumption while retaining all SRAM and register information. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze (FF) pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption; clocks can still be driven or can be toggling without impact on power consumption; all core registers and SRAM cells retain their states. I/Os are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLLs. Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The FF pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the FF pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low-power static and dynamic capabilities of the military ProASIC3EL device. Refer to Figure 1-3 for an illustration of entering/exiting Flash*Freeze mode.

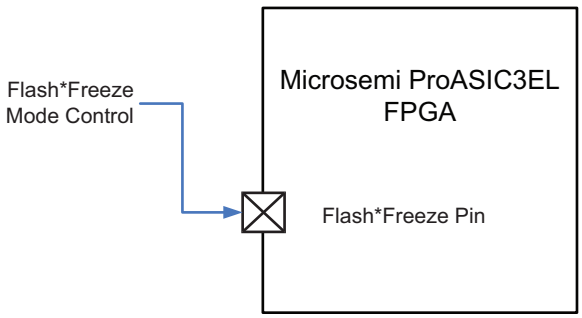

Figure 1-3 • **Military ProASIC3EL Flash*Freeze Mode**

VersaTiles

The military ProASIC3/EL core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The military ProASIC3/EL VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-4 for VersaTile configurations.

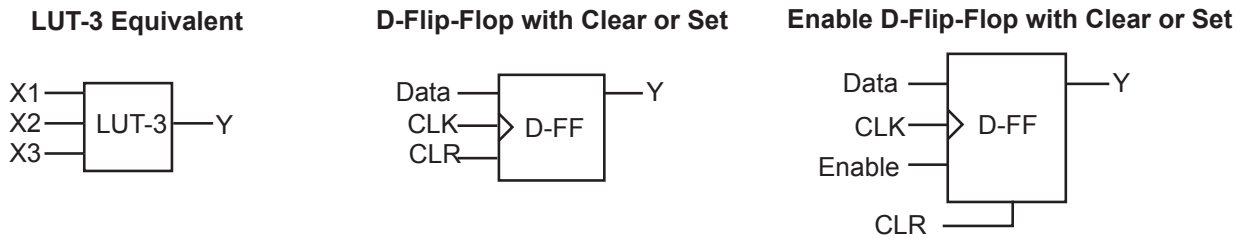

Figure 1-4 • **VersaTile Configurations**

*††Flash*Freeze technology is not supported for A3P1000.*

User Nonvolatile FlashROM

Military ProASIC3/EL devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

FlashROM is written using the standard military ProASIC3/EL IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

Microsemi military ProASIC3/EL development software solutions, Libero SoC has extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Military ProASIC3/EL devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

Military ProASIC3 devices provide designers with flexible clock conditioning circuit (CCC) capabilities. Each member of the military ProASIC3 family contains six CCCs, located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

Military ProASIC3EL devices also contain six CCCs; however, all six are equipped with a PLL.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time is 300 µs
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC}

Global Clocking

Military ProASIC3/EL devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The military ProASIC3/EL family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). In addition, 1.2 V I/O operation is supported for military ProASIC3EL devices. Military ProASIC3/EL FPGAs support different I/O standards, including single-ended, differential, and voltage-referenced (military ProASIC3EL). The I/Os are organized into banks, with two, four, or eight (military ProASIC3EL only) banks per device. The configuration of these banks determines the I/O standards supported. For military ProASIC3EL, each I/O bank is subdivided into V_{REF} minibanks, which are used by voltage-referenced I/Os. V_{REF} minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common V_{REF} line. Therefore, if any I/O in a given V_{REF} minibank is configured as a V_{REF} pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-data-rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

Military ProASIC3EL banks support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

2 – Military ProASIC3/EL DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings[1]**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage for A3PE600/3000L DC output buffer supply voltage for A3P250/A3P1000	–0.3 to 3.75	V
VMV	DC input buffer supply voltage for A3P250/A3P1000	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+150	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-4 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

Table 2-2 • Recommended Operating Conditions [1]

Symbol	Parameter		Military	Units
T_J	Junction temperature		–55 to 125 [2]	°C
VCC	1.5 V DC core supply voltage[3]		1.425 to 1.575	V
	1.2 V – 1.5 V wide range DC core supply voltage [4]		1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	V
VPUMP[5]	Programming voltage	Programming mode	3.15 to 3.45	V
		Operation[6]	0 to 3.6	V
VCCPLL[5]	Analog power supply (PLL)	1.5 V DC core supply voltage[3]	1.425 to 1.575	V
		1.2 V – 1.5 V DC core supply voltage[4]	1.14 to 1.575	V
VCCI and VMV[5]	1.2 V DC supply voltage[4]		1.14 to 1.26	V
	1.2 V wide range DC supply voltage[4]		1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	V
	3.0 V DC supply voltage[7]		2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Default Junction Temperature Range in the Libero SoC software is set from 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*
3. *For A3P250 and A3P1000*
4. *For A3PE600L and A3PE3000L devices only, operating at VCCI ≥ VCC.*
5. *See the "Pin Descriptions and Packaging" section on page 3-1 for instructions and recommendations on tie-off and supply grouping.*
6. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-25 on page 2-22. VCCI should be at the same voltage within a given I/O bank.*
7. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*
8. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.*

Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • Overshoot and Undershoot Limits[1]

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot (125°C)[2]
2.7 V or less	10%	0.72 V
	5%	0.82 V
3 V	10%	0.72 V
	5%	0.82 V
3.3 V	10%	0.69 V
	5%	0.79 V
3.6 V	10%	N/A
	5%	N/A

Notes:

1. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
2. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Military)

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

Military ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI **Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC **Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.

- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic, at least until VCC and VCCPLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low-Power Flash Devices" chapter of the *Military ProASIC3/EL FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

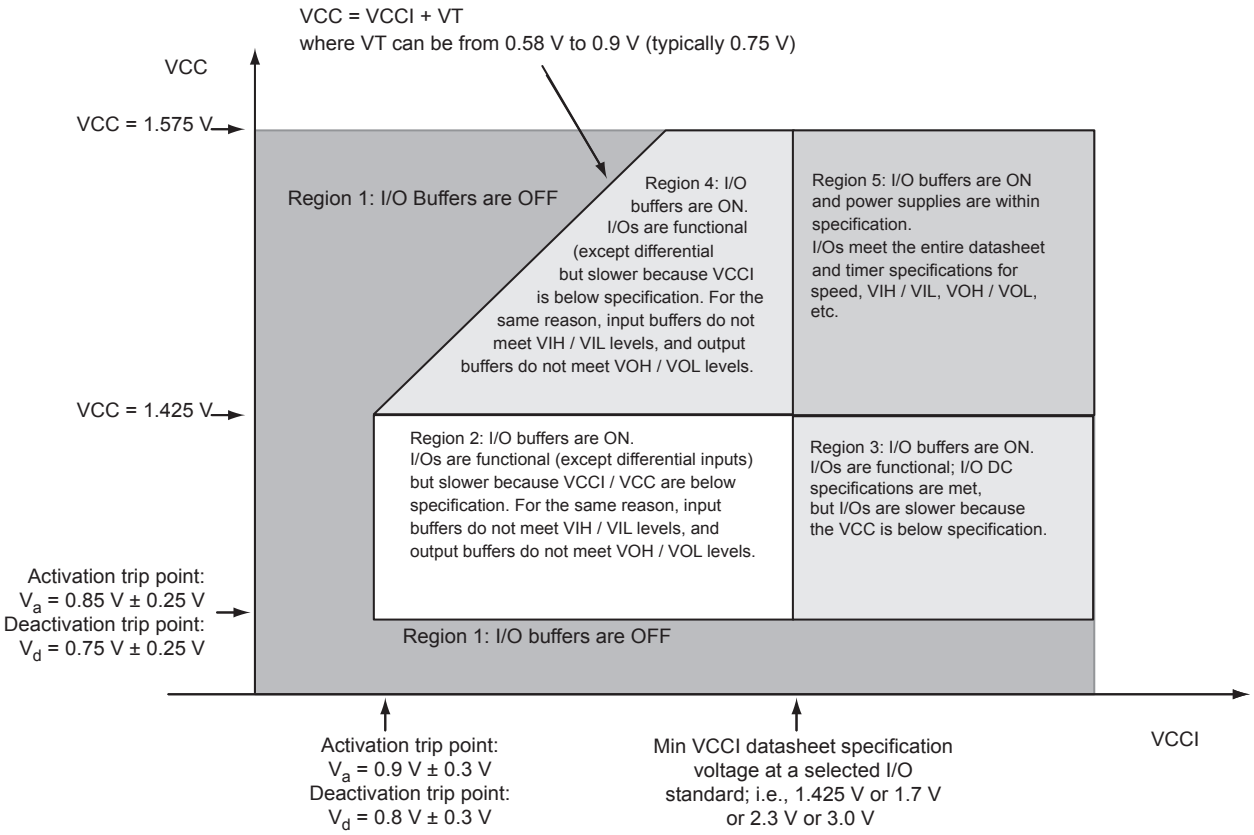

Figure 2-1 • **Devices Operating at 1.5 V Core – I/O State as a Function of VCCI and VCC Voltage Levels**

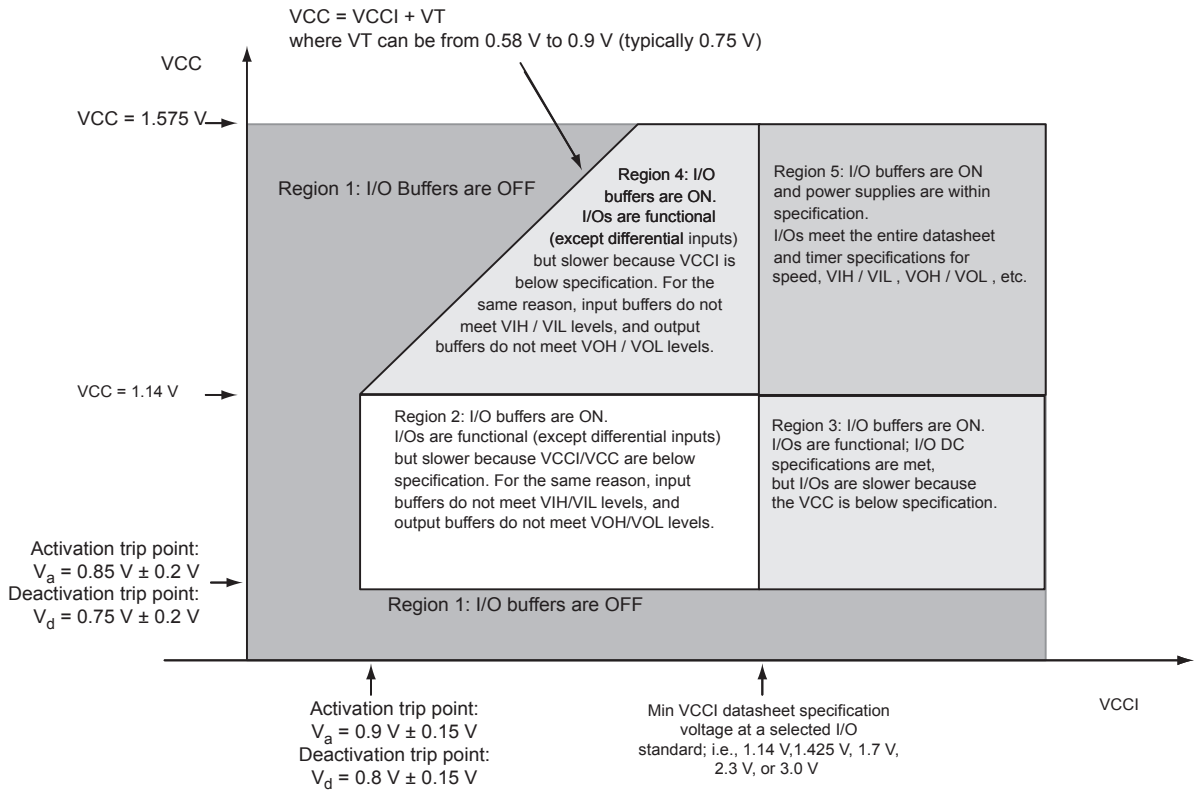

Figure 2-2 • **Device Operating at 1.2 V Core Voltage – I/O State as a Function of VCCI and VCC Voltage Levels; Only A3PE600L and A3PE3000L Devices Operate at 1.2 V Core Voltage**

Thermal Characteristics

Introduction

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A \qquad \textit{EQ 1}$$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The recommended maximum junction temperature is 125°C. EQ 2 shows a sample calculation of the recommended maximum power dissipation allowed for a 484-pin FBGA package at military temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°C) - \text{Max. ambient temp. } (°C)}{\theta_{ja}(°C/W)} = \frac{125°C - 70°C}{20.6°C/W} = 2.670$$

EQ 2

Table 2-5 • Package Thermal Resistivities

Package Type	Device	Pin Count	θ_{jc}	θ_{ja}			Units
				Still Air	200 ft./min.	500 ft./min.	
Very Thin Quad Flat Pack (VQ100)	A3P250	100	10.0	35.3	29.4	27.1	C/W
Plastic Quad Flat Pack (PQ208)*	A3P1000	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	A3P1000	144	6.3	31.6	26.2	24.2	C/W
	A3P1000	256	6.6	28.1	24.4	22.7	C/W
	A3P1000	484	8.0	23.3	19.0	16.7	C/W
	A3PE600L	484	9.5	27.5	21.9	20.2	C/W
	A3PE3000L	484	4.7	20.6	15.7	14.0	C/W
	A3PE3000L	896	2.4	13.6	10.4	9.4	C/W

* *Embedded heatspreader*

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 125°C, VCC = 1.14 V) Applicable to A3PE600L and A3PE3000L Only

	Junction Temperature						
Array Voltage VCC (V)	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
1.14	0.85	0.86	0.89	0.92	0.96	0.97	1.00
1.2	0.82	0.83	0.86	0.88	0.92	0.93	0.96
1.26	0.79	0.80	0.83	0.85	0.89	0.90	0.93
1.30	0.77	0.78	0.81	0.83	0.86	0.88	0.90
1.35	0.74	0.75	0.78	0.80	0.84	0.85	0.88
1.40	0.72	0.73	0.75	0.77	0.81	0.82	0.85
1.425	0.71	0.71	0.74	0.76	0.79	0.80	0.83
1.5	0.67	0.68	0.70	0.72	0.75	0.76	0.79
1.575	0.65	0.66	0.68	0.70	0.73	0.74	0.76

Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 125°C, VCC = 1.425 V) Applicable to A3P250 and A3P1000 Devices Only

	Junction Temperature						
Array Voltage VCC (V)	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
1.425	0.80	0.82	0.87	0.89	0.94	0.96	1.00
1.5	0.76	0.78	0.82	0.84	0.89	0.91	0.95
1.575	0.73	0.75	0.79	0.82	0.86	0.87	0.91

Calculating Power Dissipation

Quiescent Supply Current

Table 2-8 • **Power Supply State Per Mode**

	Power Supply Configurations				
Modes/Power Supplies	**VCC**	**VCCPLL**	**VCCI**	**VJTAG**	**VPUMP**
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
Static and Active	On	On	On	On	On/off/floating

Table 2-9 • **Quiescent Supply Current (IDD) Characteristics, Flash*Freeze Mode***

	Core Voltage	A3PE600L	A3PE3000L	Units
Nominal (25°C)	1.2 V	0.55	2.75	mA
	1.5 V	0.83	4.2	mA
Typical maximum (25ºC)	1.2 V	9	17	mA
	1.5 V	12	20	mA
Military maximum (125ºC)	1.2 V	65	165	mA
	1.5 V	85	185	mA

*Note: *IDD includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents. Values do not include I/O static contribution (PDC6 and PDC7).*

Table 2-10 • **Quiescent Supply Current (IDD) Characteristics, Sleep Mode (VCC = 0 V)***

	Core Voltage	A3PE600L	A3PE3000L	Units
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	µA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	µA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	µA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	µA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	µA

*Note: *IDD = N_{BANKS} × ICCI. Values do not include I/O static contribution, which is shown in Table 2-22 on page 2-14 (PDC6 and PDC7).*

Table 2-11 • **Quiescent Supply Current (IDD) Characteristics, Shutdown Mode***

	Core Voltage	A3P250	A3P1000	A3PE600L	A3PE3000L	Units
Nominal (25°C)	1.2 V / 1.5 V	N/A		0		µA
Military (125ºC)	1.2 V / 1.5 V	N/A		0		µA

*Note: *This is applicable to A3PE600L and A3PE3000L only for cold-sparable I/O devices. Not available on A3P250 or A3P1000.*

Table 2-12 • Quiescent Supply Current (IDD), Static Mode and Active Mode [1]

	Core Voltage	A3PE600L	A3PE3000L	Units
ICCA Current[2]				
Nominal (25°C)	1.2 V	0.55	2.75	mA
	1.5 V	0.83	4.2	mA
Typical maximum (25°C)	1.2 V	9	17	mA
	1.5 V	12	20	mA
Military maximum (125°C)	1.2 V	65	165	mA
	1.5 V	85	185	mA
ICCI or IJTAG Current[3]				
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	µA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	µA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	µA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	µA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	µA

Notes:

1. *IDD = N_{BANKS} × ICCI + ICCA. JTAG counts as one bank when powered.*
2. *Includes VCC, VCCPLL, and VPUMP currents.*
3. *Values do not include I/O static contribution (PDC6 and PDC7).*

Table 2-13 • Quiescent Supply Current (IDD) Characteristics for A3P250 and A3P1000

	Core Voltage	A3P250	A3P1000	Units
Nominal (25°C)	1.5 V	3	8	mA
Typical maximum (25°C)	1.5 V	15	30	mA
Military maximum (125°C)	1.5 V	65	150	mA

Note: IDD includes VCC, VPUMP, VCCI, and VMV currents. Values do not include I/O static contribution (PDC6 and PDC7), which is shown in Table 2-22 on page 2-14.

Power per I/O Pin

Table 2-14 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
3.3 V LVCMOS Wide Range	3.3	–	16.34
3.3 V LVCMOS – Schmitt trigger Wide Range	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS – Schmitt trigger	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS	1.2	–	0.60
1.2 V LVCMOS (JESD8-11) – Schmitt trigger	1.2	–	0.53
1.2 V LVCMOS Wide Range	1.2	–	0.60
1.2 V LVCMOS Schmitt trigger Wide Range	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.14
2.5 V GTL	2.5	2.13	3.54
3.3 V GTL+	3.3	2.81	2.91
2.5 V GTL+	2.5	2.57	2.61
HSTL (I)	1.5	0.17	0.79
HSTL (II)	1.5	0.17	0.79
SSTL2 (I)	2.5	1.38	3.26
SSTL2 (II)	2.5	1.38	3.26
SSTL3 (I)	3.3	3.21	7.97
SSTL3 (II)	3.3	3.21	7.97
Differential			
LVDS	2.5	2.26	0.89
LVPECL	3.3	5.71	1.94

Notes:

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*

Table 2-15 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

	VMV (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.22
3.3 V LVCMOS – Wide Range	3.3	–	16.22
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.65
1.5 V LVCMOS (JESD8-11)	1.5	–	0.98
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64
Differential			
LVDS	2.5	2.26	0.83
LVPECL	3.3	5.72	1.81

Notes:

1. *PDC6 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VMV.*

Table 2-16 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

	VMV (V)	Static Power PDC6 (mW) [1]	Dynamic Power PAC9 (µW/MHz) [2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.23
3.3 V LVCMOS – Wide Range	3.3	–	16.23
2.5 V LVCMOS	2.5	–	4.66
1.8 V LVCMOS	1.8	–	1.64
1.5 V LVCMOS (JESD8-11)	1.5	–	0.99
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64

Notes:

1. *PDC6 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VMV.*

Table 2-17 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL/LVCMOS	5	3.3	–	148.00
3.3 V LVCMOS Wide Range	5	3.3	–	148.00
2.5 V LVCMOS	5	2.5	–	83.23
1.8 V LVCMOS	5	1.8	–	54.58
1.5 V LVCMOS (JESD8-11)	5	1.5	–	37.05
1.2 V LVCMOS	5	1.2	–	17.94
1.2 V LVCMOS Wide Range	5	1.2	–	17.94
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.18
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.48
SSTL3 (I)	30	3.3	26.02	114.67
SSTL3 (II)	30	3.3	42.21	131.69
Differential				
LVDS	–	2.5	7.70	89.58
LVPECL	–	3.3	19.42	167.86

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC7 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCCI.*

Table 2-18 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW) [2]	Dynamic Power PAC10 (µW/MHz) [3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	141.97
3.3 V LVCMOS Wide Range	5	3.3	–	141.97
2.5 V LVCMOS	5	2.5	–	79.98
1.8 V LVCMOS	5	1.8	–	52.26
1.5 V LVCMOS (JESD8-11)	5	1.5	–	35.62
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	89.82
LVPECL	–	3.3	19.54	167.55

Notes:

1. *Dynamic Power consumption is given for software default drive strength and output slew. Output load is lower than the software default.*
2. *PDC7 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCCI.*

Table 2-19 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW) [2]	Dynamic Power PAC10 (µW/MHz) [3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	125.97
3.3 V LVCMOS – Wide Range	5	3.3	–	125.97
2.5 V LVCMOS	5	2.5	–	70.82
1.8 V LVCMOS	5	1.8	–	36.39
1.5 V LVCMOS (JESD8-11)	5	1.5	–	25.34
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. *Dynamic Power consumption is given for software default drive strength and output slew. Output load is lower than the software default.*
2. *PDC7 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCCI.*

Power Consumption of Various Internal Resources

Table 2-20 • **Different Components Contributing to Dynamic Power Consumption in Military ProASIC3/EL Devices Operating at 1.2 V VCC**

Parameter	Definition	Device-Specific Dynamic Power (µW/MHz)	
		A3PE3000L	A3PE600L
PAC1	Clock contribution of a Global Rib	8.34	3.99
PAC2	Clock contribution of a Global Spine	4.28	2.22
PAC3	Clock contribution of a VersaTile row	0.94	0.94
PAC4	Clock contribution of a VersaTile used as a sequential module	0.08	0.08
PAC5	First contribution of a VersaTile used as a sequential module	0.05	
PAC6	Second contribution of a VersaTile used as a sequential module	0.19	
PAC7	Contribution of a VersaTile used as a combinatorial module	0.11	
PAC8	Average contribution of a routing net	0.45	
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-14 on page 2-9 through Table 2-16 on page 2-10.	
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-17 on page 2-11 through Table 2-19 on page 2-12.	
PAC11	Average contribution of a RAM block during a read operation	25.00	
PAC12	Average contribution of a RAM block during a write operation	30.00	
PAC13	Dynamic contribution for PLL	1.74	