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**UG0048**  
**User Guide**  
**ProASIC3/E Starter Kit**





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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 5.1

Component description, connection section of OLED, OLED manufacturing test, and board image are updated.

## 1.2 Revision 5.0

The following was a summary of the changes in revision 5.0 of this document.

- The part number for the ProASIC3/E Starter Kit was changed from A3PE-STARTER-KIT to A3PE-STARTER-KIT-2 (SAR 42164).
- In the "FPGA – OLED Interface" section, PMO13701 was corrected to PMO18701 (SAR 42164).

## 1.3 Revision 4.0

Libero IDE software has been updated to Libero SoC throughout the document (SAR 36951).

## 1.4 Revision 3.0

The silicon for this kit has been updated, so the document has been updated accordingly (SAR 27883).



## 2 Contents and System Requirements

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This section details the contents of the ProASIC3/E Starter Kit and lists the power supply and software system requirements.

### 2.1 Kit Contents

The following table lists the contents of the ProASIC3/E Starter Kit.

**Table 1 • Kit Contents**

| <b>Item</b>  | <b>Quantity</b> |
|--|-----------------|
| ProASIC3/E Starter Kit Board with an A3PE1500-PQG208 | 1               |
| FlashPro4 programmer                                 | 1               |
| 9 V power supply with international adapters         | 1               |
| Quickstart card                                      | 1               |

## 3 Hardware Components

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This section describes the hardware components of the ProASIC3/E Starter Kit board.

### 3.1 ProASIC3/E Starter Kit Board

Figure 1, page 4 illustrates a top-level view of the ProASIC3/E Starter Kit board.

The ProASIC3/E Starter Kit board consists of the following:

- Wall mount power supply connector, with a switch and a LED indicator
- Switches to select from among 1.5 V, 1.8 V, 2.5 V, and 3.3 V — I/O voltages on banks 4 and 5 (southern side)
- 10-pin 0.1 inch pitch programming connector compatible with Altera connections
- 40 MHz oscillator and two independent manual clock options for global reset and pulse
- Eight LEDs (driven by outputs from the device)
- Jumpers (allow disconnection of all external circuitry from the FPGA)
- Two mono stable pulse generator switches (global and reset)
- Four switches (provide input to the device)
- Two hex switches to provide four inputs each to the FPGA, and which are set to a user-switchable hexadecimal input value

For more information, see [Appendix: PQ208 Package Connections](#), page 22 and [Appendix: Board Schematics](#), page 26.

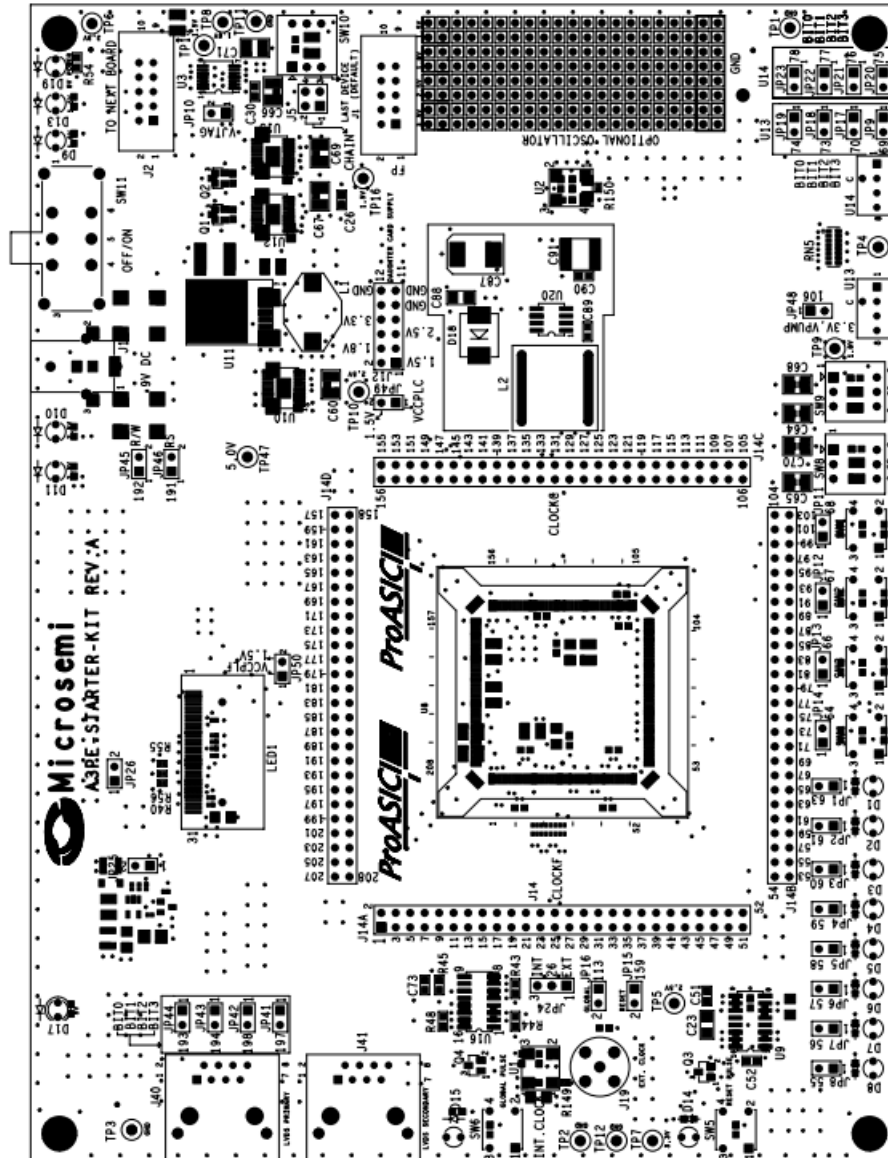
## 3.2 Board Description and Usage

The ProASIC3/E Starter Kit board is socketed and is populated with A3PE1500-PQ208 silicon. Any ProASIC3 device can be used, as all devices in both the ProASIC3 and ProASIC3E families are available in the PQ208 package.

**Note:** Device Pin-out is different among ProASIC3 and ProASIC3E device families. For more information about pinouts, see <https://www.microsemi.com/products/fpga-soc/fpga/proasic3-e#documents>.

A block diagram of the ProASIC3/E Starter kit board is shown in the following figure and will facilitate understanding of the more detailed schematics shown in the [Appendix: Board Schematics](#), page 26.

**Figure 1 • ProASIC3/E Starter Kit Board: Top-Level View**



Full schematics are available for download from the Microsemi SoC Products Group website. The electronic versions of the dedicated schematics can be enlarged to a far greater degree than shown in the printed version of this manual or even in the electronic version of this manual, hence the interested reader is referred to the dedicated schematics to see the appropriate level of detail.

## 3.3 PLL Parts and Usage on ProASIC3/E

This section describes the PLL parts and usage on ProASIC3/E.

### 3.3.1 Instructions for PLL Activation on Board

In order to use the PLLs on the ProASIC3/E Starter Kit board, power must be applied to their respective analog supply rails. For the west side PLL, known as PLF, the VCCPLF line must be connected to VCC, which is held at 1.5 V. The same is true for VCCPLC of the PLL on the east side, known as PLC. In addition, the VCOMPLF and VCOMPLC lines must be connected to ground. The jumpers JP49 and JP50 are provided on the starter kit to connect VCCPLF and VCCPLC pins to 1.5 V supply.

The ground pins of the PLL supplies are connected to ground on the board. These supply voltages are not connected by default on the board for three reasons:

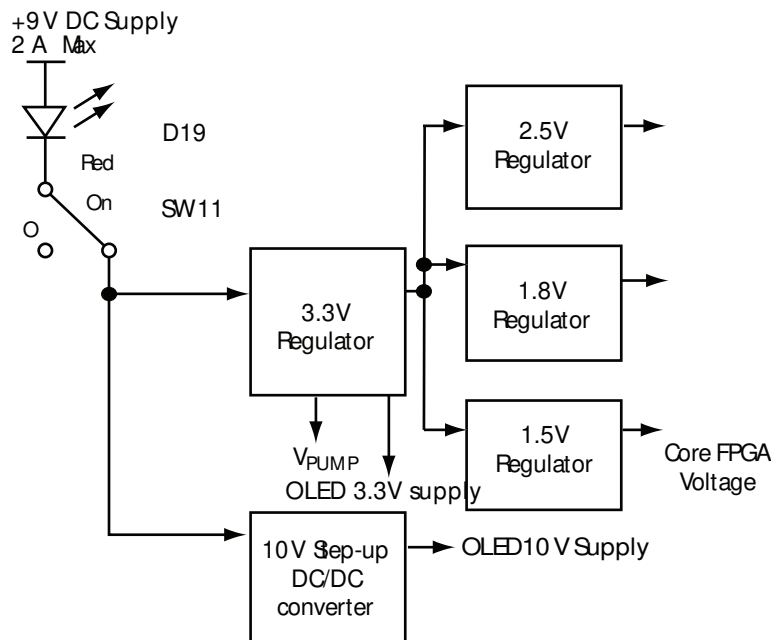
1. The PLC analog voltage rails are not available on ProASIC3 devices; only on ProASIC3E in the PQ208 package. Only the west side PLL, namely PLF, is available on ProASIC3 devices in PQ208. In ProASIC3 devices, the pins are used as general I/Os. The same board is used for ProASIC3E and ProASIC3 devices.
2. To demonstrate the lowest possible power consumption for the part. Perpetually powering the PLL lines would not achieve that.
3. It is easy to place a jumper on the appropriate jumper header when desired.

## 3.4 Power Supply

A 9 V power supply is provided with the kit, as shown in the following figure. There are many power supply components in the starter kit board to illustrate the many ways that differing voltage banks may be supported with ProASIC3 and ProASIC3E technology. These voltage banks are not required for general usage of ProASIC3 silicon. They are provided purely for illustrative purposes.

**Note:** The latest revision of ProASIC3/E Starter Kit (A3PE-STARTER-KIT-2) does not have an OLED populated on the board.

**Figure 2 • Power Supply Block Diagram**



To use the ProASIC3/E Starter Kit board with a wall mount power supply, use the switching brick power supply that is provided with the kit.

The external +9 V positive center power supply provided to the board through connector J18 goes to a voltage regulator chip U11 on the Starter Kit board. As soon as the external voltage is connected to the

board, the red LED D19 illuminates to indicate that an external supply is connected to the board. As soon as switch SW11 is moved to the ON position (to the right, as labeled on the board OFF/ON), the disabling ground signal is removed from pin 7 of U11 and the regulator begins to provide power at its output.

The U11 switching voltage regulator provides a dedicated 3.3 V supply at its output. The board's 3.3 V supply is used for feeding separate regulators that deliver 1.5 V (through U15), 1.8 V (through U12), and 2.5 V (through U15). The 1.5 V is required for the core voltage of the ProASIC3/E family, and the 2.5 V is required for demonstrating LVDS extended I/O bank capability.

The presence of these voltages is indicated by four green LEDs (D13, D9, D10, and D11) illuminating at the top right of the board. Each LED is labeled with the voltage it represents and its component identifier. All four voltages are selectable on the I/O banks 4 and 5 (the two southernmost banks) of a ProASIC3E device using SW9 and SW8 switches respectively.

**Note:** Only ProASIC3E devices have eight I/O banks. ProASIC3 devices have four I/O banks—one per side of the PQ208 package. If a ProASIC3 device is placed in the socket, then both SW8 and SW9 should be set at same voltage level to power I/O bank 2.

The 3.3 V supply is also used for optionally providing the VPUMP programming voltage. This VPUMP voltage may be provided to the chip during programming by applying a FlashPro4 programmer to the J1 interface and selecting VPUMP from the FlashPro v9.1 (or later) programming software. VPUMP voltage may also be provided directly to the chip from the board.

Leave the JP48 jumper in place to apply 3.3 V supply to the VPUMP pin (106 of the PQ208 packaged FPGA).

**Note:** If both FlashPro4 or latest and the board are selected to provide VPUMP, then it is the connection on the board that will override, as FlashPro4 will detect that a voltage is available, issue an information message in the programming software, and then move the VPUMP output pin to a tristate value, allowing the board to provide all the power.

The board must be powered-up during programming because the chip needs its core voltages to be provided and VJTAG must be detected by the FlashPro4 programmer in order for it to set its JTAG signal voltages to the right level.

The OLED device requires low current 10 V supply and 3.3 V supply to operate correctly. These voltages are provided by LT1615 and LM2678S modules, as shown in [Figure 16](#), page 35.

The external +9 V power supply is rated at 2 A maximum. On the first of the full-page dedicated schematics shown in the [Appendix: Board Schematics](#), page 26, note that the 3.3 V supply is rated at 5 A maximum. The derived power supplies of 1.5 V, 1.8 V, and 2.5 V are rated at 2 A max each, and the OLED 10 V power supply is rated at 100 mA, as shown in [Figure 16](#), page 35. Clearly, not all these derived supplies can be working at their respective maximum current outputs simultaneously. The maximum ratings are for the individual regulator ICs and cannot be numerically added together.

The U11 (LM2678S-3.3) component is rated for an input voltage range of +8 V to +40 V, so a wide range of power supplies may be used with the board with no concern about over-voltage conditions occurring from inadvertent accidental usage of the wrong power supply. However, the user must ensure that the voltage provided is positive at the center pin of the J18 connector and grounded on the outside. Greater heating of the regulator chips can be observed with higher voltages. It is recommended that only the included power supply or an equivalent substitute be used with the Starter Kit. The included power supply has been rated for this board, including Microsemi SoC Products Group Daughter Cards that may be attached to the board.

### 3.4.1 Power Supply Connections of Daughter Card

Limited power is supplied to a daughter card by the board. The connector for the daughter card is shown in [Figure 13](#), page 32 and is the J12 header. All the FPGA voltages 1.5 V, 1.8 V, 2.5 V, and 3.3 V are provided to the daughter card through a 12-pin 0.1 inch pitch connector. The voltages are arranged with a no-connection pin interspersing the voltage pins. This prevents accidental use of a jumper to short a supply rail to ground, which could connect differing supply rails together.

The purpose is not to protect the power supply regulators, as these will go high-impedance when an over-voltage condition is detected. It is to protect the FPGA from unintentional application of a higher

voltage to the 1.5 V core. Three of the twelve pins are ground pins, which will provide more than sufficient current return capability for future Microsemi SoC Products Group daughter cards that will work with this board.

## 3.4.2 Power Supplies and Chaining Boards Together

When joining multiple ProASIC3/E Starter Kit boards together through the chain programming connection, J2 connector is used to connect the J1 connector of the next board in the chain by attaching a standard 0.100-inch pitch 10-pin programming cable. The length of the cable must be kept as short as possible, because multiple boards connected form a JTAG chain of ProASIC3/E devices can provide much greater noise pick-up and may degrade the TCK clock for devices remote from the FlashPro4 programmer. A rotary switch SW10 is provided on the board to set the VJTAG supply. Select the VJTAG supply between 1.5 V, 1.8 V, 2.5 V, and 3.3 V using SW10. Set VJTAG at an absolute minimum of 1.8 V to help with signal integrity when chaining boards together. Higher voltages can give better noise and impedance mismatch immunity.

Disconnect the jumper at JP10 on all boards. This jumper can be used to provide VJTAG to a downstream board or to some element in the design that you wish to supply with the VJTAG voltage used by the ProASIC3/E component. The shunt that is normally in this location can be safely stored across pins 11 and 12, or 9 and 10 of the J12 daughter card power supply connector. For particularly long chains, the value of TCK used during programming must be reduced.

During the development, various revisions of the ProASIC3/E Starter Kit board are produced. This documentation contains additional text that documents some of these earlier versions, as well as the newest version of the board. The latest version of the board A3PE-STARTER-KIT-2 REV B does not have OLED display. A3PE-STARTER-KIT-2 REV A version is same as A3PE-PROTO-KIT except the LCD display is replaced with an OLED display and all the components are RoHS compliant. Schematics for Rev3 and Rev2 boards are the same when viewed as PDF files, but there is a short in the board layers on the Rev2 that has been corrected for Rev3. The rare Rev1 prototype boards had different schematics and are not discussed in this document.

### 3.4.2.1 Procedure for Rev A Boards

To determine if the board is a Starter Kit Rev A board: A Rev A board is recognized by examining the front of the board and looking for the part number just beneath the large Microsemi corporate logo on the board top silk-screen. The part number is A3PE-STARTER-KIT-2 followed by REV A.

To chain Starter Kit Rev A boards together: All boards from the board nearest the FlashPro4 programmer must have the shunt that is placed by default on pins 3 and 4 of the J5 header moved to connect pins 1 and 2. On the board and schematic CHAIN (pins 1 and 2) and LAST DEVICE (DEFAULT) (pins 3 and 4) are labeled clearly. Only the last board in the chain must have the shunt remaining across pins 3 and 4 of the J5 connector.

**Note:** If there is only one board in the chain then it, by definition, is the last board and should have the shunt at J5 connecting pins 3 and 4. This is why this position is labeled as the DEFAULT position for a typical customer with a single starter kit board.

### 3.4.2.2 Procedure for Rev3 Boards

To determine if the board is a Rev3 board: A Rev3 board is recognized by examining the front of the board and looking for the part number just beneath the large Microsemi SoC Products Group corporate logo on the board top silk-screen. The part number is A3PE-A3P-EVAL-BRD1 followed by REV3.

**To chain Rev3 boards together:** Treat it as Starter Kit Rev A board in the previous section.

### 3.4.2.3 Procedure for Rev2 Boards (With and Without Rework)

To determine if the board is a Rev2 board: A Rev2 board is indicated by a red LED in the upper right corner of the board and a part number underneath the Microsemi SoC Products Group corporate logo on the board top silk-screen. The part number is A3PE-A3P-EVAL-BRD1. No additional text is followed with the board number. If the board is reworked to force it to become equivalent to a Rev3 board, it contains a green wire on the top side of the board. If it does not contain green wire, it is Rev2.

To chain Rev2 boards together: If reworked, treat it as Rev3 in the previous section. If not reworked, then chaining of the boards cannot be done. The shunt on J5 must be removed for any programming to take place.

#### 3.4.2.4 Procedure for Rev1 Boards

To determine if the board is a Rev1 board: A Rev1 board is indicated by no red LED in the upper right corner of the board. The part number on the board top silk-screen is A3PE-EVAL-BRD600.

**Note:** Rev1 boards should not be used with this user guide or with design files included with this Starter Kit as the schematics are incompatible with current commercial boards.

VPUMP connections when chaining boards together: When these boards are connected through a connection from J2 of one board to J1 of another board, VPUMP will be connected from one board to another. When powering on one board with a connector in place, notice that the 1.5 V, 1.8 V, 2.5 V, and 3.3 V LEDs will light on the board to which no power has been applied. The FPGA on that board, if it is programmed, will start operating. This is clearly an inappropriate situation for a large chain of boards. This is caused by having the JP48 connector for supplying VPUMP from the board connected on other boards in the chain, as VPUMP is itself connected to the 3.3 V supply output that is used to generate the other FPGA voltages on a board. To prevent VPUMP from being used as the source of a 3.3 V supply, remove the shunt that is in place on the JP48 connector to force JP48 to be open-circuit. To prevent loss of the shunt, it may be safely stored on the J12 header for the daughter card power supply as it is impossible to cause a short by joining any adjacent pins.

### 3.5 Programming the ProASIC3/E Device with FlashPro

The base board used for all ProASIC3/E starter kits is A3PE-A3P-EVAL-BRD1.

The A3PE-STARTER-KIT-2 and A3PE-PROTO-KIT boards are socketed and are populated with A3PE1500 silicon. Any device in the ProASIC3/E family in the PQ208 package can be placed into the socket.

In a kit with a socket on the board, a reasonable number of insertions may be made if the user exercises great care in inserting components into the socket.

**Note:** Screw-down sockets are not clam shell sockets, and do have a lifetime of about 20 insertions, although far greater may be achieved with careful placement and use of a torque-limiting screwdriver. Placement of the FPGA in the socket is critical, to ensure all pins are correctly connected.

#### 3.5.1 Connecting the FlashPro4 Programmer to the Board

Connect the FlashPro4 programmer to your computer through the USB cable. For installing the software and connecting to FlashPro4, see the *FlashPro User Guide*. The amber (yellow) power LED on the FlashPro4 must be illuminated at this stage. If it is not, recheck the procedure in the FlashPro User Guide until you obtain a steady amber (yellow) power LED illumination.

Ensure the board power switch, SW11 is in the OFF position, and only the red board external power LED is illuminated on the board.

Connect the FlashPro4 programmer to the board through the 10-pin programming cable supplied with the FlashPro4 programmer hardware. The connector to use on the board is labeled FP and is the lower J1 shrouded and keyed header. The pin 1 location on the cable indicated by the red ribbon running along the side of the cable can be on the left side as it enters into the board. After connecting the FlashPro4 programmer, select **Analyze Chain** from the File menu in the FlashPro software. If all is well, the appropriate device ID for the ProASIC3 or ProASIC3E part shows in the software display on the PC. If there is a JTAG communication issue, try changing the VJTAG voltage. For overcoming noise, higher values usually work better, but all values must work with the supplied programming cable (6 inches in length) with connection to just one board.

#### 3.5.2 Programming or Re-Programming the Design

Download the latest version of the ProASIC3/E starter kit example design at:

<https://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/proasic3/proasic3-starter-kit#documents>.

Using FlashPro software, program the example design on ProASIC3/E device.

### 3.5.3 Jumpers for Isolating Switches and LEDs from FPGA

Many jumpers are provided on the board to allow the user to disconnect various switch combinations or LEDs from the FPGA I/O banks. All such jumpers are shown in the schematic in [Figure 8](#), page 27 and are labeled on the top-layer silkscreen as JP\* where \* is a number. All jumpers are also labeled with the FPGA I/O pin number to which they are connected; example, JP48 for the 3.3 V connection of VPUMP to the FPGA is labeled with 106, which indicates that it is connected to pin 106. Similarly, SW4 has a jumper above it called JP14, which is labeled with 64, indicating that SW4 is connected through to pin 64 of the FPGA when this jumper is in place.

Disconnecting the jumpers JP11, JP12, JP13, and JP14 causes the momentary push-button switches (SW1, SW2, SW3, and SW4) to be disconnected from the FPGA so that the I/O pins 68, 67, 66, and 64 are used for other purposes. Disconnecting the eight jumpers, JP1 through JP8, causes the eight light emitting diodes (D1 through D8) to be disconnected from the FPGA I/O pins 63, 61, 60, 59, 58, 57, 56, and 55, respectively.

The momentary push-button switches (SW5 and SW6, for applying a reset pulse and a global pulse) are connected through jumpers JP15 and JP16 to I/Os 159 and 113 respectively. All labeling is clearly shown on the silk screen.

The hex switches U13 and U14 each are connected to four I/Os on the FPGA. There are four separate jumpers for each of these hex switches, located on the bottom right of the board. They are labeled with Bit0, Bit1, Bit2, and Bit3 on the silk screen, as well as being labeled with the I/O pin on the FPGA to which each is connected.

This allows individually control the desired effect of a switch and, by connecting directly to the FPGA side of a disconnected jumper, hold a particular pin at a chosen logic level while continuing to use the hex switch to affect other pins. This flexibility is useful for experimentation with designs of your own choosing and connecting other external equipment to the board for development purposes.

The internal and external oscillator selection through JP24 is worth a mention. JP24 is a three-pin header onto which a normal two-hole shunt is fitted. Normally, the shunt is connected across pins 3 and 2 of JP24. In this position the on-board oscillator, U1, provides the internal clock to the middle pin of the jumper which in turn is connected to pin 26 of the FPGA. By moving the shunt down to connect pins 2 and 1 of JP24, the external clock at pin 1 is connected to the FPGA instead. The external clock is connected through the SMA connector J19 at the bottom left of the board.

The following table lists the jumpers available on the board with their description.

**Table 2 • Summary of Jumpers**

| Jumper               | Description  |
|----------------------|--|
| JP1 to JP8           | To connect LEDs (LED1 to LED8) to FPGA                           |
| JP10                 | VJTAG enable/disable   |
| JP11 to JP14         | To connect push-button switches (SW1, SW2, SW3, and SW4) to FPGA |
| JP15 and JP16        | To connect momentary push-button switches SW5 and SW6 to FPGA    |
| JP9 and JP17 to JP19 | To connect hex switch (U13) to FPGA                              |
| JP20 to JP23         | To connect hex switch (U14) to FPGA                              |
| JP24                 | On-board or external clock source selection                      |
| JP48                 | VPUMP voltage  |
| JP49                 | VCCPLC – Power supply to the east side PLL                       |
| JP50                 | VCCPLF – Power supply to the west side PLL                       |



### 3.5.3.1 Test Points

All test points on the board are fitted with small test loops. These test points are labeled on the silkscreen as TP1, TP2, and so on. All such test points are also labeled on the silk screen with the voltage expected to be observed at that test point. Voltages will be one of 3.3 V, 2.5 V, 1.8 V, 1.5 V, or GND. When measuring the voltage at a test point with a DVM (digital voltage multimeter), the ground lead must be connected to a test point labeled GND and the voltage lead must be connected to the voltage to be tested. All voltage labels on the board are relative to a 0 V ground reference or GND.

### 3.5.3.2 Prototyping Area

The prototyping area to the right of the board has the bottom two rows of pins connected to ground, labeled as GND on the silk screen and enclosed in a box, giving 16 holes connected to 0 V. The top two rows of pins are connected to various power supply rails internally in the board.

They are grouped into squares of four pins from left to right as follows: 3.3 V, 2.5 V, 1.8 V, and 1.5 V, giving four holes for each voltage level. All other holes in the prototyping area are unconnected and may be used to hold various discrete components as necessary for experimentation.

Next to the prototyping area is U2, which is a space for an optional oscillator. This space may be used for fitting a second oscillator to the board, similar to the one used at U1, so as to provide two different frequency clocks to the FPGA.

On the reverse side of the board, there is an area labeled U5, which is a TQ100 pattern with some surrounding pads. This area is used to solder a TQ100 part, and then connect that part by adding discrete wires to the pads and connecting it to desired pins on the board. The main purpose of this is to allow a previously programmed TQ100 packaged device to be used to provide a more interesting system application.

### 3.5.3.3 Layering on Board

The complete board design and manufacturing files are available at:  
<https://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/proasic3/proasic3-starter-kit#documents>.

The board file is in allegro format, which allows an end user to create the appropriate Gerbers and other board views as needed.

The board is fabricated with 6 layers of copper. The layers are arranged as follows from the top of the board down to the bottom:

- Layer 1: Top signal layer
- Layer 2: Ground plane
- Layer 3: Signal layer 3, used for LVDS receive and other signals
- Layer 4: Signal layer 4, used for LVDS transmit and other signals
- Layer 5: Power plane
- Layer 6: Bottom signal layer

**Note:** For signal integrity that the two LVDS layers are sandwiched between ground and power planes to isolate them as best as possible from external influences.

## 3.6 Clock Circuits

The ProASIC3/E Starter Kit board has two clock circuits: a 40 MHz oscillator and a manual clock.

### 3.6.1 40 MHz Oscillator

The 40 MHz oscillator on the board is a 10 ppm stability crystal module which gives good LVDS performance. For better stability, an external oscillator is provided through the SMA connector. Typically, a TCXO gives 1 ppm stability and an OCXO gives 0.1 ppm stability. Both the default on-board oscillator and the SMA are connected to the CLK F input of the west bank of the FPGA. Position is also provided on the board for mounting a second crystal oscillator module connected to the CLK C input of the FPGA on the east bank.

## 3.7 LED Device Connections

Eight LEDs are connected to the device through jumpers JP1 to JP8. If the jumpers are in place, the device I/O can drive the LEDs. The LEDs change based on the following output:

- A 1 on the output of the device lights the LED
- A 0 on the output of the device switches off the LED
- An un-programmed or tristated output may show a faintly lit LED

**Note:** If the I/O voltage of Bank 5 (on ProASIC3, set by SW8) or Bank 2 (ProASIC3E set by SW8 and SW7 being at the same level) is not at least 2.5 V, the LEDs will not illuminate. A setting of 1.8 V on the voltage bank will cause extremely faint illumination.

The following table lists the LED and device connections. To use the device I/O for other purposes, remove the jumpers.

**Table 3 • LED Device Connections**

| LED | Device Connection |
|-----|-------------------|
| D1  | U8 Pin 63         |
| D2  | U8 Pin 61         |
| D3  | U8 Pin 60         |
| D4  | U8 Pin 59         |
| D5  | U8 Pin 58         |
| D6  | U8 Pin 57         |
| D7  | U8 Pin 56         |
| D8  | U8 Pin 55         |

## 3.8 Switches Device Connections

Four switches are connected to the device through jumpers JP11 to JP14. If the jumpers are in place, the device I/O can be driven by the switches listed in the following table.

- Pressing a switch drives a 1 into the device. The 1 continues to drive while the switch is in place.
- Releasing a switch drives a zero into the device.

To use the device I/O for other purposes, remove the jumpers.

**Table 4 • Switch Device Connections**

| Switch | Device Connections |
|--------|--------------------|
| SW1    | U8 Pin 68          |
| SW2    | U8 Pin 67          |
| SW3    | U8 Pin 66          |
| SW4    | U8 Pin 64          |

## 3.9 LVDS Channels

Four LVDS channels with up to a maximum signaling rate of 350 MHz are supported on the Starter Kit board. These LVDS signals are brought out to a pair of RJ-45 (CAT-5E) sockets (J40 and J41). For the position of these connectors, see [Figure 1](#), page 4.

The LVDS signals are driven using 8 differential pairs (consisting of 16 I/O pins) from the west side (Bank6 and Bank7) of the FPGA device A3PE1500-PQ208. These 16 signals are terminated on the J40 and J41 connectors. The FPGA pins used for LVDS signaling are listed in [Table 7](#), page 13.

The LVDS signals are terminated on J40 and J41 connectors so that a standard patch cable can be used for doing loop-back testing. For schematic representation of connector signal details, see [Figure 16](#), page 35.

The four differential pairs (consisting of eight I/O pins) are terminated, as listed in the following table, using the following color convention on the first RJ45 connector (referred to as CAT 5E Primary for the purpose of differentiation).

**Table 5 • Color Convention on CAT 5E Primary**

| Color        | Pin | Signal |
|--------------|-----|--------|
| White/Orange | p1  | TX1+   |
| Orange       | p2  | TX1–   |
| White/Green  | p3  | RX1+   |
| Blue         | p4  | TX2–   |
| White/Blue   | p5  | TX2+   |
| Green        | p6  | RX1–   |
| White/Brown  | p7  | RX2+   |
| Brown        | p8  | RX2–   |

**Note:** TXn+ refers to positive signal of the transmit side of balanced signal transmission.

**Note:** TXn– refers to negative signal of the transmit side of balanced signal transmission.

**Note:** RXn+ refers to positive signal of the receive side of balanced signal transmission.

**Note:** RXn– refers to negative signal of the receive side of balanced signal transmission.

The four differential pairs (consisting of eight I/O pins) are terminated, as listed in the following table, using the following color convention on the second LVDS connector (referred to as "CAT 5E SECONDARY" for the purpose of differentiation).

**Table 6 • Color Convention on CAT 5E Secondary**

| Color        | Pin | Signal |
|--------------|-----|--------|
| White/Orange | p1  | RX3+   |
| Orange       | p2  | RX3–   |
| White/Green  | p3  | TX3+   |
| Blue         | p4  | RX4–   |
| White/Blue   | p5  | RX4+   |
| Green        | p6  | TX3–   |
| White/Brown  | p7  | TX4+   |
| Brown        | p8  | TX4–   |

**Note:** The colors refer to the colors that will appear on the CAT 5E cable. The pin numbers correspond to the pin numbers of an RJ-45 connector. Note that the CAT-5E PRIMARY connections are labeled for the purposes of what is regarded as standard connections for CAT-5E on Ethernet-type connectors. The connections on the CAT-5E SECONDARY are reversed so as to allow a standard patch cable to check loop-back on these LVDS signals.

A 1-foot CAT5 standard patch cable supplied with the ProASIC3/E Starter Kit can be used for LVDS signals loop-back. Also note that the VCCI and VMV voltages of Bank6 and Bank7 (west side) are

connected to a fixed 2.5 volts, which is required in ProASIC3 (LVDS only available in A3P250 and larger) and ProASIC3E (LVDS available in all devices) for LVDS signaling.

**Table 7 • FPGA – LVDS I/O Pin Details**

| FPGA Pin No. | FPGA I/O Pin Name <sup>1</sup> | Signal Name | CAT5E Connector Pin No. |
|--------------|--------------------------------|-------------|-------------------------|
| 7            | GAC2/IO132PDB7V1               | TX1+        | CAT 5E – PRI – 1        |
| 8            | IO132NDB7V1                    | TX1–        | CAT 5E – PRI – 2        |
| 9            | IO130PDB7V1                    | TX2+        | CAT 5E – PRI – 5        |
| 10           | IO130NDB7V1                    | TX2–        | CAT 5E – PRI – 4        |
| 11           | IO127PDB7V1                    | RX1+        | CAT 5E – PRI – 3        |
| 12           | IO127NDB7V1                    | RX1–        | CAT 5E – PRI – 6        |
| 13           | IO126PDB7V0                    | RX2+        | CAT 5E – PRI – 7        |
| 14           | IO126NDB7V0                    | RX2–        | CAT 5E – PRI – 8        |
| 30           | GFA2/IO117PDB6V1               | TX3+        | CAT 5E – SEC – 3        |
| 31           | IO117NDB6V1                    | TX3–        | CAT 5E – SEC – 6        |
| 37           | IO112PDB6V1                    | TX4+        | CAT 5E – SEC – 7        |
| 38           | IO112NDB6V1                    | TX4–        | CAT 5E – SEC – 8        |
| 42           | IO106PDB6V0                    | RX3+        | CAT 5E – SEC – 1        |
| 43           | IO106NDB6V0                    | RX3–        | CAT 5E – SEC – 2        |
| 44           | GEC1/IO104PDB6V0               | RX4+        | CAT 5E – SEC – 5        |
| 45           | GEC0/IO104NDB6V0               | RX4–        | CAT 5E – SEC – 4        |

1. Pin names are valid only for the A3PE600-PQ208 part. They are not correct for use with an A3P250.
2. J40: RJ45 connector is referred as CAT 5E PRIMARY connector.
3. J41: RJ45 connector is referred as CAT 5E SECONDARY connector.

For the location of J40 and J41 connectors on the ProASIC3/E Starter Kit board, see [Figure 1](#), page 4.

## 4 Setup and Self Test

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This section provides information about how to set up and test the ProASIC3/E Starter Kit board.

### 4.1 Software Installation

The ProASIC3/E Starter Kit includes Libero SoC software. For the latest version of Libero SoC software, go to <https://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc#overview>.

For Libero SoC software installation instructions, see the *Libero SoC Quick Start Guide*.

### 4.2 Hardware Installation

FlashPro4 is required to use the ProASIC3/E Starter Kit. For software and hardware installation instructions, see the *FlashPro User Guide*.

### 4.3 Testing the Starter Kit Board

See *Testing the Board*, page 19.

### 4.4 Programming the Test File

To retest the Starter Kit board at any time, use the test program to reprogram the board. Download the ProASIC3/E Starter Kit example design at: <https://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/proasic3/proasic3-starter-kit#documents>.

Using FlashPro software, program the example design on ProASIC3/E device. This design is currently implemented for the A3PE1500 die size. For a device of a different size, it is possible to recompile the design into other device sizes. For information about retargeting the device, see the *Designer User's Guide*.

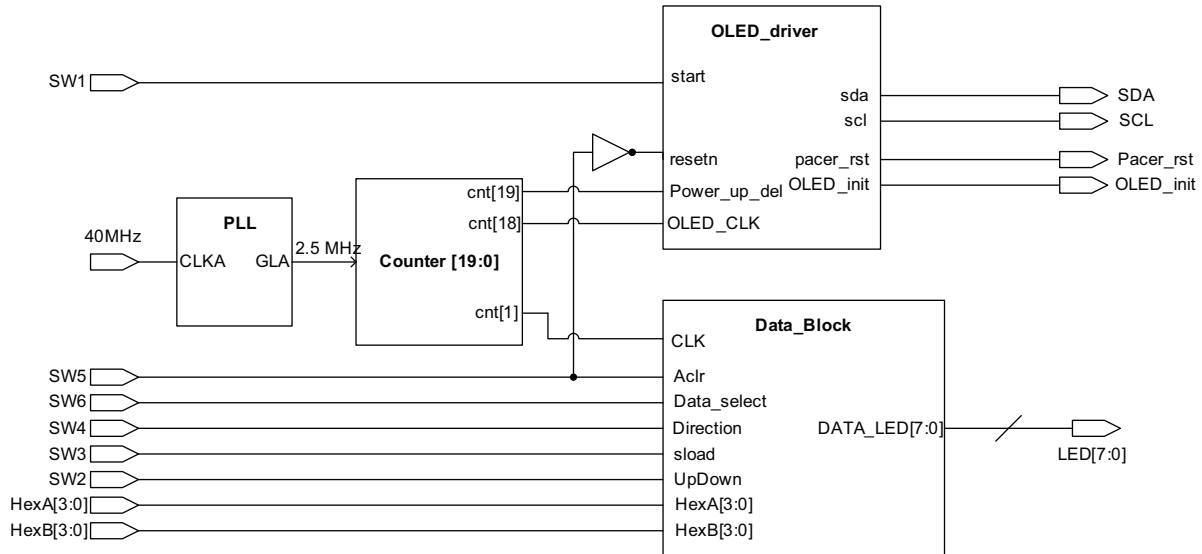
For instructions on programming the device using FlashPro4, see the *FlashPro User Guide*.

## 5 Description of Test Design

The description of the test design is provided with the Starter Kit. This design contains a data generator block for LEDs, PLL for clock generation, and an OLED display driver block. A block diagram of the design is shown in the following figure.

**Note:** The latest version of the board A3PE-STARTER-KIT-2 REV B does not have OLED display. For more information, see the [CN1418A: Addendum A: Designing without OLED Display on Kits](#).

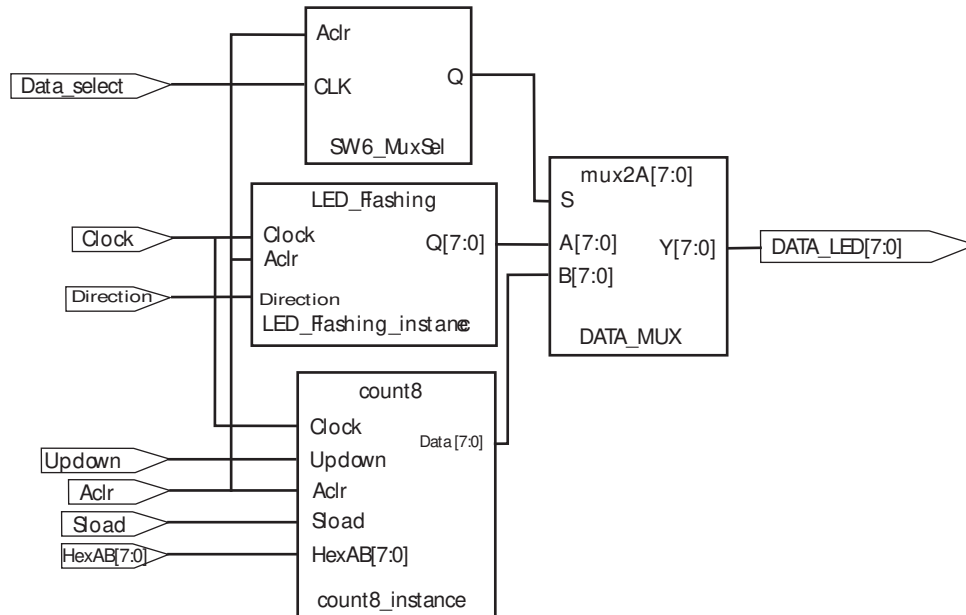
**Figure 3 • Design Block Diagram**



The on-chip PLL takes a 40 MHz oscillator clock as reference input and generates 2.5 MHz clock for the design. The data generator (Data\_Block) generates an eight-bit up-down counter and eight-bit flashing signal. The data generator output is displayed on the ProASIC3/E starter kit board LEDs. By default, an eight-bit flashing signal is displayed on the LEDs. The LEDs flashing direction can be changed by pressing SW4. Switch the data using the SW6 signal. The counter has synchronous load and an asynchronous clear. The counter can be loaded with the hex switches data by pressing SW3. Press and hold SW2 for down counting.

The following figure shows a block diagram of the Data\_Block.

**Figure 4 • Data Block Diagram**



The following table lists the functionality of different switches.

**Table 8 • Switches**

| Action                                  | Results   |
|---|---|
| Press SW2                               | Up-Down control for the 8-bit counter. Press and hold SW2 for down count.   |
| Press SW3                               | Synchronous load for the 8-bit counter. Press SW3 for loading from the hex switches. Holding the SW3 displays the hex switches value on LEDs. |
| Press SW4                               | Direction control for LEDs flashing. While LEDs flashing is selected with SW6, SW4 can be used to change the LEDs flashing direction.         |
| Press SW5                               | Asynchronous clear for the whole design.  |
| Press SW6                               | Select for DATA_BLOCK. It allows switching LED output between the counter and flashing data.  |
| Change Hex Switch setting (U13 and U14) | Changes the loaded data for the eight-bit counter.  |

## 6 LVDS Signal Evaluation

This section explains the test setup and design for the LVDS signal evaluation. It reports the measurements performed on the board, and at the end, makes recommendations to increase the LVDS signal quality in order to meet the performance criteria.

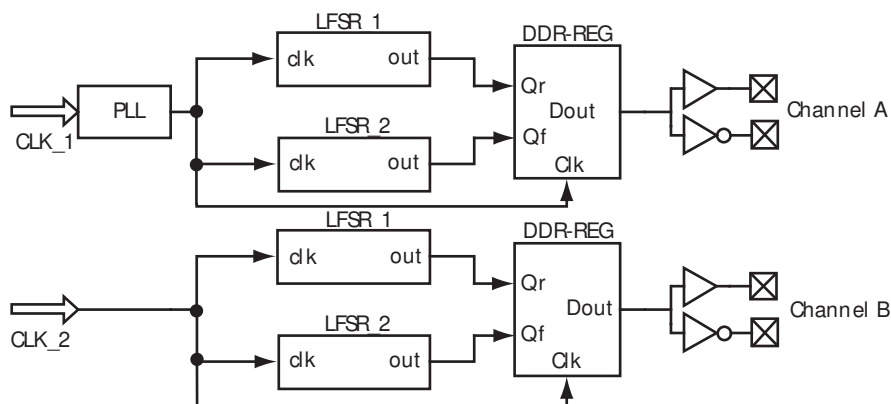
### 6.1 Hardware Test Setup

The test setup uses a ProASIC3 Development Kit containing an A3PE600-PQ208 engineering sample. LVDS loop-back is closed using various lengths of CAT-5E cables (1-, 3-, and 6-foot). The measurements are taken using a 1159A-1 GHz Agilent differential probe.

### 6.2 Design Test Setup

The following figure shows the block diagram of the transmitter section of the test design programmed inside the ProASIC3 FPGA. The design contains two similar channels of data. Channel A is driven by a PLL to achieve high data rates, and Channel B uses an external clock in the event that slow data rates are needed for test or debugging purposes.

Figure 5 • TX Portion of Test Design



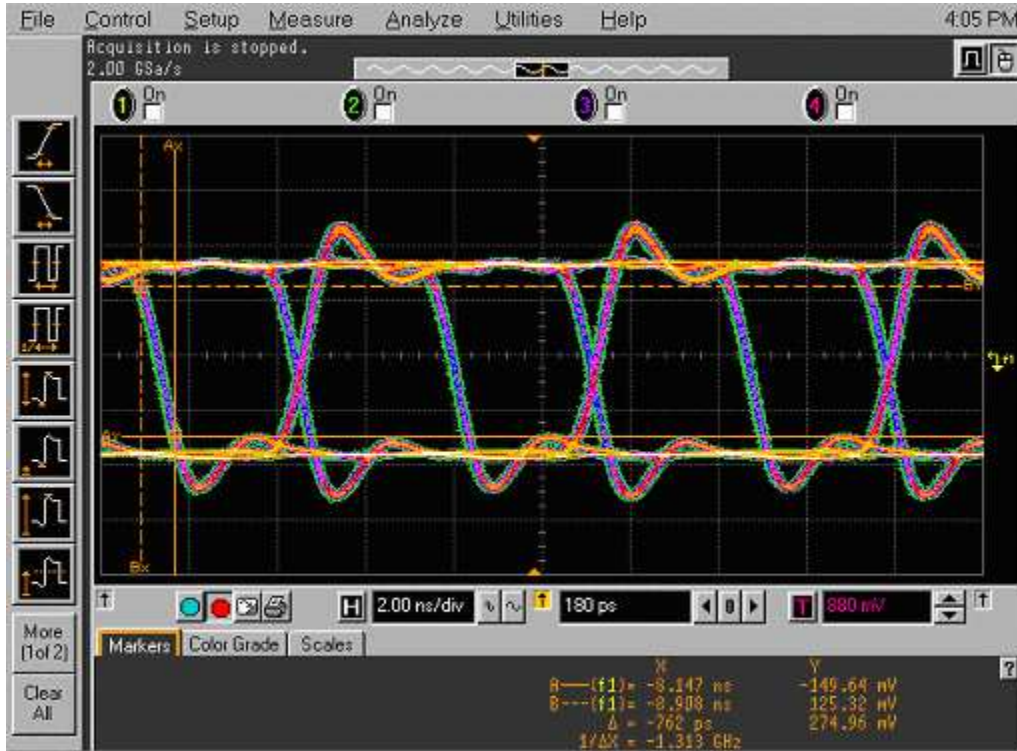
Each channel uses an LFSR to generate a pseudo-random data stream. The data stream is entered in DDR registers to achieve higher data rates from relatively slower clocks (e.g., 300 Mbps data rate from 150 MHz clock). The output of the DDR registers is sent out using the LVDS I/O standard. The output data is looped back and received by the FPGA using LVDS receivers.



### 6.3 Measurement Results

The following figure shows the LVDS signal across the 100 Ohm termination resistor at 300 Mbps. The eye height across the termination is about 275 mV which is well within the LVDS specification.

Figure 6 • LVDS Signal across RX Termination at 300 Mbps



## 7 Testing the Board

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This section defines the test procedure required to be carried out by the Microsemi SoC Products Group designated manufacturer's testing facility on the ProASIC3/E Starter Kit board with silkscreen labeling A3PE-STARTER-KIT-2. This testing is specific to the socketed version of the board. All steps in the following enumerated test procedure should be followed in sequence for testing the board. Deviations in the sequence are explained in the text.

### 7.1 Equipment Required

This section provides the equipments required for testing the board.

#### 7.1.1 Equipment Provided to Testing Facility

Microsemi SoC Products Group provides the following:

- Test procedure document.
- FlashPro v9.1 software or latest on Microsemi website
- FlashPro4 programmer and programming cable for connecting to the A3PE-STARTER-KIT-2.
- Pre-programmed A3PE1500-PQ208 silicon. Ten devices will be provided for ten boards. The initial silicon will not be labeled as having been programmed. (this is just for the testing associated with the first manufacturing build.) Additional devices will be provided for testing further boards and this change will be detailed in an update to the procedure.
- Power supply (+9 V, 2 A CUI) for the ProASIC3/E Starter Kit board plus a mains cable for the power supply.

#### 7.1.2 Testing Facility Equipment

The manufacturer's testing facility will provide the following equipment for testing of the board: Digital Multimeter to measure voltages on the circuit board at the known test points.

### 7.2 Test Procedure for the A3PE-STARTER-KIT-2

In this section, full test procedure for the boards is outlined. This procedure applies to socketed boards. For boards fitted with directly soldered parts, the procedure is the same except for fitting of the FPGA. In such cases, adjust the procedure accordingly and ignore references to fitting parts to sockets.

#### 7.2.1 Initial Power-On Procedure

This part of the procedure may be carried out independently and ahead of the other parts of the test procedure. Boards passing this procedure may be transferred to a passing set of boards.

The following steps describe the procedure to perform the initial power-on.

1. Record the time of the test and the board serial number (written by the bar code on the back of the board) into a test log.
2. Plug the +9 V power supply into the wall.
3. Take an A3PE-STARTER-KIT-2 that has an empty socket. Ensure the switch SW11 is in the OFF position, (the switch should be moved to the left). This corresponds with the labeling of the silkscreen on the board.
4. Connect +9 V DC output of the CUI power supply to the J18 connector on the board. You should observe the red LED at the top right of the board; LED D19 should light, indicating +9 V DC has been applied to the board.
5. Move the SW11 switch to the ON position—to the right. Observe that LEDs, D13, D9, D10, D11, and D17 light up green on the board. All LEDs are on the top edge of the board (same edge as red D19 power connector LED, which should remain lit).
6. Using a DVM, measure DC voltages using TP11 as ground:
7. TP6 and TP7 should be 3.3 V (values  $\pm 0.2$  V are acceptable). Values outside this range are a failure.
8. TP15 should be 1.5 V (values  $\pm 0.1$  V are acceptable).
9. TP8 should be 1.8 V (values  $\pm 0.1$  V are acceptable).