Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Adjustable Frequency Buck or Buck/Boost Pre-Regulator with a Synchronous Buck, 3 Internal LDOs, Window Watchdog Timer, and NPOR

FEATURES AND BENEFITS

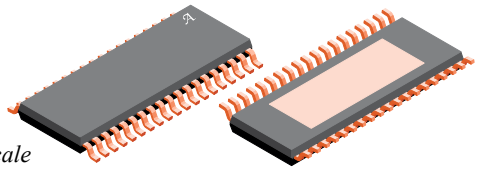
- Automotive AEC-Q100 qualified
- 2.8 V_{IN} to 36 V_{IN} operating range, 40 V_{IN} maximum
- Buck or buck/boost pre-regulator (VREG)
- Adjustable PWM switching frequency: 250 kHz – 2.4 MHz
- PWM frequency can be synchronized to external clock
- 1.25 V/750 mA_{DC}/1 A_{PEAK} synchronous buck (1V25)
- 3.3 V (3V3) and 5 V (V5) internal LDO regulators with fold back short circuit protections
- 5 V (V5P) internal tracking LDO regulator with fold back short circuit and short-to-battery protections
- TRACK sets either 3V3 or V5 as the reference for V5P
- Power-on reset with fixed delay of 15 ms for 1V25/3V3 UV and OV protection (NPOR)
- Programmable watchdog timer with a 30 ms activation delay
- Active low, watchdog timer enable/disable pin (WD_{ENn})
- Dual band gaps for increased reliability: BG_{VREF}, BG_{FAULT}

Continued on next page...

APPLICATIONS

- Automotive Control Modules for:
  - □ Electronic Power Steering (EPS)
  - □ Transmission Control (TCU)
  - □ Advanced Braking Systems (ABS)
  - □ Emissions Control Modules
  - □ Other automotive applications

PACKAGE: 38-Pin eTSSOP (suffix LV)



Not to scale

DESCRIPTION

The A4410 is power management IC that uses a buck or buck/boost pre-regulator to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics, and protections. The output of the pre-regulator supplies a 5 V/250 mA_{MAX} tracking/protected LDO, a 3.3 V/160 mA_{MAX} LDO, a 5 V/150 mA_{MAX} LDO, and a 1.25 V/750 mA_{DC}/1 A_{PEAK} synchronous buck regulator. Designed to supply CAN or microprocessor power supplies in high temperature environments the A4410 is ideal for under hood applications.

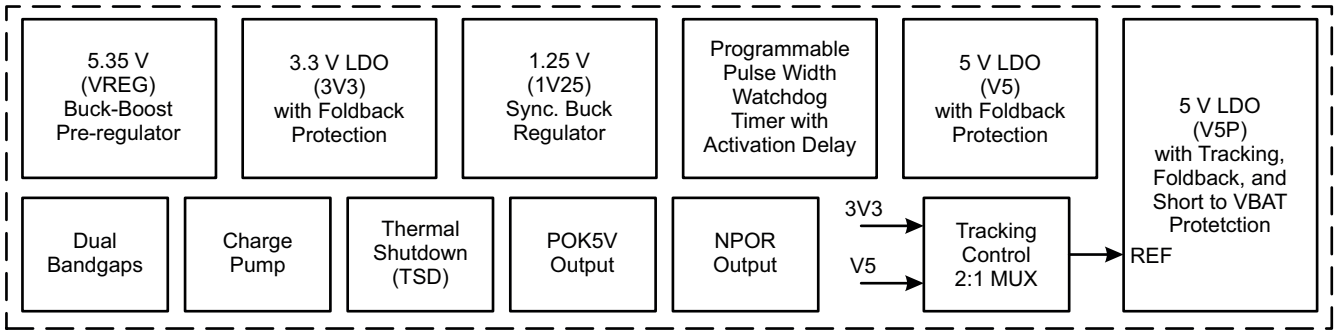
Enable inputs to the A4410 include a logic level (ENB) and two high-voltage (ENBAT1 and ENBAT2). The A4410 provides flexibility by including a TRACK pin to set the reference of the tracking regulator to either the 5 V or the 3.3 V output, so the A4410 can be adapted across multiple platforms with different sensors and supply rails.

Diagnostic outputs from the A4410 include a power-on-reset output (NPOR) with a fixed 15 ms delay, an ENBAT1 and ENBAT2 status outputs, and a PowerOK output for the 5 V and 5 V protected LDOs (POK5V). Dual bandgaps, one for regulation and one for fault checking, improve long-term reliability of the A4410.

The A4410 contains a Window Watchdog timer that can be programmed to accept a wide range of clock frequencies (WD_{ADJ}). The watchdog timer has a fixed 30 ms activation delay to accommodate processor startup. The watchdog timer has an enable/disable pin (active LOW, WD_{ENn}) to facilitate initial factory programming or field re-flash programming.

Protection features include under and over voltage lockout on all four CPU supply rails. In case of a shorted output, all linear regulators feature fold back over current protection. In addition, the V5P output is protected from a short-to-battery event. Both

Continued on next page...



A4410 Simplified Block Diagram

Features and Benefits (continued)

- PowerOK output for V5/V5P UV and OV (POK5V)
- Logic enable input (ENB) for microprocessor control
- Two ignition enable inputs (ENBAT1 and ENBAT2)
- ENBAT1 and ENBAT2 status indicator outputs
- SLEW rate control pin helps reduce EMI/EMC
- Frequency dithering helps reduce EMI/EMC
- OV and UV protection for all four CPU supply rails
- Pin-to-pin and pin-to-ground tolerant at every pin
- Thermal shutdown protection
- −40ºC to 150ºC junction temperature range

Description (continued)

switching regulators include pulse-by-pulse current limit, hiccup mode short circuit protection, LX short circuit protection, missing asynchronous diode protection (VREG only) and thermal shutdown.

The A4410 is supplied in a low profile, 38-lead eTSSOP package (suffix “LV”) with exposed power pad.

Selection Guide

Part Number	Temp. Range	Package	Packing[1]	Lead Frame
A4410KLVTR-T	–40 to 135°C	38-pin eTSSOP w/ thermal pad	4000 pieces per 7-in reel	100% Matte Tin

[1] Contact Allegro for additional packing options.

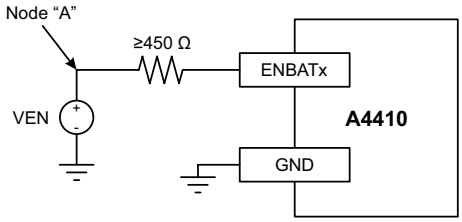
SPECIFICATIONS

Absolute Maximum Ratings[1]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V_{VIN}		−0.3 to 40	V
ENBAT1, ENBAT2	V_{ENBATx}	With current limiting resistor[2]	−13 to 40	V
			−0.3 to 8	
	I_{ENBATx}		±75	mA
LX1, SLEW			−0.3 to VVIN+0.3	V
		t < 250 ns	−1.5	
		t < 50 ns	VVIN+3 V	
VCP, CP1, CP2			−0.3 to 50	V
V5P	V_{V5P}		−1.0 to 40 [3]	V
All other pins			−0.3 to 7	V
Ambient Temperature	T_A	Range K for automotive	−40 to 135	ºC
Junction Temperature	T_J		−40 to 150	ºC
Storage Temperature Range	T_S		−40 to 150	ºC

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

[2] The higher ENBAT1 and ENBAT2 ratings (-13 V and 40 V) are measured at node “A” in the following circuit configuration:



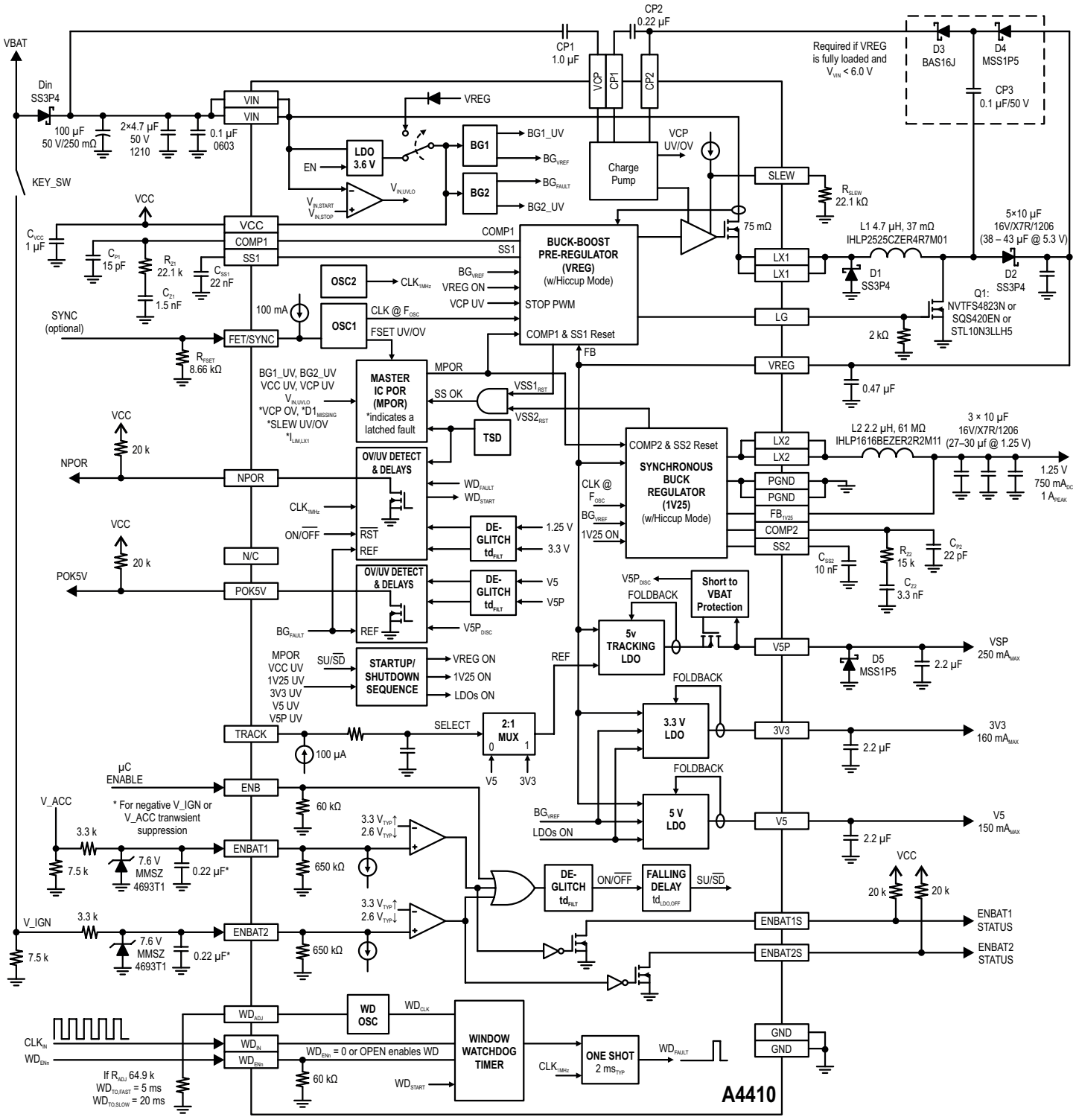
[3] Independent of V_{VIN}.

Table 3: Thermal Characteristics

(may require derating at maximum conditions, see application information)

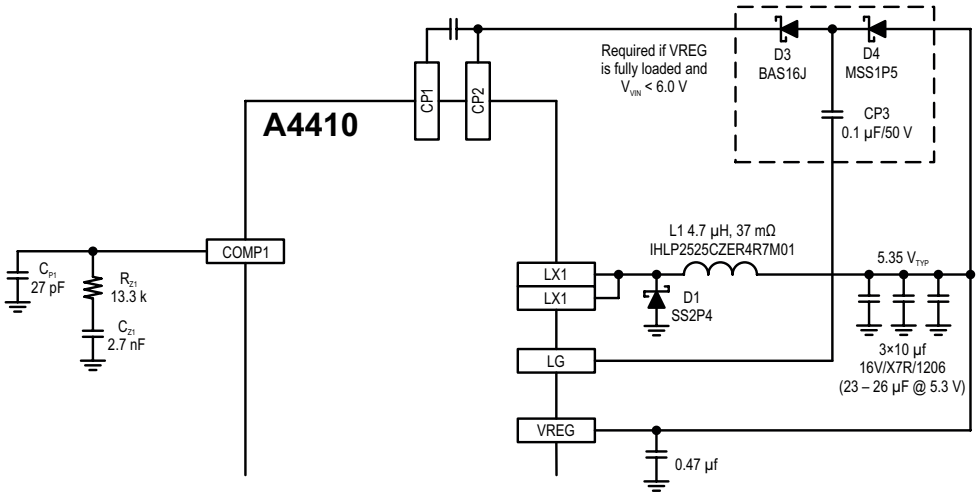
Characteristic	Symbol	Test Conditions*	Value	Unit
Junction to Pad Thermal Resistance	$R_{\theta JC}$	eTSSOP-38 (LV) Package	30	ºC/W

*Additional thermal information available on the Allegro website.

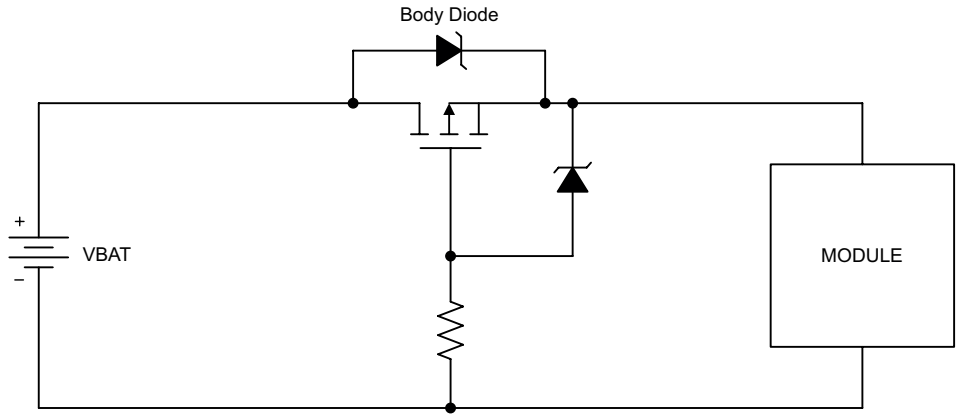


Functional Block Diagram/Typical Schematic

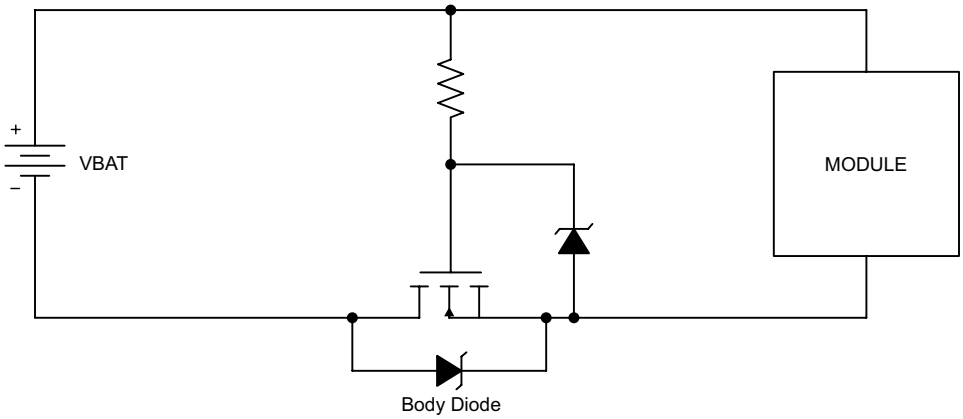
Buck-Boost Mode (f_{OSC} = 2 MHz)



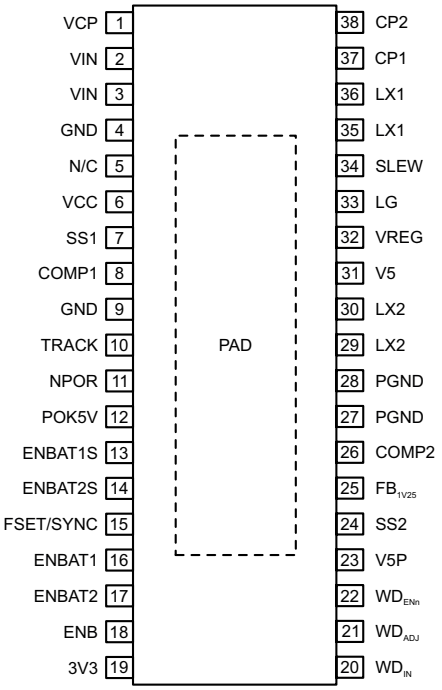
Functional Block Diagram Modifications for Buck Only Mode (f_{OSC} = 2.0 MHz)



Functional Block Diagram Using a PMOS FET for Reverse Battery Protection Instead of a Series Schottky Diode (D_{IN})



Functional Block Diagram Using an NMOS FET for Reverse Battery Protection Instead of a Series Schottky Diode (D_{IN})



Package LV, 38-Pin eTSSOP Pin-out Diagram

Terminal List Table

Number	Name	Function
1	VCP	Charge pump reservoir capacitor
2,3	VIN	Input voltage
4,9	GND	Ground
5	N/C	No Connect
6	VCC	Internal voltage regulator bypass capacitor pin
7	SS1	Soft start programming pin for the buck/boost pre-regulator
8	COMP1	Error amplifier compensation network pin for the buck/boost pre-regulator
10	TRACK	Tracking control: Open/High – V5P tracks 3V3, GND/Low – V5P tracks V5
11	NPOR	Active LOW, open-drain regulator fault detection output
12	POK5V	PowerOK output indicating when either the V5 or V5P rail is under-voltage (UV)
13	ENBAT1S	Open drain ignition status output, for ENBAT1 only
14	ENBAT2S	Open drain ignition status output, for ENBAT2 only
15	FSET/ SYNC	Frequency setting and synchronization input
16	ENBAT1	Ignition enable input from the key/switch via a 1K of resistance
17	ENBAT2	Ignition enable input from the key/switch via a 1K of resistance
18	ENB	Logic enable input from the micro-controller
19	3V3	3.3 V regulator output
20	WD_{IN}	Watchdog refresh input (rising edge triggered) from a micro-controller or DSP
21	WD_{ADJ}	The watchdog wait/delay time is programmed by connecting R_{ADJ} from this pin to ground
22	WD_{ENn}	Watchdog enable pin: Open/Low – WD is enabled, High – WD is disabled
23	V5P	5 V tracking/protected regulator output
24	SS2	Soft start programming pin for the 1.25 V synchronous buck
25	FB1V25	Feedback pin for the 1.25 V regulator
26	COMP2	Error amplifier compensation network pin for the 1.25 V synchronous regulator
27,28	PGND	Power ground for the 1.25 V synchronous regulator / gate driver
29,30	LX2	Switching node for the 1.25 V synchronous regulator
31	V5	5 V regulator output
32	VREG	Output of the buck-boost and input for the LDOs and 1.25 V_{OUT} sync. Buck
33	LG	Boost gate drive output for the buck/boost pre-regulator
34	SLEW	Slew rate adjustment for the rise time of LX1
35,36	LX1	Switching node for the buck/boost pre-regulator
37	CP1	Charge pump capacitor connection
38	CP2	Charge pump capacitor connection
–	PAD	

ELECTRICAL CHARACTERISTICS – GENERAL SPECIFICATIONS[1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
General Specifications						
Operating Input Voltage	V_{VIN}	After V_{VIN} > VIN_{START}, and V_{ENB} > 2.0 V or V_{ENBATx} > 3.5V, Buck-Boost Mode	2.8	13.5	36	V
		After V_{VIN} > VIN_{START}, and V_{ENB} > 2.0 V or V_{ENBATx} > 3.5V, Buck Mode	5.1	13.5	36	
VIN UVLO START Voltage	VIN_{START}	V_{VIN} rising	4.55	4.80	5.05	V
VIN UVLO STOP Voltage	VIN_{STOP}	V_{VIN} falling, V_{ENBATx} ≥ 3.6 V or V_{ENB} ≥ 2.0 V, V_{VREG} = 5.2 V	2.52	2.65	2.78	V
VIN UVLO Hysteresis	VIN_{HYS}	VIN_{START} – VIN_{STOP}	—	2.2	—	V
Supply Quiescent Current [1]	I_Q	V_{VIN} = 13.5 V, V_{ENBATx} ≥ 3.6 V or V_{ENB} ≥ 2.0 V, V_{VREG} = 5.6 V (no PWM)	—	13	—	mA
	$I_{Q,SLEEP}$	V_{VIN} = 13.5 V, V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V	—	—	10	µA
PWM Switching Frequency and Dithering						
Switching Frequency	f_{OSC}	R_{FSET} = 8.66 kΩ	1.8	2.0	2.2	MHz
		R_{FSET} = 20.5 kΩ [2]	—	1.0	—	
		R_{FSET} = 57.6 kΩ [2]	343	400	457	kHz
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	—	±12	—	%
Dither/Slew START Threshold	$VIN_{DS,ON}$		8.5	9.0	9.5	V
Dither/Slew STOP Threshold	$VIN_{DS,OFF}$		7.8	8.3	8.8	V
VIN Dithering/Slew Hysteresis			—	700	—	mV
Charge Pump (VCP)						
Output Voltage	V_{VCP}	V_{VCP} – V_{VIN}, V_{VIN} = 13.5 V, V_{VREG} = 5.50 V, I_{VCP} = 6.5 mA, V_{COMP1} = V_{COMP2} = 0 V, V_{ENB} = 3.3 V	4.1	6.6	—	V
		V_{VCP} – V_{VIN}, V_{VIN} = 6.5 V, V_{VREG} = 5.50 V, I_{VCP} = 6.5 mA, V_{COMP1} = V_{COMP2} = 0 V, V_{ENB} = 3.3 V	3.1	3.8	—	
Switching Frequency	$f_{SW,CP}$		—	65	—	kHz
VCC Pin Voltage						
Output Voltage	V_{VCC}	V_{VREG} = 5.35 V	—	4.65	—	V
Thermal Protection						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	155	170	185	ºC
Thermal Shutdown Hysteresis [2]	T_{HYS}		—	20	—	

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

ELECTRICAL CHARACTERISTICS – BUCK AND BUCK-BOOST PRE-REGULATOR SPECIFICATIONS[1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Voltage Specifications						
Buck Output Voltage – Regulating	V_{VREG}	V_{VIN} = 13.5 V, ENB = 1, 0.1 A < I_{VREG} < 1.25 A	5.25	5.35	5.45	V
Pulse Width Modulation (PWM)						
PWM Ramp Offset	$PWM1_{OFFS}$	V_{COMP1} for 0% duty cycle	—	400	—	mV
LX1 Rising Slew Rate Control [2]	$LX1_{RISE}$	V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A, R_{SLEW} = 22.1 k	—	0.9	—	V/ns
		V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A, R_{SLEW} = 249 k	—	0.3	—	
LX1 Falling Slew Rate [2]	$LX1_{FALL}$	V_{VIN} = 13.5 V, 90% to 10%, I_{VREG} = 1 A	—	1.5	—	V/ns
Buck Min. Controllable ON-time	$t_{ON,MIN,BUCK}$		—	195	—	ns
Buck Maximum Duty Cycle	$D_{MAX,BUCK}$	$t_{OFF,BUCK}$ < 50 ns	—	100	—	%
Boost Minimum OFF-time	$t_{ON,MIN,BST}$		—	100	130	ns
Boost Maximum Duty Cycle	$D_{MAX,BST}$	After V_{VIN} > VIN_{START}, V_{VIN} = 3.6 V	—	65	—	%
COMP1 to LX1 Current Gain	gm_{POWER1}		—	4.5	—	A/V
Slope Compensation (2)	S_{E1}	f_{OSC} = 2.0 MHz	1.04	1.48	1.92	A/µs
		f_{OSC} = 400 kHz	0.22	0.33	0.44	
Internal MOSFET						
MOSFET On Resistance	R_{DSon}	V_{VIN} = 13.5 V, T_J = –40°C [2], I_{DS} = 0.1 A	—	50	65	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [3], I_{DS} = 0.1 A	—	75	90	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	—	150	180	mΩ
MOSFET Leakage	$I_{FET,LKG}$	V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX1} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 85°C [3]	—	—	10	µA
		V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX1} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 150°C	—	50	150	µA
Error Amplifier						
Open Loop Voltage Gain	AVOL1		—	60	—	dB
Transconductance	gm_{EA1}	V_{SS1} = 750 mV	550	750	950	µA/V
		V_{SS1} = 500 mV	275	400	525	
Output Current	I_{EA1}		—	±75	—	µA
Maximum Output Voltage	$EA1_{VO(max)}$		1.10	1.45	1.85	V
Minimum Output Voltage	$EA1_{VO(min)}$		—	—	300	mV
COMP1 Pull Down Resistance	R_{COMP1}	HICCUP1 = 1 or FAULT1 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤0.8 V, latched until V_{SS1} < $VSS1_{RST}$	—	1	—	KΩ

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

ELECTRICAL CHARACTERISTICS – BUCK AND BUCK-BOOST PRE-REGULATOR SPECIFICATIONS (continued)[1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Boost MOSFET (LG) Gate Driver						
LG High Output Voltage	$V_{LG,ON}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V	4.6	—	5.5	V
LG Low Output Voltage	$V_{LG,OFF}$	V_{VIN} = 13.5 V, V_{VREG} =5.35 V	—	0.2	0.4	V
LG Source Current [1]	$I_{LG,ON}$	V_{VIN} =6 V, V_{VREG} =5.35 V, V_{LG} = 1 V	—	−300	—	mA
LG Sink Current [1]	$I_{LG,OFF}$	V_{VIN} =13.5 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	—	150	—	mA
Soft Start						
SS1 Offset Voltage	$VSS1_{OFFS}$	V_{SS1} rising due to $ISS1_{SU}$	—	400	—	mV
SS1 Fault/Hiccup Reset Voltage	$VSS1_{RST}$	V_{SS1} falling due to HICCUP1 = 1 or FAULT1 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V	140	200	275	mV
SS1 Startup (Source) Current	$ISS1_{SU}$	V_{SS1} = 100 mV, HICCUP1 = FAULT1 = 0	−10	−20	−30	µA
SS1 Hiccup (Sink) Current	$ISS1_{HIC}$	V_{SS1} = 0.5 V, HICCUP1 = 1	5	10	15	µA
SS1 Delay Time	$t_{SS1,DLY}$	C_{SS1} = 22 nF	—	440	—	µs
SS1 Ramp Time	t_{SS1}	C_{SS1} = 22 nF	—	880	—	µs
SS1 Pull Down Resistance	RPD_{SS1}	FAULT1 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, latched until V_{SS1} < $VSS1_{RST}$	—	3	—	kΩ
SS1 PWM Frequency Foldback	$f_{SW1,SS}$	V_{VREG} < 2.7 V_{TYP} & V_{COMP1} = $EA1_{VO(max)}$	—	f_{OSC}/4	—	—
		V_{VREG} < 2.7 V_{TYP}	—	f_{OSC}/2	—	—
		V_{VREG} > 2.7 V_{TYP}	—	f_{OSC}	—	—
Hiccup Mode						
Hiccup1 OCP PWM Counts	$t_{HIC1,OCP}$	V_{SS1} > $V_{HIC1,EN}$, V_{VREG} < 1.95 V_{TYP}, V_{COMP} = $EA1_{VO(max)}$	—	30	—	PWM cycles
		V_{SS1} > $V_{HIC1,EN}$, V_{VREG} > 1.95 V_{TYP}, V_{COMP} = $EA1_{VO(max)}$	—	120	—	PWM cycles
Current Protections						
Pulse by pulse current limit	$I_{LIM1,ton(min)}$	t_{ON} = $t_{ON(MIN)}$	3.6	4.1	4.6	A
LX1 Short Circuit Current Limit	$I_{LIM,LX1}$	Latched OFF after 1 detection	7.5	10	—	A
Missing Asynchronous Diode (D1) Protection						
Detection Level	$V_{D,OPEN}$		−1.50	−1.30	−0.80	V
Time Filtering [2]	$t_{D,OPEN}$		50	—	250	ns

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

ELECTRICAL CHARACTERISTICS – 1.25 V SYNCHRONOUS BUCK REGULATOR[1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
1V25 Output Voltage						
Output Voltage Accuracy	V_{1V25}	50 mA < I_{1V25} < 750 mA	1.23	1.25	1.27	V
Pulse Width Modulation (PWM)						
PWM Ramp Offset	$PWM2_{OFFS}$	V_{COMP2} for 0% duty cycle	–	350	–	mV
High-Side MOSFET Minimum ON-Time	$t_{ON(MIN)}$		–	65	105	ns
High-Side MOSFET Minimum OFF-Time	$t_{OFF(MIN)}$	Does not include total gate driver non-overlap time, t_{NO}	–	100	130	ns
Gate Driver Non-Overlap Time [2]	t_{NO}		–	15	–	ns
COMP2 to LX2 Current gain	gm_{POWER2}		–	2.5	–	A/V
Slope Compensation [2]	S_{E2}	f_{OSC} = 2.0 MHz	0.45	0.63	0.81	A/µs
		f_{OSC} = 400 kHz	0.12	0.14	0.19	
Internal MOSFETs						
High-Side MOSFET ON Resistance	$RDS_{ON\ (HS)}$	T_A = 25°C [3], I_{DS} = 100 mA	–	200	235	mΩ
		I_{DS} = 100 mA	–	–	400	mΩ
LX2 Node Rise/Fall Time [2]	$t_{R/F,LX2}$	V_{VREG} = 5.5 V	–	12	–	ns
High-Side MOSFET Leakage [1]	$I_{DSS\ (HS)}$	V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX2} = 0 V, V_{VREG} = 5.5 V, –40˚C < T_J < 85˚C [3]	–	–	2	µA
		V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX2} = 0 V, V_{VREG} = 5.5 V, −40°C < T_J < 150°C	–	3	15	µA
Low-Side MOSFET ON Resistance	$RDS_{ON\ (LS)}$	T_A = 25°C [3], I_{DS} = 100 mA	–	55	65	mΩ
		I_{DS} = 100 mA	–	–	110	mΩ
Low-Side MOSFET Leakage [1]	$I_{DSS\ (LS)}$	V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX2} = 5.5 V, –40˚C < T_J < 85˚C [3]	–	–	1	µA
		V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, V_{LX2} = 5.5 V, −40°C < T_J < 150°C	–	8	20	µA

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

ELECTRICAL CHARACTERISTICS – 1.25 V SYNCHRONOUS BUCK REGULATOR (continued)[1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
1V25 Output Voltage						
Open Loop Voltage Gain [2]	AVOL2		–	60	–	dB
Transconductance	gm_{EA2}	I_{COMP2} = 0 µA, V_{SS2} > 500 mV	550	750	950	µA/V
		0 V < V_{SS2} < 500 mV	–	250	–	µA/V
Source & Sink Current	I_{EA2}	V_{COMP2} = 1.5 V	–	±50	–	µA
Maximum Output Voltage	$EA2_{VO(max)}$		1.00	1.25	1.50	V
Minimum Output Voltage	$EA2_{VO(min)}$		–	–	150	mV
COMP2 Pull Down Resistance	R_{COMP2}	HICCUP2 = 1 or FAULT2 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, latched until V_{SS2} < $VSS2_{RST}$	–	1.5	–	kΩ
Soft Start						
SS2 Offset Voltage	$VSS2_{OFFS}$	V_{SS2} rising due to $ISS2_{SU}$	120	200	270	mV
SS2 Fault/Hiccup Reset Voltage	$VSS2_{RST}$	V_{SS2} falling due to HICCUP2 = 1 or FAULT2 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V	–	100	120	mV
SS2 Startup (Source) Current	$ISS2_{SU}$	V_{SS2} = 1 V, HICCUP2 = FAULT2 = 0	−10	–20	−30	µA
SS2 Hiccup (Sink) Current	$ISS2_{HIC}$	V_{SS2} = 0.5 V, HICCUP2 = 1	5	10	20	µA
SS2 to V_{1V2} Delay Time	$t_{SS2,DLY}$	C_{SS2} = 10 nF	–	100	–	µs
V_{1V2} Soft Start Ramp Time	t_{SS2}	C_{SS2} = 10 nF	–	400	–	µs
SS2 Pull Down Resistance	RPD_{SS2}	FAULT2 = 1 or V_{ENBATx} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, latched until V_{SS2} < $VSS2_{RST}$	–	2	–	kΩ
SS2 PWM Frequency Foldback	$f_{SW2,SS}$	V_{1V25} < 315 mV_{TYP}	–	f_{OSC}/4	–	–
		315 mV_{TYP} < V_{1V25} < 740 mV_{TYP}	–	f_{OSC}/2	–	–
		V_{1V25} > 740 mV_{TYP}	–	f_{OSC}	–	–
Hiccup Mode						
Hiccup2 OCP Enable Threshold	$V_{HIC2,EN}$	V_{SS2} rising	–	1.2	–	V
Hiccup2 OCP Counts	$t_{HIC2,OCP}$	V_{SS2} > $V_{HIC2,EN}$, V_{1V25} < 315 mV_{TYP}	–	30	–	PWM cycles
		V_{SS2} > $V_{HIC2,EN}$, V_{1V25} > 315 mV_{TYP}	–	120	–	PWM cycles
Current Protections						
Pulse-by-Pulse Current Limit	$I_{LIM2,ton(min)}$	t_{ON} = $t_{ON(MIN)}$	1.8	2.1	2.4	A

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

ELECTRICAL CHARACTERISTICS – LINEAR REGULATOR (LDO) SPECIFICATIONS [1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V5 and V5P Linear Regulators						
V5 Accuracy & Load Regulation	V_{V5}	10 mA < I_{V5} < 155 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5 Output Capacitance Range [2]	$C_{OUT,V5}$		1.0	–	22	µF
V5P Accuracy & Load Regulation	V_{V5P}	10 mA < I_{V5P} < 255 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5P Output Capacitance [2]	$C_{OUT,V5P}$		1.6	2.2	4.1	µF
V5 and V5P Minimum Output Voltage[2]	$V_{V5x,MIN1}$	V_{VCP} = 9 V, TRACK = 1, I_{V5} = 25 mA, I_{V5P} = 80 mA, I_{3V3} = 150 mA, I_{1V25} = 700 mA (192 mA to V_{REG}) 1) T_A = 150ºC, V_{VIN} = 5.12 V, V_{VREG} = 5.01 V 2) T_A = –40ºC [2], V_{VIN} = 5.12 V, V_{VREG} = 5.06 V	4.85	–	–	V
	$V_{V5x,MIN2}$	V_{VCP} = 8.5 V, TRACK = 1, I_{V5} = 25 mA, I_{V5P} = 80 mA, I_{3V3} = 150 mA, I_{1V25} = 700 mA (213 mA to V_{REG}) 1) T_A = 150ºC, V_{VIN} = 4.50 V, V_{VREG} = 4.39 V 2) T_A = –40ºC [2], V_{VIN} = 4.50 V, V_{VREG} = 4.44 V	4.25	–	–	
V5P Tracking						
V5P/3V3 Tracking Ratio		V_{V5P} ÷ V_{3V3}	1.505	1.515	1.525	–
V5P/3V3 Tracking Accuracy	$TRACK_{3V3}$	3.0 V < V_{3V3} < 3.3 V, TRACK = 1, I_{3V3} = I_{V5P} = 75 mA	−0.66	–	+0.66	%
V5P/V5 Tracking Accuracy	$TRACK_{V5}$	3.5 V < V_{V5} < 5.0 V, TRACK = 0, I_{V5P} = I_{V5} = 75 mA	−35	–	+35	mV
V5P Over Current Protection						
V5P Current Limit [1]	$V5P_{ILIM}$	V_{V5P} = 5 V	−285	−400	–	mA
V5P Foldback Current [1]	$V5P_{IFBK}$	V_{V5P} = 0 V	−60	−115	−170	mA
V5 Over Current Protection						
V5 Current Limit [1]	$V5_{ILIM}$	V_{V5} = 5 V	−175	−245	–	mA
V5 Foldback Current [1]	$V5_{IFBK}$	V_{V5} = 0 V	−35	−70	−105	mA
V5P & V5 Startup Timing						
V5P Startup Time [2]		C_{V5P} ≤ 2.9 µF, Load = 25 Ω ±5% (200 mA)	–	0.17	0.60	ms
V5 Startup Time [2]		C_{V5} ≤ 2.9 µF, Load = 33 Ω ±5% (150 mA)	–	0.24	1.0	ms

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

ELECTRICAL CHARACTERISTICS – CONTROL INPUTS [1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
3V3 Linear Regulator						
3V3 Accuracy & Load Regulation	V_{3V3}	10 mA < I_{3V3} < 165 mA, V_{VREG} = 5.25 V	3.23	3.30	3.37	V
3V3 Output Capacitance Range [2]	$C_{OUT,3V3}$		1.0	–	22	µF
3V3 Minimum Output Voltage [2]	$V_{3V3,MIN1}$	V_{VCP} = 9 V, TRACK = 1, I_{V5} = 25 mA, I_{V5P} = 80 mA, I_{3V3} = 150 mA, I_{1V25} = 700 mA (192 mA to VREG) 1) T_A = 150ºC, V_{VIN} = 5.12 V, V_{VREG} = 5.01 V 2) T_A = –40ºC [2], V_{VIN} = 5.12 V, V_{VREG} = 5.06 V	3.23	3.30	–	V
	$V_{3V3,MIN2}$	V_{VCP} = 8.5 V, TRACK = 1, I_{V5} = 25 mA, I_{V5P} = 80 mA, I_{3V3} = 150 mA, I_{1V25} = 700 mA (213 mA to VREG) 1) T_A = 150ºC, V_{VIN} = 4.50 V, V_{VREG} = 4.39 V 2) T_A = –40ºC [2], V_{VIN} = 4.50 V, V_{VREG} = 4.44 V	3.15	3.30	–	
3V3 Over Current Protection						
3V3 Current Limit [1]	$3V3_{ILIM}$	V_{3V3} = 3.3 V	−185	−260	–	mA
3V3 Foldback Current [1]	$3V3_{IFBK}$	V_{3V3} = 0 V	−40	−75	−130	mA
3V3 Startup Timing						
3V3 Startup Time [2]		C_{3V3} ≤ 2.9 µF, Load = 33 Ω ±5% (100 mA)	–	0.17	0.55	ms
Ignition Enable (ENBAT1 and ENBAT2) Inputs						
ENBAT1, ENBAT2 Thresholds	$V_{ENBATx,H}$	V_{ENBATx} rising	2.9	3.3	3.5	V
	$V_{ENBATx,L}$	V_{ENBATx} falling	2.2	2.6	2.9	V
ENBAT1, ENBAT2 Hysteresis	$V_{ENBATx,HYS}$	$V_{ENBATx,H}$ – $V_{ENBATx,L}$	–	700	–	mV
ENBAT1, ENBAT2 Bias Current [1]	$I_{ENBATx,BIAS}$	T_J = 25°C [3], V_{ENBATx} = 3.51 V	–	28	45	µA
		T_J = 150°C, V_{ENBATx} = 3.51 V	–	35	55	
ENBAT1, ENBAT2 Pull-Down Resistance	R_{ENBATx}	V_{ENBATx} < 1.2 V	–	650	–	kΩ
Logic Enable (ENB) Input						
ENB Thresholds	$V_{ENB,H}$	V_{ENB} rising	–	–	2.0	V
	$V_{ENB,L}$	V_{ENB} falling	0.8	–	–	V
ENB Bias Current [1]	$I_{ENB,IN}$	V_{ENB} = 3.3 V	–	–	175	µA
ENB Resistance	R_{ENB}		–	60	–	kΩ
ENB/ENBATx Filter/Deglitch						
Enable Filter/Deglitch Time	$EN_{td,FILT}$		10	15	20	µs
ENB/ENBATx Shutdown Delay						
LDO Shutdown Delay	$td_{LDO,OFF}$	Measure $td_{LDO,OFF}$ from the falling edge of ENB and ENBAT1 and ENBAT2 to the time when all LDOs begin to decay	15	50	100	µs

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

ELECTRICAL CHARACTERISTICS – CONTROL INPUTS (continued) [1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
TRACK Input						
TRACK Thresholds	VT_H	V_{TRACK} rising	–	–	2.0	V
	VT_L	V_{TRACK} falling	0.8	–	–	V
TRACK Bias Current [1]	IB_T		–	−100	–	µA
FSET/SYNC Input						
FSET/SYNC Pin Voltage	$V_{FSET/SYNC}$	No external SYNC signal	–	800	–	mV
FSET/SYNC Open Circuit (Under Current) Detection Time	$V_{FSET/SYNC,UC}$	PWM switching disabled upon detection	–	3	–	µs
FSET/SYNC Short Circuit (Over Current) Detection Time	$V_{FSET/SYNC,OC}$	PWM switching disabled upon detection	–	3	–	µs
Sync. High Threshold	$SYNC_{VIH}$	V_{SYNC} rising	–	–	2.0	V
Sync. Low Threshold	$SYNC_{VIL}$	V_{SYNC} falling	0.5	–	–	V
Sync. Input Duty Cycle	DC_{SYNC}		–	–	80	%
Sync. Input Pulse Width	tw_{SYNC}		200	–	–	ns
Sync. Input Transition Times [2]	tt_{SYNC}		–	10	15	ns
SLEW Input						
SLEW Pin Operating Voltage	V_{SLEW}		–	800	–	mV
SLEW Pin Open Circuit (Under Current) Detection Time	$V_{SLEW,UC}$	PWM latched off upon detection	–	3	–	µs
SLEW Pin Short Circuit (Over Current) Detection Time	$V_{SLEW,OC}$	PWM latched off upon detection	–	3	–	µs
SLEW Bias Current [1]	I_{SLEW}		–	−100	–	nA

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS [1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR OV/UV Protection Thresholds						
3V3 OV Thresholds	$V_{3V3,OV,H}$	V_{3V3} rising	3.41	3.51	3.60	V
	$V_{3V3,OV,L}$	V_{3V3} falling	–	3.49	–	
3V3 OV Hysteresis	$V_{3V3,OV,HYS}$	$V_{3V3,OV,H}$ – $V_{3V3,OV,L}$	10	20	40	mV
3V3 UV Thresholds	$V_{3V3,UV,H}$	V_{3V3} rising	–	3.12	–	V
	$V_{3V3,UV,L}$	V_{3V3} falling	3.00	3.10	3.19	
3V3 UV Hysteresis	$V_{3V3,UV,HYS}$	$V_{3V3,UV,H}$ – $V_{3V3,UV,L}$	10	20	40	mV
1V25 OV Thresholds	$V_{1V25,OV,H}$	V_{1V25} rising	1.29	1.32	1.35	V
	$V_{1V25,OV,L}$	V_{1V25} falling	–	1.31	–	
1V25 OV Hysteresis	$V_{3V3,OV,HYS}$	$V_{1V25,OV,H}$ – $V_{1V25,OV,L}$	5	10	20	mV
1V25 UV Thresholds	$V_{1V25,UV,H}$	V_{1V25} rising, triggers turn on of LDOs	–	1.19	–	V
	$V_{1V25,UV,L}$	V_{1V25} falling	1.15	1.18	1.21	
1V25 UV Hysteresis	$V_{3V3,UV,HYS}$	$V_{1V25,UV,H}$ – $V_{1V25,UV,L}$	5	10	20	mV
NPOR Turn-on and Turn-off Delays						
NPOR Turn-on Delay	$td_{NPOR,ON}$		12	15	18	ms
NPOR Turn-off Propagation Delay	$td_{NPOR,OFF}$	ENB and ENBAT1 and ENBAT2 low to NPOR low	–	15	23	µs
NPOR Output Voltages						
NPOR Output Low Voltage	$V_{NPOR,L}$	ENB or ENBAT1 or ENBAT2 high, VIN ≥ 2.5 V, I_{NPOR} = 4 mA	–	150	400	mV
		ENB or ENBAT1 or ENBAT2 high, VIN = 1.5 V, I_{NPOR} = 2 mA	–	–	800	
NPOR Leakage Current [1]	$I_{NPOR,LKG}$	V_{NPOR} = 3.3 V	–	–	2	µA
NPOR and POK5V OV Delay Time						
Over Voltage Detection Delay	td_{OV}	V5P, V5, 3V3, and 1V25 over voltage detection delay time, WD_{ENn} = 0	6.40	8.00	9.60	ms
NPOR and POK5V UV Filtering/Deglitch						
UV Filter/Deglitch Times	td_{FILT}	Applies to under-voltage of the 3V3, 1V25, V5, and V5P voltages	10	15	20	µs

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS (continued) [1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POK5V OV/UV Protection Thresholds						
V5 OV Thresholds	$V_{V5,OV,H}$	V_{V5} rising	5.15	5.33	5.50	V
	$V_{V5,OV,L}$	V_{V5} falling	–	5.30	–	
V5 OV Hysteresis	$V_{V5,OV,HYS}$	$V_{V5,OV,H}$ – $V_{V5,OV,L}$	15	30	50	mV
V5 UV Thresholds	$V_{V5,UV,H}$	V_{V5} rising	–	4.71	–	V
	$V_{V5,UV,L}$	V_{V5} falling	4.50	4.68	4.85	
V5 UV Hysteresis	$V_{V5,UV,HYS}$	$V_{V5,UV,H}$ – $V_{V5,UV,L}$	15	30	50	mV
V5P Output Disconnect Threshold	$V_{V5P,DISC}$	V_{V5P} rising	–	7.2	–	V
V5P OV Thresholds	$V_{V5P,OV,H}$	V_{V5P} rising	5.15	5.33	5.50	V
	$V_{V5P,OV,L}$	V_{V5P} falling	–	5.30	–	
V5P OV Hysteresis	$V_{V5P,OV,HYS}$	$V_{V5P,OV,H}$ – $V_{V5P,OV,L}$	15	30	50	mV
V5P UV Thresholds	$V_{V5P,UV,H}$	V_{V5P} rising	–	4.71	–	V
	$V_{VP5,UV,L}$	V_{V5P} falling	4.50	4.68	4.85	
V5P UV Hysteresis	$V_{V5P,UV,HYS}$	$V_{V5P,UV,H}$ – $V_{V5P,UV,L}$	15	30	50	mV
POK5V Output Voltages						
POK5V Output Voltage	$V_{POK5V,L}$	ENB = 1 or ENBAT1 = 1 or ENBAT2 = 1, V_{VIN} ≥ 2.5 V, I_{POK5V} = 4 mA	–	150	400	mV
		ENB = 1 or ENBAT1 = 1, ENBAT2 = 1, V_{VIN} = 1.5 V, I_{POK5V} = 2 mA	–	–	800	
POK5V Leakage Current	$I_{POK5V,LKG}$	V_{POK5V} = 3.3 V	–	–	2	µA
VREG, VCP, and BG Thresholds						
VREG OV Thresholds	$VREG_{OV,H}$	V_{VREG} rising, LX1 PWM disabled	5.70	5.95	6.20	V
	$VREG_{OV,L}$	V_{VREG} falling, LX1 PWM enabled	–	5.85	–	
VREG OV Hysteresis	$VREG_{OV,HYS}$	$V_{REGOV,H}$ – $V_{REGOV,L}$	–	100	–	mV
VREG UV Thresholds	$VREG_{UV,H}$	V_{VREG} rising, triggers rise of SS2	4.14	4.38	4.62	V
	$VREG_{UV,L}$	V_{VREG} falling	–	4.28	–	
VREG UV Hysteresis	$VREG_{UV,HYS}$	$V_{REGUV,H}$ – $V_{REGUV,L}$	–	100	–	mV
VCP OV Thresholds	$VCP_{OV,H}$	V_{VCP} rising, latches all regulators off	11.0	12.5	14.0	V
VCP UV Thresholds	$VCP_{UV,H}$	V_{VCP} rising, PWM enabled	2.95	3.15	3.35	V
	$VCP_{UV,L}$	V_{VCP} falling, PWM disabled	–	2.8	–	
VCP UV Hysteresis	$VCP_{UV,HYS}$	$V_{CPUV,H}$ – $V_{CPUV,L}$	–	350	–	mV
BGREF & BGFAULT UV Thresholds [2]	BGx_{UV}	BG_{VREF} or BG_{FAULT} rising	1.00	1.05	1.10	V
Ignition Status (ENBAT1S and ENBAT2S)						
ENBATxS Thresholds	$V_{ENBATxS,H}$	V_{ENBATx} rising	2.9	3.3	3.5	V
	$V_{ENBATxS,L}$	V_{ENBATx} falling	2.2	2.6	2.9	V
ENBATxS Output Voltage	$VO_{ENBATxS,LO}$	I_{ENBATS} = 4 mA	–	–	400	mV
ENBATxS Leakage Current (1)	$I_{ENBATxS}$	V_{ENBATS} = 3.3 V	–	–	1	µA

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

ELECTRICAL CHARACTERISTICS – WINDOW WATCHDOG TIMER (WWDT) [1]: valid at 3.6 V [4] < V_{IN} < 36 V, –40ºC < T_A = T_J < 150ºC, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
WD Enable\ Input (WDENn)						
WD_{ENn} Voltage Thresholds	$WD_{ENn,LO}$	V_{WDENn} falling, WDT enabled	0.8	–	–	V
	$WD_{ENn,HI}$	V_{WDENn} rising, WDT disabled	–	–	2.0	V
WD_{ENn} Input Resistance	$R_{WD,ENn}$		–	60	–	kΩ
WD_{IN} Voltage Thresholds & Current						
WD_{IN} Input Voltage Thresholds	$WD_{IN,LO}$	$V_{WD,IN}$ falling, WD_{ADJ} pulled low by R_{ADJ}	0.8	–	–	V
	$WD_{IN,HI}$	$V_{WD,IN}$ rising, WD_{ADJ} charging	–	–	2.0	V
WD_{IN} Input Current [1]	$WD_{I,IN}$	$V_{WD,IN}$ = 5 V	−10	±1	10	µA
WD_{IN} Timing Specifications						
WD_{IN} Frequency	$WD_{IN,FREQ}$		–	–	750	Hz
WD_{IN} Duty Cycle	$WD_{IN,DUTY}$		20	50	80	%
Watchdog Activation Delay	$WD_{START,DLY}$		24	30	36	ms
WD Programming (WD_{ADJ})						
WD Timeout FAST Range [2]			1.0	–	25	ms
WD Timeout SLOW Range [2]	—		4.0	–	100	ms
WD Timeout, FAST Clock	$WD_{TO,FAST}$	R_{ADJ} = 13 kΩ	0.8	1.0	1.2	ms
		R_{ADJ} = 324 kΩ	20	25	30	
WD Timeout, SLOW Clock	$WD_{TO,SLOW}$	R_{ADJ} = 13 kΩ	3.2	4.0	4.8	ms
		R_{ADJ} = 324 kΩ	80	100	120	
WD One-Shot Time						
WD Pulse Time after a WD Fault	$t_{WD,FAULT}$		1.6	2.0	2.4	ms

[1] Negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN,START}$ and V_{VCP} – V_{VIN} > $VCP_{UV,H}$ and V_{VREG} > $VREG_{UV,H}$ are satisfied before VIN is reduced.

FUNCTIONAL DESCRIPTION

Overview

The A4410 is a power management IC designed for automotive applications. It contains a pre-regulator plus four DC post regulators to create the voltages necessary for typical automotive applications such as electrical power steering and automatic transmission control.

The pre-regulator can be configured as a buck or buck boost regulator. Buck boost is required for applications that need to work with extremely low battery voltages. This pre-regulator generates a fixed 5.35 V and can deliver up to 1.2 A to power the internal or external post-regulators. These post-regulators generate the various voltage levels for the end system.

The A4410 includes four internal post regulators; three linear regulators and one fixed output synchronous buck regulator.

Buck-Boost Pre-Regulator (VREG)

The pre-regulator incorporates an internal high side buck switch and a boost switch gate driver. An external freewheeling diode and LC filter are required to complete the buck converter. By adding a MOSFET and boost diode the boost functionality can maintain all outputs with input voltages down to 2.8 V. The A4410 includes a compensation pin (COMP1) and a soft-start pin (SS1) for the pre-regulator.

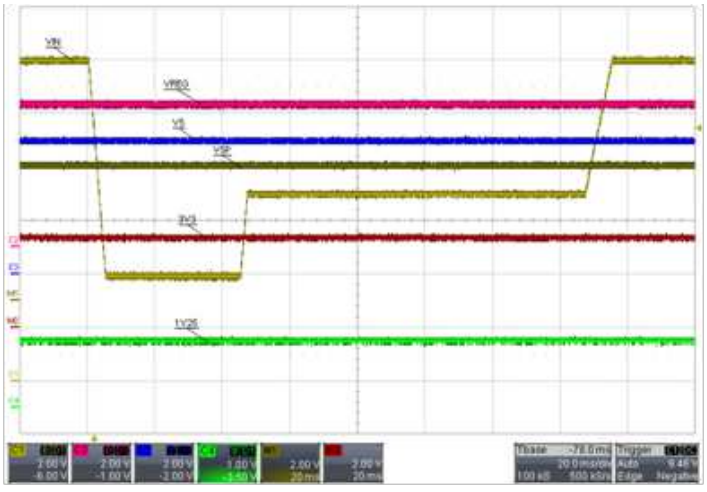


Figure 1: Performance for Representative VIN Start/Stop Transients

VIN_{TYP} = 12 V, VIN_{MIN} = 4 V, 20 ms/DIV

The pre-regulator provides protection and diagnostic functions.

1. Over voltage protection
2. High voltage rating for load dump
3. Switch node to ground short circuit protection
4. Open freewheeling diode protection
5. Pulse-by-pulse current limit
6. Hiccup mode short circuit protection (shown below)

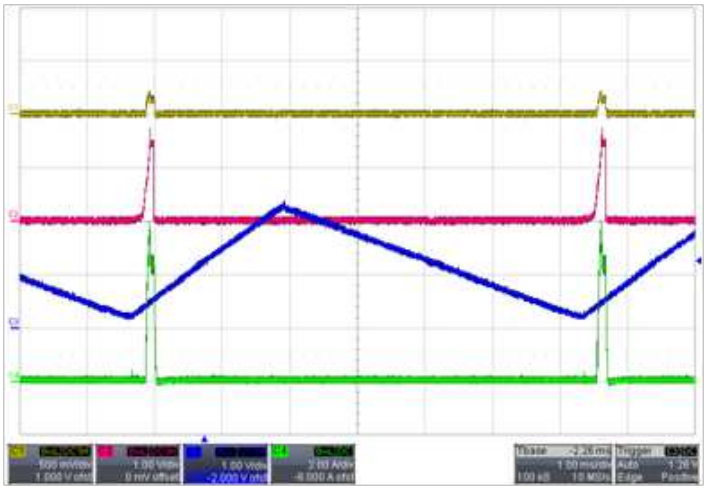


Figure 2: Pre-regulator Hiccup Mode when VREG is Shorted to GND

CH1 = VREG, CH2 = COMP1, CH3 = SS1, CH4 = I_{L1}, 1 ms/DIV

Synchronous Buck Regulator (1V25)

The A4410 integrates the high-side and low-side MOSFETs necessary for implementing a 1.25 V/750 mA_{DC}/1 A_{PEAK} synchronous buck regulator. The synchronous buck is powered by the 5.35 V pre-regulator output. An LC filter is required to complete the synchronous buck regulator. The A4410 includes a compensation pin (COMP2) and a soft-start pin (SS2) for the synchronous buck.

Protection and safety functions provided by the synchronous buck are:

1. Under voltage detection
2. Over voltage detection
3. Switch node to ground short circuit protection
4. Pulse-by-pulse current limit
5. Hiccup mode short circuit protection (shown below)

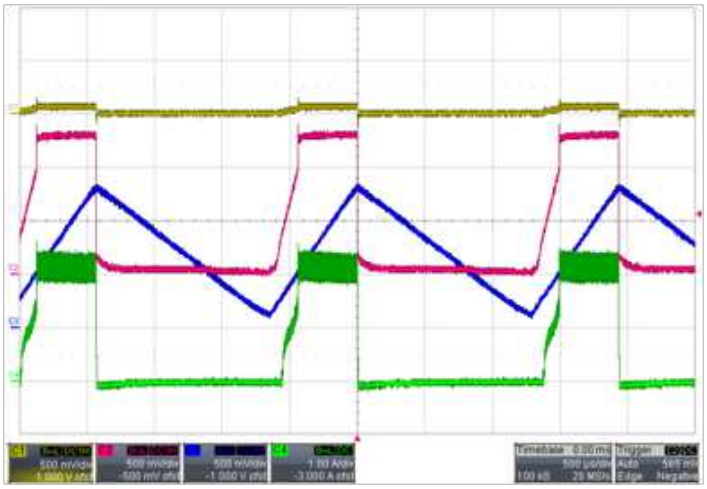


Figure 3: Synchronous Buck Hiccup Mode when V_{OUT} is Shorted to GND

CH1=V_{OUT}, CH2=COMP1, CH3=SS1, CH4=IL1, 500 µs/DIV

Low Dropout Linear Regulators (LDOs)

The A4410 has three low dropout linear regulators (LDOs), one 3.3 V/160 mA_{MAX} (3V3), one 5 V/150 mA_{MAX} (V5), and one high-voltage protected 5 V/250 mA_{MAX} (V5P). The switching pre-regulator efficiently regulates the battery voltage to an intermediate value to power the LDOs. This pre-regulator topology reduces LDO power dissipation and junction temperature.

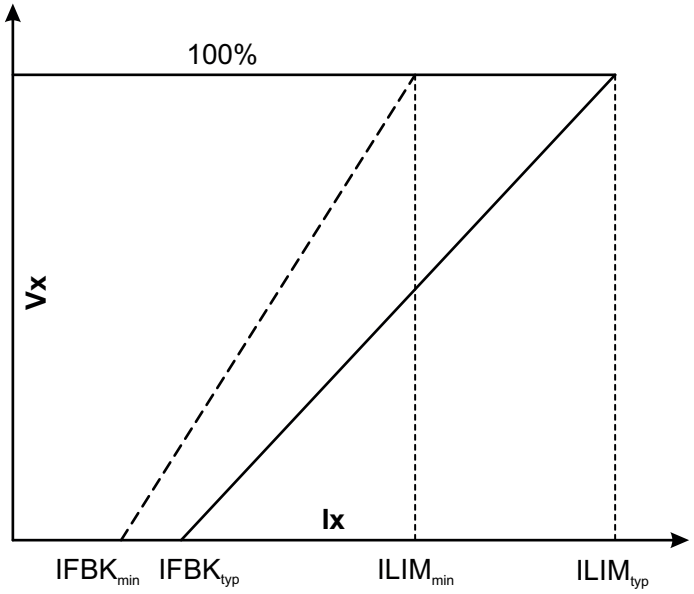


Figure 4: LDO Foldback Protection

All linear regulators provide the following protection features;

1. Under voltage and over voltage detection
2. Current limit with fold back short circuit protection

The protected 5 V regulator (V5P) includes protection against accidental short circuit to the battery voltage. This makes this output most suitable for powering remote sensors or circuitry via a wiring harness where short to battery is possible.

Tracking Input (TRACK)

The V5P LDO is a tracking regulator. It can be set to use either V5 or 3V3 as its reference by setting the TRACK input pin to a logic low or high. If the TRACK input is left unconnected an internal current source will set the TRACK pin to a logic high.

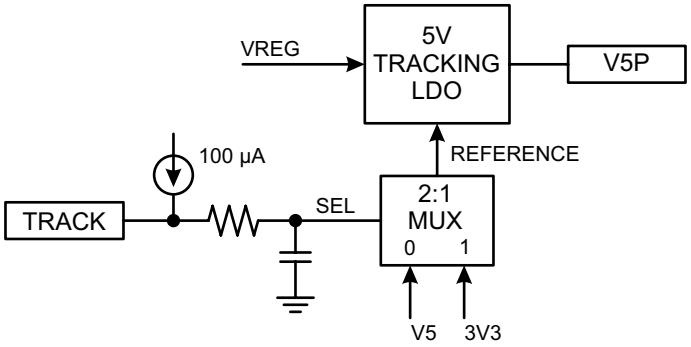


Figure 5: TRACK Input Circuit

Window Watchdog Timer (WDT)

The A4410s window watchdog circuit monitors an external clock applied to the WD_{IN} pin. This clock should be generated by the micro-controller or DSP. The time between rising edges of the clock must fall within an acceptable "window" or a watchdog fault is generated. A watchdog fault will set NPOR for $t_{WD,FAULT}$ (typically 2 ms). A watchdog fault will occur if the time between rising edges is either too short (a FAST fault) or too long (a SLOW fault).

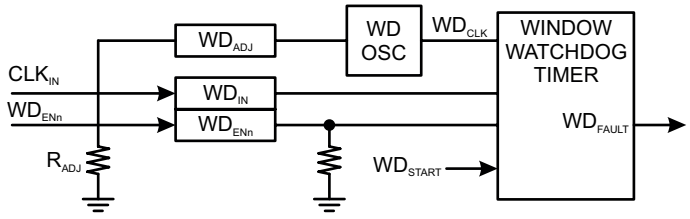


Figure 6: Window Watchdog Timer

The watchdogs time "window" is programmable via the WD_{ADJ} pin according to the following equations:

$$R_{ADJ} = 3.240 * WD_{TO,SLOW}$$

$$WD_{TO,FAST} = WD_{TO,SLOW} / 4$$

Where $WD_{TO,SLOW}$ is the nominal watchdog timeout (in ms) and R_{ADJ} is the required external resistor value (in kΩ) from the WD_{ADJ} pin to ground. Typical watchdog operation and FAST and SLOW fault conditions are shown in Figures 13a and 13b.

The watchdog is enabled if two conditions are met: (1) the WD_{ENn} pin is a logic low and (2) all the regulators (1V25, 3V3, V5, and V5P) have been above their under voltage thresholds for at least 30 ms_{TYP} ($WD_{START,DLY}$).

After startup, if no clock edges are detected at WD_{IN} for at least $WD_{START,DLY}$ + $WD_{TO,SLOW}$ the A4410 will set NPOR low for $t_{WD,FAULT}$ and reset its counters. This process will repeat until the system recovers and clock edges are applied to WD_{IN}. A timing diagram for the "missing clock" situation is shown in Figure 13c.

Dual Band Gaps (BG_{VREF}, BG_{FAULT})

Dual band gaps, or references, are implemented within the A4410. One band gap (BG_{VREF}) is dedicated solely to closed loop control of the output voltages. The second band gap (BG_{FAULT}) is employed for fault monitoring functions. Having redundant band gaps improves reliability of the A4410.

If the reference band gap is out of specification (BG_{VREF}) then the output voltages will be out of specification and the monitoring band gap will report a fault condition by setting NPOR and/or POK5V low.

If the monitoring band gap is out of specification (BG_{FAULT}) then the outputs will remain in regulation but the monitoring circuits will report a fault condition by setting NPOR and/or POK5V low.

The reference and monitoring band gap circuits include two, smaller secondary band gaps that are used to detect under voltage of the main band gaps during power-up.

Adjustable Frequency and Synchronization (FSET/SYNC)

The PWM switching frequency of the A4410 is adjustable from 250 kHz to 2.4 MHz. Connecting a resistor from the FSET/SYNC pin to ground sets the switching frequency. An FSET resistor with ±1% tolerance is recommended. The FSET resistor can be calculated using the following equation:

$$R_{FSET} = \left(\frac{f_{OSC}}{12724}\right)^{-1.175}$$

Where RFSET is in kΩ and f_{OSC} is the desired oscillator (PWM) frequency in kHz.

A graph of switching frequency versus FSET resistor values is shown below.

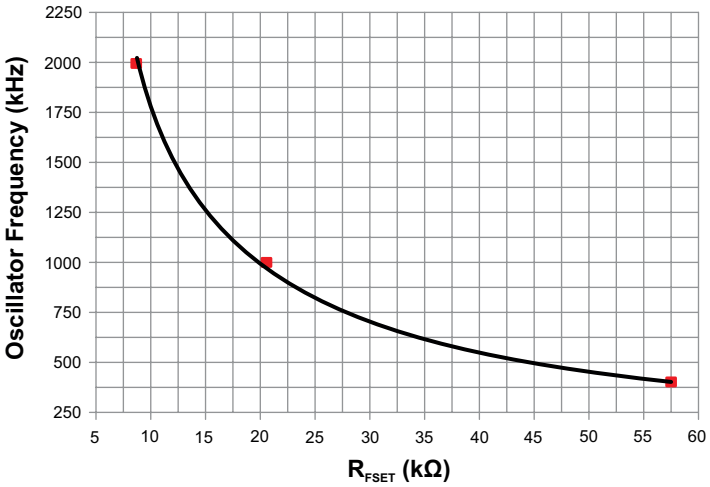


Figure 7: Switching Frequency vs. FSET Resistor Values

The PWM frequency of the A4410 may be increased or decreased by applying a clock to the FSET/SYNC pin. The clock must satisfy the voltage thresholds and timing requirements shown in the electrical characteristics table.

Frequency Dithering and LX1 Slew Rate Control

The A4410 includes two innovative techniques to help reduce EMI/EMC for demanding automotive applications.

First, the A4410 performs pseudo-random dithering of the PWM frequency. Dithering the PWM frequency spreads the energy above and below the base frequency set by R_{FSET}. A typical fixed-frequency PWM regulator will create distinct "spikes" of energy at f_{OSC}, and at higher frequency multiples of f_{OSC}. Conversely, the A4410 spreads the spectrum around f_{OSC} thus creating a lower magnitude at any comparative frequency. Frequency dithering is disabled if SYNC is used or VIN drops below approximately 8.3 V.

Second, the A4410 includes a pin to adjust the turn on slew rate of the LX1 pin by simply changing the value of the resistor from the SLEW pin to ground. Slower rise times of LX1 reduce ringing and high frequency harmonics of the regulator. The rise time may be adjusted to be quite long and will increase thermal dissipation of the pre-regulator if set too slow. Typical values of rise time versus R_{SLEW} are

Table 1: R_{SLEW} vs. Rise Time

R_{SLEW} (kΩ)	LX1 Rise Time (ns)
8.66	7
44.2	11
100	20

Enable Inputs (ENB, ENBAT1, ENBAT2)

Three enable pins are available on the A4410. A high signal on any of these pins enables the A4410. One enable (ENB) is logic level compatible for micro-controller control. The other inputs (ENBAT1 and ENBAT2) must be connected to the ignition (IGN) or accessory (ACC) switch through a relatively low value series resistance, 2 kΩ – 3.6 kΩ. For transient suppression it is recommended that a 0.1 µF – 0.22 µF capacitor be placed after the series resistance to form a low pass filter for the ENBAT1 and ENBAT2 pins as shown in the Applications Schematic.

Bias Supply (VCC)

The bias supply (VCC) is generated by an internal linear regulator. This supply is the first rail to start up. Most of the internal control circuitry is powered by this supply. The bias supply includes some unique features to ensure reliable operation of the A4410. These features include;

1. Input voltage (VIN) under voltage lockout
2. Under voltage detection
3. Short-to-ground protection
4. Operation from either VIN or VREG for low battery voltage operation

Charge Pump (VCP, CP1, CP2)

A charge pump provides the voltage necessary to drive the high-side n-channel MOSFETs in the pre-regulator and the linear regulators.

Two external capacitors are required for charge pump operation. During the first half of the charge pump cycle, the flying capacitor between pins CP1 and CP2, is charged from either VIN or VREG, whichever is highest. During the second half of the charge pump cycle the voltage on the flying capacitor charges the VCP capacitor. For most conditions the VCP minus VIN voltage is regulated to approximately 6.5 V.

The charge pump can provide enough current to operate the pre-regulator and the LDOs at full load provided VIN is greater than 6.0 V. Optional components D3, D4, and CP3 must be included if VIN drops below 6.0 V. Diode D3 should be a silicon diode rated for at least 200 mA/50 V with less than 50 µA of leakage current when V_R = 13 V and T_A = 125ºC. Diode D4 should be a 1 A schottky diode with a very low forward voltage (V_F) rated to withstand at least 30 V.

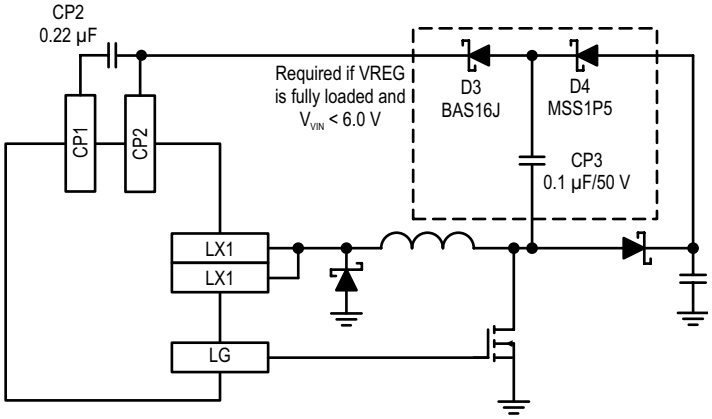


Figure 8: Charge Pump Circuit

The charge pump incorporates some protection features;

1. Under voltage lockout of PWM switching
2. Over voltage "latched" shutdown of the A4410

Startup and Shutdown Sequences

The startup and shutdown sequences of the A4410 are fixed. If no faults exist and ENBAT1 or ENBAT2 or ENB transition high the A4410 will perform its startup routine. If ENBAT1 and ENBAT2 and ENB are low for at least $EN_{td,FILT} + td_{LDO, OFF}$ (typically 65 µs) the A4410 will enter a shutdown sequence. The startup and shutdown sequences are summarized in Table 2 and shown in a timing diagram in Figure 9.

Fault Reporting (NPOR, POK5V)

The A4410 includes two open-drain outputs for error reporting. The NPOR pin monitors the 1V25 and 3V3 outputs for under and over voltage. The POK5V pin monitors the V5 and V5P pin for under and over voltage.

The NPOR pin incorporates a 15 ms delay after both the 1V25

and 3V3 outputs have risen above their under voltage thresholds. This relatively long delay allows the micro-controller plenty of time to power-up and complete its initialization. There is virtually no NPOR delay if either the 1V25 or 3V3 falls below the under voltage threshold. The NPOR pin incorporates an 8 ms delay if either of the 1V25 or 3V3 outputs exceeds its over voltage threshold.

There are no significant delays on the POK5V output after V5 and V5P have risen above or fallen below their under voltage thresholds. Similar to the NPOR pin, the POK5V pin incorporates an 8 ms delay if either the V5 or V5P outputs exceed its over voltage threshold.

The V5P monitor is a bit unique. If V5P is accidently connected to the battery voltage then POK5V will bypass the normal 8 ms over voltage delay and set itself low immediately.

The fault modes and their effects on NPOR and POK5V are covered in detail in Table 3.

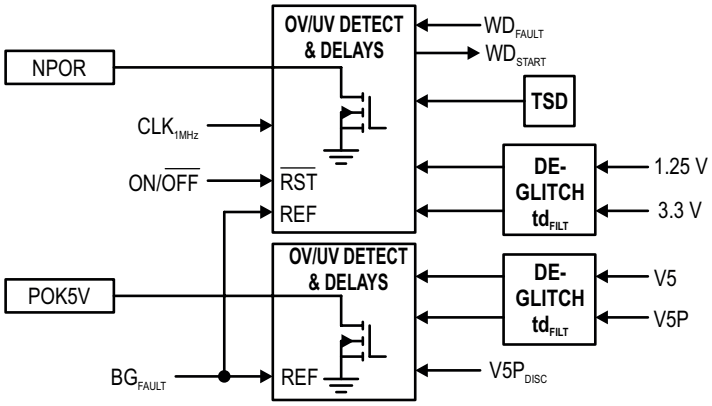


Figure 9: Fault Reporting Circuit

Table 2: Startup and Shutdown Logic (signal names consistent with Functional Block Diagram)

A4410 Status Signals					Regulator Control Bits (0=OFF, 1=ON)			A4410 MODE
EN	MPOR	VREG UV	1V25 UV	3xLDO UV	VREG ON	1V25 ON	LDOs ON	
X	1	X	X	X	0	0	0	RESET
0	0	1	1	1	0	0	0	OFF
1	0	1	1	1	1	0	0	STARTUP
1	0	0	1	1	1	1	0	↓
1	0	0	0	1	1	1	1	↓
1	0	0	0	0	1	1	1	RUN
0	0	0	0	0	1	1	1	DEGLITCH + DELAY
0	0	0	0	0	1	1	0	SHUTTING DOWN
0	0	0	0	1	1	0	0	↓
0	0	0	1	1	0	0	0	↓
0	0	1	1	1	0	0	0	OFF

TIME

X = DON'T CARE

EN = ENBAT1 + ENBAT2 + ENB

3xLDO UV = 3V3 + V5_UV + V5P_UV

MPOR = VCC_UV + VCP_UP + BG1_UV + BG2_UV + SLEW_UV/OV (latched) +FSET_UV/OV + TSD + VCP_OV (latched) + $D1_{MISSING}$ (latched) + $I_{LIM,LX1}$ (latched)

Table 3: Summary of Fault Mode Operation

FAULT TYPE and CONDITION	A4410 RESPONSE TO FAULT	NPOR	POK5V	LATCHED FAULT?	RESET METHOD
V5P short to VBAT	POK5V goes low when V5P disconnect occurs, if the fault persists longer than td_{OV} then set NPOR low and turn off all regulators	Low if fault lasts more than td_{OV}	Low when V5P disconnect occurs	NO	Check for short circuits on V5P
V5, V5P over voltage	If OV condition persists for more than td_{OV} then set POK5V low	Not effected	Low	NO	Check for short circuits on V5 or V5P
3V3 or 1V25 over voltage	If OV condition persists for more than td_{OV} then set NPOR low and shut off all regulators	Low	Low if fault lasts more than td_{OV}	YES	Check for short circuits then cycle EN or VIN
V5 or V5P under voltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	Not effected	Low	NO	Decrease the load
3V3 or 1V25 under voltage	Closed loop control will try to raise the voltage but may be constrained by the foldback or pulse-by-pulse current limit	Low	Not effected	NO	Decrease the load
V5 or V5P over current	Foldback current limit will reduce the output voltage	Not effected	Low if V5 or V5P are too low	NO	Decrease the load
3V3 over current	Foldback current limit will reduce the output voltage	Low if 3V3 < $V_{3V3,UV,L}$	Not effected	NO	Decrease the load
FB_{1V25} shorted to ground VSS2 < $V_{HIC2,EN}$, V_{1V25} < 470 mV	Continue to PWM but turn off LX2 when the high side MOSFET current exceeds I_{LIM2}	Low	Not effected	NO	Remove the short circuit
1V25 over current VSS2 > $V_{HIC2,EN}$ & V_{1V25} < 470 mV	Enters hiccup mode after 30 OCP faults	Low	Not effected	NO	Decrease the load
1V25 over current VSS2 > $V_{HIC2,EN}$ & V_{1V25} > 470 mV	Enters hiccup mode after 120 OCP faults	Low if 1V25 < $V_{1V25,UV,L}$	Not effected	NO	Decrease the load
VREG pin open circuit	VREG will decay to 0 V, LX1 will switch at maximum duty cycle so the voltage on the output capacitors will be very close to VBAT	Low if 3V3 or 1V25 are too low	Low if V5 or V5P are too low	NO	Connect the VREG pin
VREG over current V_{VREG} < 1.95 V & V_{COMP1} = $EA1_{VO(MAX)}$	Enters hiccup mode after 30 OCP faults	Low	Low	NO	Decrease the load
VREG over current V_{VREG} > 1.95 V & $V_{COMP}1$ = $EA1_{VO(MAX)}$	Enters hiccup mode after 120 OCP faults	Low if 3V3 or 1V25 are too low	Low if V5 or V5P are too low	NO	Decrease the load
VREG over voltage $VREG_{OV,H1}$ < V_{VREG}	Stop PWM switching of LX1	Low if 3V3 or 1V25 are too low	Low if V5 or V5P are too low	NO	None
VREG asynchronous diode (D1) missing	Results in an MPOR after 1 detection, so all regulators are shut off	Low if 3V3 or 1V25 are too low	Low if V5 or V5P are too low	YES	Place D1 then cycle EN or VIN
Asynchronous diode (D1) short circuited or LX1 shorted to ground	Results in an MPOR after the high side MOSFET current exceeds $I_{LIM,LX1}$ so all regulators are shut off	Low if 3V3 or 1V25 are too low	Low if V5 or V5P are too low	YES	Remove the short then cycle EN or VIN

Table 3: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	A4410 RESPONSE TO FAULT	NPOR	POK5V	LATCHED FAULT?	RESET METHOD
Slew pin open circuit (SLEW_UC)	Results in an MPOR, so all regulators are shut off	Low	Low	YES	Connect SLEW pin then cycle EN or VIN
Slew pin shorted to ground (SLEW_OC)	Results in an MPOR, so all regulators are shut off	Low	Low	YES	Remove the short then cycle EN or VIN
FSET/SYNC pin shorted to ground or open circuit	The A4410 operates at a default oscillator frequency of 450 kHz. If the fault occurs before power up: 1V25 and 3 LDOs are OFF. VREG (unloaded) runs in pulse skipping mode.	Low	Low	NO	Remove the short circuit or connect the pin
	The A4410 operates at a default oscillator frequency of 450 kHz. If the fault occurs after power up: 1V25 is OFF and 3 LDOs are ON.	Low	High		
Charge pump (VCP) over voltage	Results in an MPOR, so all regulators are shut off	Low	Low	YES	Check VCP/ CP1/CP2 pins & components, then cycle EN or VIN
Charge pump (VCP) under voltage	Results in an MPOR, so all regulators are shut off	Low	Low	NO	Check VCP/CP1/ CP2 pins and components
VCP pin open circuit	Results in VCP_UV and an MPOR, so all regulators are shut off	Low	Low	NO	Connect the VCP pin
VCP pin shorted to ground	Results on high current from the charge pump and (intentional) fusing of an internal trace. Also results in MPOR so all regulators are shut off.	Low	Low	NO	Remove the short circuit and replace the A4410
CP1 or CP2 pin open circuit	Results in VCP_UV and an MPOR, so all regulators are shut off	Low	Low	NO	Connect the CP1 or CP2 pins
CP1 pin shorted to ground	Results in VCP_UV and an MPOR, so all regulators are shut off	Low	Low	NO	Remove the short circuit
CP2 pin shorted to ground	Results on high current from the charge pump and (intentional) fusing of an internal trace. Also results in MPOR so all regulators are shut off.	Low	Low	NO	Remove the short circuit and replace the A4410
BG_{VREF} or BG_{FAULT} under voltage	Results in an MPOR, so all regulators are shut off	Low	Low	NO	Raise VIN or wait for BGs to power up
BG_{VREF} or BG_{FAULT} over voltage	If BG_{VREF} is too high, all regulators will appear to be OV (because BG_{FAULT} is good). If BG_{FAULT} is too high, all regulators will appear to be UV (because BG_{VREF} is good)	Low	Low	NO	Replace the A4410
VCC under voltage or shorted to ground	Results in an MPOR, so all regulators are shut off	Low	Low	NO	Raise VIN or remove short from VCC pin
WD_{ADJ} pin shorted to ground or open circuit	A WD_{ADJ} fault only effects the NPOR output. The remainder of the A4410 operates normally.	Low	High	NO	Remove the short circuit or connect the pin
Thermal shutdown	Results in an MPOR, so all regulators are shut off	Low	Low	NO	Let the A4410 cool

TIMING DIAGRAMS
(Not to Scale)

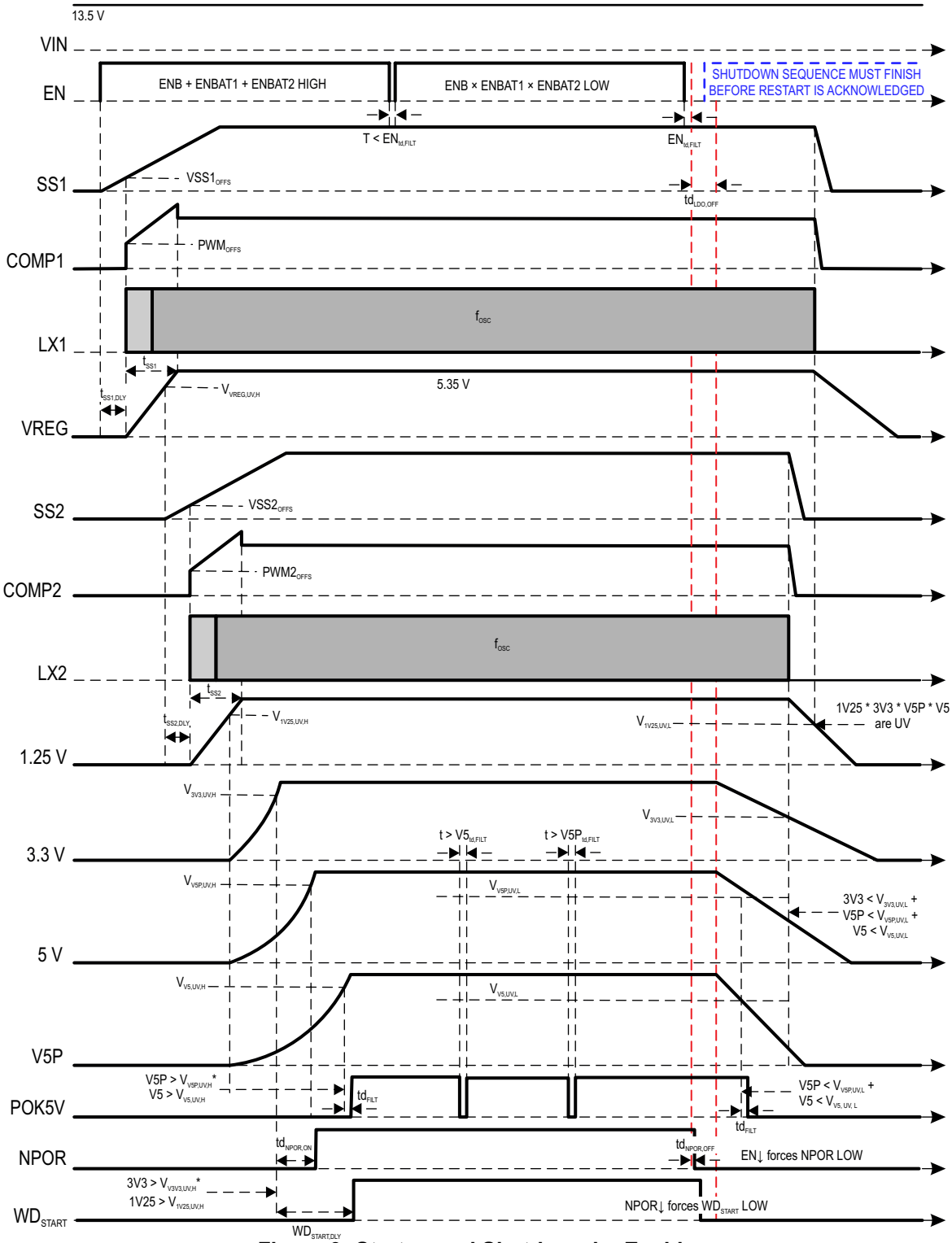


Figure 9: Startup and Shutdown by Enable

*** is for "and", + is for "or"**