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# SX-A Family FPGAs



## Leading-Edge Performance

- 250 MHz System Performance
- 350 MHz Internal Performance

## Specifications

- 12,000 to 108,000 Available System Gates
- Up to 360 User-Programmable I/O Pins
- Up to 2,012 Dedicated Flip-Flops
- 0.22  $\mu$  / 0.25  $\mu$  CMOS Process Technology

## Features

- Hot-Swap Compliant I/Os
- Power-Up/Down Friendly (No Sequencing Required for Supply Voltages)
- 66 MHz PCI Compliant
- Nonvolatile, Single-Chip Solution

- Configurable I/O Support for 3.3 V / 5 V PCI, 5 V TTL, 3.3 V LVTTTL, 2.5 V LVCMOS2
- 2.5 V, 3.3 V, and 5 V Mixed-Voltage Operation with 5 V Input Tolerance and 5 V Drive Strength
- Devices Support Multiple Temperature Grades
- Configurable Weak-Resistor Pull-Up or Pull-Down for I/O at Power-Up
- Individual Output Slew Rate Control
- Up to 100% Resource Utilization and 100% Pin Locking
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Boundary-Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft

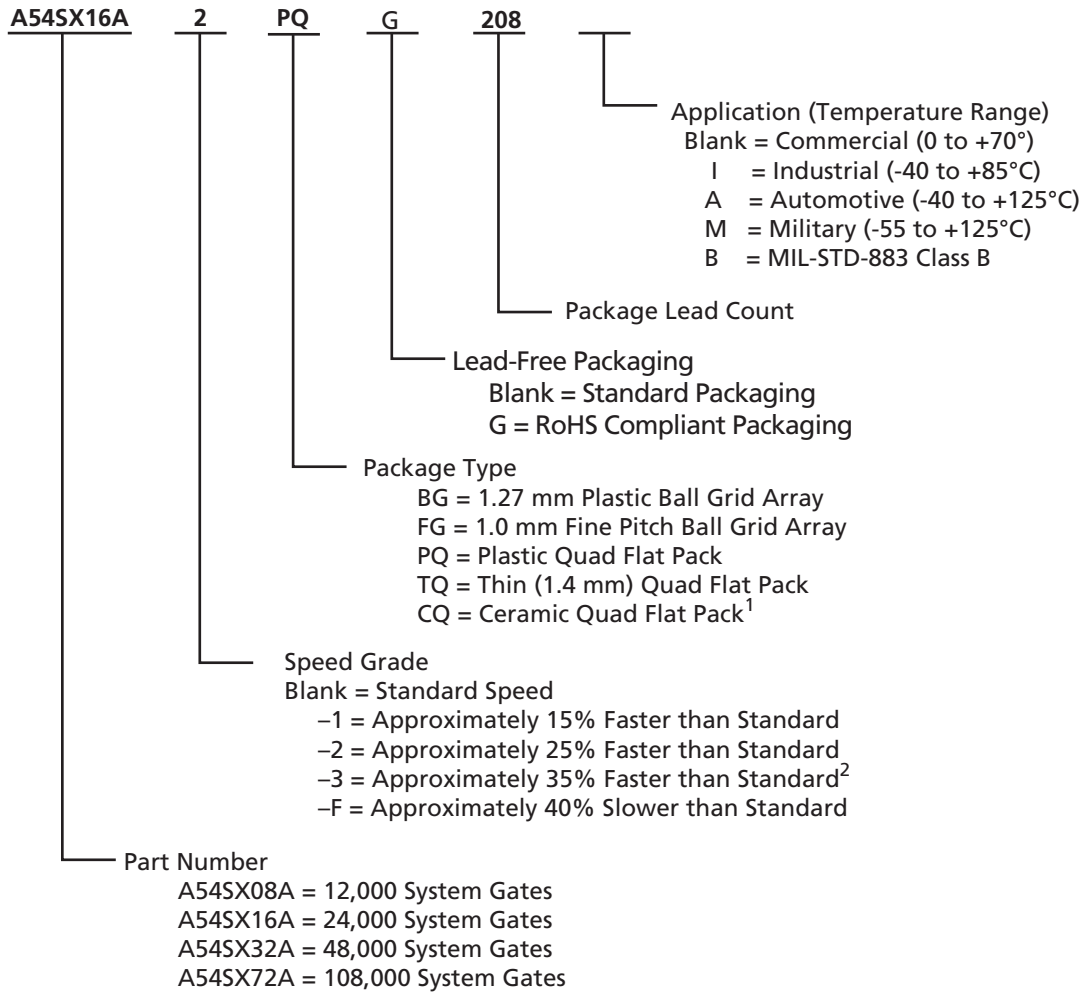
Table 1 • SX-A Product Profile

| Device                    | A54SX08A         | A54SX16A            | A54SX32A            | A54SX72A            |
|---------------------------|------------------|---------------------|---------------------|---------------------|
| Capacity                  |                  |                     |                     |                     |
| Typical Gates             | 8,000            | 16,000              | 32,000              | 72,000              |
| System Gates              | 12,000           | 24,000              | 48,000              | 108,000             |
| Logic Modules             | 768              | 1,452               | 2,880               | 6,036               |
| Combinatorial Cells       | 512              | 924                 | 1,800               | 4,024               |
| Dedicated Flip-Flops      | 256              | 528                 | 1,080               | 2,012               |
| Maximum Flip-Flops        | 512 <sup>1</sup> | 990                 | 1,980               | 4,024               |
| Maximum User I/Os         | 130              | 180                 | 249                 | 360                 |
| Global Clocks             | 3                | 3                   | 3                   | 3                   |
| Quadrant Clocks           | 0                | 0                   | 0                   | 4                   |
| Boundary Scan Testing     | Yes              | Yes                 | Yes                 | Yes                 |
| 3.3 V / 5 V PCI           | Yes              | Yes                 | Yes                 | Yes                 |
| Input Set-Up (External)   | 0 ns             | 0 ns                | 0 ns                | 0 ns                |
| Speed Grades <sup>2</sup> | -F, Std, -1, -2  | -F, Std, -1, -2, -3 | -F, Std, -1, -2, -3 | -F, Std, -1, -2, -3 |
| Temperature Grades        | C, I, A, M       | C, I, A, M          | C, I, A, M          | C, I, A, M          |
| Package (by pin count)    |                  |                     |                     |                     |
| PQFP                      | 208              | 208                 | 208                 | 208                 |
| TQFP                      | 100, 144         | 100, 144            | 100, 144, 176       | -                   |
| PBGA                      | -                | -                   | 329                 | -                   |
| FBGA                      | 144              | 144, 256            | 144, 256, 484       | 256, 484            |
| CQFP                      | -                | -                   | 208, 256            | 208, 256            |

### Notes:

1. A maximum of 512 registers is possible if all 512 C cells are used to build an additional 256 registers.
2. All -3 speed grades have been discontinued.

## Ordering Information



**Notes:**

1. For more information about the CQFP package options, refer to the [HiRel SX-A datasheet](#).
2. All -3 speed grades have been discontinued.

## Device Resources

| Device   | User I/Os (Including Clock Buffers) |              |              |              |              |              |              |              |
|----------|-------------------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
|          | 208-Pin PQFP                        | 100-Pin TQFP | 144-Pin TQFP | 176-Pin TQFP | 329-Pin PBGA | 144-Pin FBGA | 256-Pin FBGA | 484-Pin FBGA |
| A54SX08A | 130                                 | 81           | 113          | –            | –            | 111          | –            | –            |
| A54SX16A | 175                                 | 81           | 113          | –            | –            | 111          | 180          | –            |
| A54SX32A | 174                                 | 81           | 113          | 147          | 249          | 111          | 203          | 249          |
| A54SX72A | 171                                 | –            | –            | –            | –            | –            | 203          | 360          |

**Notes:** Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array

## Temperature Grade Offering

| Package | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|---------|----------|----------|----------|----------|
| PQ208   | C,I,A,M  | C,I,A,M  | C,I,A,M  | C,I,A,M  |
| TQ100   | C,I,A,M  | C,I,A,M  | C,I,A,M  |          |
| TQ144   | C,I,A,M  | C,I,A,M  | C,I,A,M  |          |
| TQ176   |          |          | C,I,M    |          |
| BG329   |          |          | C,I,M    |          |
| FG144   | C,I,A,M  | C,I,A,M  | C,I,A,M  |          |
| FG256   |          | C,I,A,M  | C,I,A,M  | C,I,A,M  |
| FG484   |          |          | C,I,M    | C,I,A,M  |
| CQ208   |          |          | C,M,B    | C,M,B    |
| CQ256   |          |          | C,M,B    | C,M,B    |

### Notes:

1. C = Commercial
2. I = Industrial
3. A = Automotive
4. M = Military
5. B = MIL-STD-883 Class B
6. For more information regarding automotive products, refer to the [SX-A Automotive Family FPGAs datasheet](#).
7. For more information regarding Mil-Temp and ceramic packages, refer to the [HiRel SX-A Family FPGAs datasheet](#).

## Speed Grade and Temperature Grade Matrix

|              | F | Std | -1 | -2 | -3           |
|--------------|---|-----|----|----|--------------|
| Commercial   | ✓ | ✓   | ✓  | ✓  | Discontinued |
| Industrial   |   | ✓   | ✓  | ✓  | Discontinued |
| Automotive   |   | ✓   |    |    |              |
| Military     |   | ✓   | ✓  |    |              |
| MIL-STD-883B |   | ✓   | ✓  |    |              |

### Notes:

1. For more information regarding automotive products, refer to the [SX-A Automotive Family FPGAs datasheet](#).
2. For more information regarding Mil-Temp and ceramic packages, refer to the [HiRel SX-A Family FPGAs datasheet](#).

Contact your Actel Sales representative for more information on availability.



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# General Description

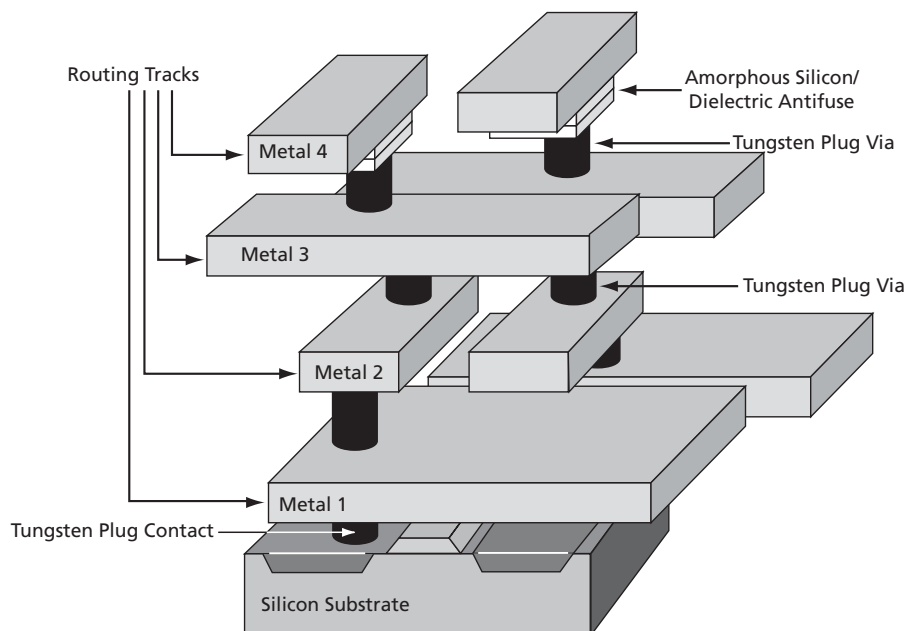
## Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22  $\mu\text{m}$  / 0.25  $\mu\text{m}$  CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

## SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



**Note:** The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements

## Logic Module Design

The SX-A family architecture is described as a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000

different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

## Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

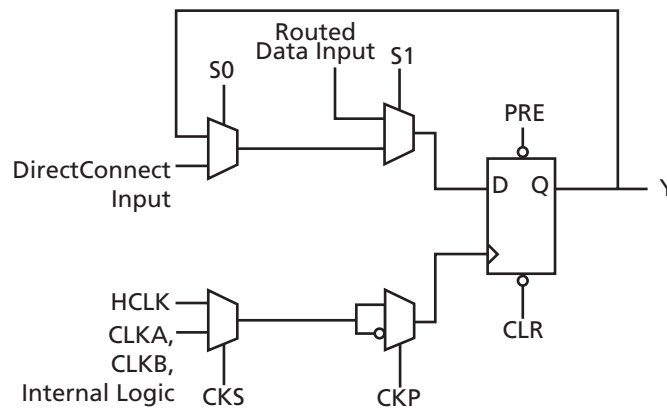


Figure 1-2 • R-Cell

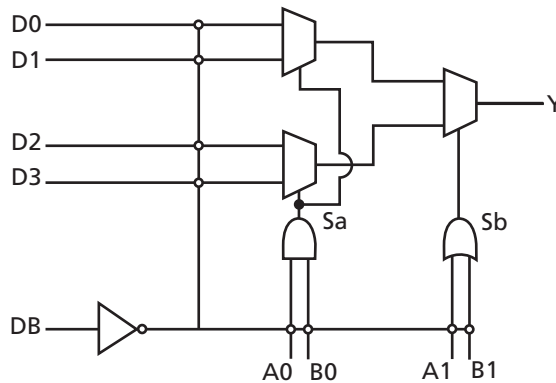


Figure 1-3 • C-Cell

## Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable

interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.

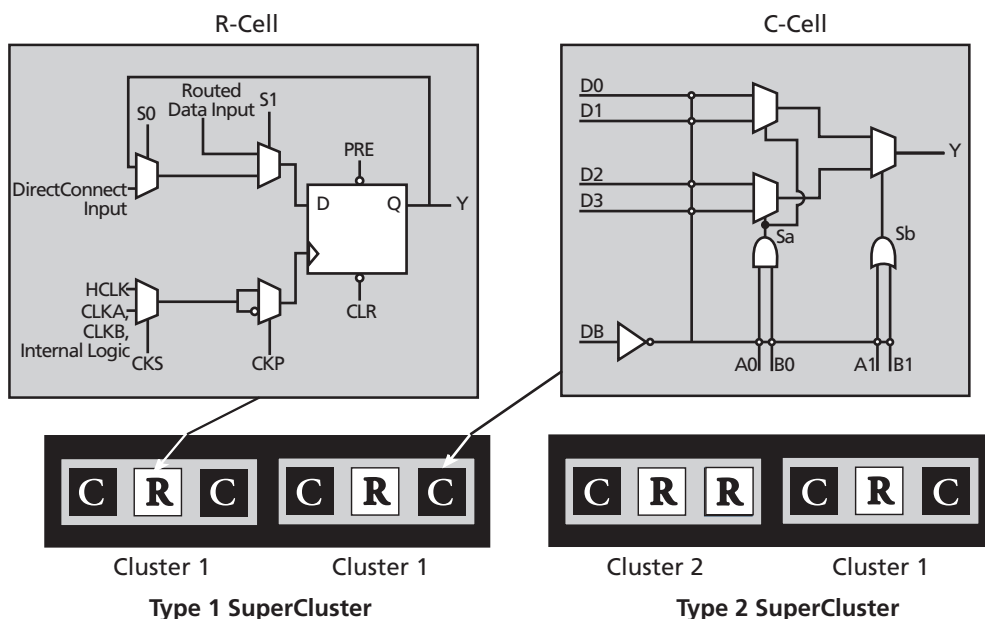


Figure 1-4 • Cluster Organization



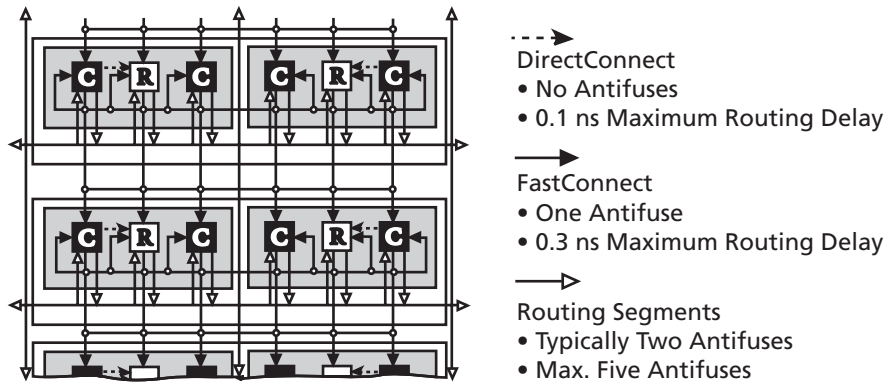


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

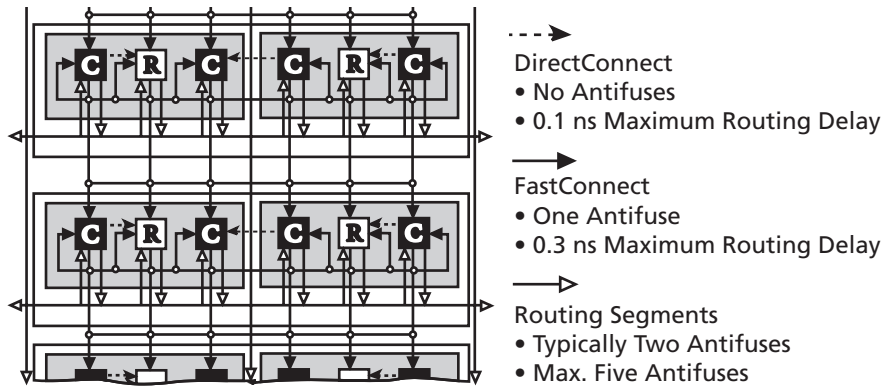


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

## Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant load HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinatorial logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA

and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD—corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an entire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Devices* and *Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15.

Table 1-1 • SX-A Clock Resources

|  | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|--|----------|----------|----------|----------|
| Routed Clocks (CLKA, CLKB)                   | 2        | 2        | 2        | 2        |
| Hardwired Clocks (HCLK)                      | 1        | 1        | 1        | 1        |
| Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD) | 0        | 0        | 0        | 4        |

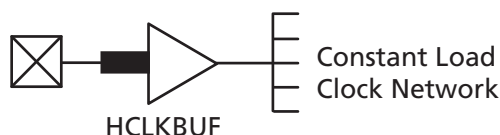


Figure 1-7 • SX-A HCLK Clock Buffer

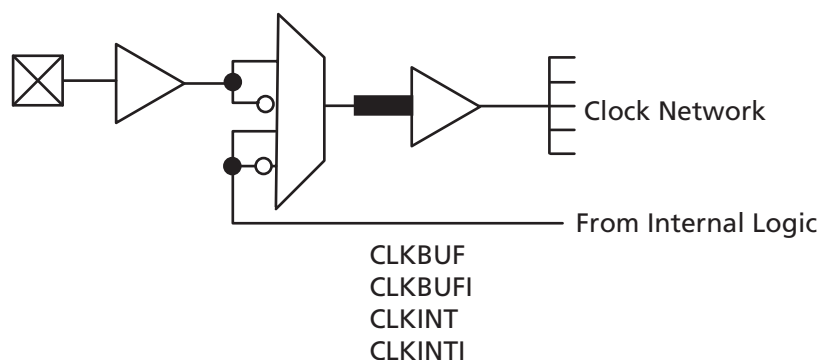


Figure 1-8 • SX-A Routed Clock Buffer

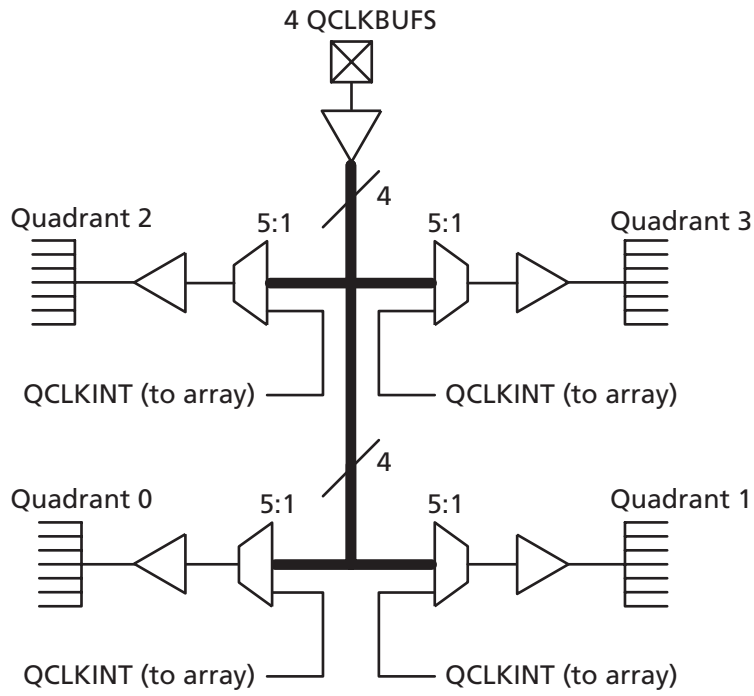


Figure 1-9 • SX-A QCLK Architecture

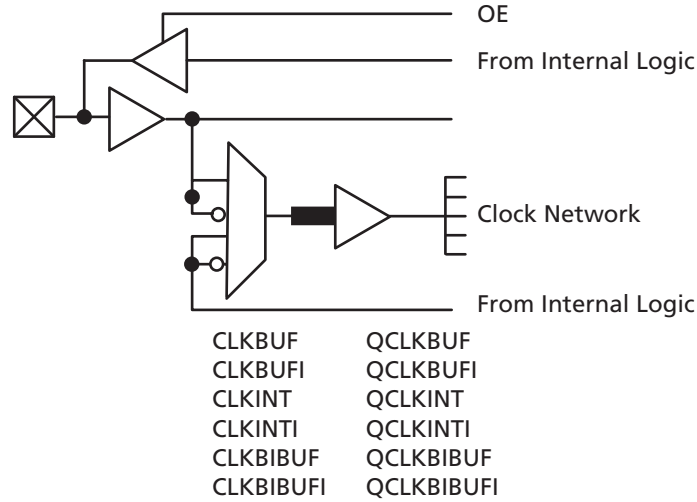


Figure 1-10 • A54SX72A Routed Clock and QCLK Buffer

## Other Architectural Features

### Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using  $0.22\ \mu\text{m} / 0.25\ \mu\text{m}$  design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of  $25\ \Omega$  with capacitance of  $1.0\ \text{fF}$  for low signal impedance.

### Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

### User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).



Figure 1-11 • FuseLock

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

## I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than  $V_{CC1}$  and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and  $V_{CC1}$  is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately  $50\ \text{k}\Omega$  that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os*. Just slightly before  $V_{CCA}$  reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

## Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated.  $V_{CCA}$  and  $V_{CCI}$  do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions

are reached. Table 1-4 summarizes the  $V_{CCA}$  voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, [Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications](#).

Table 1-2 • I/O Features

| Function                          | Description  |
|-----------------------------------|--|
| Input Buffer Threshold Selections | <ul style="list-style-type: none"> <li>5 V: PCI, TTL</li> <li>3.3 V: PCI, LVTTTL</li> <li>2.5 V: LVCMOS2 (commercial only)</li> </ul>  |
| Flexible Output Driver            | <ul style="list-style-type: none"> <li>5 V: PCI, TTL</li> <li>3.3 V: PCI, LVTTTL</li> <li>2.5 V: LVCMOS2 (commercial only)</li> </ul>  |
| Output Buffer                     | <p>"Hot-Swap" Capability (3.3 V PCI is not hot swappable)</p> <ul style="list-style-type: none"> <li>I/O on an unpowered device does not sink current</li> <li>Can be used for "cold-sparing"</li> </ul> <p>Selectable on an individual I/O basis</p> <p>Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.</p> |
| Power-Up                          | <p>Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate)</p> <p>Enables deterministic power-up of device</p> <p><math>V_{CCA}</math> and <math>V_{CCI}</math> can be powered in any order</p>   |

Table 1-3 • I/O Characteristics for All I/O Configurations

|                      | Hot Swappable | Slew Rate Control                          | Power-Up Resistor    |
|----------------------|---------------|--|----------------------|
| TTL, LVTTTL, LVCMOS2 | Yes           | Yes. Only affects falling edges of outputs | Pull-up or pull-down |
| 3.3 V PCI            | No            | No. High slew rate only                    | Pull-up or pull-down |
| 5 V PCI              | Yes           | No. High slew rate only                    | Pull-up or pull-down |

Table 1-4 • Power-Up Time at which I/Os Become Active

| Supply Ramp Rate | 0.25 V/ $\mu$ s | 0.025 V/ $\mu$ s | 5 V/ms | 2.5 V/ms | 0.5 V/ms | 0.25 V/ms | 0.1 V/ms | 0.025 V/ms |
|------------------|-----------------|------------------|--------|----------|----------|-----------|----------|------------|
| Units            | $\mu$ s         | $\mu$ s          | ms     | ms       | ms       | ms        | ms       | ms         |
| A54SX08A         | 10              | 96               | 0.34   | 0.65     | 2.7      | 5.4       | 12.9     | 50.8       |
| A54SX16A         | 10              | 100              | 0.36   | 0.62     | 2.5      | 4.7       | 11.0     | 41.6       |
| A54SX32A         | 10              | 100              | 0.46   | 0.74     | 2.8      | 5.2       | 12.1     | 47.2       |
| A54SX72A         | 10              | 100              | 0.41   | 0.67     | 2.6      | 5.0       | 12.1     | 47.2       |



## Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

### Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.



Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

| Pin                     | Function   |
|-------------------------|--|
| Reserve JTAG            | Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS) |
| Reserve JTAG Test Reset | Regular I/O or JTAG reset with an internal pull-up                                   |
| Reserve Probe           | Keeps pins from being used or regular I/O  |

### Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V<sub>CC1</sub> should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6 • Boundary-Scan Pin Configurations and Functions

| Mode                | Designer "Reserve JTAG" Selection | TAP Controller State        |
|---------------------|-----------------------------------|-----------------------------|
| Dedicated (JTAG)    | Checked                           | Any                         |
| Flexible (User I/O) | Unchecked                         | Test-Logic-Reset            |
| Flexible (JTAG)     | Unchecked                         | Any EXCEPT Test-Logic-Reset |

### TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

## JTAG Instructions

Table 1-7 lists the supported instructions with the corresponding IR codes for SX-A devices.

Table 1-8 lists the codes returned after executing the IDCODE instruction for SX-A devices. Note that bit 0 is always '1'. Bits 11-1 are always '02F', which is the Actel manufacturer code.

Table 1-7 • JTAG Instruction Code

| Instructions (IR4:IR0) | Binary Code |
|------------------------|-------------|
| EXTEST                 | 00000       |
| SAMPLE/PRELOAD         | 00001       |
| INTEST                 | 00010       |
| USERCODE               | 00011       |
| IDCODE                 | 00100       |
| HighZ                  | 01110       |
| CLAMP                  | 01111       |
| Diagnostic             | 10000       |
| BYPASS                 | 11111       |
| Reserved               | All others  |

Table 1-8 • JTAG Instruction Code

| Device   | Process     | Revision | Bits 31-28 | Bits 27-12 |
|----------|-------------|----------|------------|------------|
| A54SX08A | 0.22 $\mu$  | 0        | 8, 9       | 40B4, 42B4 |
|          |             | 1        | A, B       | 40B4, 42B4 |
| A54SX16A | 0.22 $\mu$  | 0        | 9          | 40B8, 42B8 |
|          |             | 1        | B          | 40B8, 42B8 |
|          | 0.25 $\mu$  | 1        | B          | 22B8       |
| A54SX32A | 0.2 2 $\mu$ | 0        | 9          | 40BD, 42BD |
|          |             | 1        | B          | 40BD, 42BD |
|          | 0.25 $\mu$  | 1        | B          | 22BD       |
| A54SX72A | 0.22 $\mu$  | 0        | 9          | 40B2, 42B2 |
|          |             | 1        | B          | 40B2, 42B2 |
|          | 0.25 $\mu$  | 1        | B          | 22B2       |

## Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High.

When selecting the **Reserve Probe Pin** box as shown in [Figure 1-12 on page 1-9](#), direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. [Table 1-9](#) summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved)

| JTAG Mode | TRST <sup>1</sup> | Security Fuse Programmed | PRA, PRB <sup>2</sup> | TDI, TCK, TDO <sup>2</sup> |
|-----------|-------------------|--------------------------|-----------------------|----------------------------|
| Dedicated | Low               | No                       | User I/O <sup>3</sup> | JTAG Disabled              |
|           | High              | No                       | Probe Circuit Outputs | JTAG I/O                   |
| Flexible  | Low               | No                       | User I/O <sup>3</sup> | User I/O <sup>3</sup>      |
|           | High              | No                       | Probe Circuit Outputs | JTAG I/O                   |
|           |                   | Yes                      | Probe Circuit Secured | Probe Circuit Secured      |

**Notes:**

1. If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.
2. Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.
3. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.

### SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the

PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

### Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a 70 Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

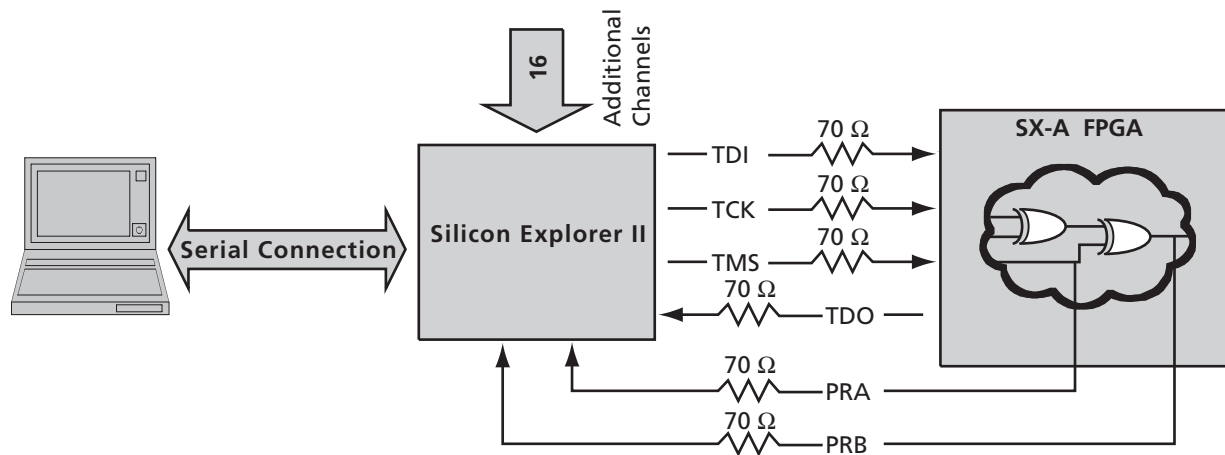


Figure 1-13 • Probe Setup

## Design Environment

The SX-A family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, ModelSim® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmarGen core generator, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

## Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor is compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor also provides extensive hardware self-testing capability.

The procedure for programming an SX-A device using Silicon Sculptor is as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For detailed information on programming, read the following documents *Programming Antifuse Devices* and *Silicon Sculptor User's Guide*.



## Related Documents

### Application Notes

*Global Clock Networks in Actel's Antifuse Devices*

[http://www.actel.com/documents/GlobalClk\\_AN.pdf](http://www.actel.com/documents/GlobalClk_AN.pdf)

*Using A54SX72A and RT54SX72S Quadrant Clocks*

[http://www.actel.com/documents/QCLK\\_AN.pdf](http://www.actel.com/documents/QCLK_AN.pdf)

*Implementation of Security in Actel Antifuse FPGAs*

[http://www.actel.com/documents/Antifuse\\_Security\\_AN.pdf](http://www.actel.com/documents/Antifuse_Security_AN.pdf)

*Actel eX, SX-A, and RTSX-S I/Os*

[http://www.actel.com/documents/AntifuseIO\\_AN.pdf](http://www.actel.com/documents/AntifuseIO_AN.pdf)

*Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*

[http://www.actel.com/documents/HotSwapColdSparing\\_AN.pdf](http://www.actel.com/documents/HotSwapColdSparing_AN.pdf)

*Programming Antifuse Devices*

[http://www.actel.com/documents/AntifuseProgram\\_AN.pdf](http://www.actel.com/documents/AntifuseProgram_AN.pdf)

### Datasheets

*HiRel SX-A Family FPGAs*

[http://www.actel.com/documents/HRSXA\\_DS.pdf](http://www.actel.com/documents/HRSXA_DS.pdf)

*SX-A Automotive Family FPGAs*

[http://www.actel.com/documents/SXA\\_Auto\\_DS.pdf](http://www.actel.com/documents/SXA_Auto_DS.pdf)

### User's Guides

*Silicon Sculptor User's Guide*

[http://www.actel.com/documents/SiliSculptII\\_Sculpt3\\_ug.pdf](http://www.actel.com/documents/SiliSculptII_Sculpt3_ug.pdf)

## Pin Description

### CLKA/B, I/O      Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

### QCLKA/B/C/D, I/O      Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

### GND      Ground

Low supply voltage.

### HCLK      Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

### I/O      Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

### NC      No Connection

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

### PRA/B, I/O      Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

### TCK, I/O      Test Clock

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to [Table 1-6 on page 1-9](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### TDI, I/O      Test Data Input

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to [Table 1-6 on page 1-9](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### TDO, I/O      Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to [Table 1-6 on page 1-9](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user I/O when checksum is complete.

### TMS      Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to [Table 1-6 on page 1-9](#)). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

### TRST, I/O      Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

### V<sub>CCI</sub>      Supply Voltage

Supply voltage for I/Os. See [Table 2-2 on page 2-1](#). All V<sub>CCI</sub> power pins in the device should be connected.

### V<sub>CCA</sub>      Supply Voltage

Supply voltage for array. See [Table 2-2 on page 2-1](#). All V<sub>CCA</sub> power pins in the device should be connected.



# Detailed Specifications

## Operating Conditions

Table 2-1 • Absolute Maximum Ratings

| Symbol    | Parameter                    | Limits                    | Units |
|-----------|------------------------------|---------------------------|-------|
| $V_{CCI}$ | DC Supply Voltage for I/Os   | -0.3 to +6.0              | V     |
| $V_{CCA}$ | DC Supply Voltage for Arrays | -0.3 to +3.0              | V     |
| $V_I$     | Input Voltage                | -0.5 to +5.75             | V     |
| $V_O$     | Output Voltage               | -0.5 to + $V_{CCI}$ + 0.5 | V     |
| $T_{STG}$ | Storage Temperature          | -65 to +150               | °C    |

**Note:** \*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".

Table 2-2 • Recommended Operating Conditions

| Parameter  | Commercial   | Industrial   | Units |
|--|--------------|--------------|-------|
| Temperature Range                                    | 0 to +70     | -40 to +85   | °C    |
| 2.5 V Power Supply Range ( $V_{CCA}$ and $V_{CCI}$ ) | 2.25 to 2.75 | 2.25 to 2.75 | V     |
| 3.3 V Power Supply Range ( $V_{CCI}$ )               | 3.0 to 3.6   | 3.0 to 3.6   | V     |
| 5 V Power Supply Range ( $V_{CCI}$ )                 | 4.75 to 5.25 | 4.75 to 5.25 | V     |

## Typical SX-A Standby Current

Table 2-3 • Typical Standby Current for SX-A at 25°C with  $V_{CCA} = 2.5$  V

| Product  | $V_{CCI} = 2.5$ V | $V_{CCI} = 3.3$ V | $V_{CCI} = 5$ V |
|----------|-------------------|-------------------|-----------------|
| A54SX08A | 0.8 mA            | 1.0 mA            | 2.9 mA          |
| A54SX16A | 0.8 mA            | 1.0 mA            | 2.9 mA          |
| A54SX32A | 0.9 mA            | 1.0 mA            | 3.0 mA          |
| A54SX72A | 3.6 mA            | 3.8 mA            | 4.5 mA          |

Table 2-4 • Supply Voltages

| $V_{CCA}$ | $V_{CCI}$ * | Maximum Input Tolerance | Maximum Output Drive |
|-----------|-------------|-------------------------|----------------------|
| 2.5 V     | 2.5 V       | 5.75 V                  | 2.7 V                |
| 2.5 V     | 3.3 V       | 5.75 V                  | 3.6 V                |
| 2.5 V     | 5 V         | 5.75 V                  | 5.25 V               |

**Note:** \*3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.

## Electrical Specifications

Table 2-5 • 3.3 V LVTTTL and 5 V TTL Electrical Specifications

| Symbol                           | Parameter   |                           | Commercial           |      | Industrial           |      | Units |
|----------------------------------|---|---------------------------|----------------------|------|----------------------|------|-------|
|                                  |   |                           | Min.                 | Max. | Min.                 | Max. |       |
| V <sub>OH</sub>                  | V <sub>CC1</sub> = Minimum<br>V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | (I <sub>OH</sub> = -1 mA) | 0.9 V <sub>CC1</sub> |      | 0.9 V <sub>CC1</sub> |      | V     |
|                                  | V <sub>CC1</sub> = Minimum<br>V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | (I <sub>OH</sub> = -8 mA) | 2.4                  |      | 2.4                  |      | V     |
| V <sub>OL</sub>                  | V <sub>CC1</sub> = Minimum<br>V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | (I <sub>OL</sub> = 1 mA)  | 0.4                  |      | 0.4                  |      | V     |
|                                  | V <sub>CC1</sub> = Minimum<br>V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | (I <sub>OL</sub> = 12 mA) | 0.4                  |      | 0.4                  |      | V     |
| V <sub>IL</sub>                  | Input Low Voltage   |                           | 0.8                  |      | 0.8                  |      | V     |
| V <sub>IH</sub>                  | Input High Voltage  |                           | 2.0                  | 5.75 | 2.0                  | 5.75 | V     |
| I <sub>IL</sub> /I <sub>IH</sub> | Input Leakage Current, V <sub>IN</sub> = V <sub>CC1</sub> or GND                  |                           | -10                  | 10   | -10                  | 10   | μA    |
| I <sub>OZ</sub>                  | Tristate Output Leakage Current   |                           | -10                  | 10   | -10                  | 10   | μA    |
| t <sub>R</sub> , t <sub>F</sub>  | Input Transition Time t <sub>R</sub> , t <sub>F</sub>                             |                           | 10                   |      | 10                   |      | ns    |
| C <sub>IO</sub>                  | I/O Capacitance   |                           | 10                   |      | 10                   |      | pF    |
| I <sub>CC</sub>                  | Standby Current   |                           | 10                   |      | 20                   |      | mA    |
| IV Curve*                        | Can be derived from the IBIS model on the web.                                    |                           |                      |      |                      |      |       |

**Note:** \*The IBIS model can be found at <http://www.actel.com/download/ibis/default.aspx>.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

| Symbol                           | Parameter   |                             | Commercial |      | Industrial |      | Units |
|----------------------------------|---|-----------------------------|------------|------|------------|------|-------|
|                                  |   |                             | Min.       | Max. | Min.       | Max. |       |
| V <sub>OH</sub>                  | V <sub>DD</sub> = MIN,<br>V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | (I <sub>OH</sub> = -100 μA) | 2.1        |      | 2.1        |      | V     |
|                                  | V <sub>DD</sub> = MIN,<br>V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | (I <sub>OH</sub> = -1 mA)   | 2.0        |      | 2.0        |      | V     |
|                                  | V <sub>DD</sub> = MIN,<br>V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | (I <sub>OH</sub> = -2 mA)   | 1.7        |      | 1.7        |      | V     |
| V <sub>OL</sub>                  | V <sub>DD</sub> = MIN,<br>V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | (I <sub>OL</sub> = 100 μA)  | 0.2        |      | 0.2        |      | V     |
|                                  | V <sub>DD</sub> = MIN,<br>V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | (I <sub>OL</sub> = 1 mA)    | 0.4        |      | 0.4        |      | V     |
|                                  | V <sub>DD</sub> = MIN,<br>V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | (I <sub>OL</sub> = 2 mA)    | 0.7        |      | 0.7        |      | V     |
| V <sub>IL</sub>                  | Input Low Voltage, V <sub>OUT</sub> ≤ V <sub>VOL(max)</sub>                   |                             | -0.3       | 0.7  | -0.3       | 0.7  | V     |
| V <sub>IH</sub>                  | Input High Voltage, V <sub>OUT</sub> ≥ V <sub>VOH(min)</sub>                  |                             | 1.7        | 5.75 | 1.7        | 5.75 | V     |
| I <sub>IL</sub> /I <sub>IH</sub> | Input Leakage Current, V <sub>IN</sub> = V <sub>CC1</sub> or GND              |                             | -10        | 10   | -10        | 10   | μA    |
| I <sub>OZ</sub>                  | Tristate Output Leakage Current, V <sub>OUT</sub> = V <sub>CC1</sub> or GND   |                             | -10        | 10   | -10        | 10   | μA    |
| t <sub>R</sub> , t <sub>F</sub>  | Input Transition Time t <sub>R</sub> , t <sub>F</sub>                         |                             | 10         |      | 10         |      | ns    |
| C <sub>IO</sub>                  | I/O Capacitance   |                             | 10         |      | 10         |      | pF    |
| I <sub>CC</sub>                  | Standby Current   |                             | 10         |      | 20         |      | mA    |
| IV Curve*                        | Can be derived from the IBIS model on the web.                                |                             |            |      |            |      |       |

**Note:** \*The IBIS model can be found at <http://www.actel.com/download/ibis/default.aspx>.



## PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • DC Specifications (5 V PCI Operation)

| Symbol           | Parameter                               | Condition                     | Min. | Max. | Units |
|------------------|---|-------------------------------|------|------|-------|
| V <sub>CCA</sub> | Supply Voltage for Array                |                               | 2.25 | 2.75 | V     |
| V <sub>CCI</sub> | Supply Voltage for I/Os                 |                               | 4.75 | 5.25 | V     |
| V <sub>IH</sub>  | Input High Voltage                      |                               | 2.0  | 5.75 | V     |
| V <sub>IL</sub>  | Input Low Voltage                       |                               | -0.5 | 0.8  | V     |
| I <sub>IH</sub>  | Input High Leakage Current <sup>1</sup> | V <sub>IN</sub> = 2.7         | -    | 70   | μA    |
| I <sub>IL</sub>  | Input Low Leakage Current <sup>1</sup>  | V <sub>IN</sub> = 0.5         | -    | -70  | μA    |
| V <sub>OH</sub>  | Output High Voltage                     | I <sub>OUT</sub> = -2 mA      | 2.4  | -    | V     |
| V <sub>OL</sub>  | Output Low Voltage <sup>2</sup>         | I <sub>OUT</sub> = 3 mA, 6 mA | -    | 0.55 | V     |
| C <sub>IN</sub>  | Input Pin Capacitance <sup>3</sup>      |                               | -    | 10   | pF    |
| C <sub>CLK</sub> | CLK Pin Capacitance                     |                               | 5    | 12   | pF    |

### Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Table 2-8 • AC Specifications (5 V PCI Operation)

| Symbol              | Parameter              | Condition                                 | Min.                            | Max.               | Units |
|---------------------|------------------------|---|---------------------------------|--------------------|-------|
| I <sub>OH(AC)</sub> | Switching Current High | $0 < V_{OUT} \leq 1.4$ <sup>1</sup>       | -44                             | -                  | mA    |
|                     |                        | $1.4 \leq V_{OUT} < 2.4$ <sup>1, 2</sup>  | $(-44 + (V_{OUT} - 1.4)/0.024)$ | -                  | mA    |
|                     |                        | $3.1 < V_{OUT} < V_{CCI}$ <sup>1, 3</sup> | -                               | EQ 2-1 on page 2-5 | -     |
|                     | (Test Point)           | $V_{OUT} = 3.1$ <sup>3</sup>              | -                               | -142               | mA    |
| I <sub>OL(AC)</sub> | Switching Current Low  | $V_{OUT} \geq 2.2$ <sup>1</sup>           | 95                              | -                  | mA    |
|                     |                        | $2.2 > V_{OUT} > 0.55$ <sup>1</sup>       | $(V_{OUT}/0.023)$               | -                  | mA    |
|                     |                        | $0.71 > V_{OUT} > 0$ <sup>1, 3</sup>      | -                               | EQ 2-2 on page 2-5 | -     |
|                     | (Test Point)           | $V_{OUT} = 0.71$ <sup>3</sup>             | -                               | 206                | mA    |
| I <sub>CL</sub>     | Low Clamp Current      | $-5 < V_{IN} \leq -1$                     | $-25 + (V_{IN} + 1)/0.015$      | -                  | mA    |
| slew <sub>R</sub>   | Output Rise Slew Rate  | 0.4 V to 2.4 V load <sup>4</sup>          | 1                               | 5                  | V/ns  |
| slew <sub>F</sub>   | Output Fall Slew Rate  | 2.4 V to 0.4 V load <sup>4</sup>          | 1                               | 5                  | V/ns  |

**Notes:**

1. Refer to the V/I curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

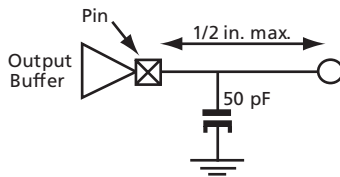


Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

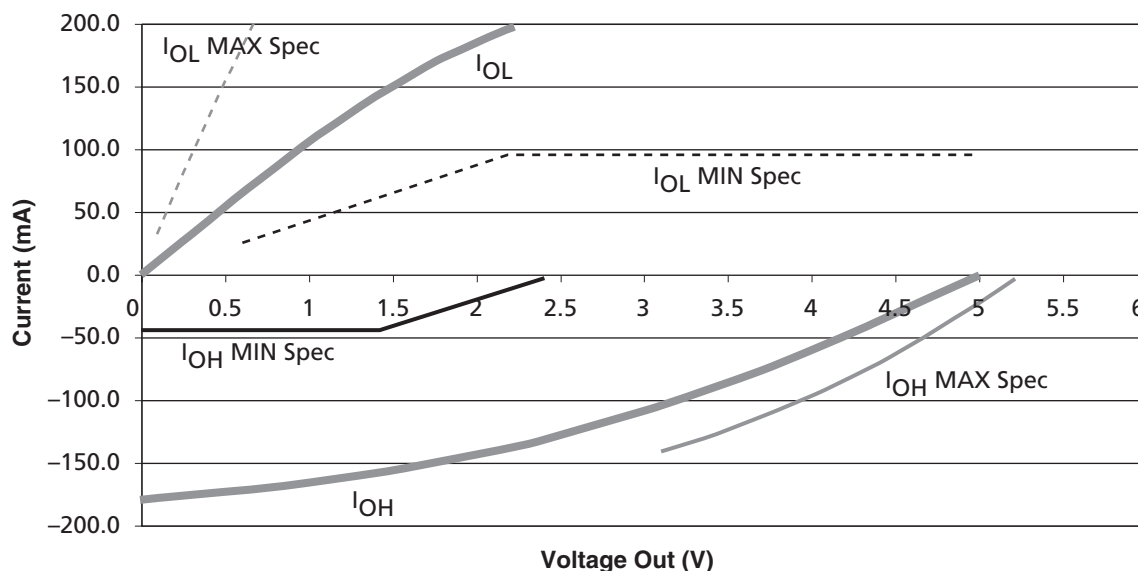


Figure 2-1 • 5 V PCI V/I Curve for SX-A Family

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$

for  $V_{CCI} > V_{OUT} > 3.1V$

EQ 2-1

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$

for  $0V < V_{OUT} < 0.71V$

EQ 2-2

Table 2-9 • DC Specifications (3.3 V PCI Operation)

| Symbol    | Parameter                          | Condition               | Min.         | Max.            | Units   |
|-----------|------------------------------------|-------------------------|--------------|-----------------|---------|
| $V_{CCA}$ | Supply Voltage for Array           |                         | 2.25         | 2.75            | V       |
| $V_{CCI}$ | Supply Voltage for I/Os            |                         | 3.0          | 3.6             | V       |
| $V_{IH}$  | Input High Voltage                 |                         | $0.5V_{CCI}$ | $V_{CCI} + 0.5$ | V       |
| $V_{IL}$  | Input Low Voltage                  |                         | -0.5         | $0.3V_{CCI}$    | V       |
| $I_{IPU}$ | Input Pull-up Voltage <sup>1</sup> |                         | $0.7V_{CCI}$ | -               | V       |
| $I_{IL}$  | Input Leakage Current <sup>2</sup> | $0 < V_{IN} < V_{CCI}$  | -10          | +10             | $\mu A$ |
| $V_{OH}$  | Output High Voltage                | $I_{OUT} = -500 \mu A$  | $0.9V_{CCI}$ | -               | V       |
| $V_{OL}$  | Output Low Voltage                 | $I_{OUT} = 1,500 \mu A$ |              | $0.1V_{CCI}$    | V       |
| $C_{IN}$  | Input Pin Capacitance <sup>3</sup> |                         | -            | 10              | pF      |
| $C_{CLK}$ | CLK Pin Capacitance                |                         | 5            | 12              | pF      |

**Notes:**

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).