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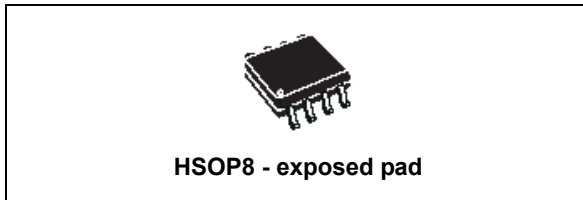
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## Up to 2 A step-down switching regulator for automotive applications

Datasheet - production data



### Applications

- Dedicated to automotive applications

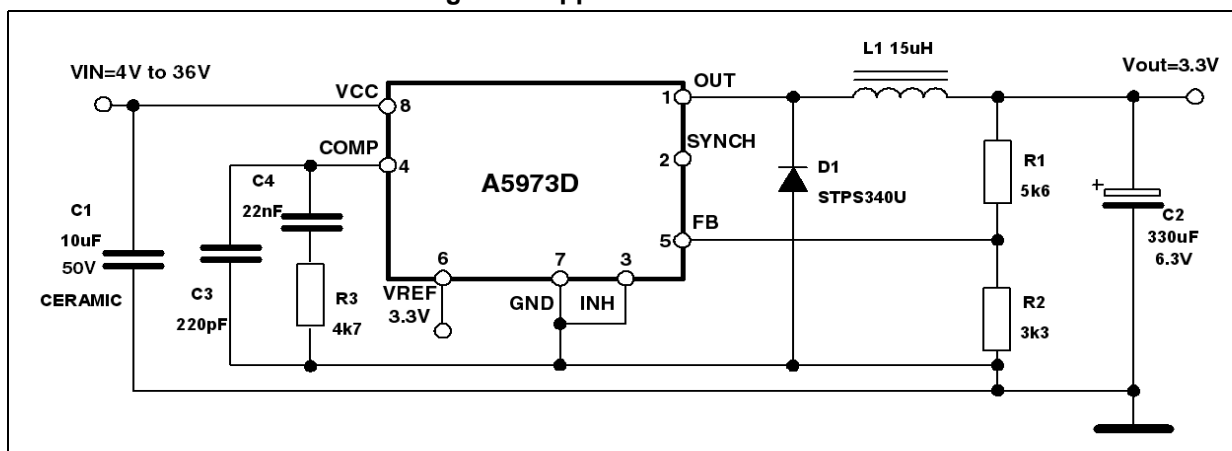
### Description

The A5973D is a step-down monolithic power switching regulator with a minimum switch current limit of 2.25 A so it is able to deliver up to 2 A DC current to the load depending on the application conditions. The output voltage can be set from 1.235 V to 35 V. The high current level is also achieved thanks to an HSOP8 package with exposed frame, that allows to reduce the  $R_{th(JA)}$  down to approximately 40 °C/W. The device uses an internal P-channel DMOS transistor (with a typical  $R_{DS(on)}$  of 250 mΩ) as switching element to minimize the size of the external components. An internal oscillator fixes the switching frequency at 250 kHz. Having a minimum input voltage of 4 V only it fits the automotive applications requiring the device operation even in cold crank conditions. A pulse-by-pulse current limit with the internal frequency modulation offers an effective constant current short-circuit protection.

### Features

- Qualified following the AEC-Q100 requirements (see PPAP for more details)
- 2 A DC output current
- Operating input voltage from 4 V to 36 V
- 3.3 V / ( $\pm 2\%$ ) reference voltage
- Output voltage adjustable from 1.235 V to 35 V
- Low dropout operation: 100% duty cycle
- 250 kHz internally fixed frequency
- Voltage feedforward
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- Synchronization
- Protection against feedback disconnection
- Thermal shutdown

Figure 1. Application schematic



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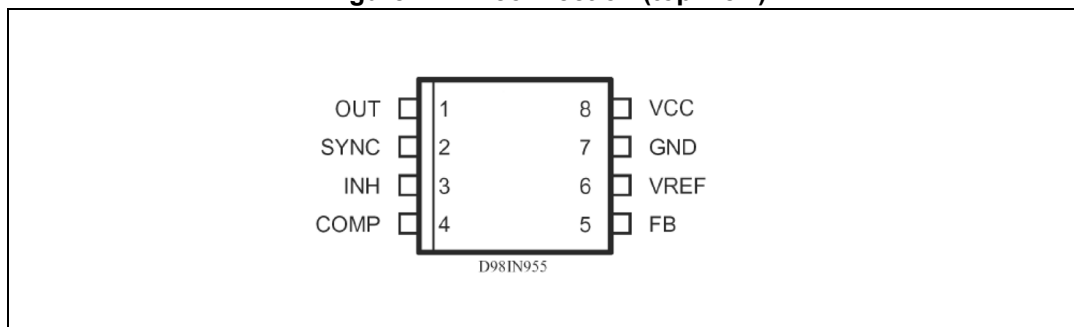
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# 1 Pin settings

## 1.1 Pin connection

Figure 2. Pin connection (top view)



## 1.2 Pin description

Table 1. Pin description

No.	Pin	Description
1	OUT	Regulator output.
2	SYNCH	Master/slave synchronization.
3	INH	A logical signal (active high) disables the device. If INH not used the pin must be grounded. When it is open an internal pull-up disables the device.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23 V. An external resistive divider is required for higher output voltages.
6	VREF	3.3 V $V_{REF}$ . No cap is requested for stability.
7	GND	Ground.
8	VCC	Unregulated DC input voltage.

## 2 Electrical data

### 2.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_8$	Input voltage	40	V
$V_1$	OUT pin DC voltage	-1 to 40	V
	OUT pin peak voltage at $\Delta t = 0.1 \mu\text{s}$	-5 to 40	V
$I_1$	Maximum output current	Int. limit.	
$V_4, V_5$	Analog pins	4	V
$V_3$	INH	-0.3 to $V_{CC}$	V
$V_2$	SYNCH	-0.3 to 4	V
$P_{TOT}$	Power dissipation at $T_A \leq 70 \text{ }^\circ\text{C}$	2.25	W
$T_J$	Operating junction temperature range	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^\circ\text{C}$

### 2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}$	Maximum thermal resistance junction ambient	40 <sup>(1)</sup>	$^\circ\text{C}/\text{W}$

1. Package mounted on the evaluation board.

### 3 Electrical characteristics

$T_J = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 12\text{ V}$ , unless otherwise specified.

**Table 4. Electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating input voltage range	$V_0 = 1.235\text{ V}$ ; $I_0 = 2\text{ A}$	4		36	V
$R_{DS(on)}$	MOSFET on resistance			0.250	0.5	$\Omega$
$I_L$	Maximum limiting current <sup>(1)</sup>	$V_{CC} = 5\text{ V}$	2.25	3	3.5	A
		$V_{CC} = 5\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$	2.5	3	3.5	
$f_{SW}$	Switching frequency		212	250	280	kHz
	Duty cycle		0		100	%
<b>Dynamic characteristics (see test circuit)</b>						
$V_5$	Voltage feedback	$4.4\text{ V} < V_{CC} < 36\text{ V}$ , $20\text{ mA} < I_0 < 2\text{ A}$	1.198	1.235	1.272	V
h	Efficiency	$V_0 = 5\text{ V}$ , $V_{CC} = 12\text{ V}$		90		%
<b>DC characteristics</b>						
$I_{qop}$	Total operating quiescent current			3	5	mA
$I_q$	Quiescent current	Duty cycle = 0; $V_{FB} = 1.5\text{ V}$			2.5	mA
$I_{qst-by}$	Total standby quiescent current	$V_{inh} > 2.2\text{ V}$		50	100	$\mu\text{A}$
		$V_{CC} = 36\text{ V}$ ; $V_{inh} > 2.2\text{ V}$		80	150	$\mu\text{A}$
<b>Inhibit</b>						
	INH threshold voltage	Device ON			0.8	V
		Device OFF	2.2			V
<b>Error amplifier</b>						
$V_{OH}$	High level output voltage	$V_{FB} = 1\text{ V}$	3.5			V
$V_{OL}$	Low level output voltage	$V_{FB} = 1.5\text{ V}$			0.4	V
$I_{o\ source}$	Source output current	$V_{COMP} = 1.9\text{ V}$ ; $V_{FB} = 1\text{ V}$	190	300		$\mu\text{A}$
$I_{o\ sink}$	Sink output current	$V_{COMP} = 1.9\text{ V}$ ; $V_{FB} = 1.5\text{ V}$	1	1.5		mA
$I_b$	Source bias current			2.5	4	$\mu\text{A}$
	DC open loop gain	$R_L = \infty$	50	65		dB
gm	Transconductance	$I_{COMP} = -0.1\text{ mA}$ to $0.1\text{ mA}$ ; $V_{COMP} = 1.9\text{ V}$		2.3		mS
<b>Synch function</b>						
	High input voltage	$V_{CC} = 4.4$ to $36\text{ V}$	2.5		$V_{REF}$	V
	Low input voltage	$V_{CC} = 4.4$ to $36\text{ V}$			0.74	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
	Slave synch current <sup>(2)</sup>	$V_{\text{synch}} = 0.74 \text{ V}$ $V_{\text{synch}} = 2.33 \text{ V}$	0.11 0.21		0.25 0.45	mA
	Master output amplitude	$I_{\text{source}} = 3 \text{ mA}$	2.75	3		V
	Output pulse width	no load, $V_{\text{synch}} = 1.65 \text{ V}$	0.20	0.35		$\mu\text{s}$
<b>Reference section</b>						
	Reference voltage	$I_{\text{REF}} = 0 \text{ to } 5 \text{ mA}$ $V_{\text{CC}} = 4.4 \text{ V to } 36 \text{ V}$	3.2	3.3	3.399	V
	Line regulation	$I_{\text{REF}} = 0 \text{ mA}$ $V_{\text{CC}} = 4.4 \text{ V to } 36 \text{ V}$		5	10	mV
	Load regulation	$I_{\text{REF}} = 0 \text{ mA}$		8	15	mV
	Short-circuit current		5	18	35	mA

1. With  $T_J = 85 \text{ }^\circ\text{C}$ ,  $I_{\text{lim\_min}} = 2.5 \text{ A}$ , assured by design, characterization and statistical correlation.
2. Guaranteed by design.

## 4 Datasheet parameters over the temperature range

The 100% of the population in the production flow is tested at three different ambient temperatures (-40 °C, +25 °C, +125 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C, +125 °C).

The device operation is so guaranteed when the junction temperature is inside the (-40 °C, +150 °C) temperature range. The designer can estimate the silicon temperature increase respect to the ambient temperature evaluating the internal power losses generated during the device operation (please refer to the [Section 2.2](#)).

However the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the  $T_{\text{SHTDWN}}$  (+150 °C  $\pm$  10 °C) temperature.

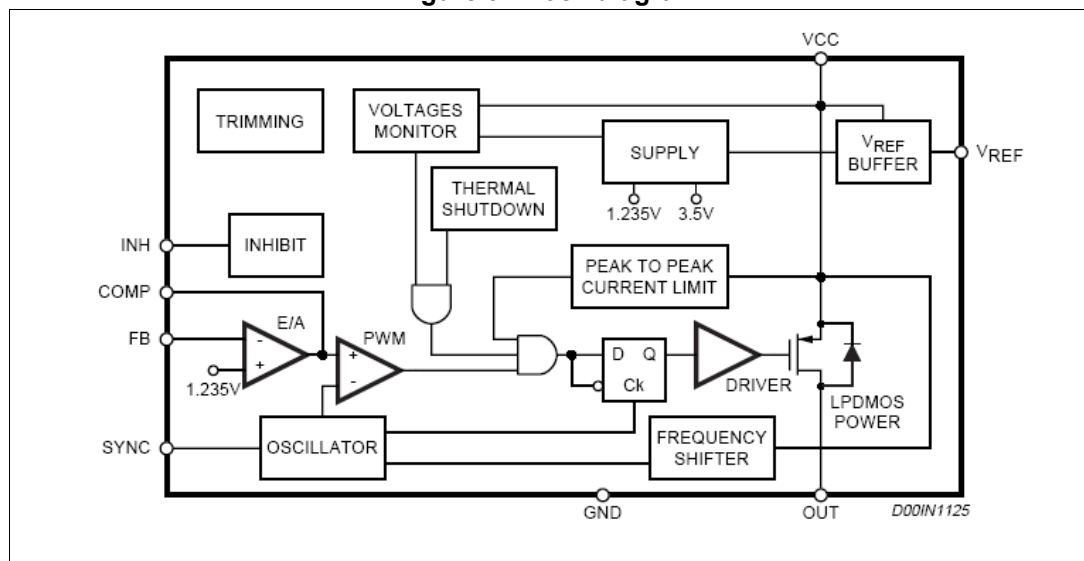
All the datasheet parameters can be guaranteed to a maximum junction temperature of +125 °C to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

## 5 Functional description

The main internal blocks are shown in the device block diagram in [Figure 3](#). They are:

- A voltage regulator supplying the internal circuitry. From this regulator, a 3.3 V reference voltage is externally available.
- A voltage monitor circuit which checks the input and the internal voltages.
- A fully integrated sawtooth oscillator with a frequency of  $250 \text{ kHz} \pm 15 \%$ , including also the voltage feedforward function and an input/output synchronization pin.
- Two embedded current limitation circuits which control the current that flows through the power switch. The pulse-by-pulse current limit forces the power switch OFF cycle by cycle if the current reaches an internal threshold, while the frequency shifter reduces the switching frequency in order to significantly reduce the duty cycle.
- A transconductance error amplifier.
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power.
- A high-side driver for the internal P-MOS switch.
- An inhibit block for standby operation.
- A circuit to implement the thermal protection function.

**Figure 3. Block diagram**



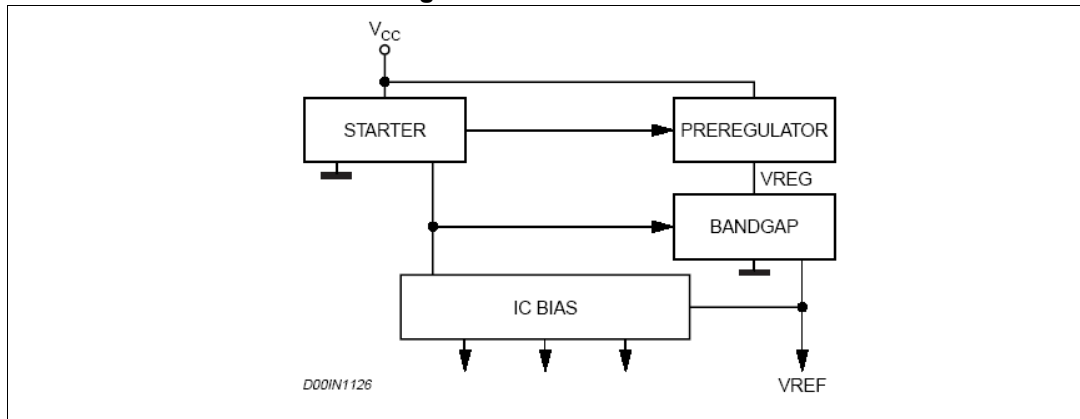
### 5.1 Power supply and voltage reference

The internal regulator circuit (shown in [Figure 4](#)) consists of a start-up circuit, an internal voltage pre-regulator, the bandgap voltage reference and the bias block that provides current to all the blocks. The starter supplies the start-up currents to the entire device when the input voltage goes high and the device is enabled (inhibit pin connected to ground). The pre-regulator block supplies the bandgap cell with a pre-regulated voltage  $V_{REG}$  that has a very low supply voltage noise sensitivity.

## 5.2 Voltages monitor

An internal block continuously senses the  $V_{CC}$ ,  $V_{REF}$  and  $V_{BG}$ . If the voltages go higher than their thresholds, the regulator begins operating. There is also a hysteresis on the  $V_{CC}$  (UVLO).

Figure 4. Internal circuit



## 5.3 Oscillator and synchronization

[Figure 5](#) shows the block diagram of the oscillator circuit.

The clock generator provides the switching frequency of the device, which is internally fixed at 250 kHz. The frequency shifter block acts to reduce the switching frequency in case of strong overcurrent or short-circuit. The clock signal is then used in the internal logic circuitry and is the input of the ramp generator and synchronizer blocks.

The ramp generator circuit provides the sawtooth signal, used for PWM control and the internal voltage feedforward, while the synchronizer circuit generates the synchronization signal. The device also has a synchronization pin which can work both as master and slave.

Beating frequency noise is an issue when more than one voltage rail is on the same board. A simple way to avoid this issue is to operate all the regulators at the same switching frequency.

The synchronization feature of a set of the A5973D is simply get connecting together their SYNCH pin. The device with highest switching frequency will be the MASTER and it provides the synchronization signal to the others. Therefore the SYNCH is an I/O pin to deliver or recognize a frequency signal. The synchronization circuitry is powered by the internal reference ( $V_{REF}$ ) so a small filtering capacitor ( $\geq 100$  nF) connected between  $V_{REF}$  pin and the signal ground of the master device is suggested for its proper operation. However when a set of synchronized devices populates a board it is not possible to know in advance the one working as master, so the filtering capacitor have to be designed for whole set of devices.

When one or more devices are synchronized to an external signal, its amplitude have to be in comply with specifications given in [Table 4 on page 6](#). The frequency of the synchronization signal must be, at a minimum, higher than the maximum guaranteed natural switching frequency of the device (275 kHz, see [Table 4](#)) while the duty cycle of the synchronization signal can vary from approximately 10% to 90%. The small capacitor under  $V_{REF}$  pin is required for this operation.

Figure 5. Oscillator circuit block diagram

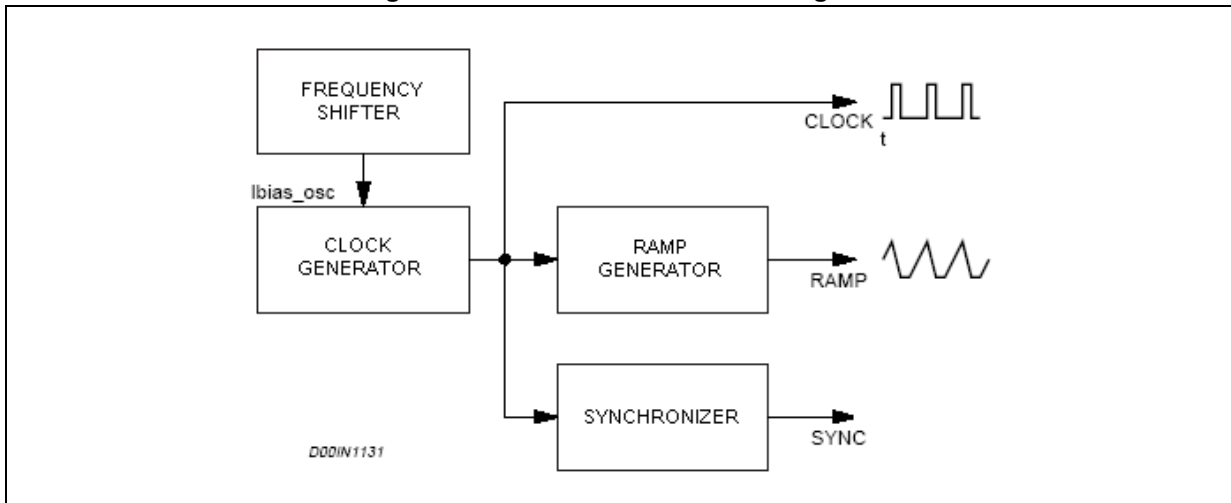
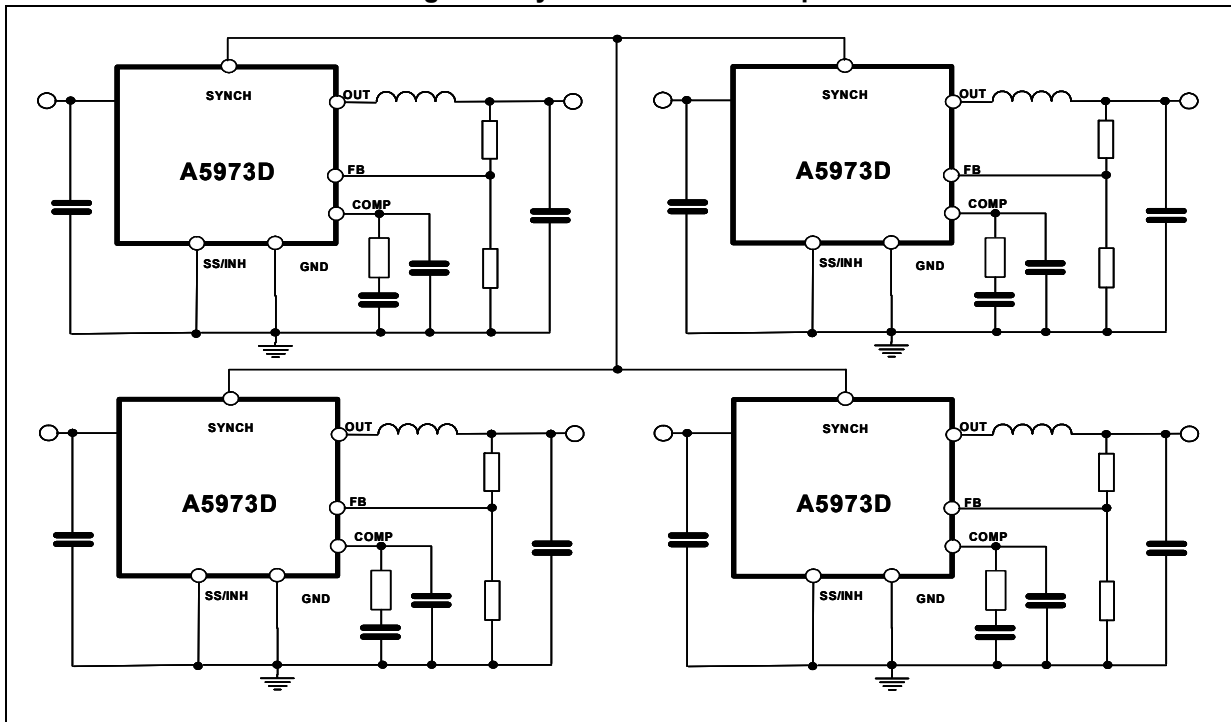


Figure 6. Synchronization example



## 5.4 Current protection

The A5973D device features two types of current limit protection: pulse-by-pulse and frequency foldback.

The schematic of the current limitation circuitry for the pulse-by-pulse protection is shown in [Figure 7](#). The output power PDMOS transistor is split into two parallel PDMOS transistors. The smallest one includes a resistor in series,  $R_{SENSE}$ . The current is sensed through  $R_{SENSE}$  and if it reaches the threshold, the mirror becomes unbalanced and the PDMOS is switched off until the next falling edge of the internal clock pulse. Due to this reduction of the



## 5.6 PWM comparator and power stage

This block compares the oscillator sawtooth and the error amplifier output signals to generate the PWM signal for the driving stage.

The power stage is a highly critical block, as it functions to guarantee a correct turn ON and turn OFF of the PDMOS. The turn ON of the power element, or more accurately, the rise time of the current at turn ON, is a very critical parameter. At a first approach, it appears that the faster the rise time, the lower the turn ON losses.

However, there is a limit introduced by the recovery time of the recirculation diode.

In fact, when the current of the power element is equal to the inductor current, the diode turns OFF and the drain of the power is able to go high. But during its recovery time, the diode can be considered a high value capacitor and this produces a very high peak current, responsible for numerous problems:

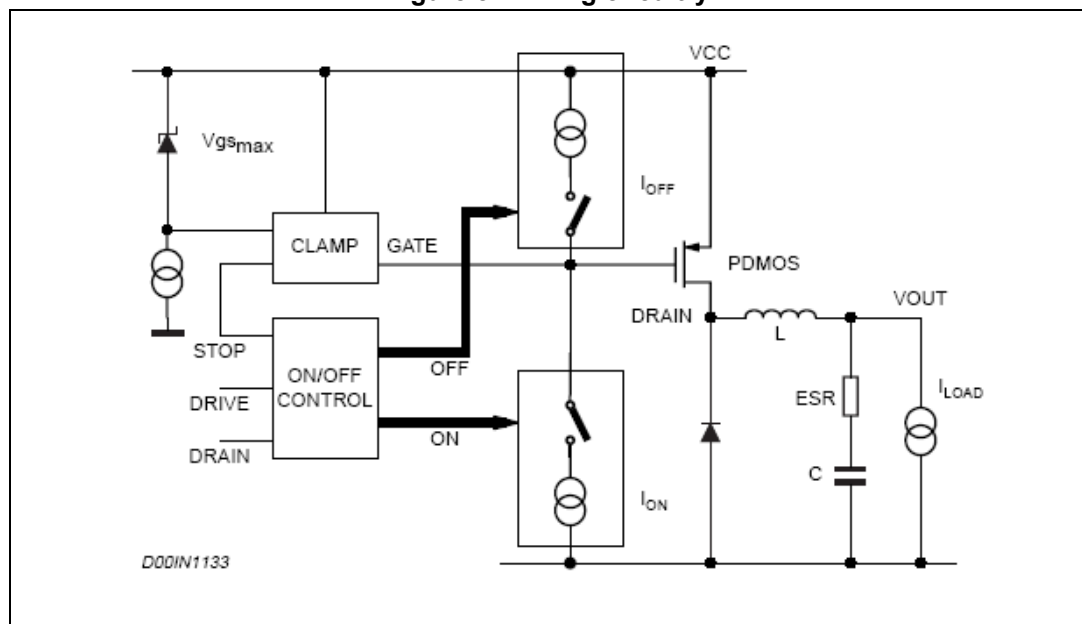
- Spikes on the device supply voltage that cause oscillations (and thus noise) due to the board parasites.
- Turn ON overcurrent leads to a decrease in the efficiency and system reliability.
- Major EMI problems.
- Shorter freewheeling diode life.

The fall time of the current during turn OFF is also critical, as it produces voltage spikes (due to the parasites elements of the board) that increase the voltage drop across the PDMOS.

In order to minimize these problems, a new driving circuit topology has been used and the block diagram is shown in [Figure 8](#). The basic idea is to change the current levels used to turn the power switch ON and OFF, based on the PDMOS and the gate clamp status.

This circuitry allows the power switch to be turned OFF and ON quickly and addresses the freewheeling diode recovery time problem. The gate clamp is necessary to ensure that  $V_{GS}$  of the internal switch does not go higher than  $V_{GSmax}$ . The ON/OFF Control block protects against any cross conduction between the supply line and ground.

Figure 8. Driving circuitry



## 5.7 Inhibit function

The inhibit feature is used to put the device in standby mode. With the INH pin higher than 2.2 V the device is disabled and the power consumption is reduced to less than 100  $\mu$ A. With the INH pin lower than 0.8 V, the device is enabled. If the INH pin is left floating, an internal pull up ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also  $V_{CC}$  compatible.

## 5.8 Thermal shutdown

The shutdown block generates a signal that turns OFF the power stage if the temperature of the chip goes higher than a fixed internal threshold ( $150 \pm 10$  °C). The sensing element of the chip is very close to the PDMOS area, ensuring fast and accurate temperature detection. A hysteresis of approximately 20 °C keeps the device from turning ON and OFF continuously.

## 6 Additional features and protection

### 6.1 Feedback disconnection

If the feedback is disconnected, the duty cycle increases towards the maximum allowed value, bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this hazardous condition, the device is turned OFF if the feedback pin is left floating.

### 6.2 Output overvoltage protection

Overvoltage protection, or OVP, is achieved by using an internal comparator connected to the feedback, which turns OFF the power stage when the OVP threshold is reached. This threshold is typically 30% higher than the feedback voltage.

When a voltage divider is required to adjust the output voltage ([Figure 15 on page 27](#)), the OVP intervention will be set at:

#### Equation 1

$$V_{\text{OVP}} = 1.3 \cdot \frac{R_1 + R_2}{R_2} \cdot V_{\text{FB}}$$

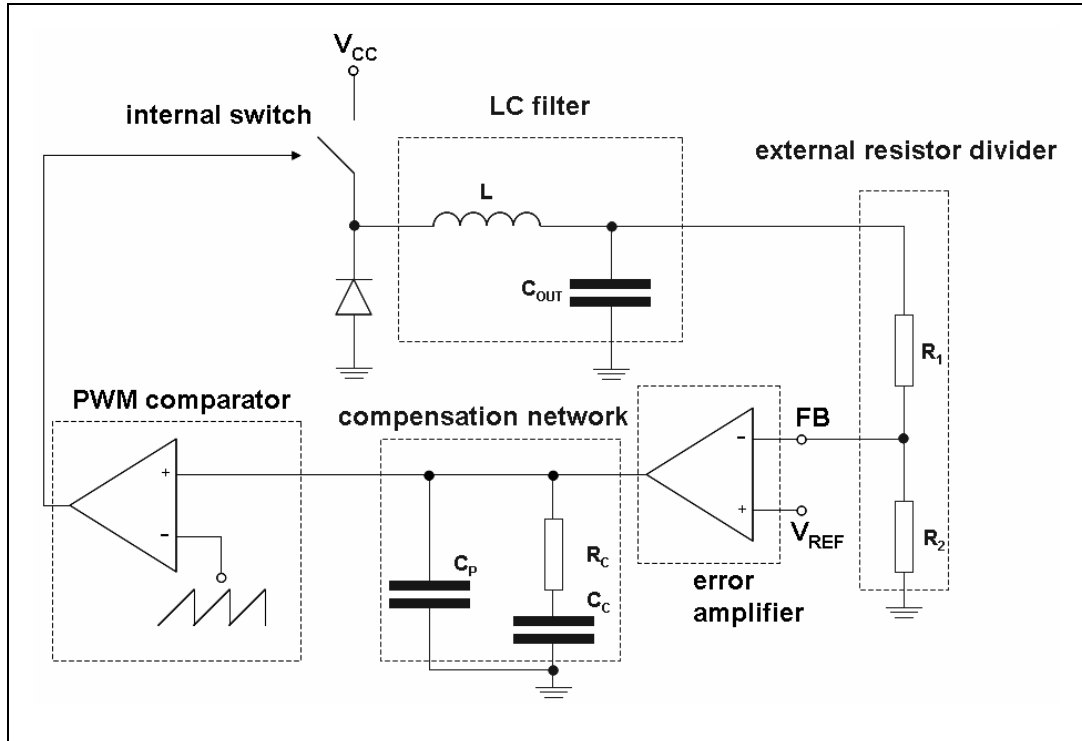
Where  $R_1$  is the resistor connected between the output voltage and the feedback pin, and  $R_2$  is between the feedback pin and ground.

### 6.3 Zero load

Due to the fact that the internal power is a PDMOS, no bootstrap capacitor is required and so the device works properly even with no load at the output. In this case it works in burst mode, with a random burst repetition rate.

# 7 Closing the loop

Figure 9. Block diagram of the loop



## 7.1 Error amplifier and compensation network

The output L-C filter of a step-down converter contributes with 180 degrees phase shift in the control loop. For this reason a compensation network between the COMP pin and GROUND is added. The simplest compensation network together with the equivalent circuit of the error amplifier are shown in *Figure 10*.  $R_C$  and  $C_C$  introduce a pole and a zero in the open loop gain.  $C_P$  does not significantly affect system stability but it is useful to reduce the noise of the COMP pin.

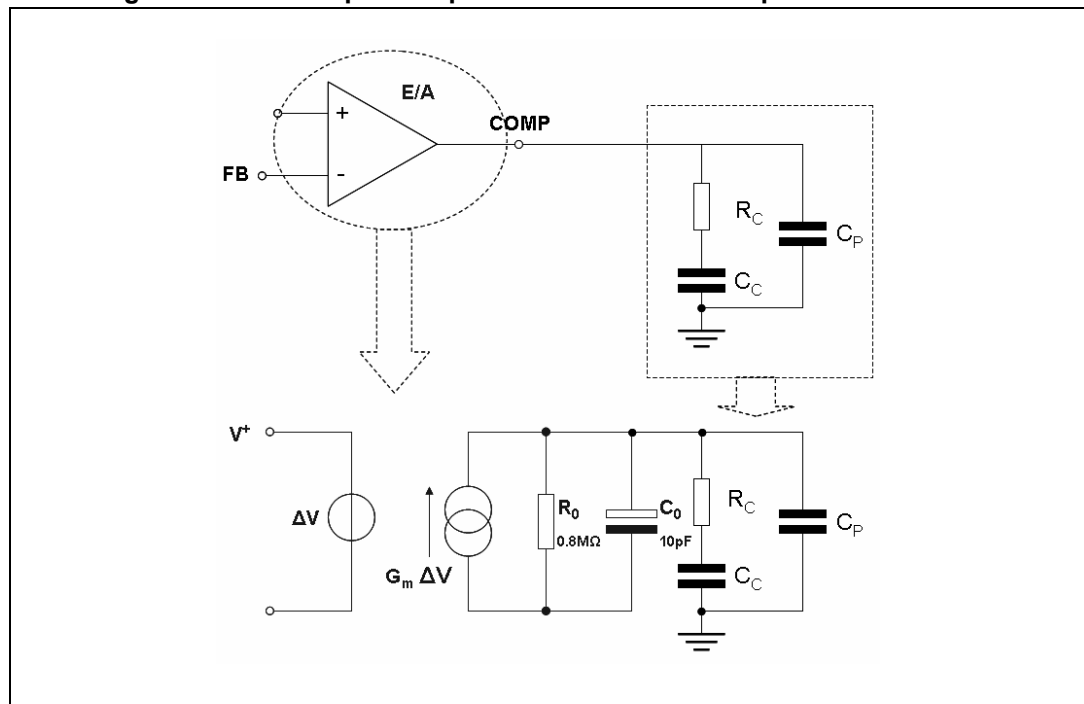
The transfer function of the error amplifier and its compensation network is:

### Equation 2

$$A_0(s) = \frac{A_{V0} \cdot (1 + s \cdot R_C \cdot C_C)}{s^2 \cdot R_0 \cdot (C_0 + C_P) \cdot R_C \cdot C_C + s \cdot (R_0 \cdot C_C + R_0 \cdot (C_0 + C_P) + R_C \cdot C_C) + 1}$$

Where  $A_{V0} = G_m \cdot R_0$

**Figure 10. Error amplifier equivalent circuit and compensation network**



The poles of this transfer function are (if  $C_C \gg C_0 + C_P$ ):

### Equation 3

$$F_{P1} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_C}$$

### Equation 4

$$F_{P2} = \frac{1}{2 \cdot \pi \cdot R_C \cdot (C_0 + C_P)}$$

whereas the zero is defined as:

**Equation 5**

$$F_{Z1} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_C}$$

$F_{P1}$  is the low frequency which sets the bandwidth, while the zero  $F_{Z1}$  is usually put near to the frequency of the double pole of the L-C filter (see below).  $F_{P2}$  is usually at a very high frequency.

## 7.2 LC filter

The transfer function of the L-C filter is given by:

**Equation 6**

$$A_{LC}(s) = \frac{R_{LOAD} \cdot (1 + ESR \cdot C_{OUT} \cdot s)}{s^2 \cdot L \cdot C_{OUT} \cdot (ESR + R_{LOAD}) + s \cdot (ESR \cdot C_{OUT} \cdot R_{LOAD} + L) + R_{LOAD}}$$

where  $R_{LOAD}$  is defined as the ratio between  $V_{OUT}$  and  $I_{OUT}$ .

If  $R_{LOAD} \gg ESR$ , the previous expression of  $A_{LC}$  can be simplified and becomes:

**Equation 7**

$$A_{LC}(s) = \frac{1 + ESR \cdot C_{OUT} \cdot s}{L \cdot C_{OUT} \cdot s^2 + ESR \cdot C_{OUT} \cdot s + 1}$$

The zero of this transfer function is given by:

**Equation 8**

$$F_O = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}}$$

$F_O$  is the zero introduced by the ESR of the output capacitor and it is very important to increase the phase margin of the loop.

The poles of the transfer function can be calculated through the following expression:

**Equation 9**

$$F_{PLC1,2} = \frac{-ESR \cdot C_{OUT} \pm \sqrt{(ESR \cdot C_{OUT})^2 - 4 \cdot L \cdot C_{OUT}}}{2 \cdot L \cdot C_{OUT}}$$

In the denominator of  $A_{LC}$  the typical second order system equation can be recognized:

**Equation 10**

$$s^2 + 2 \cdot \delta \cdot \omega_n \cdot s + \omega_n^2$$

If the damping coefficient  $\delta$  is very close to zero, the roots of the equation become a double root whose value is  $\omega_n$ .

Similarly for  $A_{LC}$  the poles can usually be defined as a double pole whose value is:

**Equation 11**

$$F_{PLC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}}$$

## 7.3 PWM comparator

The PWM gain is given by the following formula:

**Equation 12**

$$G_{PWM}(s) = \frac{V_{CC}}{(V_{OSCMAX} - V_{OSCMIN})}$$

where  $V_{OSCMAX}$  is the maximum value of a sawtooth waveform and  $V_{OSCMIN}$  is the minimum value. A voltage feedforward is implemented to ensure a constant GPWM. This is obtained by generating a sawtooth waveform directly proportional to the input voltage  $V_{CC}$ .

**Equation 13**

$$V_{OSCMAX} - V_{OSCMIN} = K \cdot V_{CC}$$

Where K is equal to 0.076. Therefore the PWM gain is also equal to:

**Equation 14**

$$G_{PWM}(s) = \frac{1}{K} = \text{const}$$

This means that even if the input voltage changes, the error amplifier does not change its value to keep the loop in regulation, thus ensuring a better line regulation and line transient response.

In summary, the open loop gain can be expressed as:

**Equation 15**

$$G(s) = G_{PWM}(s) \cdot \frac{R_2}{R_1 + R_2} \cdot A_O(s) \cdot A_{LC}(s)$$

### Example 1

Considering  $R_C = 2.7 \text{ k}\Omega$ ,  $C_C = 22 \text{ nF}$  and  $C_P = 220 \text{ pF}$ , the poles and zeroes of  $A_O$  are:

$$F_{P1} = 9 \text{ Hz}$$

$$F_{P2} = 256 \text{ kHz}$$

$$F_{Z1} = 2.68 \text{ kHz}$$

If  $L = 22 \text{ }\mu\text{H}$ ,  $C_{OUT} = 100 \text{ }\mu\text{F}$  and  $\text{ESR} = 80 \text{ m}\Omega$ , the poles and zeroes of  $A_{LC}$  become:

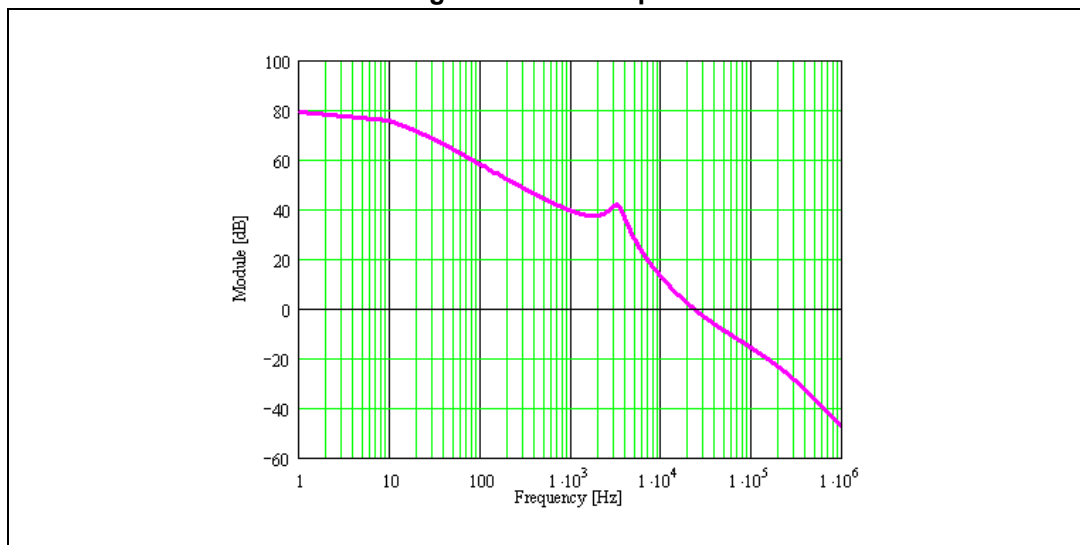
$$F_{PLC} = 3.39 \text{ kHz}$$

$$F_0 = 19.89 \text{ kHz}$$

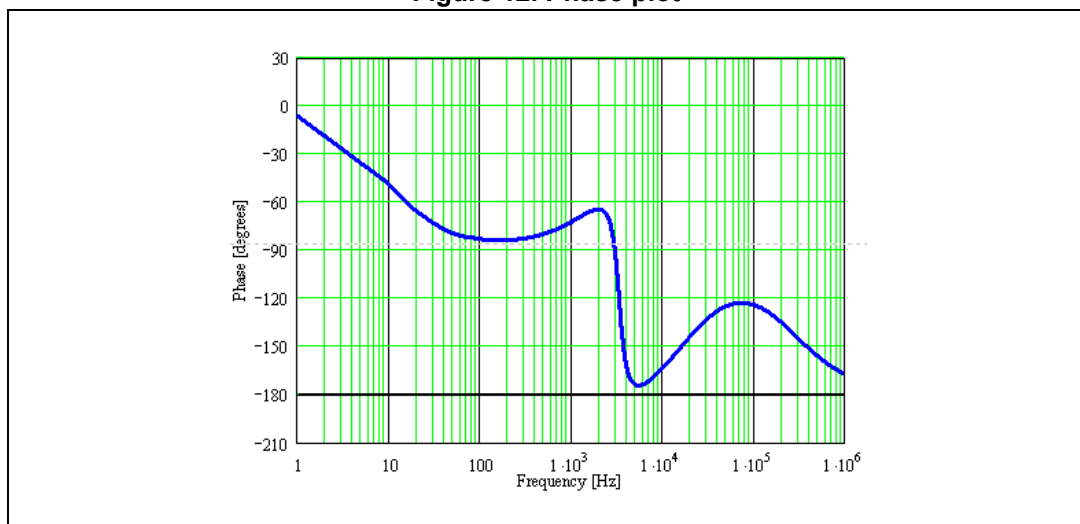
Finally  $R_1 = 5.6 \text{ k}\Omega$  and  $R_2 = 3.3 \text{ k}\Omega$ .

The gain and phase bode diagrams are plotted respectively in [Figure 11](#) and [Figure 12](#).

**Figure 11. Module plot**



**Figure 12. Phase plot**



The cut-off frequency and the phase margin are:

**Equation 16**

$$F_C = 22.8\text{KHz} \quad \text{phase margin} = 39.8^\circ$$

## 8 Application information

### 8.1 Component selection

- Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current, which can be up to the load current divided by two (worst case, with duty cycle of 50 %). For this reason, the quality of these capacitors has to be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS input current. The maximum RMS input current (flowing through the input capacitor) is:

#### Equation 17

$$I_{\text{RMS}} = I_{\text{O}} \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where  $\eta$  is the expected system efficiency,  $D$  is the duty cycle and  $I_{\text{O}}$  is the output DC current. This function reaches its maximum value at  $D = 0.5$  and the equivalent RMS current is equal to  $I_{\text{O}}$  divided by 2 (considering  $\eta = 1$ ). The maximum and minimum duty cycles are:

#### Equation 18

$$D_{\text{MAX}} = \frac{V_{\text{OUT}} + V_{\text{F}}}{V_{\text{INMIN}} - V_{\text{SW}}}$$

and

#### Equation 19

$$D_{\text{MIN}} = \frac{V_{\text{OUT}} + V_{\text{F}}}{V_{\text{INMAX}} - V_{\text{SW}}}$$

Where  $V_{\text{F}}$  is the freewheeling diode forward voltage and  $V_{\text{SW}}$  the voltage drop across the internal PDMOS. Considering the range  $D_{\text{MIN}}$  to  $D_{\text{MAX}}$ , it is possible to determine the max.  $I_{\text{RMS}}$  going through the input capacitor.

Capacitors that can be considered are:

**Electrolytic capacitors:**

These are widely used due to their low price and their availability in a wide range of RMS current ratings.

The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

**Ceramic capacitors:**

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to very low ESR).

The drawback is the considerably high cost.

**Tantalum capacitors:**

Very good, small tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current during charge.

Therefore, it is better to avoid this type of capacitor for the input filter of the device.

They can, however, be subjected to high surge current when connected to the power supply.

**Table 6. List of ceramic capacitors for the A5973D**

Manufacturer	Series	Capacitor value (µF)	Rated voltage (V)
TAIYO YUDEN	UMK325BJ106MM-T	10	50
MURATA	GRM42-2 X7R 475K 50	4.7	50

High dv/dt voltage spikes on the input side can be critical for DC/DC converters. A good power layout and input voltage filtering help to minimize this issue. In addition to the above considerations, a 1 µF/50 V ceramic capacitor as close as possible to the VCC and GND pins is always suggested to adequately filter VCC spikes.

- Output capacitor

The output capacitor is very important to meet the output voltage ripple requirement.

Using a small inductor value is useful to reduce the size of the choke but it increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system. If the zero goes to a very high frequency, its effect is negligible. For this reason, ceramic capacitors and very low ESR capacitors in general should be avoided.

Tantalum and electrolytic capacitors are usually a good choice for this purpose. A list of some tantalum capacitor manufacturers is provided in [Table 7: Output capacitor selection](#).

Table 7. Output capacitor selection

Manufacturer	Series	Cap. value ( $\mu\text{F}$ )	Rated voltage (V)	ESR ( $\text{m}\Omega$ )
Sanyo POSCAP <sup>(1)</sup>	TAE	100 to 470	4 to 16	25 to 35
	THB/C/E	100 to 470	4 to 16	25 to 55
AVX	TPS	100 to 470	4 to 35	50 to 200
KEMET	T494/5	100 to 470	4 to 20	30 to 200
Sprague	595D	220 to 390	4 to 20	160 to 650

1. POSCAP capacitors have some characteristics which are very similar to tantalum.

- Inductor

The inductor value is very important as it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20 - 40% of  $I_{Omax}$ , which is 0.4 - 0.8 A with  $I_{Omax} = 2$  A. The approximate inductor value is obtained using the following formula:

**Equation 20**

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \cdot T_{ON}$$

where  $T_{ON}$  is the ON time of the internal switch, given by  $D \cdot T$ . For example, with  $V_{OUT} = 3.3$  V,  $V_{IN} = 2$  V and  $\Delta I_O = 0.6$  A, the inductor value is about 17  $\mu\text{H}$ . The peak current through the inductor is given by:

**Equation 21**

$$I_{PK} = I_O + \frac{\Delta I}{2}$$

and it can be observed that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. So, when the peak current is fixed, a higher inductor value allows a higher value for the output current. In [Table 8](#) some inductor manufacturers are listed.

Table 8. Inductor selection

Manufacturer	Series	Inductor value ( $\mu\text{H}$ )	Saturation current (A)
Coilcraft	DO3316T	15 to 33	2.0 to 3.0
Coiltronics	UP1B	22 to 33	2.0 to 2.4
BI	HM76-3	15 to 33	2.5 to 3.3
Epcos	B82476	15 to 33	2 to 3
Würth Elektronik	74456115	15 to 33	2.5 to 3

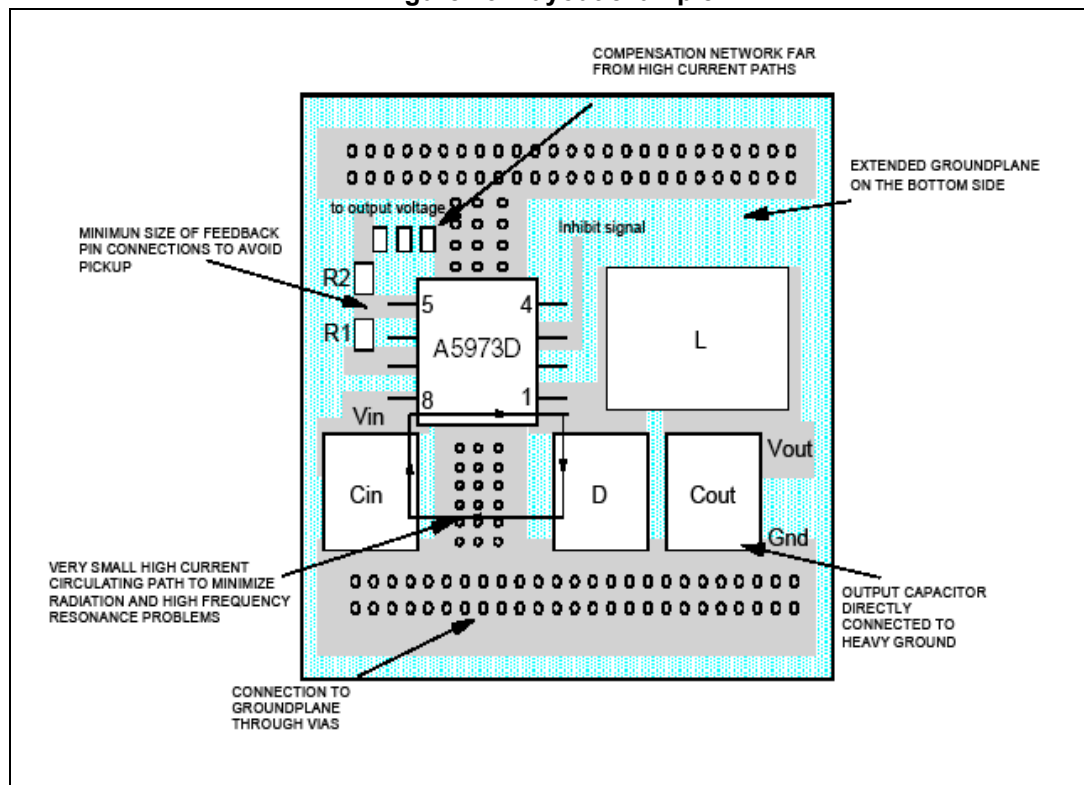
## 8.2 Layout considerations

The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths. A layout example is provided in [Figure 13](#).

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin connections to the external divider are very close to the device to avoid pick-up noise. Another important issue is the ground plane of the board. Since the package has an exposed pad, it is very important to connect it to an extended ground plane in order to reduce the thermal resistance junction to ambient.

Figure 13. Layout example



### 8.3 Thermal considerations

The dissipated power of the device is tied to three different sources:

- Conduction losses due to the not insignificant  $R_{\text{DS(ON)}}$ , which are equal to:

**Equation 22**

$$P_{\text{ON}} = R_{\text{DS(ON)}} \cdot (I_{\text{OUT}})^2 \cdot D$$

Where  $D$  is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between  $V_{\text{OUT}}$  and  $V_{\text{IN}}$ , but in practice it is substantially higher than this value to compensate for the losses in the overall application. For this reason, the switching losses related to the  $R_{\text{DS(ON)}}$  increases compared to an ideal case.

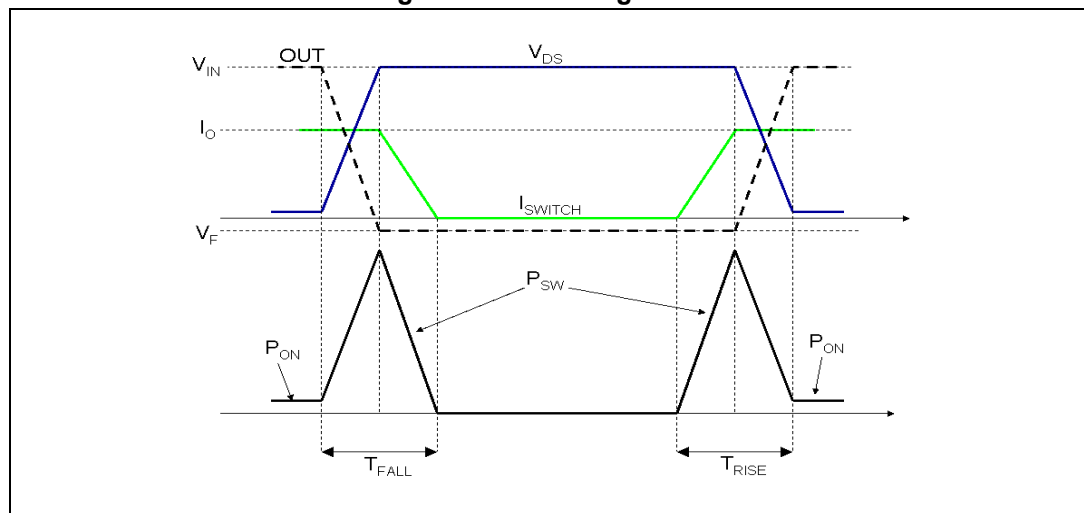
- Switching losses due to turning ON and OFF. These are derived using the following equation:

**Equation 23**

$$P_{\text{SW}} = V_{\text{IN}} \cdot I_{\text{OUT}} \cdot \frac{(T_{\text{ON}} + T_{\text{OFF}})}{2} \cdot F_{\text{SW}} = V_{\text{IN}} \cdot I_{\text{OUT}} \cdot T_{\text{SW}} \cdot F_{\text{SW}}$$

Where  $T_{\text{RISE}}$  and  $T_{\text{FALL}}$  represent the switching times of the power element that cause the switching losses when driving an inductive load (see [Figure 14](#)).  $T_{\text{SW}}$  is the equivalent switching time.

**Figure 14. Switching losses**



- Quiescent current losses.

**Equation 24**

$$P_{\text{Q}} = V_{\text{IN}} \cdot I_{\text{Q}}$$

Where  $I_{\text{Q}}$  is the quiescent current.