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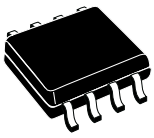
A5974D

Up to 2.5 A step-down switching regulator for automotive applications

Datasheet - production data



HSOP8 - exposed pad

Features

- Qualified following the AEC-Q100 requirements (see PPAP for more details)
- 2.5 A DC output current
- Operating input voltage from 4 V to 36 V
- 3.3 V / (± 2%) reference voltage
- Output voltage adjustable from 1.235 V to 35 V
- Low dropout operation: 100% duty cycle
- 250 kHz internally fixed frequency
- Voltage feed-forward
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- Synchronization
- Protection against feedback disconnection
- Thermal shutdown

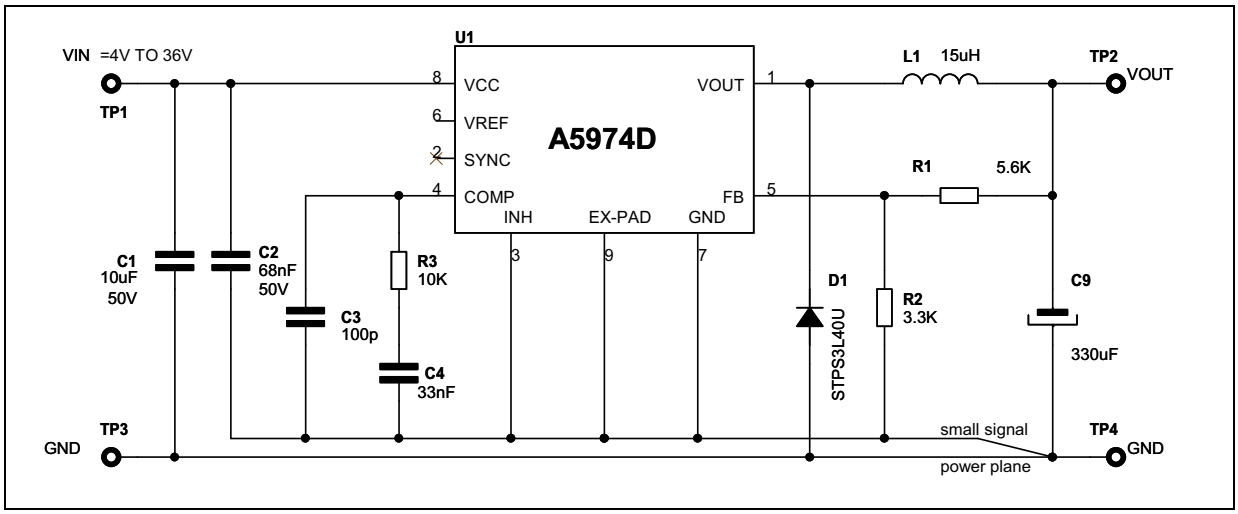
Application

- Dedicated to automotive applications

Description

The A5974D is a step-down monolithic power switching regulator with a minimum switch current limit of 3.1 A, so it is able to deliver up to 2.5 A DC current to the load depending on the application conditions. The output voltage can be set from 1.235 V to 35 V. The high current level is also achieved thanks to an HSOP8 package with an exposed frame, that allows to reduce the $R_{th(JA)}$ down to approximately 40 °C/W. The device uses an internal P-channel DMOS transistor (with a typical $R_{DS(on)}$ of 250 mΩ) as a switching element to minimize the size of the external components. An internal oscillator fixes the switching frequency at 250 kHz. Having a minimum input voltage of 4 V only it fits the automotive applications requiring the device operation even in cold crank conditions. A pulse-by-pulse current limit with the internal frequency modulation offers an effective constant current short-circuit protection.

Figure 1. Application schematic

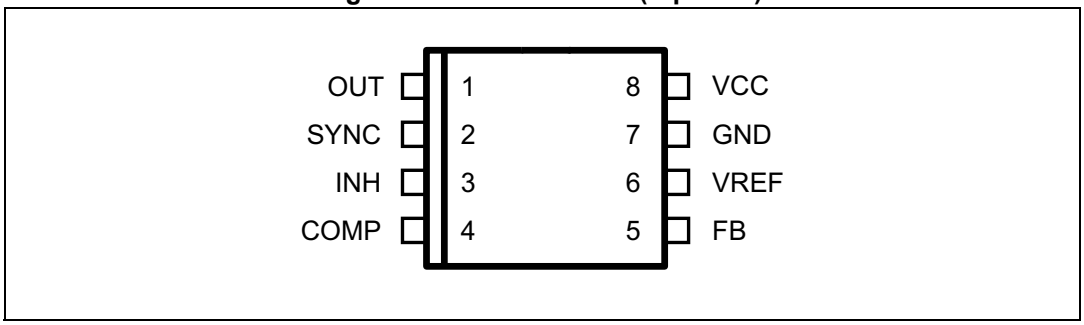


Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

No.	Pin	Description
1	OUT	Regulator output.
2	SYNCH	Master/slave synchronization.
3	INH	A logical signal (active high) disables the device. If INH not used the pin must be grounded. When it is open an internal pull-up disables the device.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23 V. An external resistive divider is required for higher output voltages.
6	VREF	3.3 V V_{REF}. No cap is requested for stability.
7	GND	Ground.
8	VCC	Unregulated DC input voltage.

2 Electrical data

2.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_8	Input voltage	40	V
V_1	OUT pin DC voltage OUT pin peak voltage at Δt = 0.1 µs	-1 to 40 -5 to 40	V V
I_1	Maximum output current	Int. limit.	
V_4, V_5	Analog pins	4	V
V_3	INH	-0.3 to V_{CC}	V
V_2	SYNCH	-0.3 to 4	V
P_{TOT}	Power dissipation at $T_A \leq 60$ °C	2.25	W
T_J	Operating junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum thermal resistance junction ambient	40(1)	°C/W

1. Package mounted on evaluation board.

3 Electrical characteristics

T_J = -40 °C to 125 °C, V_{CC} = 12 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating input voltage range	V_0 = 1.235 V; I_0 = 2 A	4		36	V
$R_{DS(on)}$	MOSFET on-resistance			0.250	0.5	Ω
I_L	Maximum limiting current	V_{CC} = 5 V	3.1	3.6	4.1	A
f_{SW}	Switching frequency		212	250	280	kHz
	Duty cycle		0		100	%
Dynamic characteristics						
V_5	Voltage feedback	4.4 V < V_{CC} < 36 V,20 mA < I_0 < 2 A	1.198	1.235	1.272	V
DC characteristics						
I_{qop}	Total operating quiescent current			3	5	mA
I_q	Quiescent current	Duty cycle = 0; V_{FB} = 1.5 V			2.5	mA
$I_{qst\text{-}by}$	Total standby quiescent current	V_{inh} > 2.2 V		50	100	µA
		$V_{C\,C}$ = 36 V; V_{inh} > 2.2 V		50	100	µA
Inhibit						
	INH threshold voltage	Device ON			0.8	V
		Device OFF	2.2			V
Error amplifier						
V_{OH}	High level output voltage	V_{FB} = 1 V	3.5			V
V_{OL}	Low level output voltage	V_{FB} = 1.5 V			0.4	V
$I_{o\ source}$	Source output current	V_{COMP} = 1.9 V; V_{FB} = 1 V	190	300		µA
$I_{o\ sink}$	Sink output current	V_{COMP} = 1.9 V; V_{FB} = 1.5 V	1	1.5		mA
I_b	Source bias current			2.5	4	µA
	DC open loop gain	R_L = ∞	50	65		dB
gm	Transconductance	I_{COMP} = -0.1 mA to 0.1 mA; V_{COMP} = 1.9 V		2.3		mS
Synch function						
	High input voltage	V_{CC} = 4.4 to 36 V	2.5		V_{REF}	V
	Low input voltage	V_{CC} = 4.4 to 36 V			0.74	V
	Slave synch current(1)	V_{synch} = 0.74 V, V_{synch} = 2.33 V	0.11 0.21		0.25 0.45	mA
	Master output amplitude	I_{source} = 3 mA	2.75	3		V
	Output pulse width	no load, V_{synch} = 1.65 V	0.20	0.35		µs

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Reference section						
	Reference voltage	I_{REF} = 0 to 5 mA V_{CC} = 4.4 V to 36 V	3.2	3.3	3.399	V
	Line regulation	I_{REF} = 0 mA V_{CC} = 4.4 V to 36 V		5	10	mV
	Load regulation	I_{REF} = 0 mA		8	15	mV
	short-circuit current		5	18	35	mA

1. Guaranteed by design.

4 Datasheet parameters over the temperature range

The 100% of the population in the production flow is tested at three different ambient temperatures (-40 °C; +25 °C, +125 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C; +125 °C).

The device operation is so guaranteed when the junction temperature is inside the (-40 °C; +150 °C) temperature range. The designer can estimate the silicon temperature increase respect to the ambient temperature evaluating the internal power losses generated during the device operation (please refer to the *Section 2.2*).

However the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHTDWN} (+150 °C ± 10 °C) temperature.

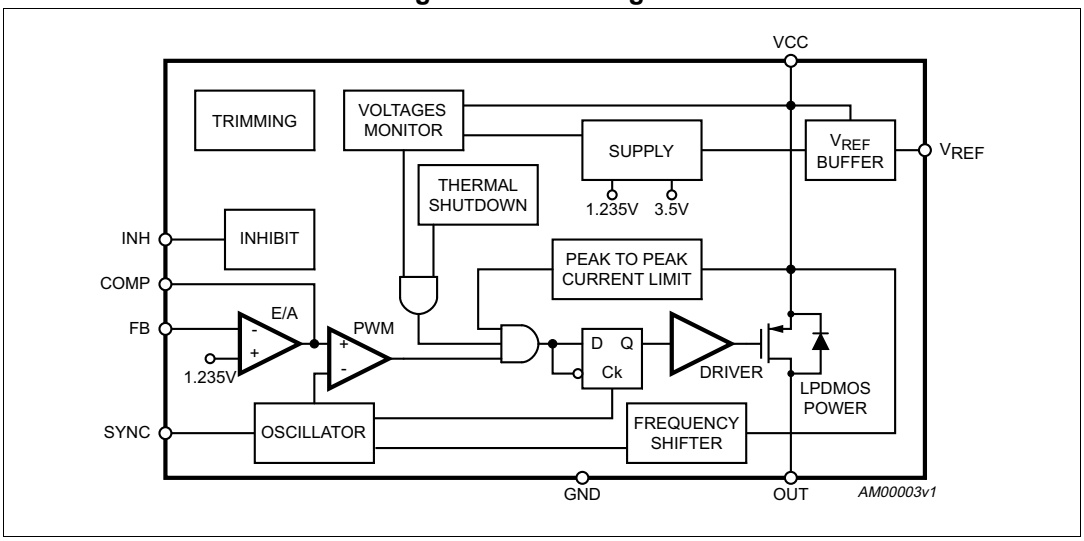
All the datasheet parameters can be guaranteed to a maximum junction temperature of +125 °C to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

5 Functional description

The main internal blocks are shown in the device block diagram in *Figure 3*. They are:

- A voltage regulator supplying the internal circuitry. From this regulator, a 3.3 V reference voltage is externally available.
- A voltage monitor circuit which checks the input and the internal voltages.
- A fully integrated sawtooth oscillator with a frequency of 250 kHz ± 15%, including also the voltage feed-forward function and an input/output synchronization pin.
- Two embedded current limitation circuits which control the current that flows through the power switch. The pulse-by-pulse current limit forces the power switch OFF cycle-by-cycle if the current reaches an internal threshold, while the frequency shifter reduces the switching frequency in order to significantly reduce the duty cycle.
- A transconductance error amplifier.
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power.
- A high-side driver for the internal P-MOS switch.
- An inhibit block for standby operation.
- A circuit to implement the thermal protection function.

Figure 3. Block diagram



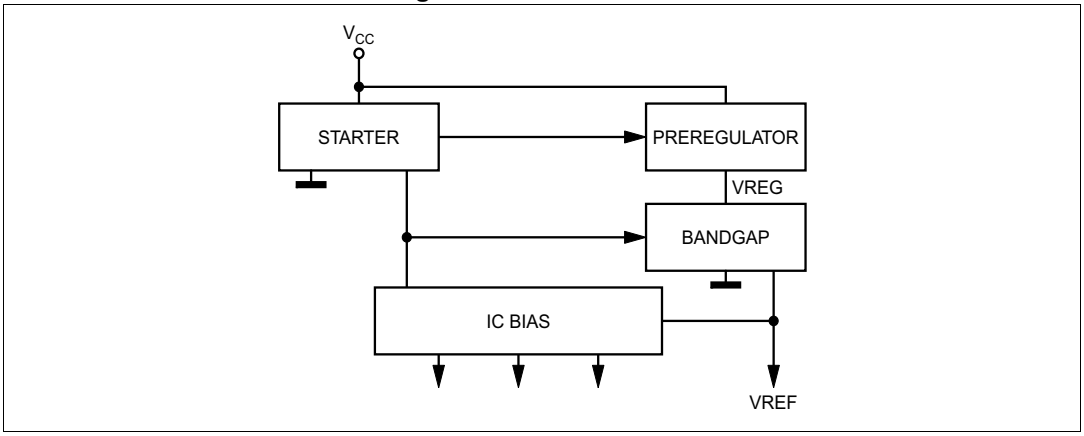
5.1 Power supply and voltage reference

The internal regulator circuit (shown in *Figure 4*) consists of a start-up circuit, an internal voltage pre-regulator, the bandgap voltage reference and the bias block that provides current to all the blocks. The starter supplies the start-up currents to the entire device when the input voltage goes high and the device is enabled (inhibit pin connected to ground). The pre-regulator block supplies the Bandgap cell with a pre-regulated voltage V_{REG} that has a very low supply voltage noise sensitivity.

5.2 Voltages monitor

An internal block continuously senses the V_{CC}, V_{ref} and V_{bg}. If the voltages go higher than their thresholds, the regulator begins operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 4. Internal circuit



5.3 Oscillator and synchronization

Figure 5 shows the block diagram of the oscillator circuit.

The clock generator provides the switching frequency of the device, which is internally fixed at 250 kHz. The frequency shifter block acts to reduce the switching frequency in case of strong overcurrent or short-circuit. The clock signal is then used in the internal logic circuitry and is the input of the ramp generator and synchronizer blocks.

The ramp generator circuit provides the sawtooth signal, used for PWM control and the internal voltage feed-forward, while the synchronizer circuit generates the synchronization signal. The device also has a synchronization pin which can work both as master and slave.

Beating frequency noise is an issue when more than one voltage rail is on the same board. A simple way to avoid this issue is to operate all the regulators at the same switching frequency.

The synchronization feature of a set of the A5974D is simply get connecting together their SYNCH pin. The device with highest switching frequency will be the MASTER and it provides the synchronization signal to the others. Therefore the SYNCH is an I/O pin to deliver or recognize a frequency signal. The synchronization circuitry is powered by the internal reference (V_{REF}) so a small filtering capacitor (≥ 100 nF) connected between V_{REF} pin and the signal ground of the master device is suggested for its proper operation. However when a set of synchronized devices populates a board it is not possible to know in advance the one working as a master, so the filtering capacitors have to be designed for whole set of devices.

When one or more devices are synchronized to an external signal, its amplitude have to be in comply with specifications given in *Table 4 on page 6*. The frequency of the synchronization signal must be, at a minimum, higher than the maximum guaranteed natural switching frequency of the device (275 kHz, see *Table 4*) while the duty cycle of the synchronization signal can vary from approximately 10% to 90%. The small capacitor under the V_{REF} pin is required for this operation.

Figure 5. Oscillator circuit block diagram

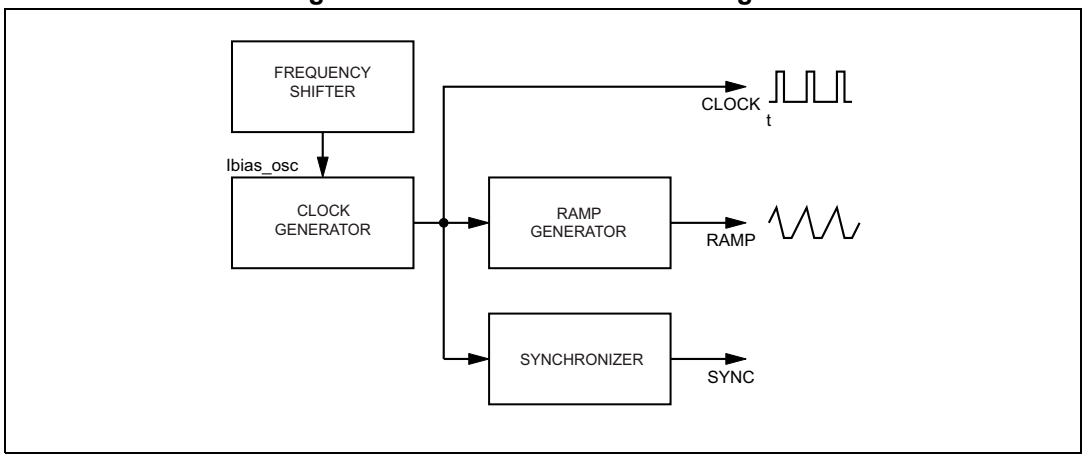
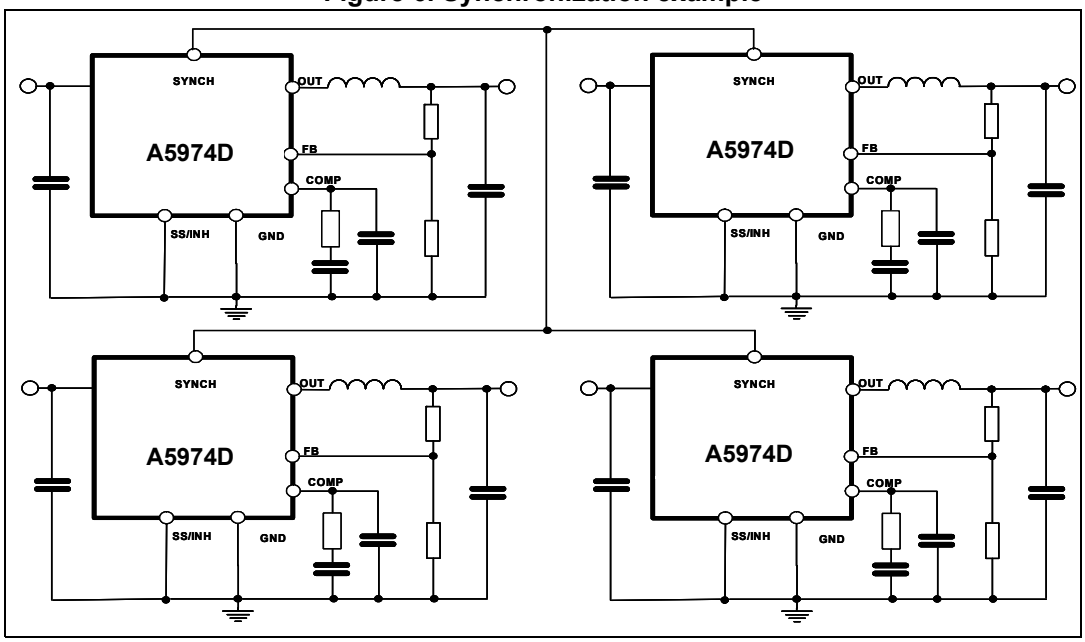


Figure 6. Synchronization example



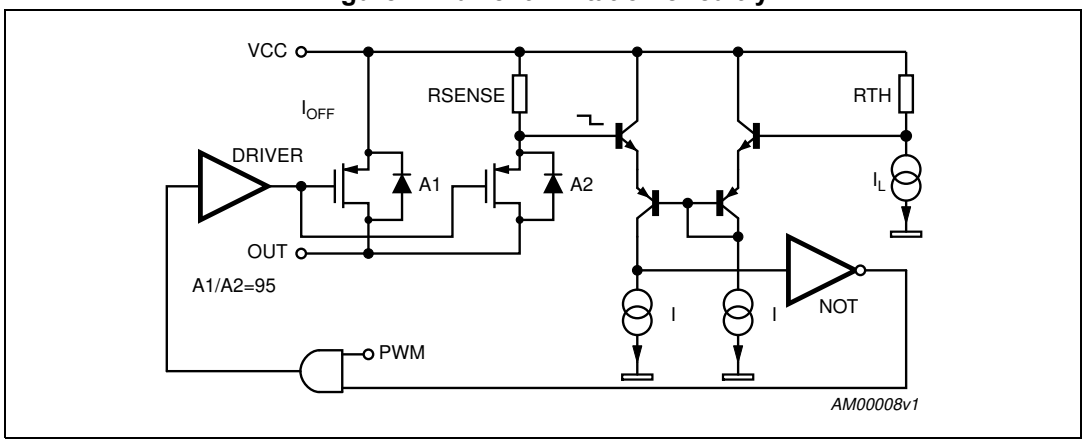
5.4 Current protection

The A5974D device features two types of current limit protection: pulse-by-pulse and frequency foldback.

The schematic of the current limitation circuitry for the pulse-by-pulse protection is shown in *Figure 7*. The output power PDMOS transistor is split into two parallel PDMOS transistors. The smallest one includes a resistor in series, R_{SENSE}. The current is sensed through R_{SENSE} and if it reaches the threshold, the mirror becomes unbalanced and the PDMOS is switched off until the next falling edge of the internal clock pulse. Due to this reduction of the ON time, the output voltage decreases. Since the minimum switch ON time necessary to sense the current in order to avoid a false overcurrent signal is too short to obtain a sufficiently low duty cycle at 250 kHz (see *Section 8.5 on page 31*), the output current in strong overcurrent or short-circuit conditions could be not properly limited. For this reason

the switching frequency is also reduced, thus keeping the inductor current under its maximum threshold. The frequency shifter (*Figure 5*) functions based on the feedback voltage. As the feedback voltage decreases (due to the reduced duty cycle), the switching frequency decreases also.

Figure 7. Current limitation circuitry



5.5 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (1.235 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage. The output (COMP) is connected to the external compensation network. The uncompensated error amplifier has the following characteristics:

Table 5. Uncompensated error amplifier characteristics

Description	Values
Transconductance	2300 µS
Low frequency gain	65 dB
Minimum sink/source voltage	1500 µA/300 µA
Output voltage swing	0.4 V/3.65 V
Input bias current	2.5 µA

The error amplifier output is compared to the oscillator sawtooth to perform PWM control.

5.6 PWM comparator and power stage

This block compares the oscillator sawtooth and the error amplifier output signals to generate the PWM signal for the driving stage.

The power stage is a highly critical block, as it functions to guarantee a correct turn-ON and turn-OFF of the PDMOS. The turn-ON of the power element, or more accurately, the rise time of the current at turn-ON, is a very critical parameter. At a first approach, it appears that the faster the rise time, the lower the turn-ON losses.

However, there is a limit introduced by the recovery time of the recirculation diode.

In fact, when the current of the power element is equal to the inductor current, the diode turns OFF and the drain of the power is able to go high. But during its recovery time, the diode can be considered a high value capacitor and this produces a very high peak current, responsible for numerous problems:

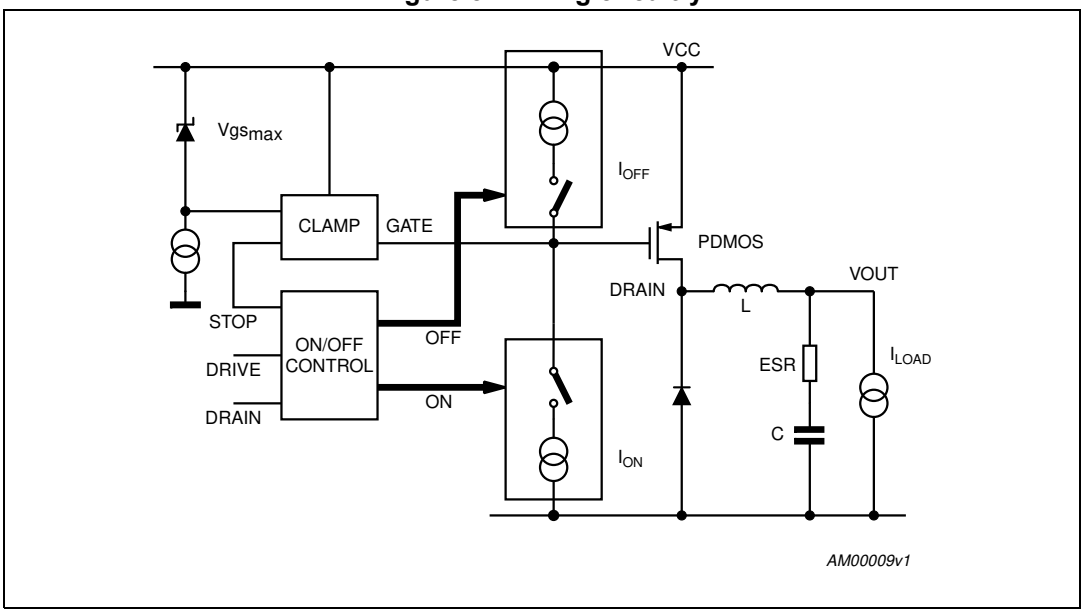
- Spikes on the device supply voltage that cause oscillations (and thus noise) due to the board parasites.
- Turn-ON overcurrent leads to a decrease in the efficiency and system reliability.
- Major EMI problems.
- Shorter freewheeling diode life.

The fall time of the current during turn-OFF is also critical, as it produces voltage spikes (due to the parasites elements of the board) that increase the voltage drop across the PDMOS.

In order to minimize these problems, a new driving circuit topology has been used and the block diagram is shown in *Figure 8*. The basic idea is to change the current levels used to turn the power switch ON and OFF, based on the PDMOS and the gate clamp status.

This circuitry allows the power switch to be turned OFF and ON quickly and addresses the freewheeling diode recovery time problem. The gate clamp is necessary to ensure that V_{GS} of the internal switch does not go higher than V_{GS}max. The ON/OFF Control block protects against any cross conduction between the supply line and ground.

Figure 8. Driving circuitry



5.7 Inhibit function

The inhibit feature is used to put the device into standby mode. With the INH pin higher than 2.2 V the device is disabled and the power consumption is reduced to less than 100 µA. With the INH pin lower than 0.8 V, the device is enabled. If the INH pin is left floating, an internal pull-up ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also V_{cc} compatible.

5.8 Thermal shutdown

The shutdown block generates a signal that turns OFF the power stage if the temperature of the chip goes higher than a fixed internal threshold (150 ± 10 °C). The sensing element of the chip is very close to the PDMOS area, ensuring fast and accurate temperature detection. A hysteresis of approximately 20 °C keeps the device from turning ON and OFF continuously.

6 Additional features and protection

6.1 Feedback disconnection

If the feedback is disconnected, the duty cycle increases towards the maximum allowed value, bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this hazardous condition, the device is turned OFF if the feedback pin is left floating.

6.2 Output overvoltage protection

Overvoltage protection, or OVP, is achieved by using an internal comparator connected to the feedback, which turns OFF the power stage when the OVP threshold is reached. This threshold is typically 30% higher than the feedback voltage.

When a voltage divider is required to adjust the output voltage (*Figure 19 on page 32*), the OVP intervention will be set at:

Equation 1

$$V_{OVP} = 1.3 \bullet \frac{R_1 + R_2}{R_2} \bullet V_{FB}$$

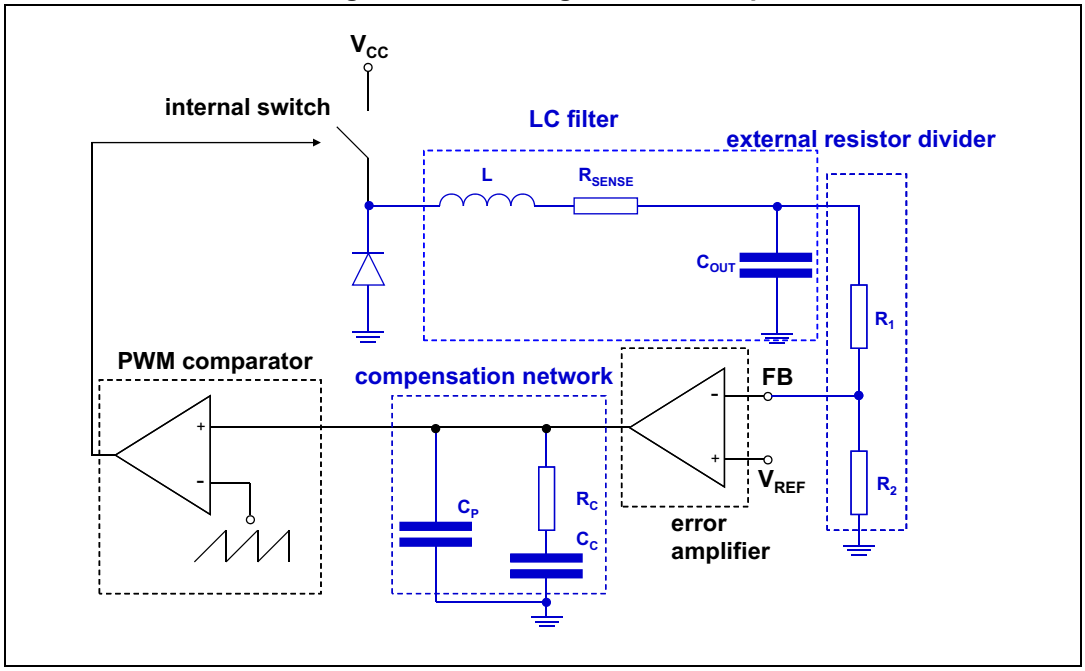
Where R_1 is the resistor connected between the output voltage and the feedback pin, and R_2 is between the feedback pin and ground.

6.3 Zero load

Due to the fact that the internal power is a PDMOS, no boostrap capacitor is required and so the device works properly even with no load at the output. In this case it works in burst mode, with a random burst repetition rate.

7 Closing the loop

Figure 9. Block diagram of the loop



7.1 Error amplifier and compensation network

The output L-C filter of a step-down converter contributes with 180° degrees phase shift in the control loop. For this reason a compensation network between the COMP pin and GROUND is added. The simplest compensation network together with the equivalent circuit of the error amplifier are shown in *Figure 10*. R_C and C_C introduce a pole and a zero in the open loop gain. CP does not significantly affect system stability but it is useful to reduce the noise of the COMP pin.

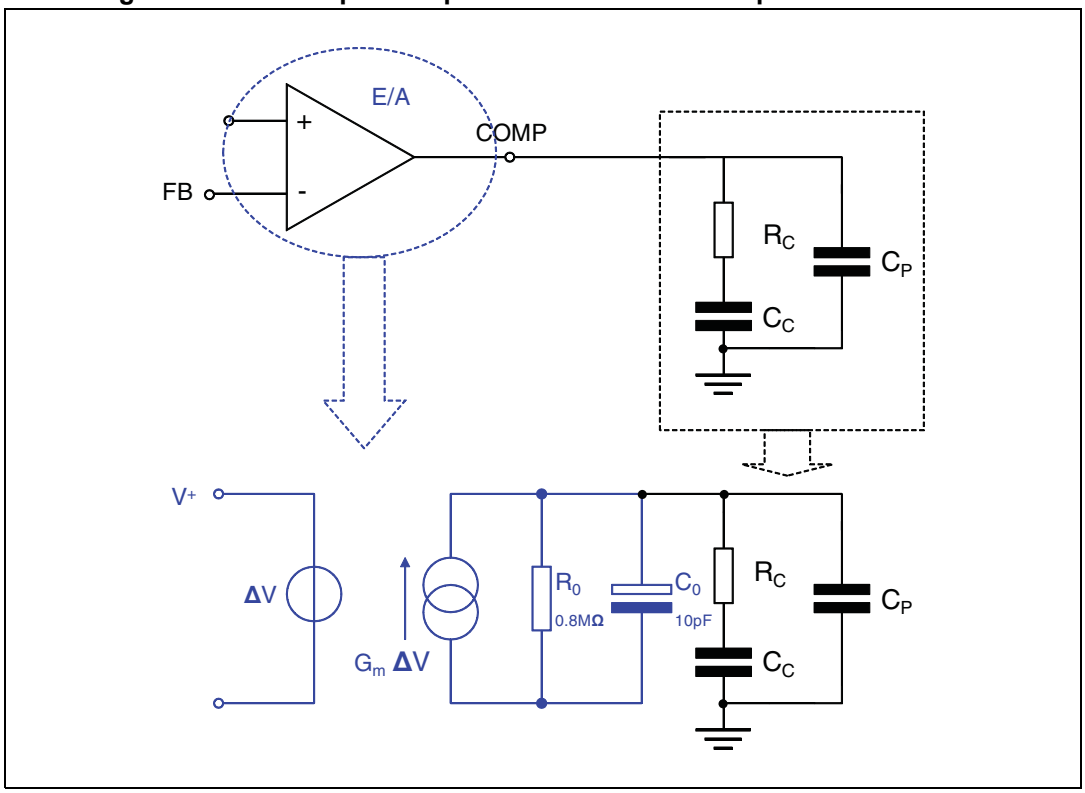
The transfer function of the error amplifier and its compensation network is:

Equation 2

$$A_0(s) = \frac{A_{V0} \bullet (1 + s \bullet R_c \bullet C_c)}{s^2 \bullet R_0 \bullet (C_0 + C_p) \bullet R_c \bullet C_c + s \bullet (R_0 \bullet C_c + R_0 \bullet (C_0 + C_p) + R_c \bullet C_c) + 1}$$

Where $A_{vo} = G_m \cdot R_o$

Figure 10. Error amplifier equivalent circuit and compensation network



The poles of this transfer function are (if $C_c >> C_0+C_P$):

Equation 3

$$F_{P1} = \frac{1}{2 \bullet \pi \bullet R_0 \bullet C_c}$$

Equation 4

$$F_{P2} = \frac{1}{2 \bullet \pi \bullet R_c \bullet (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 5

$$F_{Z1} = \frac{1}{2 \bullet \pi \bullet R_c \bullet C_c}$$

F_{P1} is the low frequency which sets the bandwidth, while the zero F_{Z1} is usually put near to the frequency of the double pole of the L-C filter (see *Section 7.2*). F_{P2} is usually at a very high frequency.

7.2 LC filter

The transfer function of the L-C filter is given by:

Equation 6

$$A_{LC}(s) = \frac{R_{LOAD} \bullet (1 + ESR \bullet C_{OUT} \bullet s)}{s^2 \bullet L \bullet C_{OUT} \bullet (ESR + R_{LOAD}) + s \bullet (ESR \bullet C_{OUT} \bullet R_{LOAD} + L) + R_{LOAD}}$$

where R_{LOAD} is defined as the ratio between V_{OUT} and I_{OUT}.

If R_{LOAD} >> ESR, the previous expression of A_{LC} can be simplified and becomes:

Equation 7

$$A_{LC}(s) = \frac{1 + ESR \bullet C_{OUT} \bullet s}{L \bullet C_{OUT} \bullet s^2 + ESR \bullet C_{OUT} \bullet s + 1}$$

The zero of this transfer function is given by:

Equation 8

$$F_O = \frac{1}{2 \bullet \pi \bullet ESR \bullet C_{OUT}}$$

F_0 is the zero introduced by the ESR of the output capacitor and it is very important to increase the phase margin of the loop.

The poles of the transfer function can be calculated through the following expression:

Equation 9

$$F_{PLC1,2} = \frac{-ESR \bullet C_{OUT} \pm \sqrt{(ESR \bullet C_{OUT})^2 - 4 \bullet L \bullet C_{OUT}}}{2 \bullet L \bullet C_{OUT}}$$

In the denominator of A_{LC} the typical second order system equation can be recognized:

Equation 10

$$s^2 + 2 \bullet \delta \bullet \omega_n \bullet s + \omega^2_n$$

If the damping coefficient δ is very close to zero, the roots of the equation become a double root whose value is ω_n.

Similarly for A_{LC} the poles can usually be defined as a double pole whose value is:

Equation 11

$$F_{PLC} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}}$$

7.3 PWM comparator

The PWM gain is given by the following formula:

Equation 12

$$G_{PWM}(s) = \frac{V_{cc}}{(V_{OSCMAX} - V_{OSCMIN})}$$

where V_{OSCMAX} is the maximum value of a sawtooth waveform and V_{OSCMIN} is the minimum value. A voltage feed-forward is implemented to ensure a constant GPWM. This is obtained by generating a sawtooth waveform directly proportional to the input voltage V_{CC}.

Equation 13

$$V_{OSCMAX} - V_{OSCMIN} = K \bullet V_{CC}$$

Where *K* is equal to 0.076. Therefore the PWM gain is also equal to:

Equation 14

$$G_{PWM}(s) = \frac{1}{K} = const$$

This means that even if the input voltage changes, the error amplifier does not change its value to keep the loop in regulation, thus ensuring a better line regulation and line transient response.

In summary, the open loop gain can be expressed as:

Equation 15

$$G(s) = G_{PWM}(s) \bullet \frac{R_2}{R_1 + R_2} \bullet A_O(s) \bullet A_{LC}(s)$$

Example 1

Considering R_C = 10 kΩ, C_C = 33 nF and C_P = 100 pF, the poles and zeroes of A_0 are:

F_{P1} = 6 Hz

F_{P2} = 150 kHz

F_{Z1} = 480 Hz

If L = 15 µH, DCR =56 mΩ, C_{OUT} = 330 µF and ESR = 25 mΩ, the poles and zeroes of A_{LC} become:

F_{PLC} = 2.2 kHz

$F_{Z\ ESR}$= 20 kHz

Finally R_1 = 5.6 kΩ and R_2 = 3.3 kΩ.

The gain and phase bode diagrams are plotted respectively in *Figure 11* and *Figure 12*.

Figure 11. Module plot

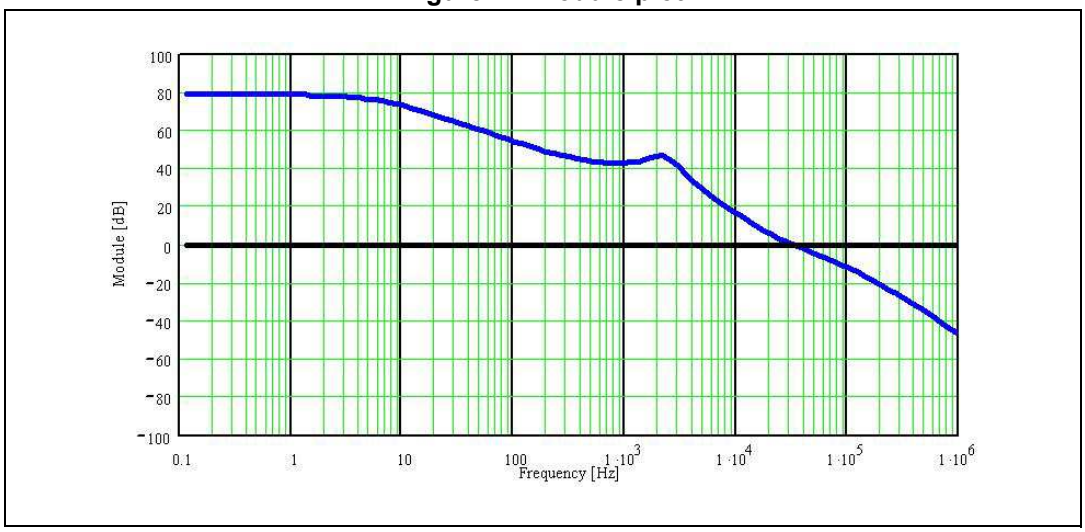
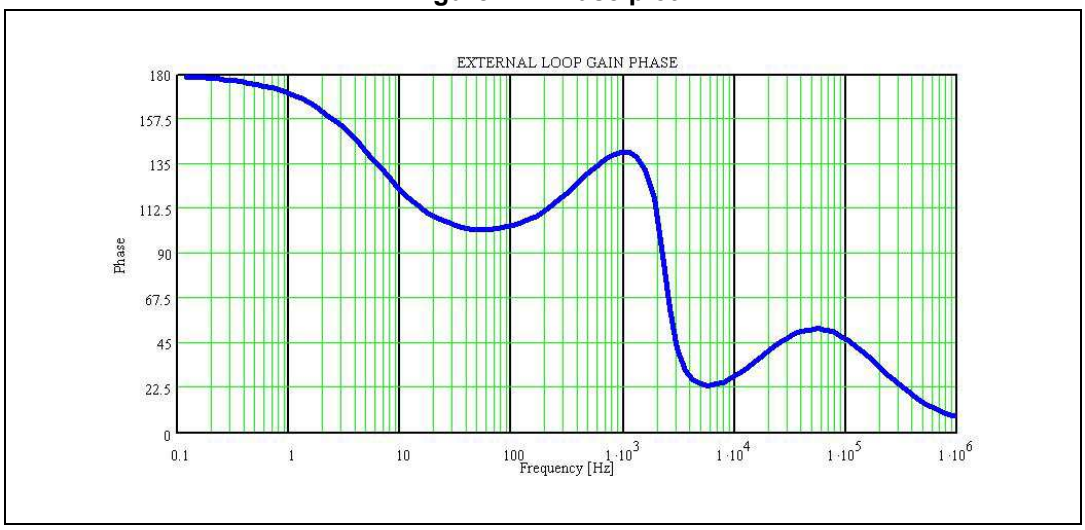


Figure 12. Phase plot



The cut-off frequency and the phase margin are:

Equation 16

$$F_C = 33KHz \quad \text{Phase margin} = 49°$$

8 Application information

8.1 Component selection

- Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current, which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors has to be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS input current. The maximum RMS input current (flowing through the input capacitor) is:

Equation 17

$$I_{RMS} = I_O \bullet \sqrt{D - \frac{2 \bullet D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where η is the expected system efficiency, D is the duty cycle and I_O is the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_O divided by 2 (considering η = 1). The maximum and minimum duty cycles are:

Equation 18

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 19

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

Where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX}, it is possible to determine the max. IRMS going through the input capacitor.

Capacitors that can be considered are:

Electrolytic capacitors:

These are widely used due to their low price and their availability in a wide range of RMS current ratings.

The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

Ceramic capacitors:

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to very low ESR).

The drawback is the considerably high cost.

Tantalum capacitors:

Very good, small tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current during charge.

Therefore, it is better to avoid this type of capacitor for the input filter of the device. They can, however, be subjected to high surge current when connected to the power supply.

Table 6. List of ceramic capacitors for the A5974D

Manufacturer	Series	Capacitor value (µF)	Rated voltage (V)
TAIYO YUDEN	UMK325BJ106MM-T	10	50
MURATA	GRM42-2 X7R 475K 50	4.7	50

High dv/dt voltage spikes on the input side can be critical for DC/DC converters. A good power layout and input voltage filtering help to minimize this issue. In addition to the above considerations, a 1 µF/50 V ceramic capacitor as close as possible to the VCC and GND pins is always suggested to adequately filter VCC spikes.

- **Output capacitor**

The output capacitor is very important to meet the output voltage ripple requirement.

Using a small inductor value is useful to reduce the size of the choke but it increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system. If the zero goes to a very high frequency, its effect is negligible. For this reason, ceramic capacitors and very low ESR capacitors in general should be avoided.

Tantalum and electrolytic capacitors are usually a good choice for this purpose. A list of some tantalum capacitor manufacturers is provided in *Table 7*.

Table 7. Output capacitor selection

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
Sanyo POSCAP(1)	TAE	47 to 680	2.5 to 10	25 to 35
	TV	68 to 330	4 to 6.3	25 to 40
AVX	TPS	100 to 470	4 to 35	50 to 200
KEMET	T494/5	100 to 470	4 to 20	30 to 200
Sprague	595D	220 to 390	4 to 20	160 to 650

1. POSCAP capacitors have some characteristics which are very similar to tantalum.

- **Inductor**

The inductor value is very important as it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20 - 40% of I_{omax}, which is 0.6 - 1.2 A with $I_O$max = 3 A. The approximate inductor value is obtained using the following formula:

Equation 20

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \bullet T_{ON}$$

where T_{ON} is the ON time of the internal switch, given by D · T. For example, with V_{OUT} = 3.3 V, V_{IN} = 12 V and ΔI_O = 0.9 A, the inductor value is about 12 µH. The peak current through the inductor is given by:

Equation 21

$$I_{PK} = I_O + \frac{\Delta I}{2}$$

and it can be observed that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. So, when the peak current is fixed, a higher inductor value allows a higher value for the output current. In *Table 8*, some inductor manufacturers are listed.

Table 8. Inductor selection

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	DO3316T	5.6 to 12	3.5 to 4.7
Coilcraft	MSS1260T	5.6 to 15	3.5 to 8
Wurth Elektronik	WE-PD L	4.7 to 27	3.55 to 6

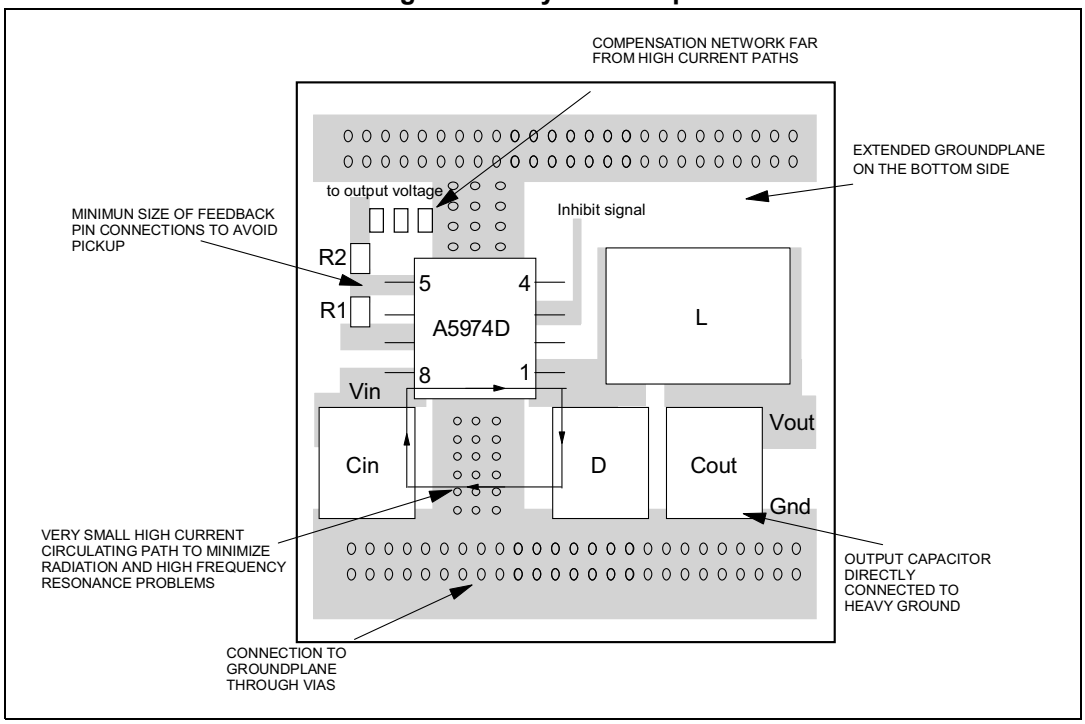
8.2 Layout considerations

The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths. A layout example is provided in *Figure 13*.

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin connections to the external divider are very close to the device to avoid pickup noise. Another important issue is the ground plane of the board. Since the package has an exposed pad, it is very important to connect it to an extended ground plane in order to reduce the thermal resistance junction to ambient.

Figure 13. Layout example



8.3 Thermal considerations

8.3.1 Thermal resistance R_{thJA}

$R_{thJ\text{-}A}$ is the equivalent static thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The static R_{thJA} measured on the application is about 40 °C/W.

The junction temperature of the device will be:

Equation 22

$$T_J = T_A + Rth_{J-A} \bullet P_{TOT}$$

The dissipated power of the device is tied to three different sources:

- Conduction losses due to the not insignificant R_{DSON}, which are equal to:

Equation 23

$$P_{ON} = R_{DSON} \bullet (I_{OUT})^2 \bullet D$$

Where *D* is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but in practice it is substantially higher than this value to compensate for the losses in the overall application. For this reason, the switching losses related to the R_{DSON} increase compared to an ideal case.

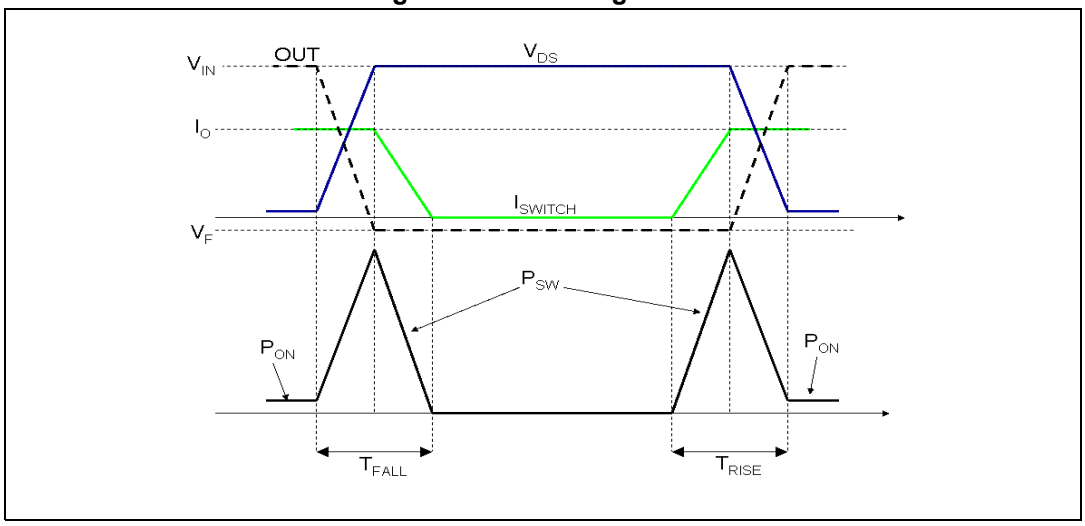
- Switching losses due to turning ON and OFF. These are derived using the following equation:

Equation 24

$$P_{SW} = V_{IN} \bullet I_{OUT} \bullet \frac{(T_{ON} + T_{OFF})}{2} \bullet F_{SW} = V_{IN} \bullet I_{OUT} \bullet T_{SW} \bullet F_{SW}$$

Where T_{RISE} and T_{FALL} represent the switching times of the power element that cause the switching losses when driving an inductive load (see *Figure 14*). T_{SW} is the equivalent switching time.

Figure 14. Switching losses



- Quiescent current losses

Equation 25

$$P_Q = V_{IN} \bullet I_Q$$

Where I_Q is the quiescent current.

Example 2

- V_{IN} = 12 V
- V_{OUT} = 3.3 V
- I_{OUT} = 2.5 A

$R_{DS(on)}$ has a typical value of 0.25 at 25 °C and increases up to a maximum value of 0.5. at 150 °C. We can consider a value of 0.4 Ω.

T_{SW} is approximately 70 ns.

I_Q has a typical value of 2.5 mA at V_{IN} = 12 V.