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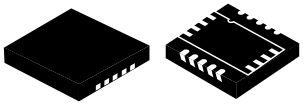
A6984

36 V, 400 mA automotive synchronous step-down switching regulator

Datasheet - production data



VFDFPN10 4 x 4 x 1.0 mm

Features

- AEC-Q100 qualified
- 400 mA DC output current
- 4.5 V to 36 V operating input voltage
- Synchronous rectification
- Low consumption mode or low noise mode
- 75 µA I_Q at light load (LCM V_{OUT} = 3.3 V)
- 13 µA $I_{Q\text{-}SHTDWN}$
- Adjustable f_{SW} (250 kHz - 600 kHz)
- Output voltage adjustable from 0.9 V
- No resistor divider required for 3.3 V V_{OUT}
- V_{BIAS} maximizes efficiency at light load
- 350 mA valley current limit
- Constant on-time control scheme
- PGOOD open collector
- Thermal shutdown

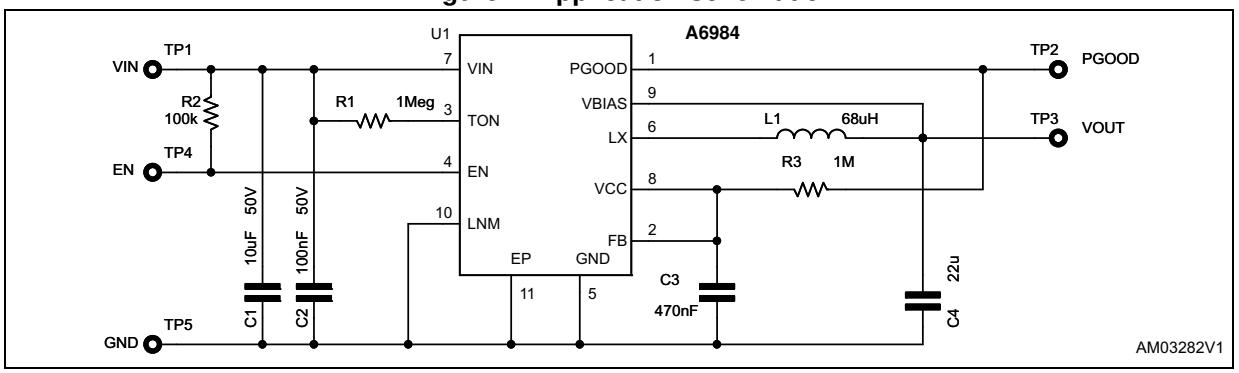
Applications

- Car body and ADAS applications (LCM)
- Car audio and low noise applications (LNM)

Description

The A6984 is a step-down monolithic switching regulator able to deliver up to 400 mA DC. The output voltage adjustability ranges from 0.9 V. The fixed 3.3 V VOUT requires no external resistor divider. The “low consumption mode” (LCM) is designed for applications active during car parking, so it maximizes the efficiency at light load with controlled output voltage ripple. The “low noise mode” (LNM) makes the switching frequency almost constant over the load current range, serving low noise application specifications such as car audio/sensors. The PGOOD open collector output can implement output voltage sequencing during the power-up phase. The synchronous rectification, designed for high efficiency at medium-heavy load, and the high switching frequency capability make the size of the application compact. Pulse-by-pulse current sensing on the low-side power element implements effective constant current protection. The package lead finishing guarantees side solderability, thus allowing visual inspection during manufacturing.

Figure 1. Application schematic

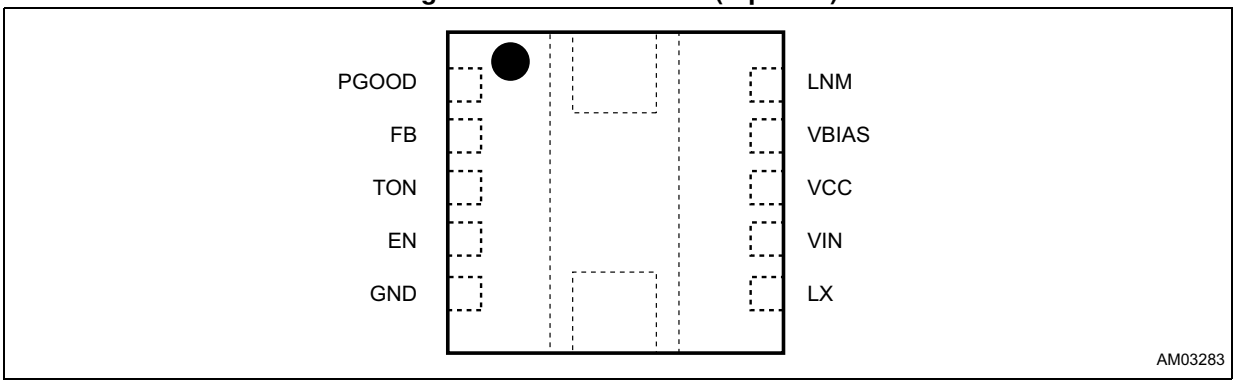


Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

N°	Pin	Description
1	PGOOD	The open collector output is driven low when the FB voltage is below the $V_{PGD\ L}$ threshold (see *Table 5*).
2	FB	Inverting input of the error amplifier
3	TON	A resistor connected between this pin and V_{IN} sets the switching frequency.
4	EN	Enable pin. A logical active high signal enables the device. Connect this pin to V_{IN} if not used.
5	GND	Power GND
6	LX	Switching node
7	VIN	DC input voltage
8	VCC	Embedded regulator output that supplies the main switching controller. Connect an external 1 µF capacitor for proper operation. An integrated LDO regulates VCC = 3.3 V if VBIAS voltage is < 2.4 V. VCC is connected to VBIAS through a MOSFET switch if VBIAS > 3.2 V and the embedded LDO is disabled to increase the light load efficiency.
9	VBIAS	Typically connected to the regulated output voltage. An external voltage reference can be used to supply the analog circuitry to increase the efficiency at light load. Connect to GND if not used.
10	LNM	Connect to V_{CC} for low noise mode (LNM) / to GND for low consumption mode (LCM) operation.

1.3 Maximum ratings

Stressing the device above the rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5* of this specification is not implied.

Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
dV_{IN}/dt (1)	Input slew rate	-	0.1	V/µs
V_{IN}	-	-0.3	38	V
LX	device ON		V_{IN} + 0.3	
	device OFF		25	
EN	see *Table 1*		V_{IN} + 0.3	
TON				
V_{CC}			6	
V_{BIAS}				
PGOOD			V_{CC} + 0.3	
FB				
LNM				
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range	-	-55 to 150	
T_{LEAD}	Lead temperature (soldering 10 sec.)	-	260	
I_{HS}, I_{LS}	High-side / low-side RMS switch current	-	400	mA

1. Maximum slew rate should be limited as detailed in *Section 5.1*.

1.4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ JA}$	Thermal resistance junction ambient (device soldered on STMicroelectronics evaluation board)	50	°C/W

1.5 ESD protection

Table 4. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	2	KV
	MM	200	V
	CDM	500	V

2 Electrical characteristics

T_J = -40 to 125 °C, V_{IN} = V_{EN} = 12 V, V_{BIAS} = 3.3 V unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		-	4.5		36	V
V_{IN_UVLO}	UVLO thresholds	Rising edge V_{CC} regulator V_{BIAS} = GND	-	3.1	3.8	4.5	
		Falling edge V_{CC} regulator V_{BIAS} = GND	-	2.9	3.6	4.3	
V_{OUT}	Fixed output voltage valley regulation	FB = V_{CC}, no load	-	3.23	3.3	3.37	
V_{FB}	Adjustable output voltage valley regulation	No load	-	0.88	0.9	0.92	
$R_{DSON\ HS}$	High-side RDSON	I_{SW} = 0.1 A	-	0.6	1.3	2.2	Ω
$R_{DSON\ LS}$	Low-side RDSON	I_{SW} = 0.1 A	-	0.4	1.0	1.9	
T_{OFF}	Minimum Low-side conduction time	V_{IN} = V_{EN} = 4.5 V	-	100	200	400	ns
Current limit and zero crossing comparator							
I_{VY}	Valley current limit	-	-	350	400	470	mA
I_{ZCD}	Zero crossing current threshold	-	(1)	12	27	46	
VCC regulator							
V_{CC}	VCC voltage	V_{FB} = 1 V, V_{BIAS} = GND	-	3	3.8	4.6	V
V_{BIAS}	V_{BIAS} falling threshold	-	-	2.4	2.6	2.8	
	V_{BIAS} rising threshold	-	-	2.6	2.9	3.2	
Power consumption							
I_{SHTDWN}	Shutdown current from V_{IN}	EN = GND	-	3	13	22	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
$I_{Q\ OPVIN}$	Quiescent current from V_{IN}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(2)	11	26	41	µA
		LCM - NO SWO $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = GND	(2)	90	160	230	
		LNM - SWO $V_{REF} < V_{FB} < V_{OVP}$ V_{BIAS} = 3.3 V	-	11	26	42	
		LNM - NO SWO $V_{REF} < V_{FB} < V_{OVP}$ V_{BIAS} = GND	-	200	320	440	
$I_{Q\ OPVBIAS}$	Quiescent current from V_{BIAS}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(2)	80	150	200	
		LNM - SWO $V_{REF} < V_{FB} < V_{OVP}$ V_{BIAS} = 3.3 V	-	180	300	390	
Enable							
EN	EN thresholds	Device inhibited	-	1.1	-	-	V
		Device enabled	-	-	-	2.6	
	EN hysteresis	-	(3)	-	650	-	mV
Overvoltage protection							
V_{OVP}	Overvoltage trip (V_{OVP}/V_{REF})	Rising edge		18	23	28	%
PGOOD							
$V_{PGD\ L}$	Power good LOW threshold	V_{FB} rising edge (PGOOD high impedance)	(3)	-	90	-	%
		V_{FB} falling edge (PGOOD low impedance)	-	84	88	92	
$V_{PGD\ H}$	Power good HIGH threshold	Internal FB rising edge (PGOOD low impedance) $V_{FB} = V_{CC}$	-	118	123	128	
		Internal FB falling edge (PGOOD high impedance) $V_{FB} = V_{CC}$	(3)	-	100	-	
V_{PGOOD}	PGOOD open collector output	$V_{IN} > V_{IN\_UVLO\_H}$, V_{FB}=GND 4 mA sinking load	-	-	-	0.6	V
		$2.9 < V_{IN} < V_{IN\_UVLO\_H}$ 100 µA sinking load	-	-	-	0.6	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature	-	(3)	-	150	-	°C
T_{HYS}	Thermal shutdown hysteresis	-	(3)	-	20	-	°C

1. Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.
2. LCM enables SLEEP mode (part of the internal circuitry is disabled) at light load.
3. Not tested in production.

3 Datasheet parameters over the temperature range

100% of the population in the production flow is tested at three different ambient temperatures (-40 °C; 25 °C, 125 °C) to guarantee datasheet parameters within the junction temperature range (-40 °C to 125 °C).

Device operation is guaranteed when the junction temperature is within the -40 °C to 150 °C temperature range. The designer can estimate the silicon temperature increase with respect to the ambient temperature evaluating the internal power losses generated during the device operation.

However, the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHTDWN} (+150 °C min) temperature.

All the datasheet parameters can be guaranteed to a maximum junction temperature of +125 °C to avoid triggering the thermal shutdown protection during the testing phase due to self-heating.

4 Device description

The A6984 device is based on a “Constant On-Time” (COT) control scheme with frequency feed-forward correction over the V_{IN} range. As a consequence the device features fast load transient response, almost constant switching frequency operation over the input voltage range and simple stability control.

The switching frequency can be adjusted in the 250 kHz - 600 kHz range.

The LNM (low noise mode) implements constant PWM control to minimize the voltage ripple over the load range, the LCM (low consumption mode) pulse skipping technique to increase the efficiency at the light load.

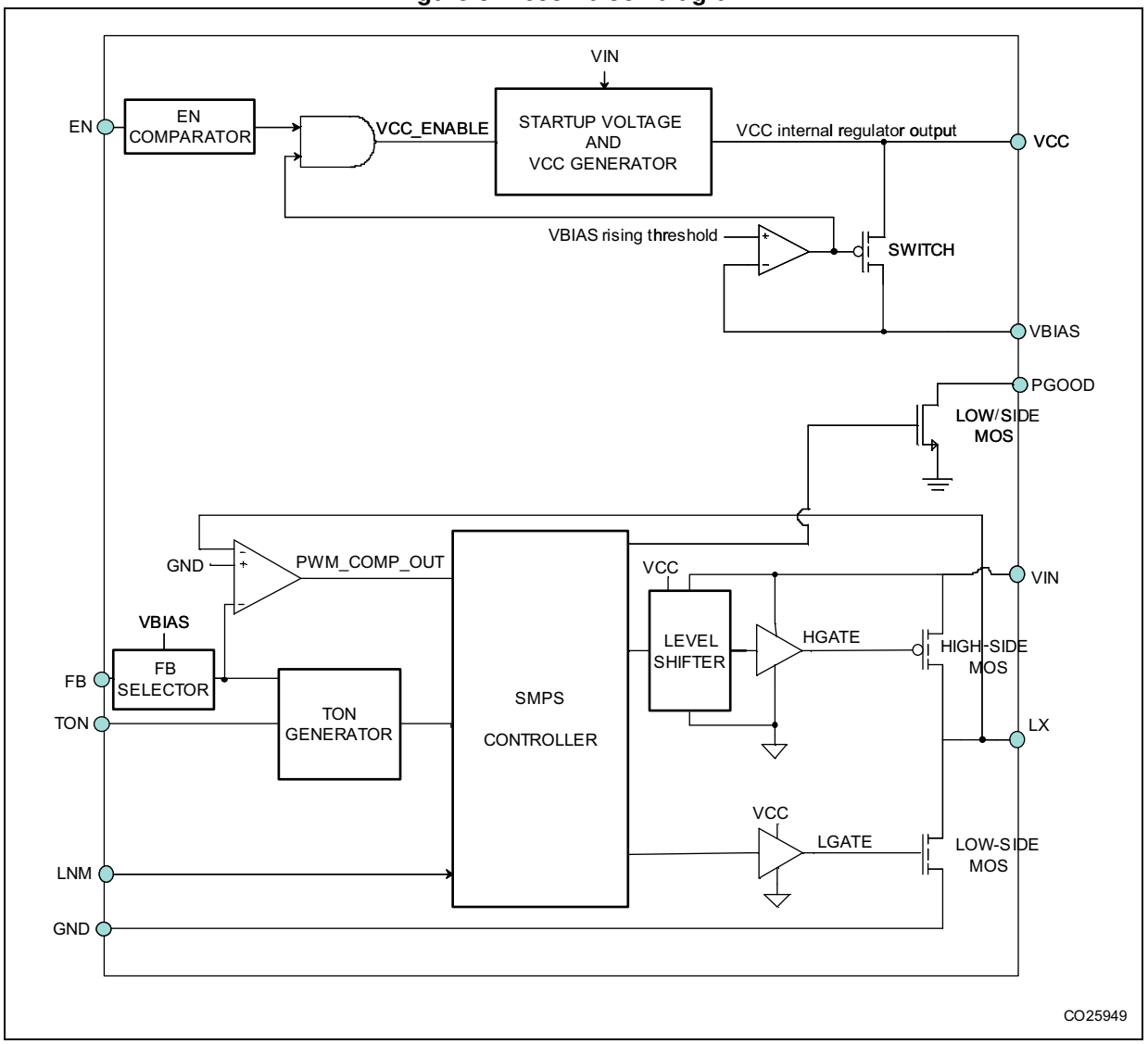
No external resistor divider is required to regulate fixed 3.3 V output voltage, connecting FB to the V_{CC} pin and V_{BIAS} to the regulated output voltage (see *Figure 1 on page 1*). An external voltage divider implements the output voltage adjustability.

The switchover capability of the internal regulator derives a portion of the quiescent current from an external voltage source (V_{BIAS} pin is typically connected to the regulated output voltage) to maximize the efficiency at the light load.

The device main internal blocks are shown in the block diagram in *Figure 6 on page 15*:

- The bandgap reference voltage
- The on-time controller
- A “pulse width modulation” (PWM) comparator and the driving circuitry of the embedded power elements
- The SMPS controller block
- The soft-start block to ramp the current limitation
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the VBIAS pin is connected to an external output voltage
- The current limitation circuit to implement the constant current protection, sensing pulse-by-pulse low-side switch current.
- A circuit to implement the thermal protection function
- LNM pin strapping sets the LNM/LCM mode
- The PG (“Power Good”) open collector output
- The thermal protection circuitry

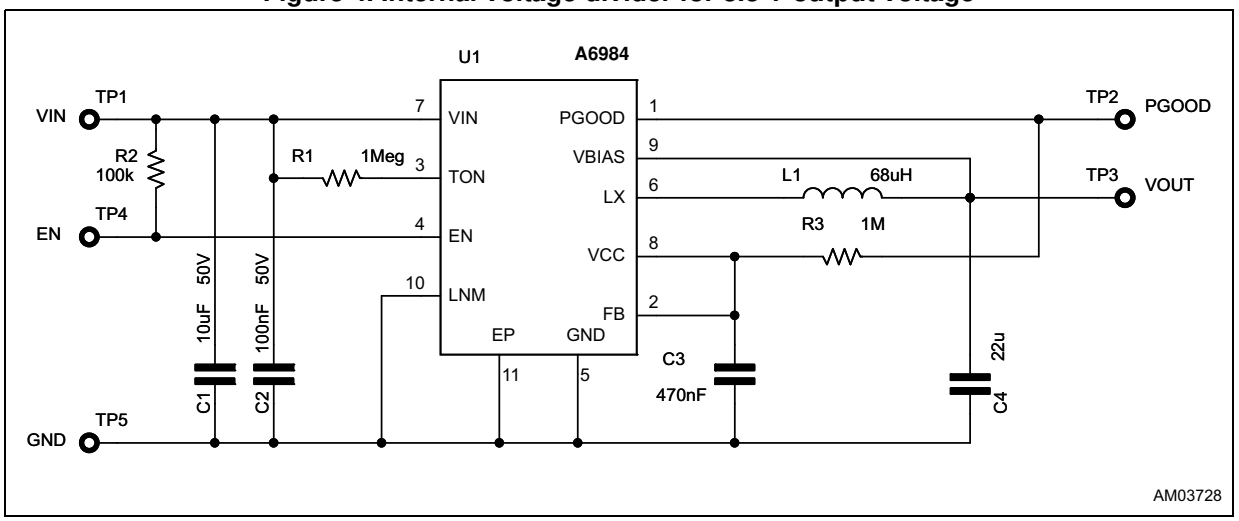
Figure 3. A6984 block diagram



4.1 Output voltage adjustment

No external resistor divider is required to regulate fixed 3.3 V output voltage, connecting FB to the V_{CC} pin and V_{BIAS} to the regulated output voltage (see *Figure 1 on page 1*). An external voltage divider otherwise implements the output voltage adjustability.

Figure 4. Internal voltage divider for 3.3 V output voltage



The error amplifier reference voltage is 0.9 V typical.

The output voltage is adjusted accordingly with the following formula (see *Figure 6*):

Equation 1

$$V_{OUT} = 0.9 \cdot \left(1 + \frac{R_3}{R_2}\right)$$

4.1.1 Maximum output voltage

The constant on-time control scheme naturally requires a minimum cycle-by-cycle off time to sense the feedback voltage and properly driving the switching activity.

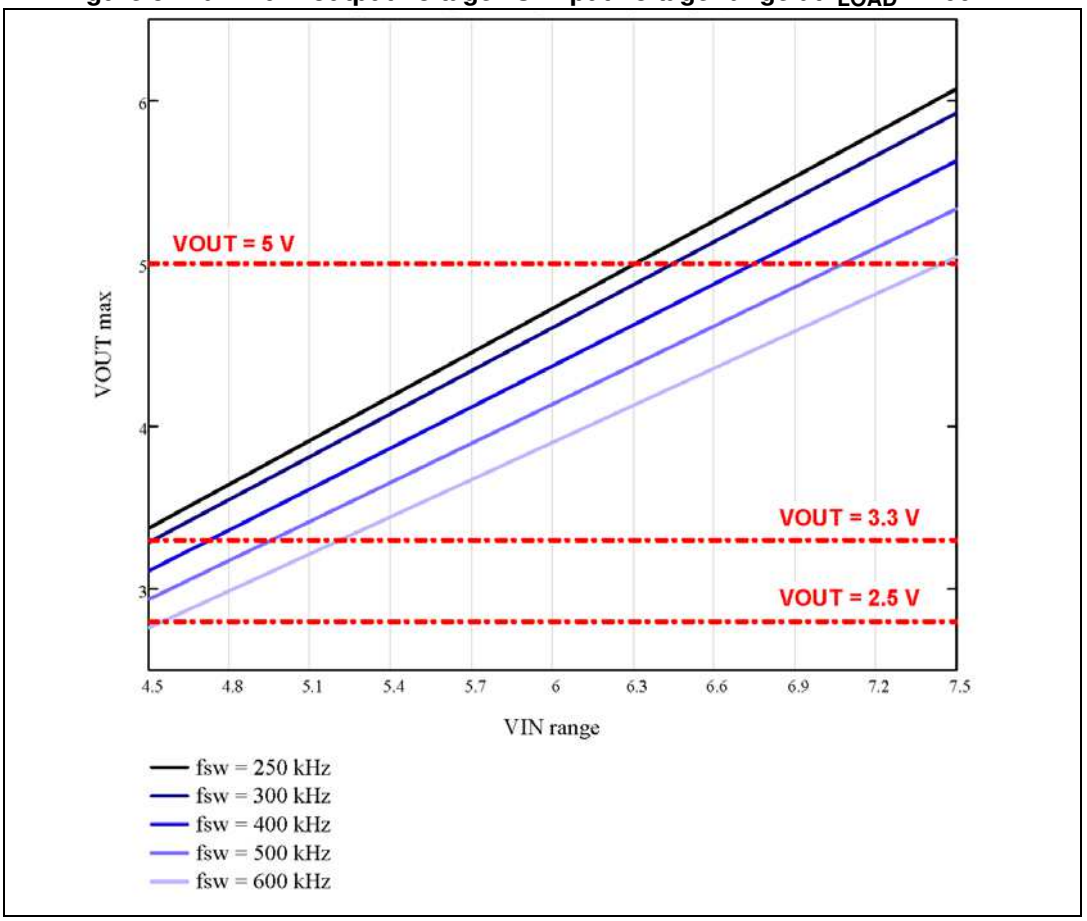
The A6984 minimum off time, as reported in *Table 2 on page 5*, is 300 nsec typical and 400 nsec max.

The control loop generates the proper PWM signal to regulate the programmed output voltage over the application conditions. Since the power losses are proportional to the delivered output power, the duty cycle increases with the load current request.

The fixed minimum off time limits the maximum duty cycle, so the maximum output voltage, depending on the selected switching frequency (see *Section 4.2*).

Figure 5 shows the worst case scenario for maximum output voltage limitation over the input voltage range, that happens at the maximum current request and considering the upper datasheet limit time for the minimum off time parameter.

Figure 5. Maximum output voltage vs. input voltage range at I_{LOAD} = 400 mA



4.1.2 Leading network

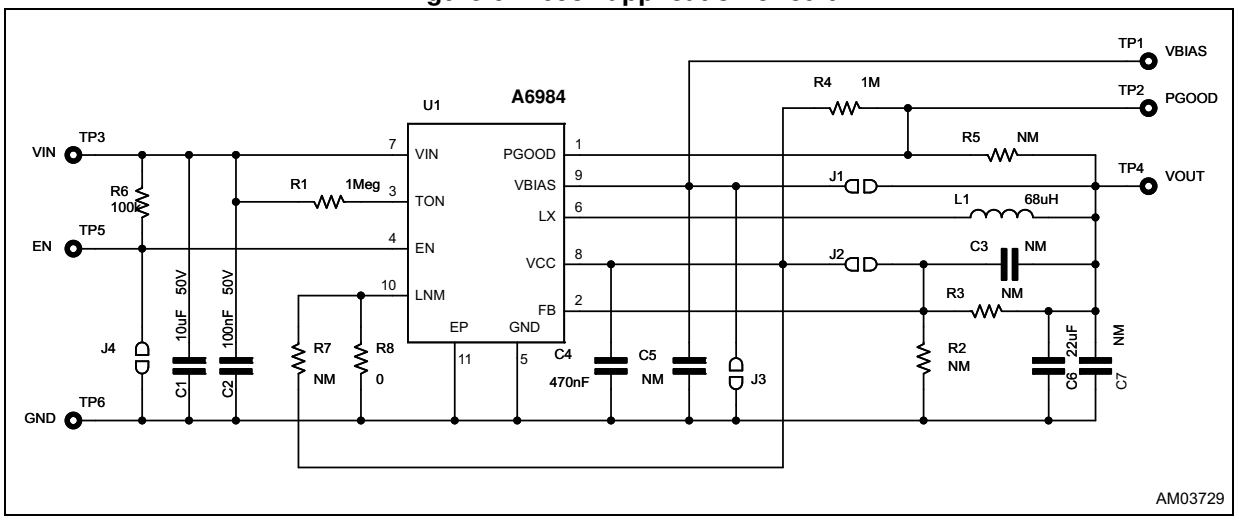
The small signal contribution of a simple voltage divider is:

Equation 2

$$G_{DIV}(s) = \frac{R_2}{R_2 + R_3}$$

A small signal capacitor in parallel to the upper resistor (see C3 in *Figure 6*) of the voltage divider implements a leading network ($f_{zero} < f_{pole}$) that can improve the dynamic regulation for boundary application conditions (high f_{SW} / high duty cycle conversion) and improves the SNR for the feedback comparator operation, entirely coupling the high frequency output voltage ripple without the resistive divider attenuation.

Figure 6. A6984 application circuit



Laplace transformer of the leading network:

Equation 3

$$G_{DIV}(s) = \frac{R_2}{R_2 + R_3} \cdot \frac{(1 + s \cdot R_3 \cdot C_{R3})}{\left(1 + s \cdot \frac{R_2 \cdot R_3}{R_2 + R_3} \cdot C_{R3}\right)}$$

where:

Equation 4

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_3 \cdot C_{R3}}$$

$$f_P = \frac{1}{2 \cdot \pi \cdot \frac{R_2 \cdot R_3}{R_2 + R_3} \cdot C_{R3}}$$

$$f_Z < f_P$$

The R2, R3 compose the voltage divider. C_{R3} is calculated as (see *Section 5.3.2: COUT specification and loop stability on page 39* for C_{OUT} selection):

Equation 5

$$C_{R3} = 28 \cdot 10^{-3} \cdot \frac{V_{OUT} \cdot C_{OUT}}{R_3}$$

4.2 Control loop

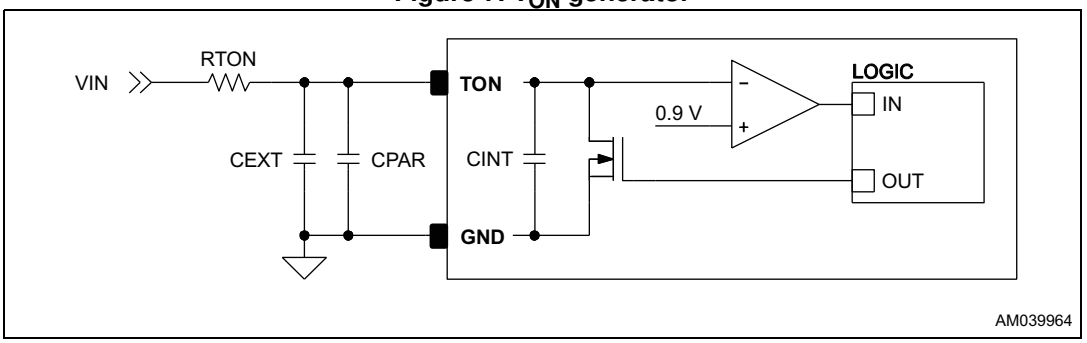
The A6984 device is based on a constant on-time control loop with frequency feed-forward correction over the input voltage range. As a consequence the on-time generator compensates the input voltage variations in order to adapt the duty cycle and so keeping the switching frequency almost constant over the input voltage range.

The general constraint for converters based on the COT architecture is the selection of the output capacitor with an ESR high enough to guarantee a proper output voltage ripple for the noiseless operation of the internal PWM comparator. The A6984 innovative control loop otherwise supports the output ceramic capacitors with the negligible ESR.

The device generates a T_{ON} duration switching pulse as soon as the voltage ripple drops below the valley voltage threshold.

The A6984 on-time is internally generated as shown in *Figure 7*.

Figure 7. T_{ON} generator



where R_{TON} represents the external resistor connected between the V_{IN} and T_{ON} pins, C_{INT} is the integrated capacitor, C_{PAR} the pin parasitic capacitor of the board trace at the pin 3.

The overall contribution of the C_{PAR} and C_{INT} for the A6984 device soldered on the STMicroelectronics evaluation board is 7.5 pF typical but the precise value depends on the parasitic capacitance connected at the pin 3 (TON) that may depend on the implemented board layouts.

As a consequence, a further fine tune of the R_{TON} value with the direct scope measurement is required for precise f_{SW} adjustment accordingly with the designed board layout.

The ON time can be calculated as:

Equation 6

$$T_{ON} = \frac{0.9 \cdot R_{TON} \cdot C_{TON}}{V_{IN}} = \frac{0.9 \cdot R_{TON} \cdot (C_{INT} + C_{PAR})}{V_{IN}} \cong \frac{0.9 \cdot R_{TON} \cdot 7.5pF}{V_{IN}}$$

The natural feedforward of the generator in *Figure 7* corrects the fixed T_{ON} time with the input voltage to achieve almost constant switching frequency over the input voltage range.

On the other hand, the PWM comparator (see *Figure 3 on page 12*) in the closed loop operation modulates the T_{OFF} time, given the programmed T_{ON}, to compensate conversion losses (i.e. conduction, switching, inductor losses, etc.) that are proportional to the output current.

As a consequence the switching frequency slightly depends on the conversion losses:

Equation 7

$$f_{SW}(I_{OUT}) = \frac{D_{REAL}(I_{OUT})}{T_{ON}}$$

where D_{REAL} is the real duty cycle accounting conduction losses:

Equation 8

$$D_{REAL}(I_{OUT}) = \frac{V_{OUT} + (R_{ON\_LS} + DCR) \cdot I_{OUT}}{V_{IN} + (R_{ON\_LS} - R_{ON\_HS}) \cdot I_{OUT}}$$

R_{ON_HS} and R_{ON_LS} represent the RDSON value of the embedded power elements (see *Table 5 on page 7*) and DCR the equivalent series resistor of the selected inductor.

Finally from *Equation 7* and *Equation 8*:

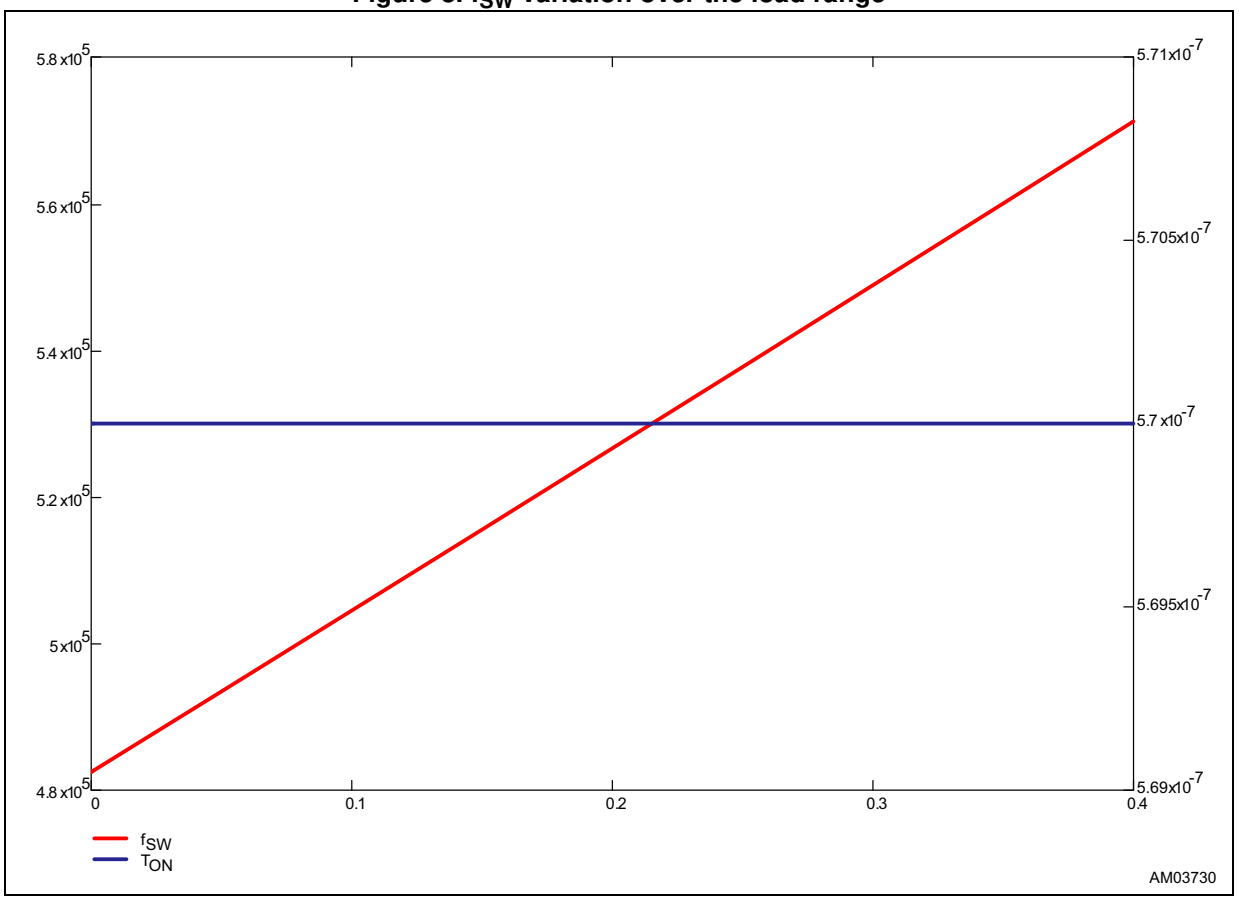
Equation 9

$$R_{TON} = \frac{1}{0.9} \cdot \frac{V_{IN} \cdot D_{REAL}(I_{OUT})}{f_{SW} \cdot C_{TON}}$$

where f_{SW} is the desired switching frequency at a certain I_{OUT} load current level.

Figure 8 shows the estimated f_{SW} variation over the load range assuming the typical RDSON of the power elements, DCR = 420 mΩ (see *Section 6 on page 40* for details on the selected inductor for the reference application board.) and R_{TON} = 1 M.

Figure 8. f_{SW} variation over the load range



A general requirement for applications compatible with humid environments, is to limit the maximum resistor value to minimize the resistor variation determined by the leakage path.

An optional external capacitor C_{TON} >> (C_{INT} + C_{PAR}) connected as shown in *Figure 9* helps to limit the R_{TON} value and also minimizes the f_{SW} variation with the p.c.b. parasitic components C_{PAR}.

Figure 9. T_{ON} generator with optional capacitor

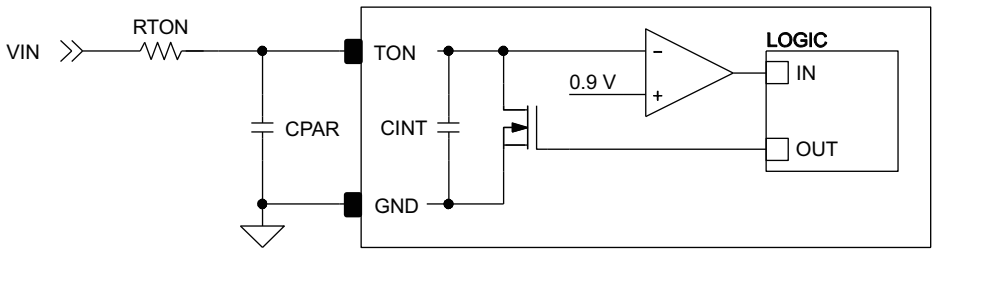


Figure 10, *Figure 11*, *Figure 12*, and *Figure 13* show the numeric example to program the switching frequency accordingly with the R_{TON}, C_{TON} pair selection.

The eDesignSuite online tool supports the A6984 and R_{TON}, C_{TON} dimensioning for proper switching frequency selection, see http://www.st.com/content/st_com/en/support/resources/edesign.html).

Figure 10. Example to select R_{TON}, C_{TON} for V_{OUT} = 1.8 V

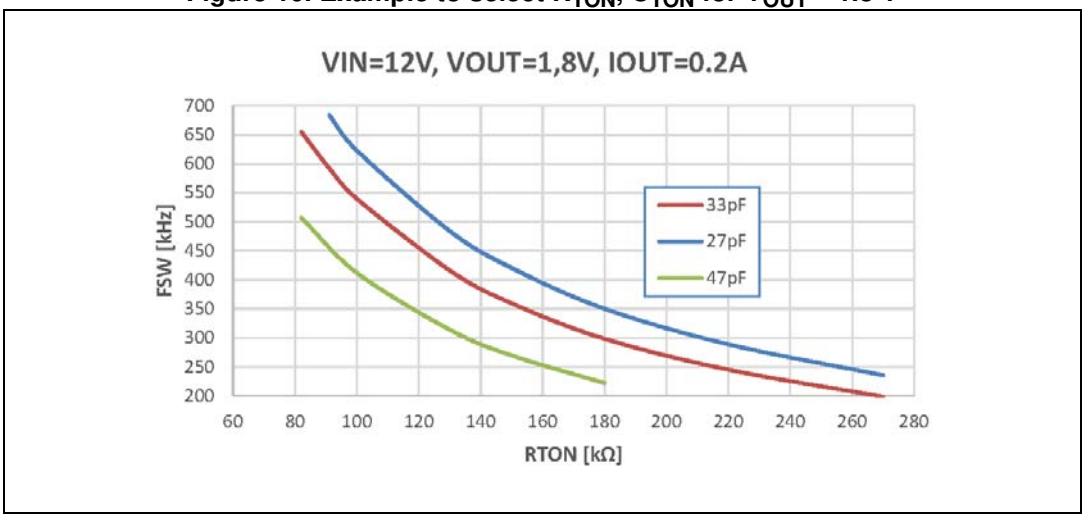


Figure 11. Example to select R_{TON}, C_{TON} for V_{OUT} = 3.3 V

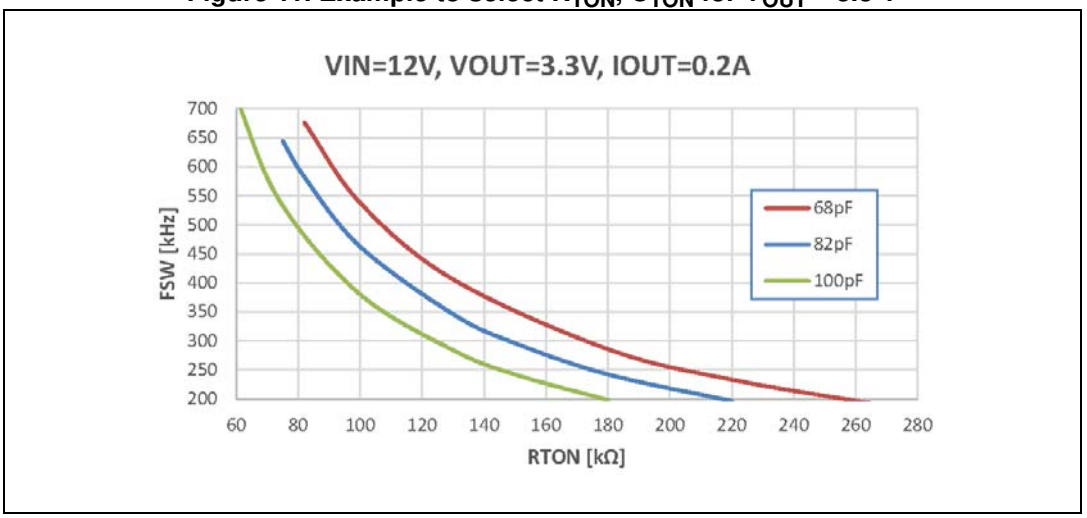


Figure 12. Example to select R_{TON}, C_{TON} for V_{OUT} = 5 V

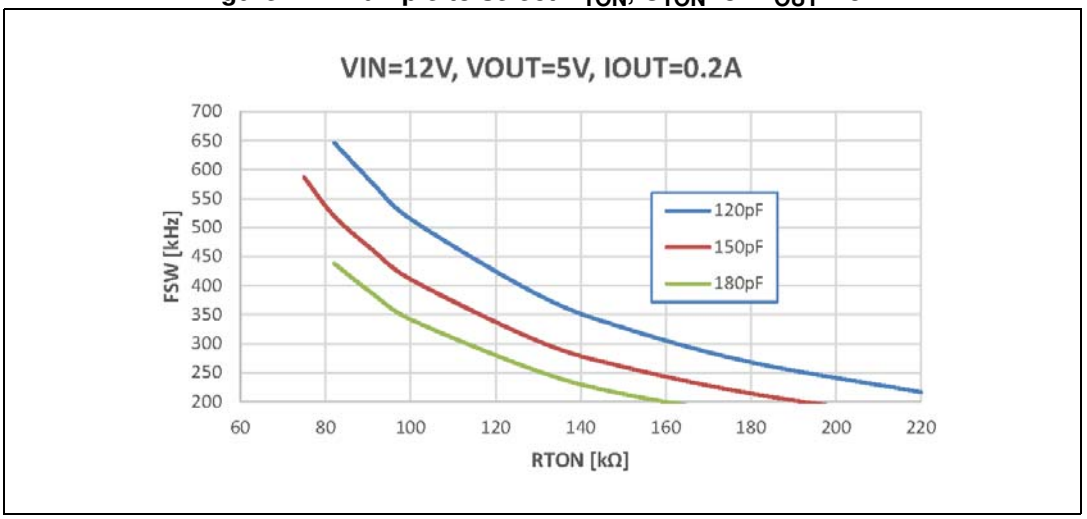
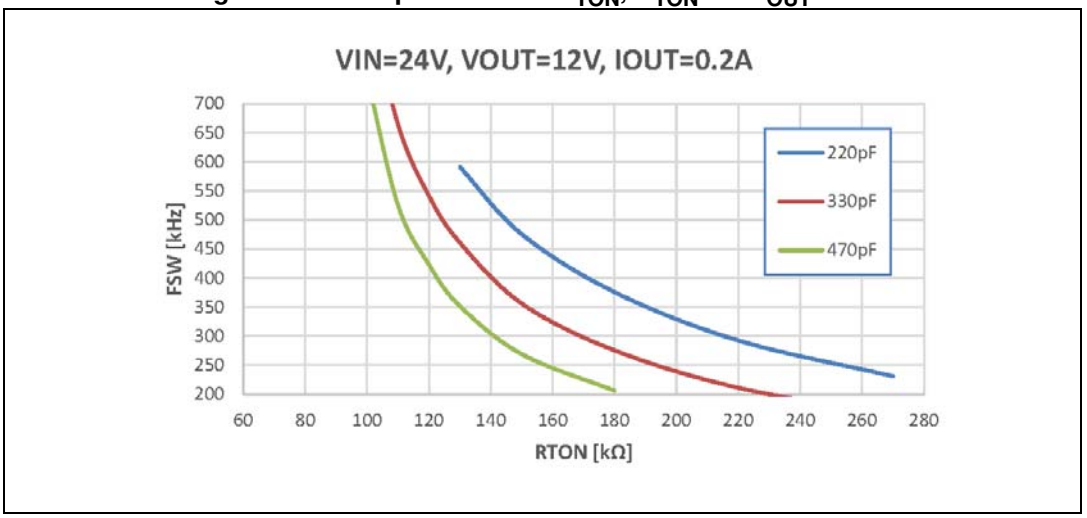


Figure 13. Example to select R_{TON}, C_{TON} for V_{OUT} = 12 V



4.3 Optional virtual ESR network

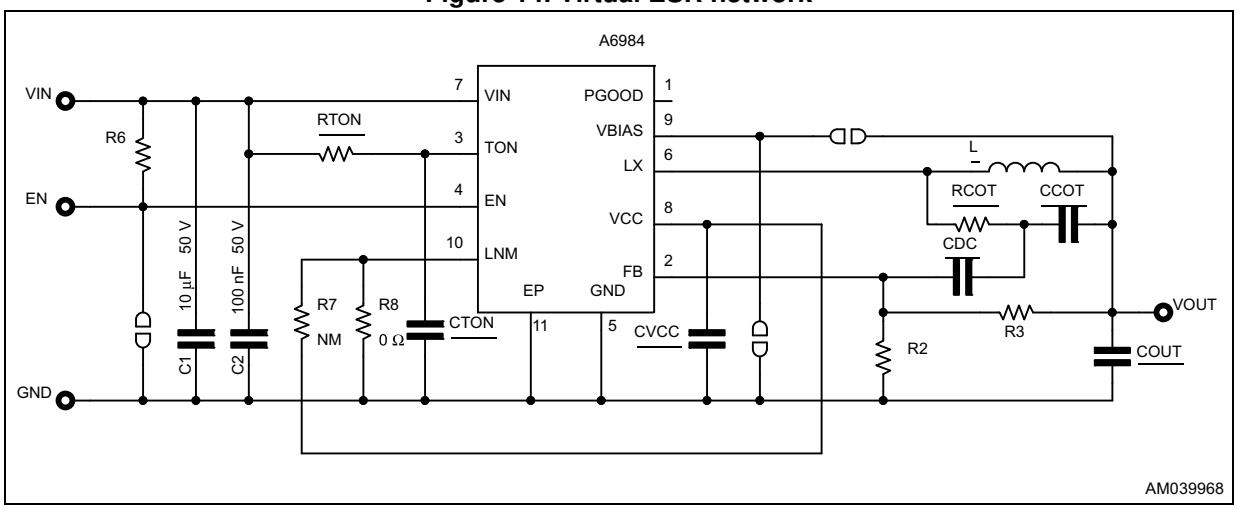
A standard COT loop requires a high ESR output capacitor to generate a proper PWM signal.

The A6984 architecture naturally supports output ceramic capacitors with the negligible ESR generating an internal voltage ramp proportional to the inductor current to emulate a high ESR output capacitor for the proper PWM comparator operation.

The control scheme is designed to guarantee the minimum signal for the PWM comparator cycle-by-cycle operation with controlled duty cycle jitter, that is a natural duty cycle dithering that helps to reduce the switching noise emission for EMC.

If required, an optional external virtual ESR network (see *Figure 14* can be designed to generate a higher signal for the PWM comparator operation and remove the duty cycle dithering. This network requires the external voltage divider to set the output voltage and supports the LNM and LCM device operation.

Figure 14. Virtual ESR network

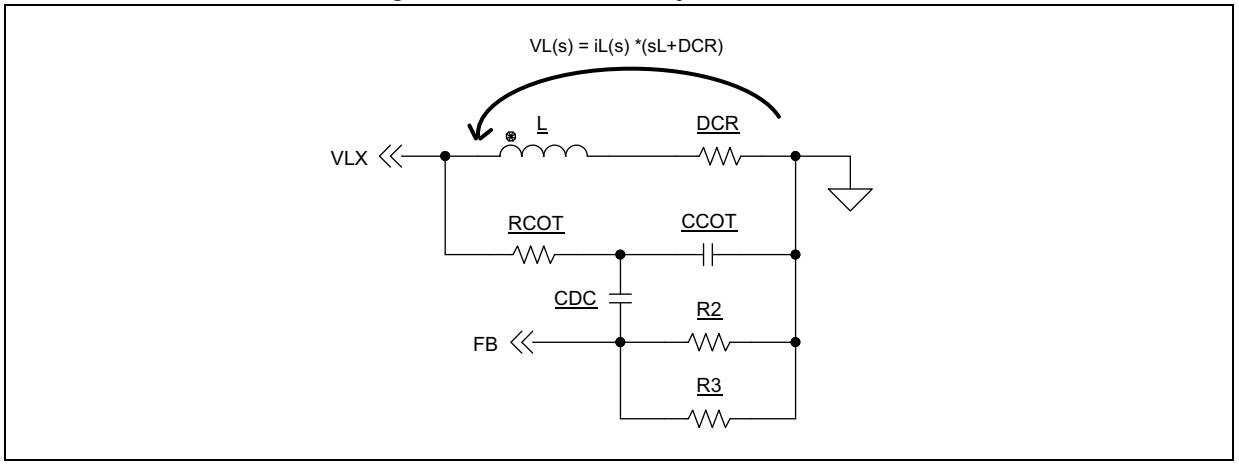


The C_{DC} capacitor decouples the feedback DC path through the R_{COT} so the output voltage is adjusted accordingly with *Section 4.1 on page 13*.

Basically the network R_{COT}, C_{COT} generates a voltage signal proportional to the inductor current ripple and superimposed with the real partitioned output voltage that increases the SNR at the input of the PWM comparator. As a consequence the PWM converter commutation is clean, removing the duty cycle dithering.

For the purpose of the signal generated by the R_{COT} and C_{COT} the output capacitor represents a virtual ground so the equivalent small signal circuit of the output of the virtual ESR network is shown in *Figure 15.*

Figure 15. Virtual ESR equivalent circuit



The switching activity drives the inductor voltage so the small signal transfer function can be calculated as:

Equation 10

$$H(s) = \frac{vFB(s)}{iL(s)} = \frac{(s \cdot L + DCR)}{R_{COT} + \frac{1}{s \cdot C_{COT} + \frac{1}{\frac{1}{s \cdot C_{DC}} + \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}}}} \cdot \frac{1}{s \cdot C_{COT} + \frac{1}{\frac{1}{s \cdot C_{DC}} + \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}}} \cdot \frac{\frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}}{\frac{1}{s \cdot C_{DC}} + \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}}$$

Equation 10 can be simplified as follows:

Equation 11

$$H(s) = \frac{vFB(s)}{iL(s)} = \frac{(s \cdot L + DCR) \cdot s}{\left[1 + s \cdot \left(R_{COT} + \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}\right) \cdot C_{DC}\right] \cdot \left[1 + s \cdot \left(\frac{1}{\frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_{COT}}}\right) \cdot C_{COT}\right]} \cdot \frac{C_{DC}}{\frac{1}{R_2} + \frac{1}{R_3}}$$

The pole splitting is guaranteed by the condition:

Equation 12

$$C_{DC} > 10 \cdot C_{COT}$$

$$R_{COT} > 10 \cdot \left(\frac{R_2 x R_3}{R_2 + R_3}\right)$$

In case:

Equation 13

$$f_z = \frac{1}{2 \cdot \pi} \cdot \frac{L}{DCR} \ll fsw$$

$$f_{PL} = \frac{1}{2 \cdot \pi \cdot R_{COT} + \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}} \cdot C_{DC}} \ll fsw$$

$$f_{PH} = \frac{1}{2 \cdot \pi \cdot \left(\frac{1}{\frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_{COT}}}\right) \cdot C_{COT}} \ll fsw$$

Equation 10 can be simplified as:

Equation 14

$$ESR_{VRT} = H(s)_{s \to (2 \cdot \pi \cdot fsw)} = \left(\frac{vFB(s)}{iL(s)}\right)_{s \to (2 \cdot \pi \cdot fsw)} = \frac{L}{R_{COT} \cdot C_{COT}}$$

which represents the virtual ESR of the network in *Figure 14*.

As a consequence, the injected triangular voltage ripple in the FB is:

Equation 15

$$VFB_{RIPPLE}(V_{IN}) = IL_{RIPPLE} \cdot ESR_{VRT} = \frac{V_{IN} - V_{OUT}}{R_{COT} \cdot C_{COT}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{fsw}$$

that does not depend on the R_2, R_3, C_{DC}, L and DCR.

A virtual ESR network able to guarantee a peak-to-peak signal higher than 20 mV at the FB pin removes any duty cycle dithering at the switching node.

Output voltage accuracy and optimized resistor divider

The constant on-time control scheme implements valley output voltage regulation: the internal comparator monitors the FB voltage cycle-by-cycle and generates a fixed T_{ON} pulse if the sensed voltage drops below the internal voltage reference (V_{EAFB} = 0.9 V typical).

The virtual ESR network generates a signal proportional to the inductor current that is AC coupled to the FB pin through the C_{DC} capacitor (refer to *Section 4.3* for dimensioning rules) and superimposed on the voltage divider contribution as shown in *Figure 16*.

Figure 16. Virtual ESR signal generation in CCM operation