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A6986F

Automotive 38 V, 1.5 A synchronous step-down switching regulator with 30 µA quiescent current

Datasheet - production data

HTSSOP16 (R_{TH} = 40 °C/W)

Features

- AEC-Q100 qualified
- 1.5 A DC output current
- 4 V to 38 V operating input voltage
- Low consumption mode or low noise mode
- 30 µA I_Q at light-load (LCM V_{OUT} = 3.3 V)
- 8 µA $I_{Q\text{-}SHTDWN}$
- Adjustable f_{SW} (250 kHz - 2 MHz)
- Fixed output voltage (3.3 V and 5 V) or adjustable from 0.85 V to V_{IN}
- Embedded output voltage supervisor
- Synchronization
- Adjustable soft-start time
- Internal current limiting
- Overvoltage protection
- Output voltage sequencing
- Peak current mode architecture
- $R_{DSON\ HS}$ = 180 mΩ, $R_{DSON\ LS}$ = 150 mΩ
- Thermal shutdown

Applications

- Designed for automotive systems
- Battery powered applications
- Car body applications (LCM)
- Car audio and low noise applications (LNM)

Description

The A6986F automotive grade device is a step-down monolithic switching regulator able to deliver up to 1.5 A DC. The output voltage adjustability ranges from 0.85 V to VIN. The 100% duty cycle capability and the wide input voltage range meet the cold crank and load dump specifications for automotive systems. The “Low Consumption Mode” (LCM) is designed for applications active during car parking, so it maximizes the efficiency at light-load with controlled output voltage ripple. The “Low Noise Mode” (LNM) makes the switching frequency constant and minimizes the output voltage ripple overload current range, meeting the low noise application specification like car audio. The output voltage supervisor manages the reset phase for any digital load (µC, FPGA). The RST open collector output can also implement output voltage sequencing during the power-up phase. The synchronous rectification, designed for high efficiency at medium - heavy load, and the high switching frequency capability make the size of the application compact. Pulse by pulse current sensing on both power elements implements an effective constant current protection.

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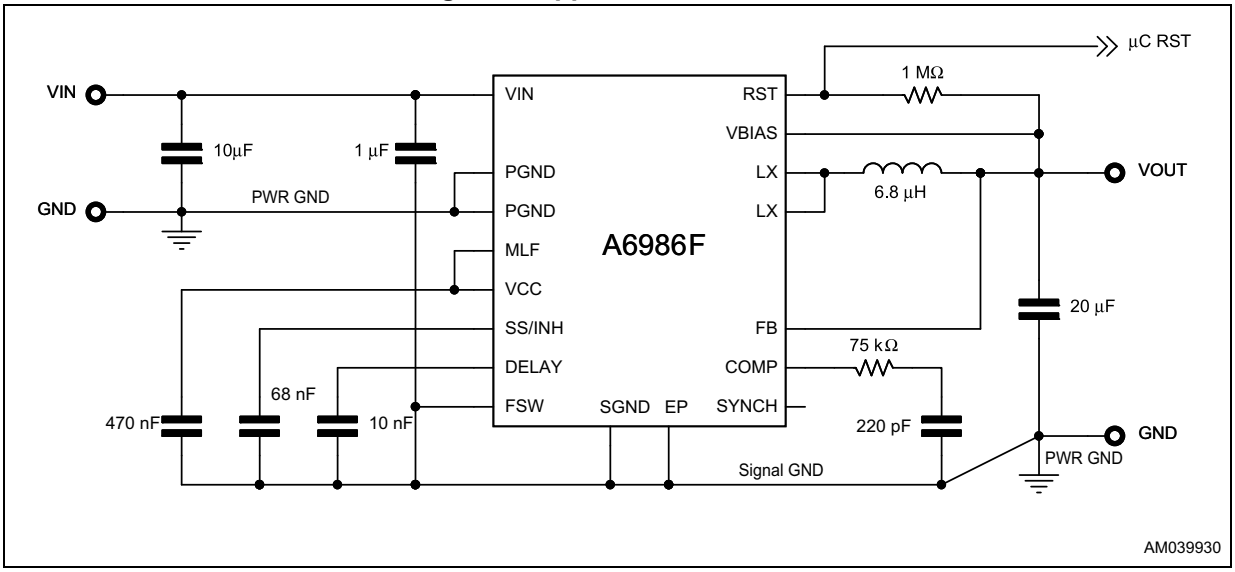
1 Application schematic

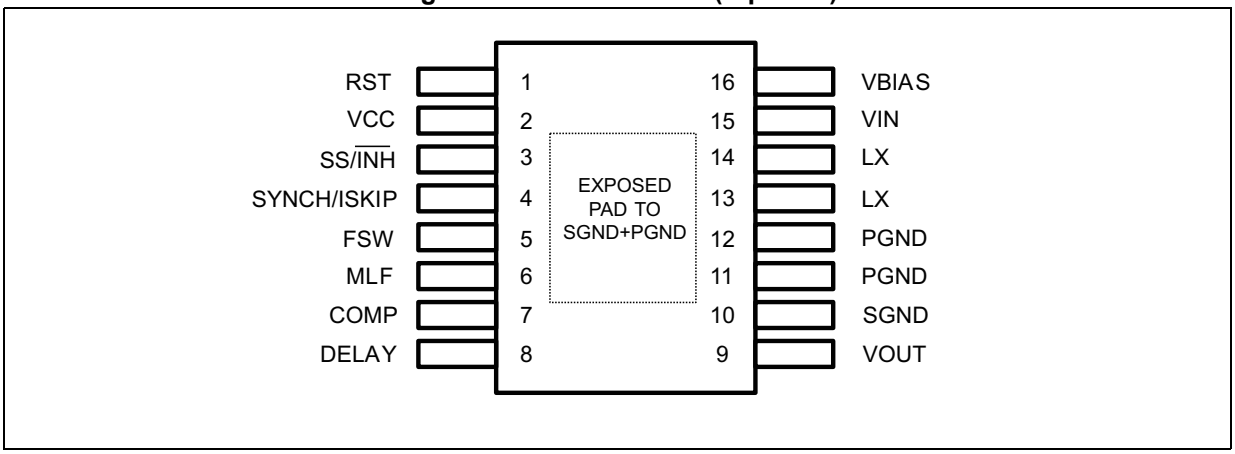
Figure 1. Application schematic



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection (top view)



2.2 Pin description

Table 1. Pin description

No.	Pin	Description
1	RST	The RST open collector output is driven low when the output voltage is out of regulation. The RST is released after an adjustable time DELAY once the output voltage is over the active delay threshold.
2	VCC	Connect a ceramic capacitor (≥ 470 nF) to filter internal voltage reference. This pin supplies the embedded analog circuitry.
3	SS/$\overline{\text{INH}}$	An open collector stage can disable the device clamping this pin to GND ($\overline{\text{INH}}$ mode). An internal current generator (4 µA typ.) charges the external capacitor to implement the soft-start.
4	SYNCH/ ISKP	The pin features Master / Slave synchronization in LNM (see *Section 5.8.1 on page 26*) and skip current level selection in LCM (see *Section 5.8.2 on page 27*). In LNM, leave this pin floating when not used.
5	FSW	A pull up resistor (E24 series only) to VCC or pull down to GND selects the switching frequency. Pinstrapping is active only before the soft-start phase to minimize the IC consumption.
6	MLF	A pull up resistor (E24 series only) to VCC or pull down to GND selects the low noise mode/low consumption mode and the active RST threshold. Pinstrapping is active only before the soft-start phase to minimize the IC consumption.
7	COMP	Output of the error amplifier. The designed compensation network is connected at this pin.
8	DELAY	An external capacitor connected at this pin sets the time DELAY to assert the rising edge of the RST o.c. after the output voltage is over the reset threshold. If this pin is left floating, RST is like a Power Good.
9	VOUT	Output voltage sensing
10	SGND	Signal GND

Table 1. Pin description (continued)

No.	Pin	Description
11	PGND	Power GND
12	PGND	Power GND
13	LX	Switching node
14	LX	Switching node
15	VIN	DC input voltage
16	V_{BIAS}	Typically connected to the regulated output voltage. An external voltage reference can be used to supply part of the analog circuitry to increase the efficiency at light-load. Connect to GND if not used.
-	E. p.	Exposed pad must be connected to SGND, PGND

2.3 Maximum ratings

Stressing the device above the rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{IN}	See *Table 1*	-0.3	40	V
DELAY		-0.3	V_{CC} + 0.3	V
PGND		SGND - 0.3	SGND + 0.3	V
SGND		-	-	V
V_{CC}		-0.3	(V_{IN} + 0.3) or (max. 4)	V
SS / $\overline{INH}$		-0.3	V_{IN} + 0.3	V
MLF		-0.3	V_{CC} + 0.3	V
COMP		-0.3	V_{CC} + 0.3	V
VOUT		-0.3	10	V
FSW		-0.3	V_{CC} + 0.3	V
SYNCH		-0.3	V_{IN} + 0.3	V
V_{BIAS}		-0.3	(V_{IN} + 0.3) or (max. 6)	V
RST		-0.3	V_{IN} + 0.3	V
LX		-0.3	V_{IN} + 0.3	V
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range	-	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)	-	260	°C
I_{HS}, I_{LS}	High-side / low-side switch current	-	2	A

2.4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ JA}$	Thermal resistance junction ambient (device soldered on the STMicroelectronics® demonstration board)	40	°C/W
$R_{th\ JC}$	Thermal resistance junction to exposed pad for board design (not suggested to estimate TJ from power losses).	5	°C/W

2.5 ESD protection

Table 4. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	2	kV
	MM	200	V
	CDM	500	V

3 Electrical characteristics

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Note	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range	-	-	4	-	38	V
V_{INH}	V_{CC} UVLO rising threshold	-	-	2.7	-	3.5	
V_{INL}	V_{CC} UVLO falling threshold	-	-	2.4	-	3.5	
I_{PK}	Peak current limit	Duty cycle < 20%	-	2.3	-	-	A
		Duty cycle = 100% closed loop operation	-	1.8	-	-	
I_{VY}	Valley current limit	-	-	2.4	-	-	
I_{SKIPH}	Programmable skip current limit	LCM, V_{SYNCH} = GND	(1)	0.2	0.4	0.6	
I_{SKIPL}		LCM, V_{SYNCH} = VCC	(2)	-	0.2	-	-
I_{VY_SNK}	Reverse current limit	LNM or V_{OUT} overvoltage	-	0.5	1	2	-
$R_{DSON\ HS}$	High-side RDSON	I_{SW} = 1 A	-	-	0.18	0.360	Ω
$R_{DSON\ LS}$	Low-side RDSON	I_{SW} = 1 A	-	-	0.15	0.300	
f_{SW}	Selected switching frequency	FSW pinstrapping before SS	-	See *Table 6: f_{SW} selection*			
I_{FSW}	FSW biasing current	SS ended	-	-	0	500	nA
LCM/LNM	Low noise mode / Low consumption mode selection	MLF pinstrapping before SS	-	See *Table 7 on page 11*, *Table 8 on page 12*, *Table 9 on page 12*			
I_{MLF}	MLF biasing current	SS ended	-	-	0	500	nA
D	Duty cycle	-	(2)	0	-	100	%
$T_{ON\ MIN}$	Minimum On time	-	-	-	80	-	ns
VCC regulator							
V_{CC}	LDO output voltage	V_{BIAS} = GND (no switchover)	-	2.9	3.3	3.6	V
		V_{BIAS} = 5 V (switchover)	-	2.9	3.3	3.6	
SWO	V_{BIAS} threshold (3 V< V_{BIAS} < 5.5 V)	Switch internal supply from V_{IN} to V_{BIAS}	-	2.85	-	3.2	
		Switch internal supply from V_{BIAS} to V_{IN}	-	2.78	-	3.15	

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Note	Min.	Typ.	Max.	Unit
Power consumption							
I_{SHTDWN}	Shutdown current from V_{IN}	$V_{SS/INH}$ = GND	-	4	8	15	µA
$I_{Q\ OPVIN}$	Quiescent current from V_{IN}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(3)	4	10	15	µA
		LCM - NO SWO $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = GND	(3)	35	70	120	
		LNM - SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = 3.3 V	-	0.5	1.5	5	mA
		LNM - NO SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = GND	-	2	2.8	6	
$I_{Q\ OPVBIAS}$	Quiescent current from V_{BIAS}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(3)	25	50	115	µA
		LNM - SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = 3.3 V	-	0.5	1.2	5	mA
Soft-start							
V_{INH}	VSS threshold	SS rising	-	200	460	700	mV
$V_{INH\ HYST}$	VSS hysteresis	-	-	-	100	140	
$I_{SS\ CH}$	C_{SS} charging current	$V_{SS} < V_{INH}$ OR $t < T_{SS\ SETUP}$ OR $V_{EA+} > V_{FB}$	(2)	-	1	-	µA
		$t > T_{SS\ SETUP}$ AND $V_{EA+} < V_{FB}$	(2)	-	4	-	
$V_{SS\ START}$	Start of internal error amplifier ramp	-	-	0.995	1.1	1.150	V
SS_{GAIN}	SS/INH to internal error amplifier gain	-	-	-	3	-	-
Error amplifier							
V_{OUT}	Voltage feedback	3.3 V (A6986F3V3)	-	3.25	3.3	3.35	V
		5 V (A6986F5V)	-	4.925	5.0.	5.075	
		A6986F	-	0.841	0.85	0.859	
I_{VOUT}	VOUT biasing current	3.3 V (A6986F3V3)	-	4	6	8.5	µA
		5 V (A6986F5V)	-	7.5	10	13.5	
		A6986F	-	-	50	500	nA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Note	Min.	Typ.	Max.	Unit
A_V	Error amplifier gain	-	(2)	-	100	-	dB
I_{COMP}	EA output current capability	-	-	±6	±12	±25	µA
		-	(4)	±4	-	-	
Inner current loop							
g_{CS}	Current sense transconductance (V_{COMP} to inductor current gain)	Ipk = 1 A	(2)	-	2.5	-	A/V
V_{PP}*g_{CS}	Slope compensation	-	(5)	0.45	0.75	1	A
Overvoltage protection							
V_{OVP}	Overvoltage trip (V_{OVP}/V_{REF})	-	-	1.15	1.2	1.25	-
$V_{OVP\ HYST}$	Overvoltage hysteresis	-	-	0.5	2	5	%
Synchronization (fan out: 6 slave devices typ.)							
$f_{SYN\ MIN}$	Synchronization frequency	LNM; f_{SW} = VCC	-	266.5	-	-	kHz
$V_{SYN\ TH}$	SYNCH input threshold	LNM, SYNCH rising	-	0.70	-	1.2	V
I_{SYN}	SYNCH pull-down current	LNM, V_{SYN} = 1.2 V	-		0.7	-	mA
$V_{SYN\ OUT}$	High level output	LNM, 5 mA sinking load	-	1.40	-	-	V
	Low level output	LNM, 0.7 mA sourcing load	-	-	-	0.6	
Reset							
V_{THR}	Selected RST threshold	MLF pinstrapping before SS	-	see *Table 7*, *Table 8*, *Table 9*			
$V_{THR\ HYST}$	RST hysteresis	-	(2)	-	2	-	%
V_{RST}	RST open collector output	$V_{IN} > V_{INH}$ AND $V_{FB} < V_{TH}$ 4 mA sinking load	-	-	-	0.4	V
		$2 < V_{IN} < V_{INH}$ 4 mA sinking load	-	-	-	0.8	
Delay							
V_{THD}	RST open collector released as soon as $V_{DELAY} > V_{THD}$	$V_{FB} > V_{THR}$	-	1.19	1.234	1.258	V
$I_{D\ CH}$	C_{DELAY} charging current	$V_{FB} > V_{THR}$	-	1	2	3	µA
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature	-	(2)	-	165	-	°C
T_{HYS}	Thermal shutdown hysteresis	-	(2)	-	30	-	

1. Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.
2. Not tested in production.
3. LCM enables SLEEP mode at light-load.
4. T_J = -40 °C.
5. Measured at f_{sw} = 250 kHz.

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 6. f_{SW} selection

Symbol	R_{VCC} (E24 series)	R_{GND} (E24 series)	Tj	f_{SW} min.	f_{SW} typ.	f_{SW} max.	Unit
f_{SW}	0 Ω	NC		225	**250**	275	kHz
	1.8 kΩ	NC	(1)	-	**285**	-	
	3.3 kΩ	NC		-	**330**	-	
	5.6 kΩ	NC		-	**380**	-	
	10 kΩ	NC		-	**435**	-	
	NC	0 Ω		450	**500**	550	
	18 kΩ	NC	(1)	-	**575**	-	
	33 kΩ	NC		-	**660**	-	
	56 kΩ	NC		-	**755**	-	
	NC	1.8 kΩ		-	**870**	-	
	NC	3.3 kΩ		900	**1000**	1100	
	NC	5.6 kΩ	(1)	-	**1150**	-	
	NC	10 kΩ		-	**1310**	-	
	NC	18 kΩ		-	**1500**(2)	-	
	NC	33 kΩ		1575	**1750**(2)	1925	
	NC	56 kΩ		1800	**2000**(2)	2200	

1. Not tested in production.
2. No synchronization as slave in LNM.

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 7. LNM / LCM selection (A6986F3V3)

Symbol	R_{VCC} (E24 1%)	R_{GND} (E24 1%)	Operating mode	V_{RST}/V_{OUT} (tgt. value)	V_{RST} min.	V_{RST} typ.	V_{RST} max.	Unit
V_{RST}	0 Ω	NC	**LCM**	**93%**	3.008	3.069	3.130	V
	8.2 kΩ	NC		**80%**	2.587	**2.640**	2.693	
	18 kΩ	NC		**87%**	2.814	**2.871**	2.928	
	39 kΩ	NC		**96%**	3.105	**3.168**	3.231	
	NC	0 Ω	**LNM**	**93%**	3.008	3.069	3.130	
	NC	8.2 kΩ		**80%**	2.587	**2.640**	2.693	
	NC	18 kΩ		**87%**	2.814	**2.871**	2.928	
	NC	39 kΩ		**96%**	3.105	**3.168**	3.231	

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 8. LNM / LCM selection (A6986F5V)

Symbol	R_{VCC} (E24 1%)	R_{GND} (E24 1%)	Operating mode	V_{RST}/V_{OUT} (tgt. value)	V_{RST} min.	V_{RST} typ.	V_{RST} max.	Unit
V_{RST}	0 Ω	NC	LCM	**93%**	4.557	**4.650**	4.743	V
	8.2 kΩ	NC		**80%**	3.920	**4.000**	4.080	
	18 kΩ	NC		**87%**	4.263	**4.350**	4.437	
	39 kΩ	NC		**96%**	4.704	**4.800**	4.896	
	NC	0 Ω	LNM	**93%**	4.557	**4.650**	4.743	
	NC	8.2 kΩ		**80%**	3.920	**4.000**	4.080	
	NC	18 kΩ		**87%**	4.263	**4.350**	4.437	
	NC	39 kΩ		**96%**	4.704	**4.800**	4.896	

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 9. LNM / LCM selection (A6986F)

Symbol	R_{VCC} (E24 1%)	R_{GND} (E24 1%)	Operating mode	V_{RST}/V_{OUT} (tgt value)	V_{RST} min.	V_{RST} typ.	V_{RST} max.	Unit
V_{RST}	0 Ω	NC	LCM	**93%**	0.779	**0.791**	0.802	V
	8.2 kΩ ± 1%	NC		**80%**	0.670	**0.680**	0.690	
	18 kΩ ± 1%	NC		**87%**	0.728	**0.740**	0.751	
	39 kΩ ± 1%	NC		**96%**	0.804	**0.816**	0.828	
	NC	0 Ω	LNM	**93%**	0.779	**0.791**	0.802	
	NC	8.2 kΩ ± 1%		**80%**	0.670	**0.680**	0.690	
	NC	18 kΩ ± 1%		**87%**	0.728	**0.740**	0.751	
	NC	39 kΩ ± 1%		**96%**	0.804	**0.816**	0.828	

4 Datasheet parameters over the temperature range

The 100% of the population in the production flow is tested at three different ambient temperatures (-40 °C, +25 °C, +135 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C, +135 °C).

The device operation is guaranteed when the junction temperature is inside the (-40 °C, +150 °C) temperature range. The designer can estimate the silicon temperature increase respect to the ambient temperature evaluating the internal power losses generated during the device operation.

However the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHTDWN} (+165 °C typ.) temperature.

All the datasheet parameters can be guaranteed to a maximum junction temperature of +135 °C to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

5 Functional description

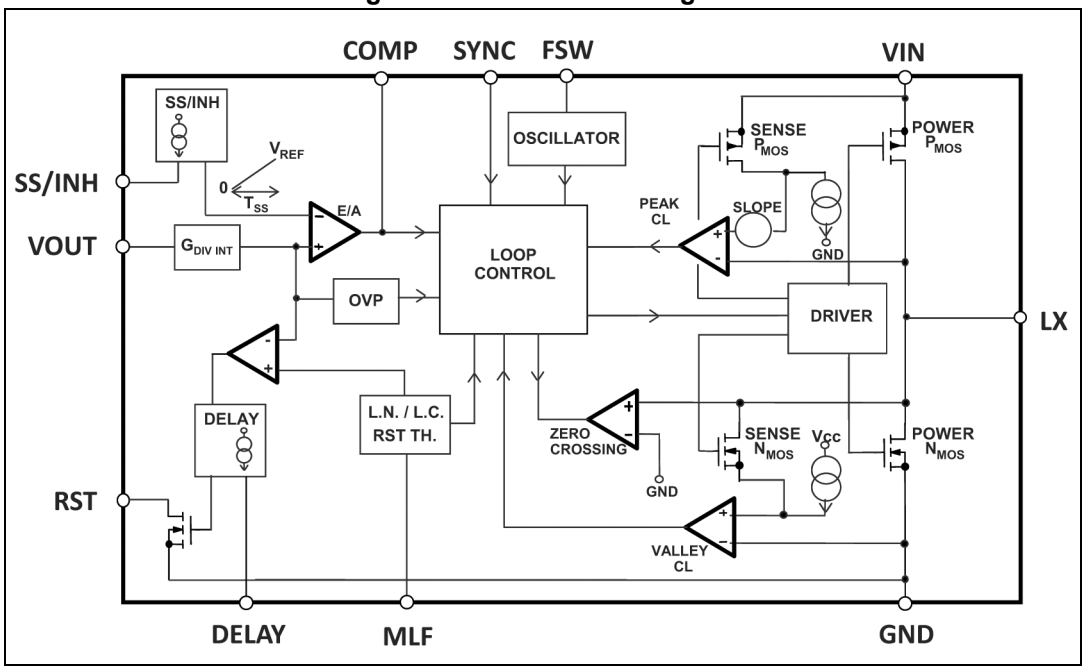
The A6986F device is based on a “peak current mode”, constant frequency control. As a consequence, the intersection between the error amplifier output and the sensed inductor current generates the PWM control signal to drive the power switch.

The device features LNM (low noise mode) that is forced PWM control, or LCM (low consumption mode) to increase the efficiency at light-load.

The main internal blocks shown in the block diagram in *Figure 3* are:

- Embedded power elements. Thanks to the P-channel MOSFET as high-side switch the device features low dropout operation
- A fully integrated sawtooth oscillator with adjustable frequency
- A transconductance error amplifier
- An internal feedback divider $G_{DIV\ INT}$
- The high-side current sense amplifier to sense the inductor current
- A “Pulse Width Modulator” (PWM) comparator and the driving circuitry of the embedded power elements
- The soft-start blocks to ramp the error amplifier reference voltage and so decreases the inrush current at power-up. The SS/$\overline{\text{INH}}$ pin inhibits the device when driven low.
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the V_{BIAS} pin is connected to an external output voltage
- The synchronization circuitry to manage master / slave operation and the synchronization to an external clock
- The current limitation circuit to implement the constant current protection, sensing pulse by pulse high-side / low-side switch current. In case of heavy short-circuit the current protection is fold back to decrease the stress of the external components
- A circuit to implement the thermal protection function
- The OVP circuitry to discharge the output capacitor in case of overvoltage event
- MLF pin strapping sets the LNM/LCM mode and the thresholds of the RST comparator
- FSW pinstrapping sets the switching frequency
- The RST open collector output

Figure 3. Internal block diagram



5.1 Power supply and voltage reference

The internal regulator block consists of a start-up circuit, the voltage pre-regulator that provides current to all the blocks and the bandgap voltage reference. The starter supplies the startup current when the input voltage goes high and the device is enabled (SS/INH pin over the inhibits threshold).

The pre-regulator block supplies the bandgap cell and the rest of the circuitry with a regulated voltage that has a very low supply voltage noise sensitivity.

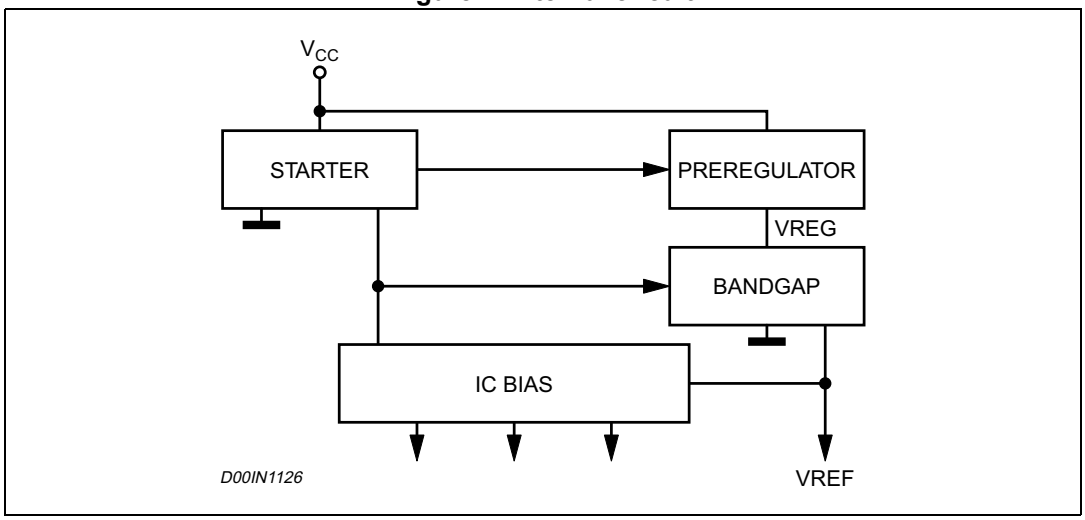
Switchover feature

The switchover scheme of the pre-regulator block features to derive the main contribution of the supply current for the internal circuitry from an external voltage (3 V < V_{BIAS} < 5.5 V is typically connected to the regulated output voltage). This helps to decrease the equivalent quiescent current seen at V_{IN}. (Please refer to *Section 5.9: Switchover feature on page 35*).

5.2 Voltages monitor

An internal block continuously senses the V_{CC}, V_{BIAS} and V_{BG}. If the monitored voltages are good, the regulator starts operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 4. Internal circuit



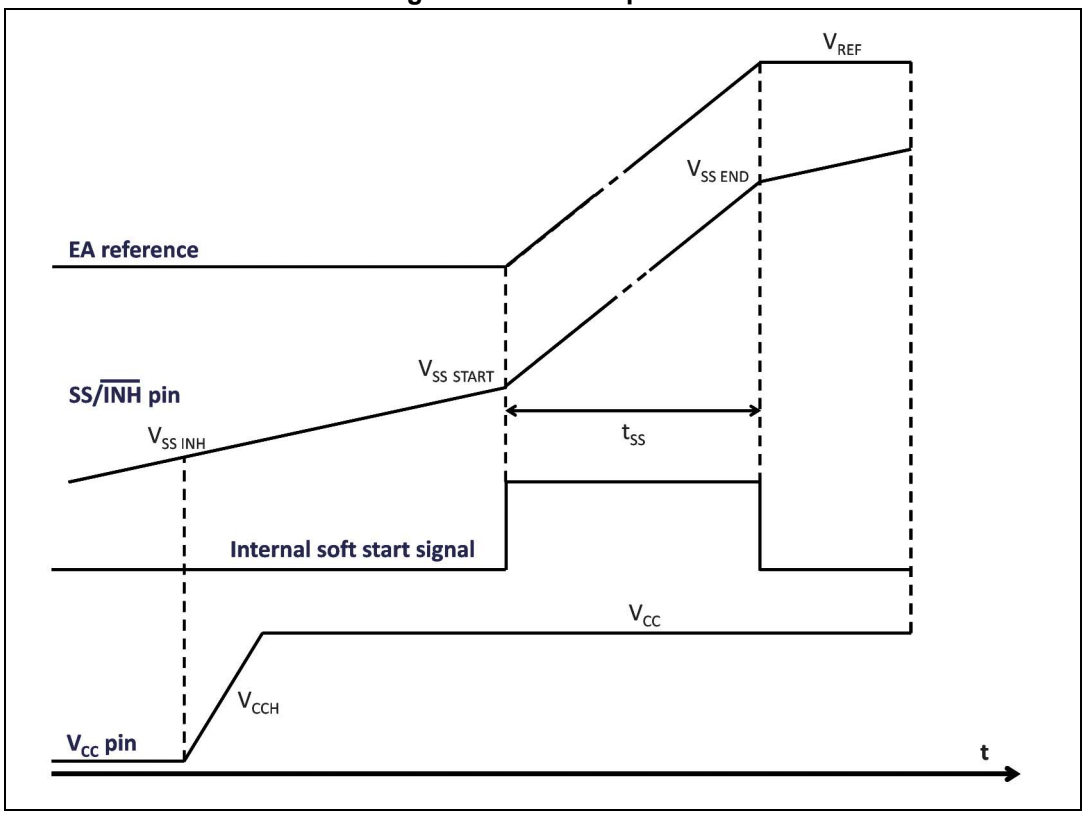
5.3 Soft-start and inhibit

The soft-start and inhibit features are multiplexed on the same pin. An internal current source charges the external soft-start capacitor to implement a voltage ramp on the SS/INH pin. The device is inhibited as long as the SS/INH pin voltage is lower than the V_{INH} threshold and the soft-start takes place when SS/INH pin crosses $V_{SS\ START}$. (See *Figure 5: Soft-start phase*).

The internal current generator sources 1 µA typ. current when the voltage of the VCC pin crosses the UVLO threshold. The current increases to 4 µA typ. as soon as the SS/INH voltage is higher than the V_{INH} threshold. This feature helps to decrease the current consumption in inhibit mode. An external open collector can be used to set the inhibit operation clamping the SS/INH voltage below V_{INH} threshold.

The startup feature minimizes the inrush current and decreases the stress of the power components during the power-up phase. The ramp implemented on the reference of the error amplifier has a gain three times higher (SS_{GAIN}) than the external ramp present at SS/INH pin.

Figure 5. Soft-start phase



The C_{SS} is dimensioned accordingly with *Equation 1*:

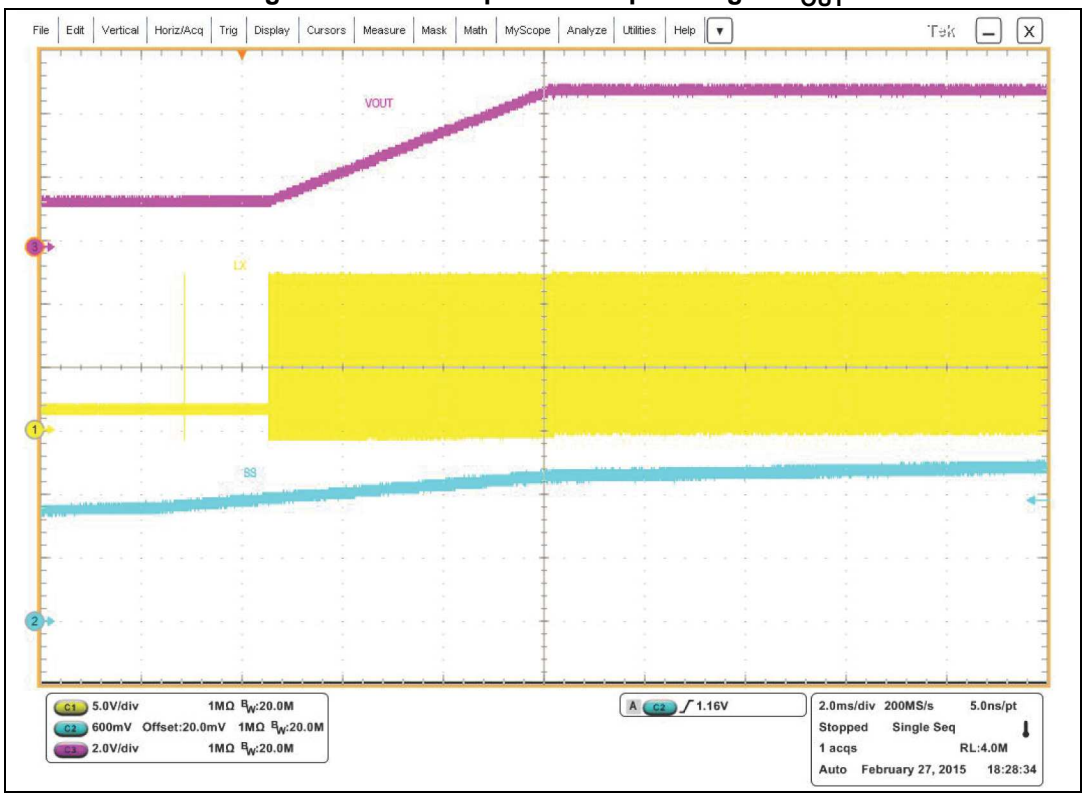
Equation 1

$$C_{SS} = SS_{GAIN} \bullet \frac{I_{SSCH} \bullet T_{SS}}{V_{FB}} = 3 \bullet \frac{4\mu A \bullet T_{SS}}{0.85V}$$

where T_{SS} is the soft-start time, $I_{SS\ CH}$ the charging current and V_{FB} the reference of the error amplifier.

The soft-start block supports the precharged output capacitor.

Figure 6. Soft-start phase with precharged C_{OUT}



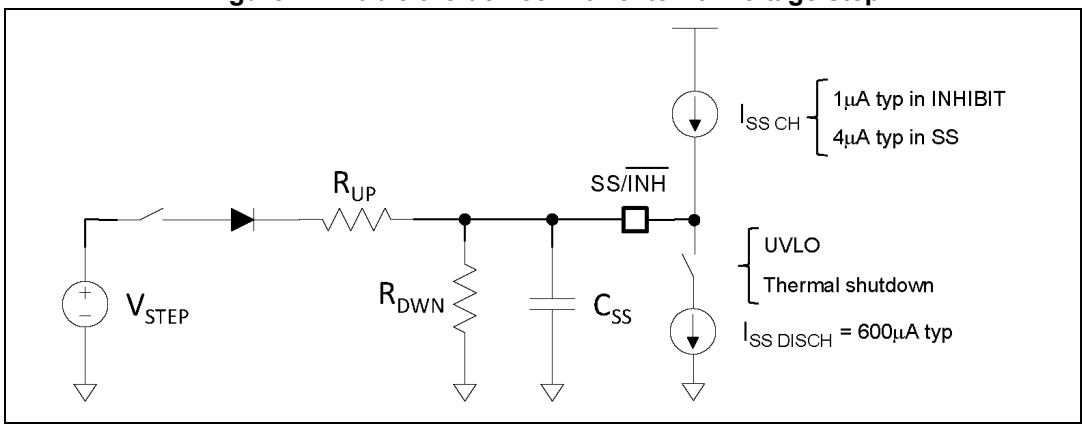
During normal operation a new soft-start cycle takes place in case of:

- Thermal shutdown event
- UVLO event
- The device is driven in $\overline{INH}$ mode

The soft-start capacitor is discharged with a 0.6 mA typ. current capability for 1 msec time max. For complete and proper capacitor discharge in case of fault condition, a maximum C_{SS} = 67 nF value is suggested.

The application example in *Figure 7* shows how to enable the A6986F and perform the soft-start phase driven by an external voltage step, for example the signal from the ignition switch in automotive applications.

Figure 7. Enable the device with external voltage step



The maximum capacitor value has to be limited to guarantee the device can discharge it in case of thermal shutdown and UVLO events (see *Figure 9*), so restart the switching activity ramping the error amplifier reference voltage.

Equation 2

$$C_{SS} < \frac{-1\ \text{msec}}{R_{SS\_EQ} \cdot \ln\left(1 - \frac{V_{SS\_FINAL} - 0.9\ V}{600\ \mu A - R_{SS\_EQ}}\right)}$$

where:

Equation 3

$$R_{SS\_EQ} = \frac{R_{UP} \cdot R_{DWN}}{R_{UP} + R_{DWN}} \qquad V_{SS\_FINAL} = (V_{STEP} - V_{DIODE}) \cdot \frac{R_{DWN}}{R_{UP} + R_{DWN}}$$

The optional diode prevents to disable the device if the external source drops to ground.

R_{UP} value is selected in order to make the capacitor charge at first approximation independent from the internal current generator (4 µA typ. current capability, see *Table 5 on page 8*), so:

Equation 4

$$\frac{V_{STEP} - V_{DIODE} - V_{SS\ END}}{R_{UP}} \gg I_{SS\ CHARGE} \equiv 4\ \mu A$$

where:

Equation 5

$$V_{SS\ END} = V_{SS\ START} + \frac{V_{FB}}{SS_{GAIN}}$$

represents the SS/$\overline{\text{INH}}$ voltage correspondent to the end of the ramp on the error amplifier (see *Figure 5*); refer to *Table 5* for $V_{SS\ START}$, V_{FB} and SS_{GAIN} parameters.

As a consequence the voltage across the soft-start capacitor can be written as:

Equation 6

$$v_{SS}(t) = V_{SS\_FINAL} \cdot \frac{1}{1 - e^{-\frac{t}{C_{SS} \cdot R_{SS\_EQ}}}}$$

R_{SS_DOWN} is selected to guarantee the device stays in inhibit mode when the internal generator sources 1 µA typ. out of the SS/INH pin and V_{STEP} is not present:

Equation 7

$$R_{DWN} \cdot I_{SS\ INHIBIT} \equiv R_{DWN} \cdot 1\ \mu A \ll V_{INH} \equiv 200\ mV$$

so:

Equation 8

$$R_{DWN} < 100\ k\Omega$$

R_{UP} and R_{DWN} are selected to guarantee:

Equation 9

$$V_{SS\_FINAL} \cong 2\ V > V_{SS\_END}$$

The time to ramp the internal voltage reference can be calculated from *Equation 10*:

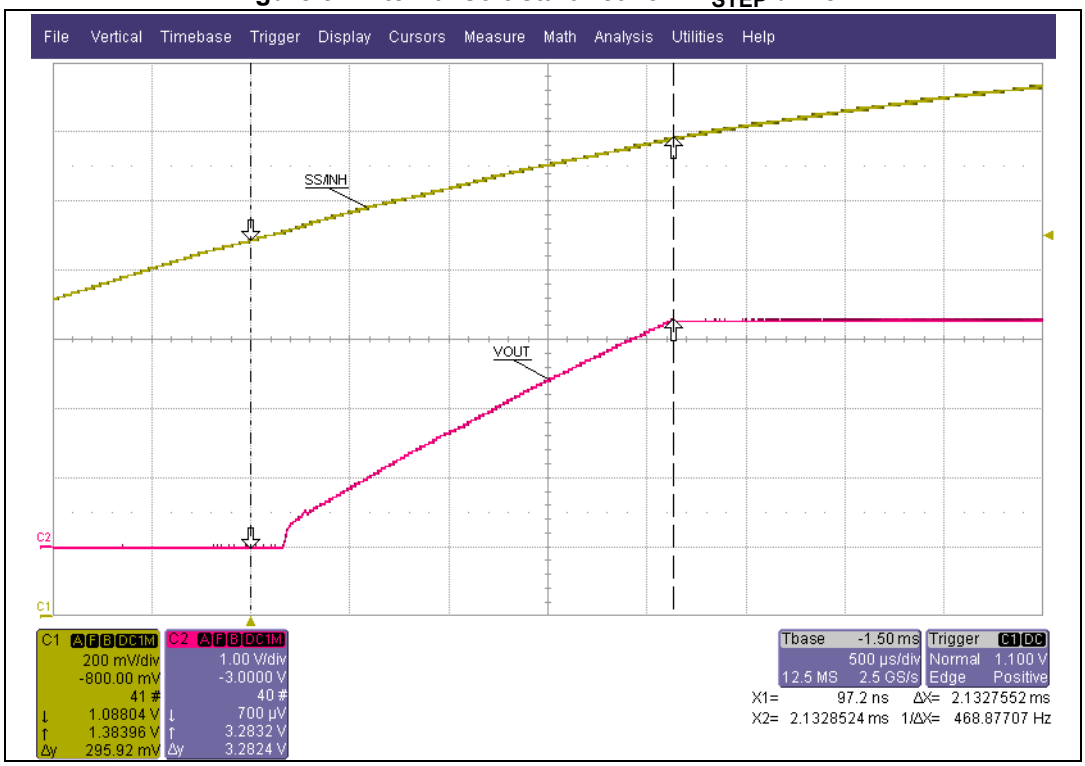
Equation 10

$$T_{SS} = C_{SS} \cdot R_{SS\_EQ} \cdot \ln\left(\frac{V_{SS\_FINAL} - V_{SS\ START}}{V_{SS\_FINAL} - V_{SS\ END}}\right)$$

that is the equivalent soft-start time to ramp the output voltage.

Figure 8 shows the soft-start phase with the following component selection: R_{UP} = 180 kΩ, R_{DWN} = 33 kΩ, C_{SS} = 200 nF, the 1N4148 is a small signal diode and V_{STEP} = 13 V.

Figure 8. External soft-start network V_{STEP} driven



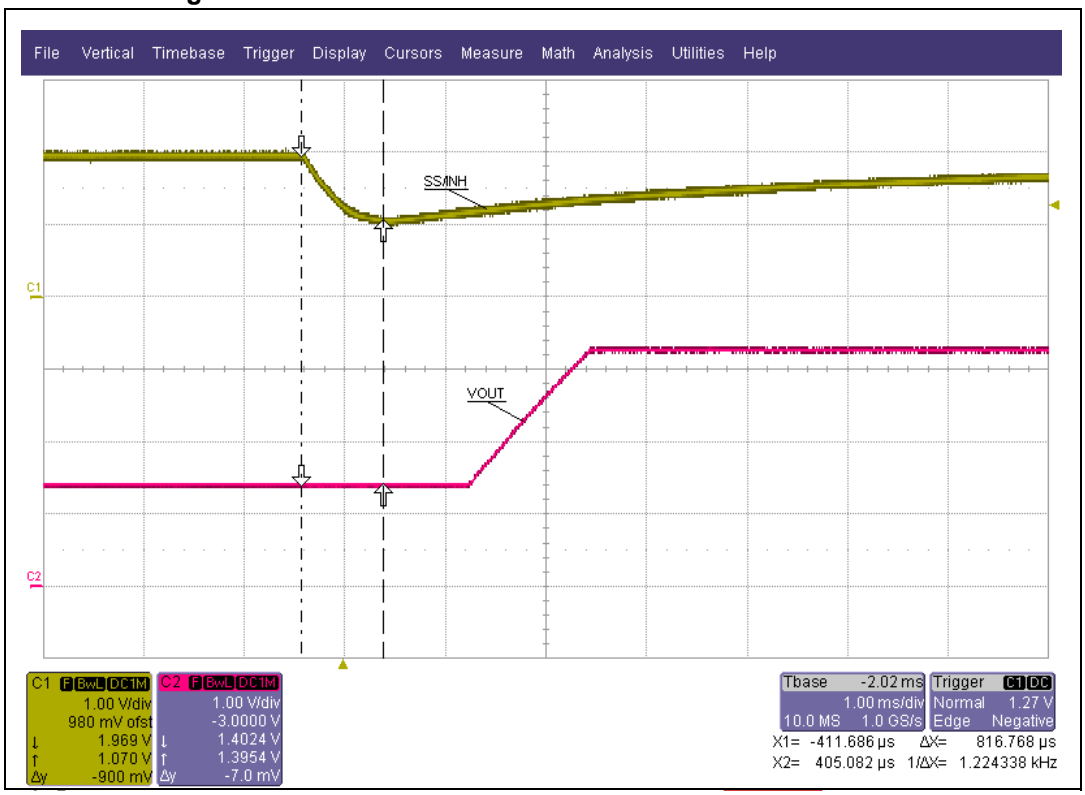
The circuit in *Figure 7* introduces a time delay between V_{STEP} and the switching activity that can be calculated as:

Equation 11

$$T_{SS\ DELAY} = C_{SS} \cdot R_{SS\_EQ} \cdot \ln\left(\frac{V_{SS\_FINAL}}{V_{SS\_FINAL} - V_{SS\ START}}\right)$$

Figure 9 shows how the device discharges the soft-start capacitor after an UVLO or thermal shutdown event in order to restart the switching activity ramping the error amplifier reference voltage.

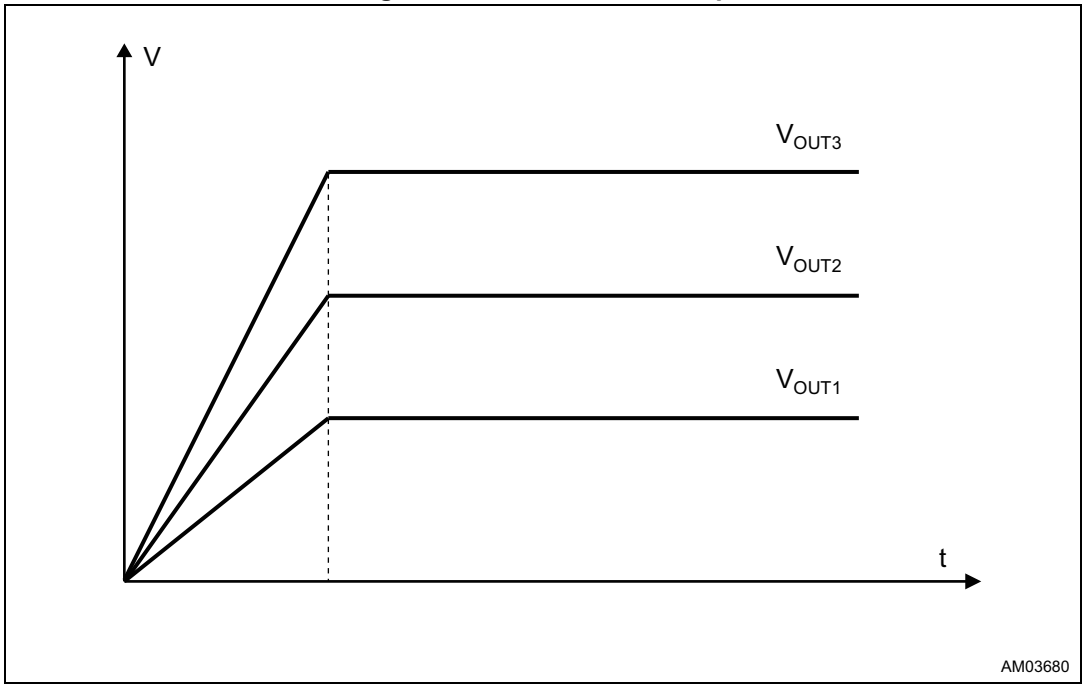
Figure 9. External soft-start after UVLO or thermal shutdown



5.3.1 Ratiometric startup

The ratiometric startup is implemented sharing the same soft-start capacitor for a set of the A6986F devices.

Figure 10. Ratiometric startup



As a consequence all the internal current generators charge in parallel the external capacitor. The capacitor value is dimensioned accordingly with *Equation 12*:

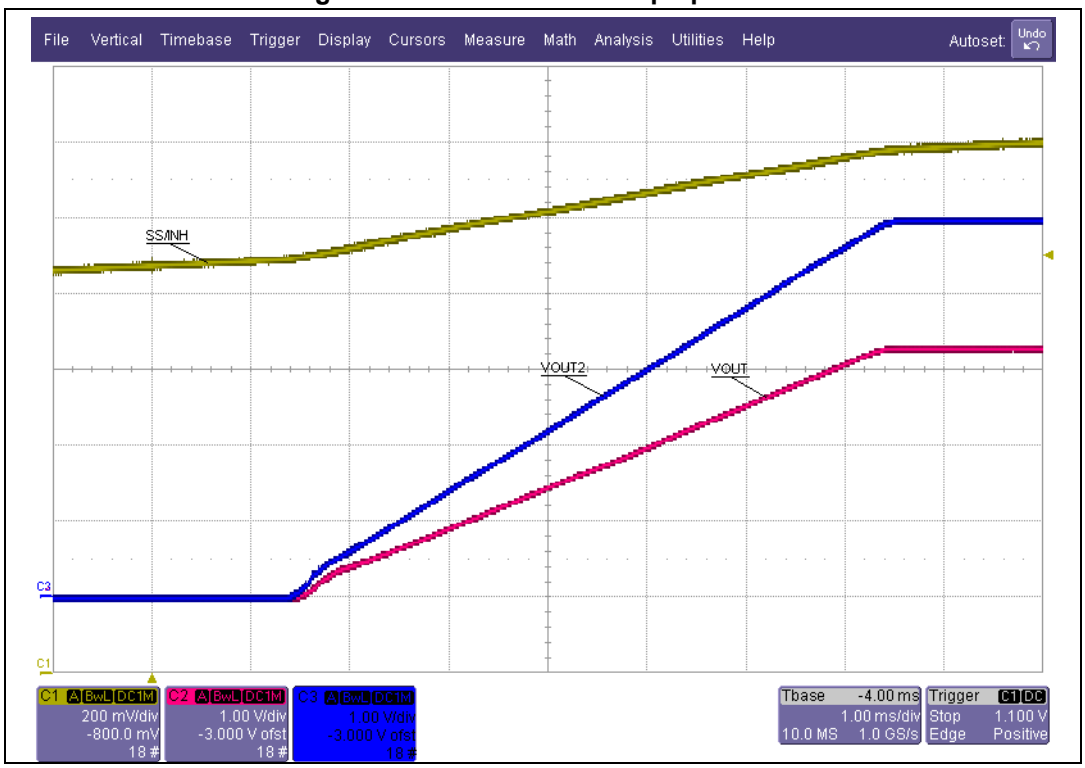
Equation 12

$$C_{SS} = n_{A6986F} \bullet SS_{GAIN} \bullet \frac{I_{SSCH} \bullet T_{SS}}{V_{FB}} = n_{A6986F} \bullet 3 \bullet \frac{4\mu A \bullet T_{SS}}{0.85V}$$

where n_{A6986F} represents the number of devices connected in parallel.

For better tracking of the different output voltages the synchronization of the set of regulators is suggested.

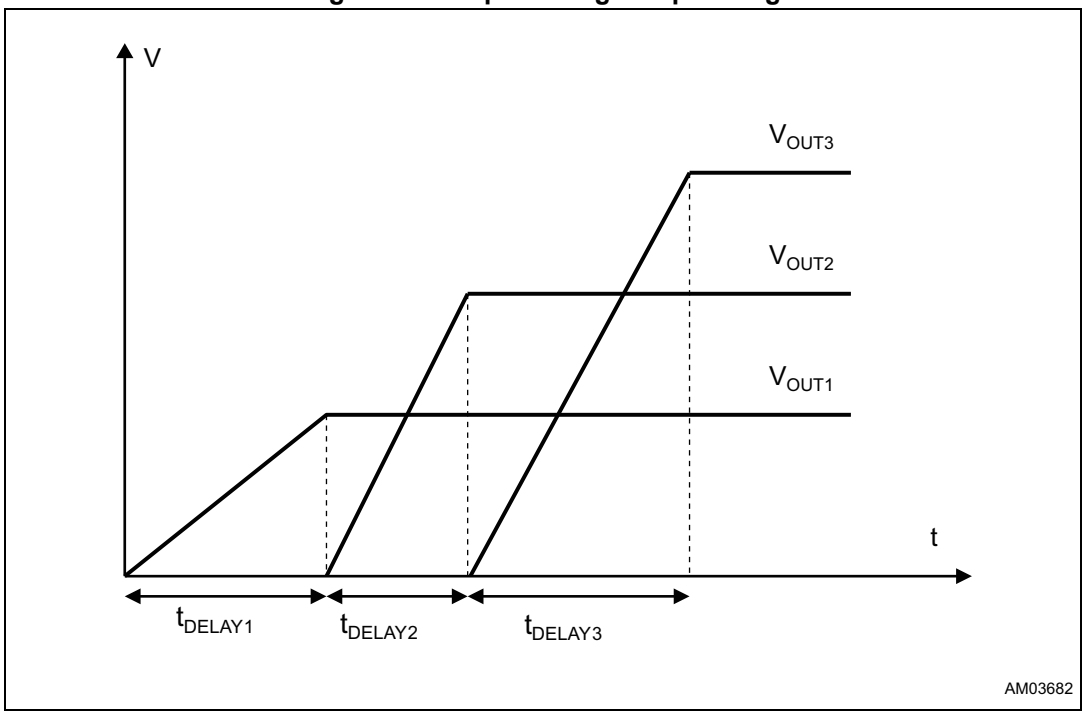
Figure 11. Ratiometric startup operation



5.3.2 Output voltage sequencing

The A6986F device implements sequencing connecting the RST pin of the master device to the SS/INH of the slave. The slave is inhibited as long as the master output voltage is outside regulation so implementing the sequencing (see *Figure 12*).

Figure 12. Output voltage sequencing



High flexibility is achieved thanks to the programmable RST thresholds (*Table 7 on page 11* and *Table 8 on page 12*) and programmable delay time. To minimize the component count the DELAY pin capacitor can be also omitted so the pin works as a normal Power Good.

5.4 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (0.85 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage.

Table 10. Uncompensated error amplifier characteristics

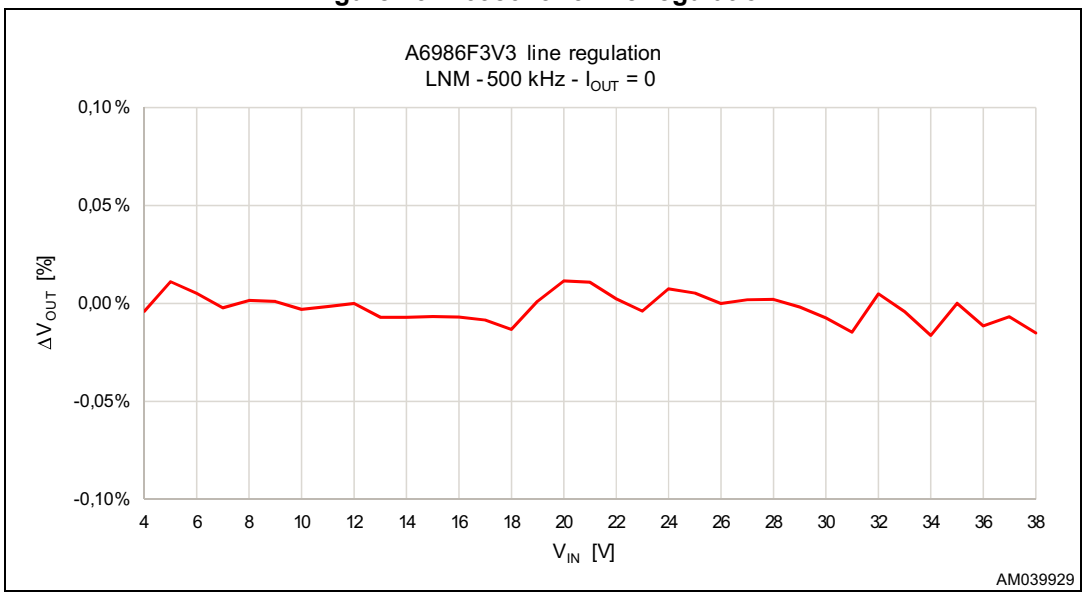
Description	Values
Transconductance	155 µS
Low frequency gain	100 dB

The error amplifier output is compared with the inductor current sense information to perform PWM control. The error amplifier also determines the burst operation at light-load when the LCM is active.

5.5 Output voltage line regulation

The regulator features an enhanced line regulation thanks to the peak current mode architecture. *Figure 13* shows negligible output voltage variation (normalized to the value measured at V_{IN} = 12 V) over the entire input voltage range for the A6986F3V3.

Figure 13. A6986F3V3 line regulation



5.6 Output voltage load regulation

Figure 14 shows negligible output voltage variation (normalized to the value measured at I_{OUT} = 0 A) over the entire output current range for the A6986F3V3, measured on the A6986F3V3 evaluation board (see *Section 8: Application board on page 61*).

Figure 14. A6986F3V3 load regulation