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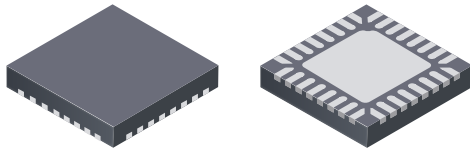
## Dual LNB Supply and Control Voltage Regulators

### Features and Benefits

- Integrated boost MOSFET, current sensing, and compensation
- Configurable boost capacitor option through I<sup>2</sup>C™ control register: ceramic or electrolytic
- Two switching frequency settings programmable through I<sup>2</sup>C™ control register (563 kHz and 939 kHz)
- Adjustable LNB output current limit from 250 to 950 mA
  - Covers a wide array of application requirements
  - Minimizes component sizing to fit each application
  - For startup, reconfiguration, and continuous output
  - Optional temporary increased current limit (+25%)
  - Internal gate drive output BFGATE<sub>x</sub> for bypass FET used in DiSEqC™ applications

*Continued on the next page...*

**Package: 32-contact MLP/QFN with exposed thermal pad (suffix ET)**



5 mm × 5 mm × 0.90 mm

### Description

The A8302 is a dual channel low noise block converter regulator (LNBR). The A8302 consists of a monolithic linear and switching voltage regulator, specifically designed to provide the power and the interface signals to an LNB down converter via coaxial cable in satellite TV receivers systems. The A8302 requires few external components, with the boost switch and compensation circuitry integrated inside of the device. The boost converter switching frequency and user-controlled current limit minimize the size of the passive filtering components. User controlled current limit and two switching frequency settings allow to optimize size of passive filtering components.

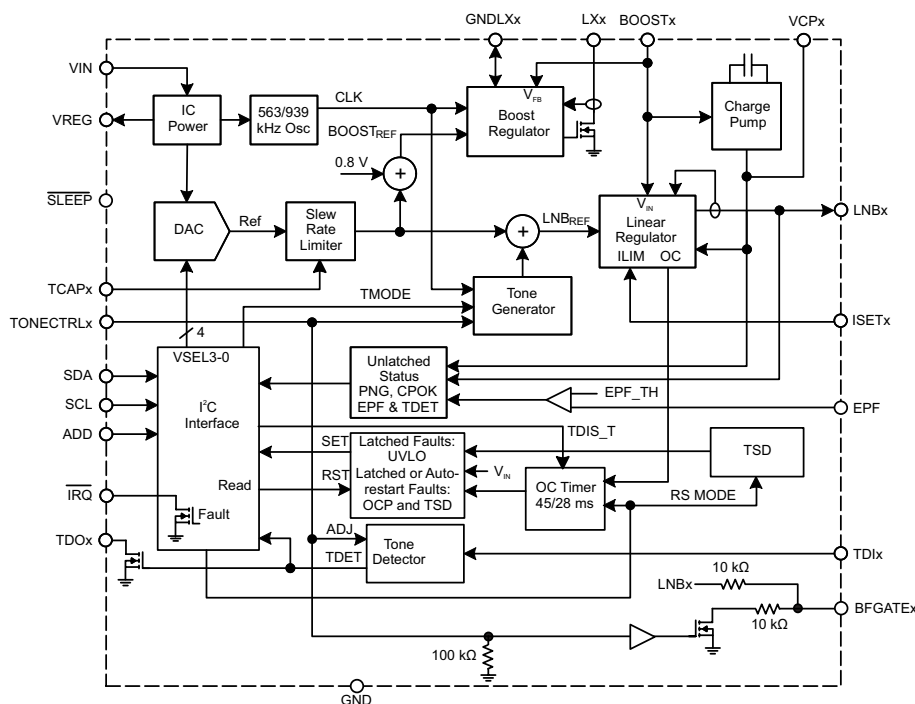
A sleep pin is available to maximize power savings and to quickly shut down the device if needed, without using I<sup>2</sup>C™ control.

The A8302 has integrated tone detection capability and the internal driver allows full two-way DiSEqC™ communications. For DiSEqC™ communication, the IC provides an internal 22-kHz tone that is gated with the TONCTRL<sub>x</sub> pin or accepts an external 22-kHz tone through the TONCTRL<sub>x</sub> pin.

*Continued on the next page...*

### Functional Block Diagram

(One of two channels shown, x in pin name indicates channel: 1 or 2)



## Features and Benefits (continued)

- Boost peak current limit scales with LNB current limit setting
- Early Power Failure (EPF) warning
- SINK\_DIS bit to control maximum output reverse current
- 8 programmable LNB output voltage (DAC) levels
- LNB overcurrent limit protection and TSD with auto-restart or latched
- LNB transition times configurable by external capacitor
- Built-in 22-kHz tone oscillator facilitates DiSEqC™ tone encoding
  - Tone generation does not require additional external components
- Diagnostic features: PNGx, TDET<sub>x</sub>, BOOST<sub>x</sub>H and EPF
- Dynamic tone detect amplitude and frequency transmit/receive thresholds
- Extensive protection features: UVLO, TSD, OCP<sub>x</sub>, and CPOK<sub>x</sub>
- Sleep mode with shutdown current < 15 μA (typ)

## Description (continued)

The A8302 offers Early Power Failure (EPF) warning, which helps to initiate shutdown routines. The A8302 maximum output reverse current can be set using the SINK\_DIS bit.

A comprehensive set of fault registers are provided, which comply with all the common standards, including: overcurrent, thermal shutdown, undervoltage, and power not good.

The device uses a 2-wire bidirectional serial interface, compatible with the I<sup>2</sup>C™ standard, that operates up to 400 kHz.

The A8302 is supplied in a 5 mm × 5 mm, 32-contact, lead (Pb) free QFN package (suffix ET), with 100% matte tin plated leadframe.

## Selection Guide

Part Number	Packing <sup>1</sup>	Description
A8302SETTR-T <sup>2</sup>	7 in. reel, 1500 pieces/reel 12 mm carrier tape	ET package, QFN surface mount 5 mm × 5 mm × 0.90 mm nominal height



<sup>1</sup>Contact Allegro for additional packing options.

<sup>2</sup>Leadframe plating 100% matte tin.

## Absolute Maximum Ratings

Characteristic	Symbol	Conditions	Rating	Unit
Load Supply Voltage, VIN Pin	V <sub>IN</sub>		25	V
Output Current <sup>1</sup>	I <sub>OUT</sub>		Internally Limited	A
Output Voltage; BOOST <sub>x</sub> and BFGATE <sub>x</sub> Pins			-0.3 to 43	V
LNB <sub>x</sub> Pin <sup>2</sup>		Surge	-1.0 to 43	V
LX <sub>x</sub> Pin			-0.3 to 30	V
VCP <sub>x</sub> Pin			-0.3 to 48	V
Logic Input Voltage			-0.3 to 5.5	V
Logic Output Voltage			-0.3 to 5.5	V
EPF and VREG Pins			-0.3 to 6	V
Operating Ambient Temperature	T <sub>A</sub>	Range S; T <sub>A</sub> (max) depends on thermal design; overriding factor is T <sub>J</sub> (max)	-20 to 85	°C
Junction Temperature	T <sub>J</sub> (max)		150	°C
Storage Temperature	T <sub>stg</sub>		-55 to 150	°C

<sup>1</sup>Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current ratings, or a junction temperature, T<sub>J</sub>, of 150°C.

<sup>2</sup>See application schematics 3 and 4 on pages 38 and 40.



**Thermal Characteristics** may require derating at maximum conditions

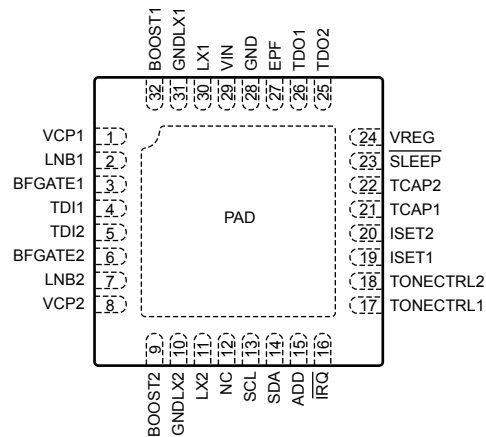
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	30	°C/W

\*Additional thermal information available on the Allegro website

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Pin-out Diagram



Terminal List Table

Number	Name	Function
1	VCP1	Channel 1 gate supply voltage
2	LNB1	Channel 1 output voltage to LNB
3	BFGATE1	Channel 1 gate driver point for the external P-channel bypass MOSFET
4	TDI1	Channel 1 Tone Detect input
5	TDI2	Channel 2 Tone Detect input
6	BFGATE2	Channel 2 gate driver point for the external P-channel bypass MOSFET
7	LNB2	Channel 2 output voltage to LNB
8	VCP2	Channel 2 gate supply voltage
9	BOOST2	Tracking supply voltage to channel 2 linear regulator
10	GNDLX2	Channel 2 boost switch ground
11	LX2	Channel 2 internal boost switch drain node
12	NC	No connect
13	SCL	I <sup>2</sup> C-compatible clock input
14	SDA	I <sup>2</sup> C-compatible data input/output
15	ADD	Address select
16	IRQ	Interrupt request output
17	TONECONTRL1	Apply a 22-kHz tone or tone on-and-off signal to enable/disable internal tone of channel1
18	TONECONTRL2	Apply a 22-kHz tone or tone on-and-off signal to enable/disable internal tone of channel2
19	ISET1	Terminal for external resistor that sets the LNB1 current limit
20	ISET2	Terminal for external resistor that sets the LNB2 current limit
21	TCAP1	Capacitor for setting the rise and fall time of the LNB1 output
22	TCAP2	Capacitor for setting the rise and fall time of the LNB2 output
23	SLEEP	Disables LNB output, boost, I <sup>2</sup> C communication, and charge pump, to reduce input quiescent current to <15 μA
24	VREG	Analog supply
25	TDO2	Open-drain logic output that transitions high when a 22-kHz tone is present at the TDI2 pin
26	TDO1	Open-drain logic output that transitions high when a 22-kHz tone is present at the TDI1 pin
27	EPF	Early Power Failure warning comparator output
28	GND	Signal ground
29	VIN	Input supply voltage
30	LX1	Channel 1 internal boost switch drain node
31	GNDLX1	Channel 1 boost switch ground
32	BOOST1	Tracking supply voltage to channel 1 linear regulator
-	PAD	Exposed pad for thermal dissipation; connect to the ground plane

**ELECTRICAL CHARACTERISTICS<sup>1</sup>** at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 10$  to  $16$  V, ● as noted<sup>2</sup>; unless noted otherwise

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>General</b>						
Output Voltage Accuracy	$V_{OUTx}$	$V_{IN} = 12$ V, $I_{OUTx} = 10$ mA, see table 3a for DAC settings	● -2	-	2	%
Load Regulation	$\Delta V_{OUTx(Load)}$	$V_{IN} = 12$ V, $V_{OUTx} = 13.667$ V, $\Delta I_{OUTx} = 10$ to $700$ mA	● -	75	120	mV
		$V_{IN} = 12$ V, $V_{OUTx} = 19.000$ V, $\Delta I_{OUTx} = 10$ to $700$ mA	● -	85	150	mV
Line Regulation	$\Delta V_{OUTx(Line)}$	$V_{IN} = 10$ to $16$ V, $V_{OUTx} = 13.667$ V, $I_{OUTx} = 10$ mA	● -10	0	10	mV
		$V_{IN} = 10$ to $16$ V, $V_{OUTx} = 19.000$ V, $I_{OUTx} = 10$ mA	● -10	0	10	mV
Supply Current	$I_{IN(OFF)}$	ENB1 and ENB2 bits = 0, $V_{IN} = 12$ V	-	7	-	mA
	$I_{IN(ON)}$	ENB1 and ENB2 bits = 1, $V_{IN} = 12$ V, $V_{OUTx} = 19$ V, $I_{LOAD} = 10$ mA, TONCTRLx = 0	-	65	-	mA
		ENB1 and ENB2 bits = 1, $V_{IN} = 12$ V, $V_{OUTx} = 19$ V, $I_{LOAD} = 10$ mA, TONCTRLx = 1	-	85	-	mA
		$\overline{SLEEP} = 0$ V, $V_{IN} = 12$ V, TONCTRLx = 0	-	-	15	$\mu\text{A}$
Boost Switch On Resistance	$R_{DS(on)BOOST}$	$I_{LOAD} = 450$ mA	-	300	-	m $\Omega$
Switching Frequency	$f_{SW}$	FSW bit = 0	507	563	619	kHz
		FSW bit = 1	845	939	1032	kHz
Minimum Controllable On-Time	$t_{ON(min)}$		-	85	-	ns
Linear Regulator Voltage Drop	$\Delta V_{REGx}$	$V_{BOOSTx} - V_{LNBx}$ , no tone signal, $I_{LOAD} = 700$ mA	600	800	1000	mV
TCAPx Pin Current	$I_{CHGx}$	TCAP capacitor (CTCAP in application drawings) charging	-13	-10	-7	$\mu\text{A}$
	$I_{DISCHGx}$	TCAP capacitor (CTCAP in application drawings) discharging	7	10	13	$\mu\text{A}$
Output Voltage Rise Time <sup>3</sup>	$t_r(V_{LNB})$	For $V_{LNBx}$ 13 $\rightarrow$ 19 V; CTCAP (see application drawings) = 100 nF, $I_{LOADx} = 700$ mA	-	10	-	ms
Output Voltage Pull-Down Time <sup>3</sup>	$t_r(V_{LNB})$	For $V_{LNBx}$ 19 $\rightarrow$ 13 V; $C_{LOAD} = 100$ $\mu\text{F}$ , $I_{LOADx} = 0$ mA, SINK_DIS bit = 0	-	20	-	ms

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### ELECTRICAL CHARACTERISTICS<sup>1</sup> (continued) at T<sub>A</sub> = 25°C, V<sub>IN</sub> = 10 to 16 V, ● as noted<sup>2</sup>; unless noted otherwise

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Reverse Current	I <sub>RLNBx</sub>	ENBx bit = 0	–	2	4	mA
		SINK_DIS bit = 1, ENBx bit = 1, TONECTRLx = 0	–	7	10	mA
		SINK_DIS bit = 0, ENBx bit = 1, TONECTRLx = 0,  V <sub>LNBx</sub> - V <sub>SELx</sub>   < 1.5 V	–	25	40	mA
		SINK_DIS bit = 0, ENBx bit = 1, TONECTRLx = 1,  V <sub>LNBx</sub> - V <sub>SELx</sub>   < 1.5 V	–	60	85	mA
		SINK_DIS bit = 0, ENBx bit = 1, TONECTRLx = 0 or 1,  V <sub>LNBx</sub> - V <sub>SELx</sub>   > 1.5 V	–	7	10	mA
LNBx Off Current	I <sub>LNBx(OFF)</sub>	V <sub>IN</sub> = 16 V	–	–	10	μA
<b>General (continued)</b>						
Ripple and Noise on LNBx Output <sup>4</sup>	V <sub>ripn(pp)</sub>	20 MHz BWL; reference circuit shown in Functional Block diagram; contact Allegro for additional information on application circuit board design	–	30	–	mV <sub>PP</sub>
VREG Voltage	V <sub>VREG</sub>	V <sub>IN</sub> = 10 V	4.97	5.25	5.53	V
ISETx Voltage	V <sub>ISETx</sub>	V <sub>IN</sub> = 10 V	3.4	3.5	3.6	V
TCAPx Voltage	V <sub>TCAPx</sub>	V <sub>IN</sub> = 10 V, V <sub>OUTx</sub> = 13.667 V	–	2.28	–	V
		V <sub>IN</sub> = 10 V, V <sub>OUTx</sub> = 19.000 V	–	3.17	–	V
<b>Protection Circuitry</b>						
Output Overcurrent Limit <sup>5</sup>	I <sub>OUTx(MAX)</sub>	R <sub>SETx</sub> = 100 kΩ ●	220	300	380	mA
		R <sub>SETx</sub> = 37.4 kΩ ●	720	800	880	mA
Overcurrent Disable Time	t <sub>DIS</sub>	TDIS_T bit = 1	–	45	–	ms
		TDIS_T bit = 0	–	28	–	ms
Overcurrent Re-Enable Time	t <sub>REN</sub>	RSMODE bit = 1	–	1	–	s
Boost MOSFET Current Limit	I <sub>BOOSTx(MAX)</sub>	R <sub>SETx</sub> = 100 kΩ	1300	1800	2300	mA
		R <sub>SETx</sub> = 37.4 kΩ	2800	3300	3800	mA
VIN Undervoltage Lockout Threshold	V <sub>UVLO</sub>	V <sub>IN</sub> falling	8.05	8.35	8.65	V
VIN Turn-On Threshold	V <sub>IN(th)</sub>	V <sub>IN</sub> rising	8.40	8.70	9.00	V
I <sup>2</sup> C™ Undervoltage Lockout Threshold	V <sub>UVLO_I2C</sub>	V <sub>IN</sub> falling	–	5.5	–	V
I <sup>2</sup> C™ Turn-On Threshold	V <sub>IN(th)_I2C</sub>	V <sub>IN</sub> rising	–	5.7	–	V
Undervoltage Hysteresis	V <sub>UVLOHYS</sub>		–	350	–	mV
Thermal Shutdown Threshold <sup>3</sup>	T <sub>J</sub>		–	165	–	°C

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**ELECTRICAL CHARACTERISTICS<sup>1</sup>** (continued) at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 10$  to  $16\text{ V}$ , ● as noted<sup>2</sup>; unless noted otherwise

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Thermal Shutdown Hysteresis <sup>3</sup>	$\Delta T_J$		–	20	–	$^\circ\text{C}$
Power Not Good (Low)	PNG <sub>x</sub> LOSET	With respect to $V_{LNBx}$ setting; $V_{LNBx}$ low, PNG <sub>x</sub> bit set to 1	88	91	94	%
	PNG <sub>x</sub> LORESET	With respect to $V_{LNBx}$ setting; $V_{LNBx}$ low, PNG <sub>x</sub> bit reset to 0	92	95	98	%
Power Not Good (Low) Hysteresis	PNG <sub>x</sub> LOHYS	With respect to $V_{LNBx}$ setting	–	4	–	%
Power Not Good (High)	PNG <sub>x</sub> HISET	With respect to $V_{LNBx}$ setting; $V_{LNBx}$ high, PNG <sub>x</sub> bit set to 1	106	109	112	%
	PNG <sub>x</sub> HIRESET	With respect to $V_{LNBx}$ setting; $V_{LNBx}$ high, PNG <sub>x</sub> bit reset to 0	102	105	108	%
Power Not Good (High) Hysteresis	PNG <sub>x</sub> HIHYS	With respect to $V_{LNBx}$ setting	–	4	–	%
<b>Tone</b>						
Amplitude	$V_{TONE(PP)x}$	$I_{LNBx} = 0$ to $700\text{ mA}$ , $C_{LNBx} = 750\text{ nF}$	● 500	700	900	$\text{mV}_{PP}$
Frequency	$f_{TONEx}$		● 20	22	24	$\text{kHz}$
Duty Cycle	$D_{TONEx}$		40	50	60	%
Rise Time	$t_{r(TONE)x}$		5	10	15	$\mu\text{s}$
Fall Time	$t_{f(TONE)x}$		5	10	15	$\mu\text{s}$
<b>Tone Detection</b>						
Amplitude	$V_{TDX(PP)x}$	Tone transmit	500	700	900	$\text{mV}_{PP}$
	$V_{TDR(PP)x}$	Tone receive, 22 kHz sine wave	250	650	900	$\text{mV}_{PP}$
Reject Amplitude, Low	$V_{TD(XMT)Lx}$	Tone transmit	–	–	250	$\text{mV}_{PP}$
	$V_{TD(RCV)Lx}$	Tone receive, 22 kHz sine wave	–	–	100	$\text{mV}_{PP}$
Reject Amplitude, High	$V_{TD(XMT)Hx}$	Tone transmit	–	–	1.1	$V_{PP}$
	$V_{TD(RCV)Hx}$	Tone receive, 22 kHz sine wave	–	–	1.1	$V_{PP}$
Frequency Capture	$f_{TD(RCV)x}$	Tone receive, 650 $\text{mV}_{PP}$ sine wave	17	22	27	$\text{kHz}$
	$f_{TD(XMT)x}$	Tone transmit, 650 $\text{mV}_{PP}$ sine wave	20	22	24	$\text{kHz}$
Frequency Reject, Low	$f_{TD(RCV)Lx}$	Tone receive, 650 $\text{mV}_{PP}$ sine wave	12	14	–	$\text{kHz}$
	$f_{TD(XMT)Lx}$	Tone transmit, 650 $\text{mV}_{PP}$ sine wave	15	17	–	$\text{kHz}$
Frequency Reject, High	$f_{TD(RCV)Hx}$	Tone receive, 650 $\text{mV}_{PP}$ sine wave	–	34	37	$\text{kHz}$
	$f_{TD(XMT)Hx}$	Tone transmit, 650 $\text{mV}_{PP}$ sine wave	–	30	33	$\text{kHz}$
Detection Delay	$t_{DETx}$	Tone receive, 650 $\text{mV}_{PP}$ , 22 kHz sine wave	–	1.5	3	cycle
TDI Input Impedance	$Z_{TDIx}$		–	8.6	–	$\text{k}\Omega$
TDO Output Voltage	$V_{TDO(L)x}$	Tone present, $I_{LOAD} = 3\text{ mA}$	–	–	0.4	$\text{V}$

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**ELECTRICAL CHARACTERISTICS<sup>1</sup>** (continued) at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 10$  to  $16$  V, ● as noted<sup>2</sup>; unless noted otherwise

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
TDO Output Leakage	$I_{TDOx}$	Tone absent, $0\text{ V} < V_{TDO} < 5\text{ V}$	–	–	10	$\mu\text{A}$
EPF Pin Threshold	$V_{EPF\_TH}$	$V_{IN}$ voltage falling	–	3.325	–	V
EPF Threshold Hysteresis	$V_{EPF\_TH\_hys}$		–	175	–	mV
BFGATE/LNB Voltage	$V_{BFG\_ON}$	TONCTRLx = high	–	50	–	%
	$V_{BFG\_OFF}$	TONCTRLx = low	–	99	–	%
<b>Tone Control (TONCTRL pin)</b>						
Logic Input	$V_{TNCTL(H)x}$		2.0	–	–	V
	$V_{TNCTL(L)x}$		–	–	0.8	V
Input Leakage Current	$I_{TNCTL(Ik)x}$		–1	–	1	$\mu\text{A}$
<b>Sleep Mode Control ( SLEEP pin)</b>						
Logic Input	$V_{SLP(H)}$		2.0	–	–	V
	$V_{SLP(L)}$		–	–	0.8	V
Input Leakage Current	$I_{SLP(Ik)}$		–	50	–	$\mu\text{A}$
<b>I<sup>2</sup>C™ - Compatible Interface</b>						
Logic Input (SDA and SCL pins)	$V_{SCL(L)}$		–	–	0.8	V
	$V_{SCL(H)}$		2.0	–	–	V
Logic Input Hysteresis	$V_{I2CIHYS}$		–	150	–	mV
Logic Input Current	$I_{I2CI}$	$V_{I2CI} = 0$ to $5\text{ V}$	–10	< $\pm$ 1.0	10	$\mu\text{A}$
Logic Output Voltage (SDA and $\overline{\text{IRQ}}$ pins)	$V_{I2COUT(L)}$	$I_{LOAD} = 3\text{ mA}$	–	–	0.4	V
Logic Output Leakage Current (SDA and $\overline{\text{IRQ}}$ pins)	$I_{I2CLKG}$	$V_{I2COUT(L)} = 0$ to $5\text{ V}$	–	–	10	$\mu\text{A}$
SCL Clock Frequency	$f_{CLK}$		–	–	400	kHz
<b>I<sup>2</sup>C™ Address Setting</b>						
ADD Pin Voltage for Address 0001 000	Address1		0	–	0.7	V
ADD Pin Voltage for Address 0001 001	Address2		1.3	–	1.7	V
ADD Pin Voltage for Address 0001 010	Address3		2.3	–	2.7	V
ADD Pin Voltage for Address 0001 011	Address4		3.0	–	5.0	V

<sup>1</sup>Operation at 16 V may be limited by power loss in the linear regulator.

<sup>2</sup>Indicates specifications guaranteed from  $0 \leq T_J \leq 125^\circ\text{C}$  (min), design goal is  $0 \leq T_J \leq 150^\circ\text{C}$ .

<sup>3</sup>Guaranteed by worst case process simulations and system characterization. Not production tested.

<sup>4</sup>LNB output ripple and noise are dependent on component selection and PCB layout. Refer to the application schematic drawings and the PCB layout recommendations. Not production tested.

<sup>5</sup>Current from the LNB output may be limited by the choice of BOOST components.

## Functional Description

### Boost Converter/Linear Regulator

The A8302 solution contains two tracking current-mode boost converters and Linear regulators. The boost converter tracks the requested LNB voltage to within 800 mV, to minimize power dissipation. Under conditions where the input voltage,  $V_{\text{BOOSTx}}$ , is greater than the output voltage,  $V_{\text{LNBx}}$ , the linear regulator must drop the differential voltage. When operating in these conditions, care must be taken to ensure that the safe operating temperature range of the A8302 is not exceeded.

The A8302 has internal pulse-by-pulse current limiting on the boost converter and DC current limiting on the LNB output to protect the IC against output short to GND faults.

### Boost Converter Operation Under Light Load

At extremely light load or no load, if the BOOSTx voltage tries to exceed the BOOSTx target voltage, the boost converter operates with minimum on-time. The BOOSTx settling voltage depends on: supply voltage, boost inductance, minimum on-time, switching frequency, output power, as well as power loss in the boost inductor, capacitor, and the A8302. If the BOOSTx voltage tries

to exceed 23.7 V, the optionally-enabled adjustable sink is turned on. This internal sink helps to avoid pulse skipping and audible noise with ceramic capacitors on BOOSTx. The internal sink on BOOSTx gradually increases from 0 mA proportional to the result of  $V_{\text{BOOSTx}} - 23.7 \text{ V}$ , and the sink current reaches a maximum value of 17.9 mA when  $V_{\text{BOOSTx}}$  reaches 27 V. Beyond this, if the BOOSTx voltage tries to exceed 27 V, the internal sink current on BOOSTx will be held at 17.9 mA till  $V_{\text{BOOSTx}}$  reaches 28 V. Beyond this, if the BOOSTx voltage tries to exceed 28 V, the A8302 enters into pulse skipping with 350 mV hysteresis. During pulse skipping the internal sink on BOOSTx is turned off when BOOSTx stops switching.

The optional internal sink on BOOSTx is enabled/disabled by setting/resetting Control Register 0 bit 7 (SINK\_NL). This bit is common to both channels. When the SINK\_NL bit is set to 1, the adjustable internal sink is enabled. When the SINK\_NL bit is set to 0, the internal sink on BOOSTx is disabled.

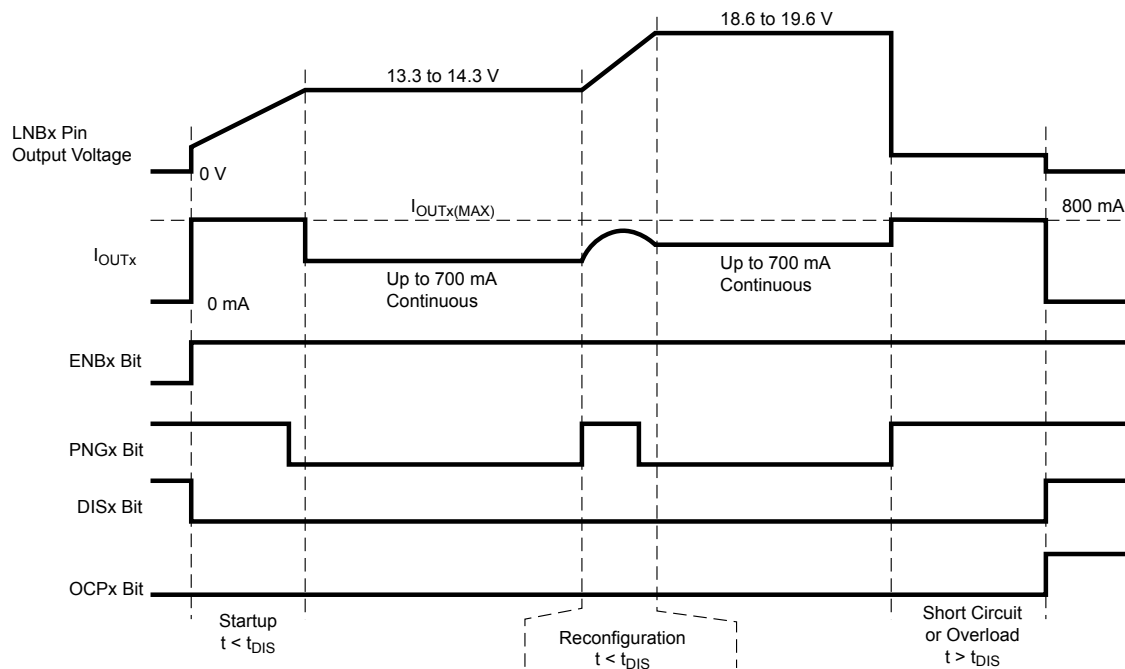


Figure 1. Startup, reconfiguration, and short circuit operation using  $R_{\text{SETx}} = 37.4 \text{ k}\Omega$ , and a capacitive load (OCPx\_25P bit = 0)

### Multiple Outputs

In the case that two or more set top box LNB outputs are connected together by the customer (such as with a splitter), it is possible that one output could be programmed at a higher voltage than the other. This would cause a voltage on one output that is higher than its programmed voltage (for example, 19 V on the output of a 13 V programmed voltage). The output with the highest voltage will effectively turn off the other outputs. As soon as this voltage is reduced below the value of the other outputs, the A8302 output will auto-recover to its programmed levels.

### Charge Pump

Generates a supply voltage above the internal tracking regulator output to drive the linear regulator control.

### LNBx and BOOSTx Current Limits Setting

The LNB output current limit,  $I_{OUTx(MAX)}$  can be set by connecting a resistor ( $R_{SETx}$ ) from the  $ISETx$  pin to GND as shown in the applications schematics. The LNBx current limit can be set from 300 to 1000 mA, corresponding to an  $R_{SETx}$  value of 100 to 30 k $\Omega$ , respectively. See figure 1 for a typical circuit timing example.

The LNBx output current limit can be set as high as 1000 mA (by selecting an  $R_{SETx}$  of 30 k $\Omega$ ), but care should be taken not to exceed the thermal limit of the package, or thermal shutdown (TSD) will occur. The typical LNB output current limit can be set according to the following equation:

$$I_{OUTx(MAX)} = 29,925 / R_{SETx},$$

where  $I_{OUTx(MAX)}$  is in mA and  $R_{SETx}$  is in k $\Omega$ .

If the voltage at the  $ISETx$  pin is 0 V (that is, shorted to GND),  $I_{OUTx(MAX)}$  will be clamped to a moderately high value, 1.2 A. Care should be taken to ensure that  $ISETx$  is not inadvertently grounded. If no resistor is connected to the  $ISETx$  pin (that is, if  $ISETx$  is open-circuit),  $I_{OUTx(MAX)}$  will be set to approximately 0 A and the A8302 will not support any load (OCP will occur prematurely).

The BOOSTx pulse-by-pulse current limit,  $I_{BOOSTx(MAX)}$ , is automatically scaled along with the LNBx output current limit. The typical BOOSTx current limit is set according to the following equation:

$$I_{BOOSTx(MAX)} = 3.0 \times I_{OUTx(MAX)} + 900 \text{ (mA)},$$

where both  $I_{BOOSTx(MAX)}$  and  $I_{OUTx(MAX)}$  are in mA.

Automatically scaling the BOOSTx current limit allows the

designer to choose the lowest possible saturation current of the boost inductor, reducing its physical size and PCB area, thus minimizing cost.

### Protection

The A8302 has a wide range of protection features and fault diagnostics which are detailed in the Status Register section.

### Undervoltage Lockout (UVLO)

The Undervoltage Lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the lockout threshold,  $V_{IN(th)}$ . The UVLO comparator incorporates enough hysteresis,  $V_{UVLOHYS}$ , to prevent on-off cycling of the regulator due to IR drops in the VIN path during heavy loading or during startup.

### Overload and Short Circuit Handling

The A8302 protects the IC against output overload and short circuit. The short circuit disable timer is controlled with the  $TDIS\_T$  bit. If this bit is set to 1, the IC allows an overcurrent condition to persist up to 45 ms and if this bit is set to 0, the maximum overcurrent time allowed is 28 ms. The A8302 provides the option either to latch or to auto-restart on fault. If the  $RSMODE$  bit is set to 1, with an overcurrent condition that exceeds typically 45 ms ( $TDIS\_T$  set to 1) or 28 ms ( $TDIS\_T$  set to 0), the IC turns off output for 1 s and then auto-restarts with the previous settings. This hiccup mode continues as long as output current is greater than the OCP level. The device returns to normal operation when the fault is removed. If  $RSMODE$  is set to 0, the IC turns off after  $t_{DIS}$  time expires, and remains latched. Figures 2a and 2b explain overcurrent protection operation with  $RSMODE$  at 1 and at 0.

The A8302 has an optional 25% bump up on the current limit for  $t_{dis}/4$  period. This feature is enabled/disabled by setting or resetting Control Register 2 bits 0 and 1 for channel 1 and channel 2 respectively. When this bit is enabled, the output current limit is 25% more than the set current limit, or 1000 mA (max), for both limits a minimum of  $t_{dis}/4$  period. After the  $t_{dis}/4$  period, the output current limit comes down to the set limit and the  $OCPx\_25P$  bit is reset to zero. The user must set this bit again to enable the 25% bump up at the next current limit event. If the  $OCPx\_25P$  bit is zero when LNBx output is shorted to ground, the LNBx output current will be clamped to  $I_{OUTx(MAX)}$ . If the short circuit condition lasts for more than 45 ms, the A8302 will be disabled and the  $OCPx$  bit will be set. Refer to figures 16a and 16b.

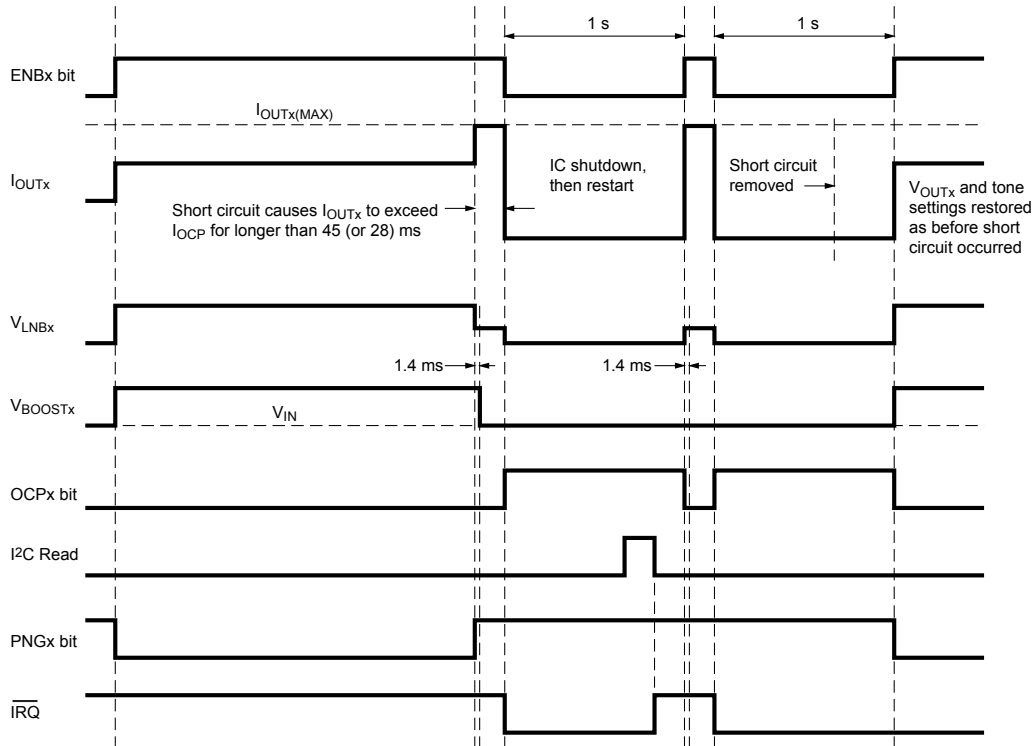


Figure 2a.  $\overline{IRQ}$  and Fault Clearing in Response to Overcurrent (OCP) with auto-retry enabled (RSMODE = 1) and an OCP delay of 45 (or 28) ms (TDIS\_T = 1 (or 0)).  $\overline{IRQ}$  transitions to low at an OCP fault and is reset by an I<sup>2</sup>C Read sequence. The OCP bit clears automatically after 1 s, and the device restarts with the previous settings. This hiccup mode continues as long as the output current is greater than the OCP level. The device returns to normal operation when the fault is removed.

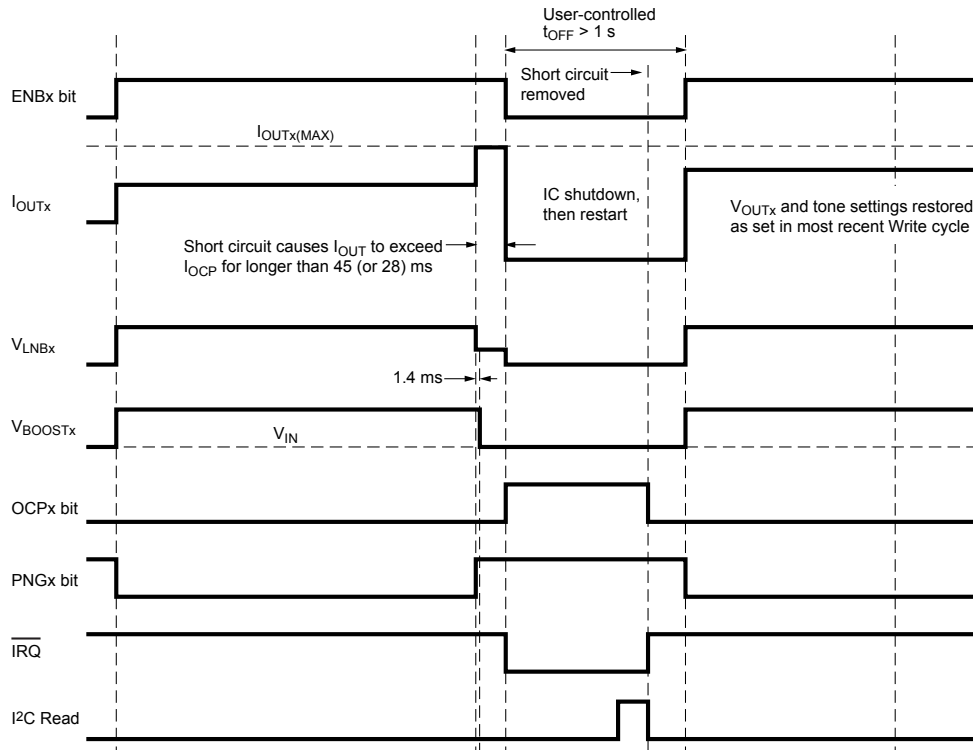


Figure 2b.  $\overline{IRQ}$  and Fault Clearing in Response to Overcurrent (OCP) with latch mode (RSMODE = 0) and an OCP delay of 45 (or 28) ms (TDIS\_T = 1(or 0)).  $\overline{IRQ}$  transitions low at an overcurrent fault, and an I<sup>2</sup>C Read sequence clears the OCP bit and  $\overline{IRQ}$ . An I<sup>2</sup>C Write sequence is required to reenble the part. The retry wait time should be longer than 1 s, to prevent TSD.



### Switching Frequency Selection

The A8302 offers two switching frequencies: 563 kHz and 939 kHz. High switching frequency allows minimizing the component size, which also increases switching losses. Use a high switching frequency setting to optimize component size and take care of A8302 power dissipation. High switching frequency is preferred for low output current applications. Where the A8302 power dissipation is of a concern, use a low switching frequency setting. Refer to application schematic section for details. Switching frequency is adjusted using Control Register 0, bit 4. User program should select a correct switching frequency setting for which the hardware is designed.

### Compensation Network Selection

The A8302 is designed to work with ceramic or electrolytic capacitors on BOOST output. Boost loop compensation required is different for ceramic and electrolytic capacitor options. The proper compensation network is selected by setting Control Register 0, bit 5. User program should select a correct compensation network setting based on the boost capacitor selection.

When  $V_{IN}$  goes below UVLO level, all control registers are reset to default value, that is, 0. The user must write proper bits upon each power-up. Application based bits all are bunched into Control Register 0, which are normally not required to change during operation. Switching frequency, compensation network, and over-current disable delay bits must not be changed during operation.

### Slew Rate Control

During either startup, or when the output voltage at the LNBx pin is transitioning, the output voltage rise and fall times can be set by the value of the capacitor connected from the TCAPx pin to GND (CTCAPx in the applications schematics). Note that during start-up, the BOOSTx pin is pre-charged to the input voltage minus a diode voltage drop. As a result, the slew rate control for the BOOSTx pin occurs from this voltage. See figure 3.

The value of CTCAPx can be calculated using the following formula:

$$CTCAPx = (I_{TCAPx} \times 6) / SR$$

where SR is the required slew rate of the LNB output voltage, in V/s, and  $I_{TCAPx}$  is the TCAPx pin current specified in the Electrical Characteristics table. The recommended value for CTCAPx, 100 nF, should provide satisfactory operation for most applications.

The minimum value of CTCAPx is 10 nF. There is no theoretical maximum value of CTCAPx however too large a value will probably cause the voltage transition specification to be exceeded. Tone generation is unaffected by the value of CTCAPx.

### Pull-Down Rate

In applications that have to operate at very light loads and that require large load capacitances (in the order of tens to hundreds of microfarads), set the SINK\_DIS bit to 0, so the output linear

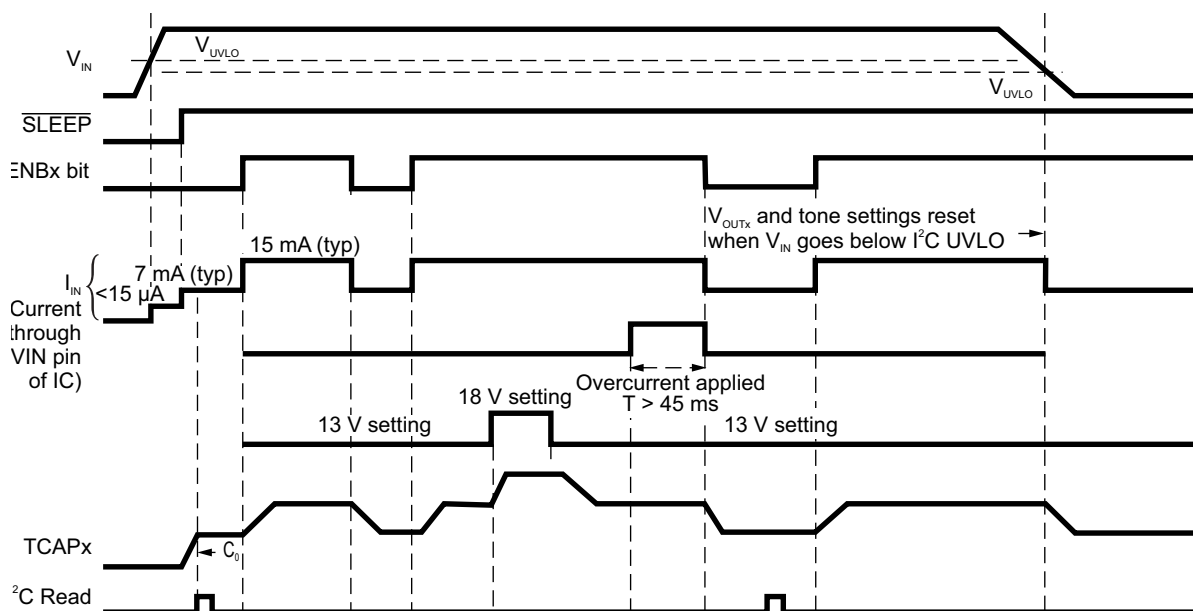


Figure 3. TCAPx timing at startup, transition, and OCP faults. In latch mode (RSMODE = 0).

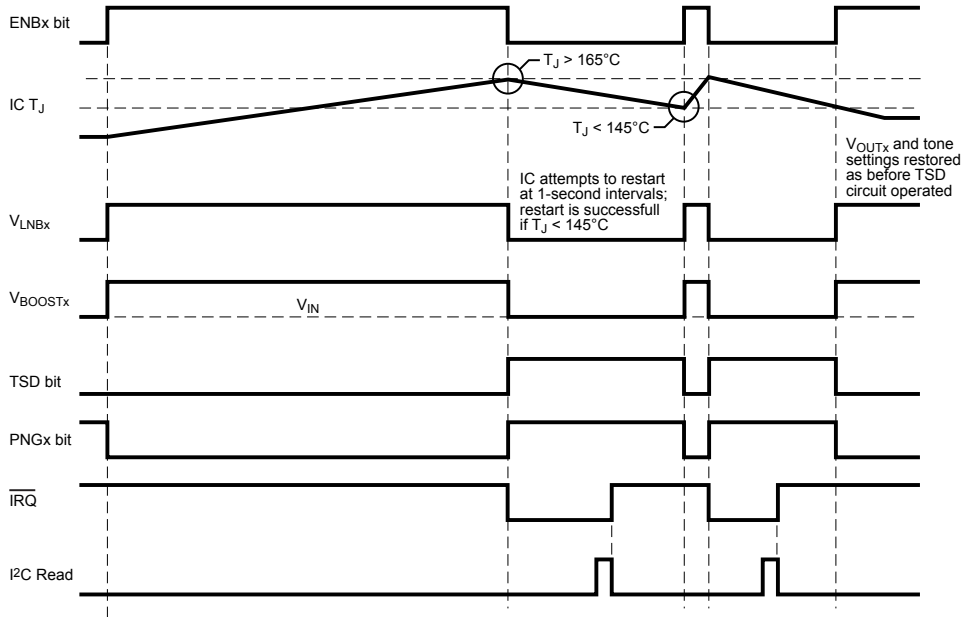


Figure 4a.  $\overline{\text{IRQ}}$  and Fault Clearing in Response to Overtemperature (TSD) with auto-retry (RSMODE = 1). If for any reason the junction temperature exceeds  $165^\circ\text{C}$  (typ), the device LNBx output and the boost converter are disabled. The IC attempts to restart at 1-second intervals, but the LNBx output restarts only when  $T_J$  cools below  $145^\circ\text{C}$ . The  $\overline{\text{IRQ}}$  pin resets on an I<sup>2</sup>C Read sequence, and the TSD bit resets along with an LNBx output restart.

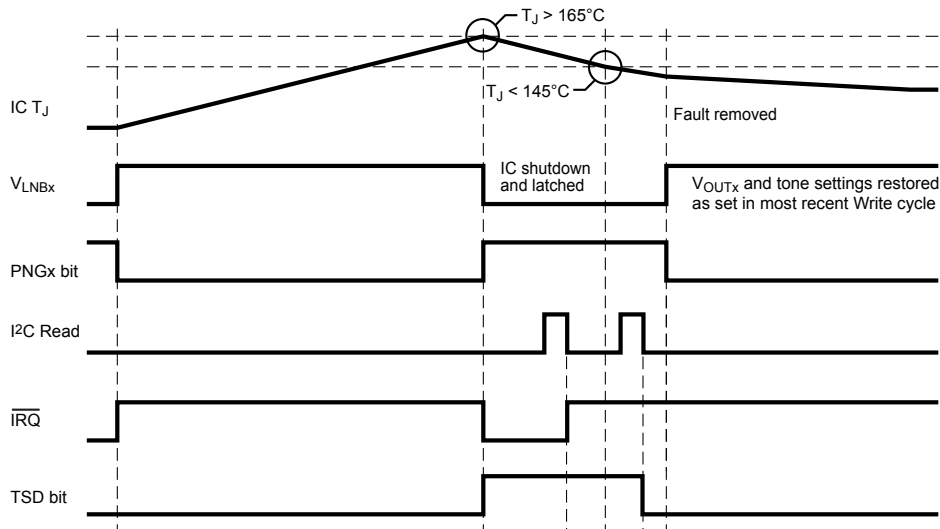


Figure 4b.  $\overline{\text{IRQ}}$  and Fault Clearing in Response to Overtemperature (TSD) with latch mode (RSMODE = 0).  $\overline{\text{IRQ}}$  transitions low after TSD fault, and an I<sup>2</sup>C Read sequence immediately resets the  $\overline{\text{IRQ}}$  pin. The TSD bit is cleared by an I<sup>2</sup>C Read sequence only after the device has cooled to a  $T_J$  below  $145^\circ\text{C}$ . An I<sup>2</sup>C Write sequence is required to reenble the device.

stage provides approximately 25 mA of pull-down capability. This ensures that the LNBx output voltage is ramped from 18 to 13 V in a reasonable amount of time. When the tone is on, the output linear stage increases its pull-down capability to approximately 60 mA. This ensures that the tone signal meets all specifications, even with no load on the on the LNBx output.

### Thermal Shutdown (TSD)

The A8302 protects the IC against overheating. If junction temperature exceeds 165°C (typ), LNBx output and the boost converter output are disabled until  $T_J$  cools below 145°C. The A8302 provides the option either to latch or to auto-restart on fault. If the RSMODE bit is set to 1, the A8302 IC attempts to restart at 1-second intervals, but restart is successful only with  $T_J < 145^\circ\text{C}$ . This hiccup mode continues as long as  $T_J > 145^\circ\text{C}$ . The device returns to normal operation when the fault is removed. If RSMODE is set to 0, the IC turns off, and remains latched. Figures 4a and 4b explain thermal shutdown protection operation with RSMODE at 1 and at 0.

### SINK\_DIS Mode Selection

The A8302 SINK\_DIS bit allows to select the maximum output reverse current. When the SINK\_DIS bit is set to 1, the maximum LNBx back feed current,  $I_{RLNBx}$ , is less than 10 mA. When the outputs of the LNBx converters are shorted, a 10 mA back feed current will prevent loading of one converter output by another converter output.

### Sleep Mode

The A8302 includes a sleep mode that instantly turns off the LNBx output and resets the internal Control register to its default (power-on) state. When the SLEEP pin is low, the A8302 will draw  $I_{IN(OFF)}$  less than 15  $\mu\text{A}$  from the input supply.

### In-Rush Current

At startup or during an LNB Reconfiguration event, a transient surge current above the normal DC operating level can be provided by the A8302. This current increase can be as high as the set output current.

### Tone Generation

The A8302 offers two options for tone generation (figure 5). The TONECTRLx pin with the TMODE control bit provides the necessary control. The TMODE bit controls whether the tone source is internal or external.

When the internal source is used (TMODE bit set to 0), the tone is gated with the TONECTRLx pin. The internal tone frequency

is 22 kHz. Note: This tone can be generated under no-load conditions and does not require an external DiSEqC™ filter.

When the TMODE bit is set to 1, an external 22-kHz tone signal can be applied to the TONECTRLx pin. This tone frequency appears at the LNBx output.  $V_{OUTx}$  reaches the  $V_{LNBref}$  level after TONECTRLx has been low for longer than 42  $\mu\text{s}$ .

### Tone Detection

A 22-kHz tone detector is provided in the A8302. The detector extracts the 22 kHz signal from the AC-coupled TDix pin and provides it as an open-drain logic output at the TDOx pin. Also, when a tone is present, the TDET bit in the Status register is set to 1 and can be seen via the I<sup>2</sup>C interface. The tone detection delay is typically shorter than 1.5 cycles.

The tone detector dynamically adjusts its amplitude and frequency thresholds depending on whether the A8302 is transmitting or receiving a tone signal. If the A8302 is transmitting, the tone detect amplitude threshold is relatively high and the acceptable frequency range is tight. This provides a high quality tone signal is always generated by the A8302. Conversely,

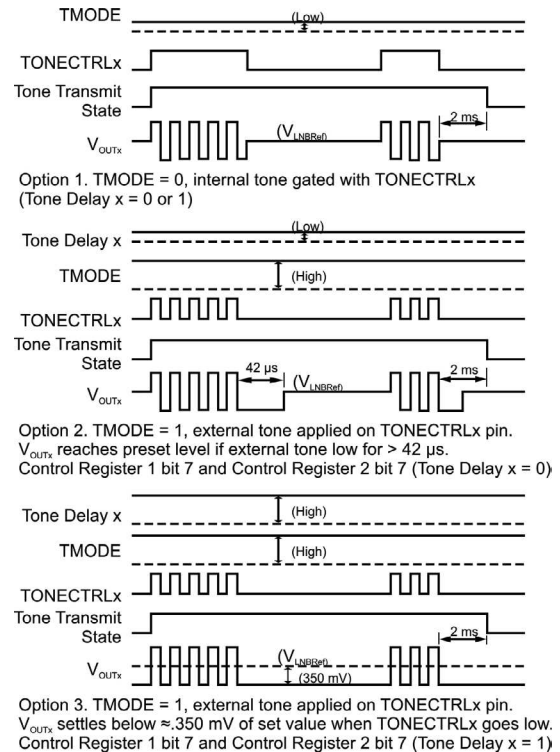


Figure 5. Options for tone generation

if the A8302 is receiving, the tone detect amplitude threshold is reduced and the acceptable frequency range is increased slightly. This provides the A8302 has maximum sensitivity to remotely generated tone signals that may be degraded by long lengths of coaxial cable. The Electrical Characteristics table of this datasheet documents the guaranteed specifications of the tone detector and how they are adjusted by tone transmission or receiving mode.

To help in the understanding, typical tone detector operation is shown graphically in figures 6a and 6b. The shaded areas in figure 6a indicate the accept range of the detector when TONECTRLx is a logic high (transmit) and a logic low (receive). The shaded areas in figure 6b indicate the reject range of the detector when TONECTRLx is a logic high (transmit) and a logic low (receive).

### Early Power Failure Warning (EPF)

The EPF signal gives the microcontroller early warning that the supply voltage is falling below the EPF threshold value, so the microcontroller can start to shed non-critical loads (such as the LNBR) and begin its shutdown routines.

When the voltage on the EPF pin falls below  $V_{EPF\_TH}$ , the EPF bit is set and IRQ is pulled low. When the EPF pin voltage goes above  $V_{EPF\_TH} + V_{EPF\_TH\_hys}$ , the EPF bit is reset after the pro-

grammed delay. The EPF bit resets automatically when the EPF pin voltage goes above  $V_{EPF\_TH} + V_{EPF\_TH\_hys}$ .

The delay between when the EPF pin voltage goes to  $V_{EPF\_TH} + V_{EPF\_TH\_hys}$  and when the EPF bit is reset, is programmed by the EPF0 and EPF1 bits. See table 3b for description.

The following examples explain selection of resistors R1 and R2 to set the EPF warning when  $V_{IN}$  falls to 10.5 V or 7 V.

Case 1: EPF warning when  $V_{IN}$  falls to 10.5 V

Assume:

Nominal Input Voltage = 12 V,

$V_{EPF\_TH} = 3.5$  V,

$V_{EPF\_TH\_hys} = 0.175$  V, and

EPF\_TH1 ( $V_{IN}$  corresponding to setting EPF bit) = 10.5 V.

Given:

$V_{EPF\_TH} = EPF\_TH1 \times R_2 / (R_1 + R_2)$ , where

$R_2 / (R_1 + R_2) = 3.5 / 10.5 = 1/3$ , then

choose  $R_2 = 10$  k $\Omega$ ,  $R_1 = 20$  k $\Omega$ .

Given:

$V_{EPF\_TH} = EPF\_TH2 \times R_2 / (R_1 + R_2)$ , then

EPF\_TH2 ( $V_{IN}$  corresponding to resetting EPF bit) = 11 V

Case2: EPF warning when  $V_{IN}$  falls to 7 V

Assume:

Nominal Input Voltage = 12 V,

$V_{EPF\_TH} = 3.5$  V,

$V_{EPF\_TH\_hys} = 0.175$  V, and

EPF\_TH1 ( $V_{IN}$  corresponding to setting EPF bit) = 7 V.

Given:

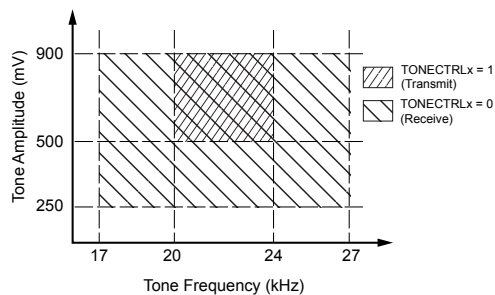


Figure 6a. Accept ranges of Tone Detection feature

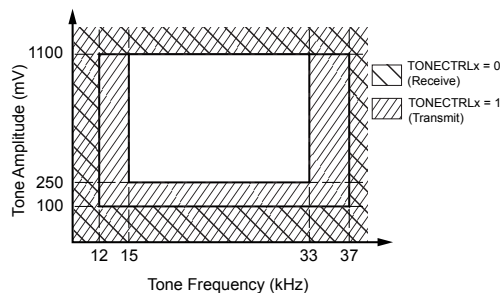


Figure 6b. Reject ranges of Tone Detection feature

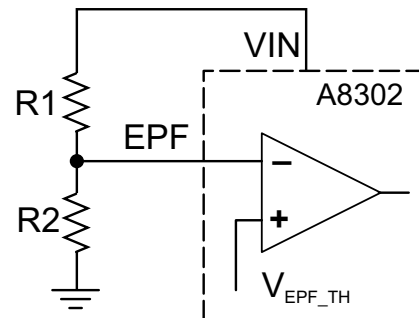


Figure 7. Example circuit for Early Power Failure feature

$V_{EPF\_TH} = EPF\_TH1 \times R_2 / (R_1 + R_2)$ , where  
 $R_2 / (R_1 + R_2) = 3.5 / 7 = 1/2$ , then  
 choose  $R_2 = 10\text{ k}\Omega$ ,  $R_1 = 10\text{ k}\Omega$ .

Given:

$V_{EPF\_TH} + V_{EPF\_TH\_hys} = EPF\_TH2 \times R_2 / (R_1 + R_2)$   
 $EPF\_TH2$  ( $V_{IN}$  corresponding to resetting EPF bit) = 7.35 V.

### Cable Disconnect Detection

A8302 does not go to pulse skipping if the BOOSTx voltage settles below 28V(typ), this facilitates increased boost voltage can be used to detect the cable disconnect. If the given application and supply voltage will ensure BOOSTxH voltage exceed 23.7V (typ) at no-load, Status register 1 bits BOOSTxH can be used for cable disconnect detection.

For the application requirements shown in schematic 3 and 4 at  $V_{in} = 12 \pm 5\%$ , Boost voltage is expected to exceed 23.7V and which sets status register 1 bits BOOSTxH to high. Host controller can decode these bits for the cable disconnect detection.

In the applications where Boost voltage cannot exceed 23.7V (typ) at no-load, A simple potential divider connection on BOOST, as shown in Figure 8, is used to sense the BOOST voltage. When the voltage on EPF pin is below  $V_{EPF\_TH}$ , the EPF

bit is set to 1. When voltage on the EPF pin exceeds  $V_{EPF\_TH} + V_{EPF\_TH\_hys}$ , the EPF bit is reset to 0. The combination of Rc1 and Rc2 is selected such that, when the cable is disconnected, the voltage on the EPF pin exceeds  $V_{EPF\_TH} + V_{EPF\_TH\_hys}$  and resets the EPF bit to 0; otherwise the EPF bit is set to 1.

To enable the cable disconnect test, set the LNB output voltage to 13.333 V and read the Status register bit. If the EPF bit is reset, the cable is disconnected, otherwise the cable is connected. When the cable disconnect feature is used, the EPF pin senses the BOOST voltage, so the Early Power Failure warning (EPF) feature cannot be used.

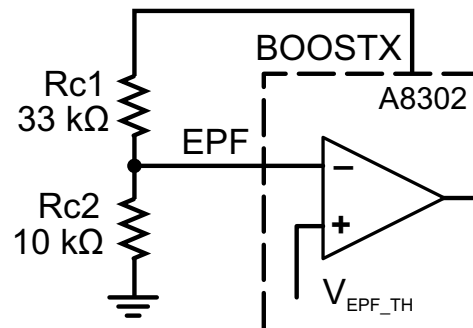


Figure 8. Cable Disconnect Detection



**Component Selection**

**Boost Inductor**

The A8302 is designed to operate with a boost inductor value of either 10  $\mu\text{H} \pm 30\%$  ( Set Fsw bit =0 ) or 4.7  $\mu\text{H} \pm 30\%$  ( Set Fsw bit =1 ) with a DCR less than 75 m $\Omega$ . The error amplifier loop compensation, current sense gain, and PWM slope compensation were chosen for this value of inductor. The boost inductor must be able to support the peak currents required to maintain the maximum LNBx output current without saturating. Figure 9a can be used to determine the peak current in the inductor for given the LNBx load current. The curve labeled Typical uses VIN = 12 V, VBOOST = 20 V, L = 10  $\mu\text{H}$ , and f = 563 kHz, while the curve

labeled Maximum assumes VIN = 10.8 V, VBOOST = 21 V, L = 7  $\mu\text{H}$ , and f = 507 kHz.

Figure 9b can be used to determine the peak current in the inductor for given the LNBx load current. The curve labeled Typical uses VIN = 12 V, VBOOST = 20 V, L = 4.7  $\mu\text{H}$ , and f = 939 kHz, while the curve labeled Maximum assumes VIN = 10.8 V, VBOOST = 21 V, L = 3.3  $\mu\text{H}$ , and f = 845 kHz

**Boost Ceramic Capacitor Option**

The A8302 can be configured to operate with two or three, high-quality ceramic capacitors on the boost node. Allegro recommends capacitors that are rated at least 35 V,  $\pm 10\%$ , X7R, 1210

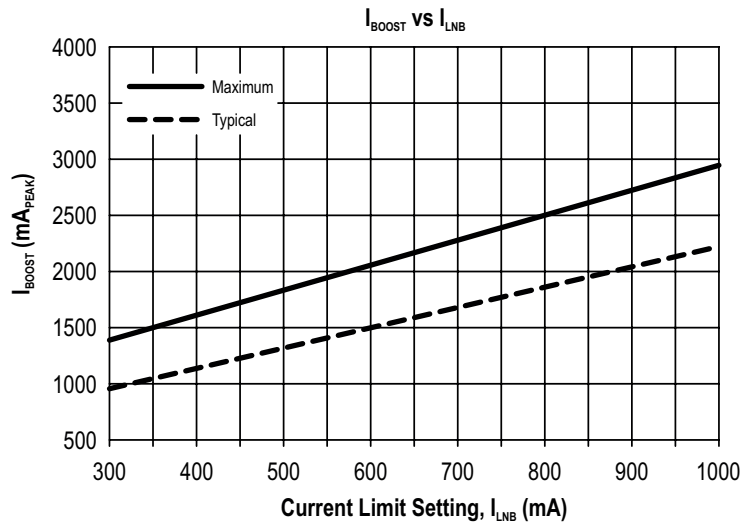


Figure 9a. Boost inductor peak current versus  $I_{LNB}$  for the A8302 (L= 10uH, Fsw bit =0)

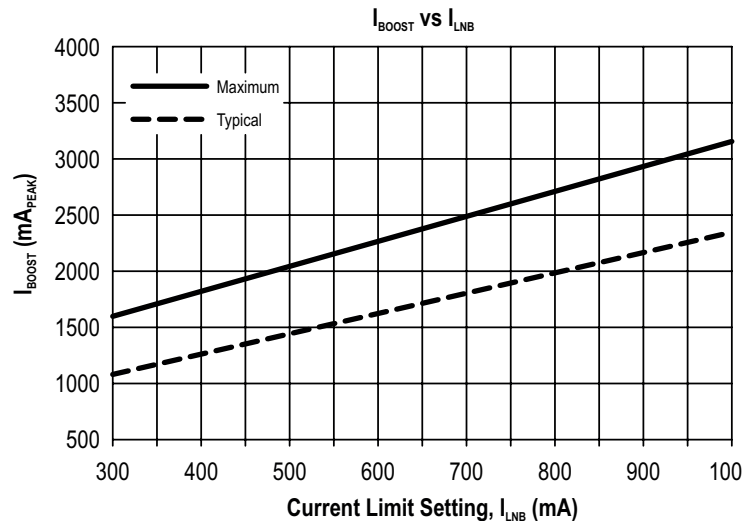


Figure 9b. Boost inductor peak current versus  $I_{LNB}$  for the A8302 (L= 4.7uH, Fsw bit =1)

Table 1a. Recommended Boost Capacitor Characteristics for Ceramic Capacitor Option

Quantity of Capacitors in Parallel	Value of Each Capacitor ( $\mu\text{F}$ )	Tolerance (%)	Rating (V)	Temperature Coefficient of Capacitance	Size
3	4.7	$\pm 10$	50	X7R	1210
2	10	$\pm 10$	35	X7R	1210

Table 1b. Recommended Boost Capacitor Characteristics for Electrolytic Capacitor Option

Quantity of Capacitors in Parallel	Value of Each Capacitor ( $\mu\text{F}$ )	Tolerance (%)	Rating (V)	Temperature Coefficient of Capacitance	Size
1	100	$\pm 25$	35	–	–

size. Physically smaller capacitors, such as the 0603 and 0805, with lower temperature ratings, such as X5R and Z5U, should be avoided.

The nominal boost capacitance should total 14.1 to 20  $\mu\text{F}$ . Allegro recommends either three 4.7  $\mu\text{F}$  or two 10  $\mu\text{F}$  capacitors, with the characteristics shown in table 1.

Figure 10 provides typical and maximum values of rms current required for a given LNR current:

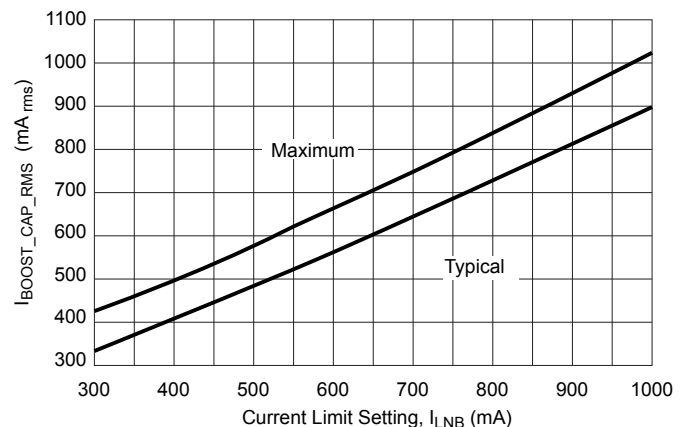
Rating	$V_{\text{IN}}$ (V)	$V_{\text{OUT}}$ (V)	L ( $\mu\text{H}$ )	$f_{\text{SW}}$ (kHz)
Typical	12	19	10	563
Maximum	9	20	7	507

Two possible ceramic based capacitor solutions have been presented. Other capacitor combinations are certainly possible, such as a very low ESR electrolytic capacitor in parallel with several microfarads of ceramic capacitance. However, there are two critical requirements that must be satisfied: 1) the zero formed by the electrolytic capacitor and its ESR should be at least 1 decade higher than the 0 dB crossover of the boost loop (typically around 25 kHz), and 2) the ceramic capacitors must eliminate the high frequency switching spikes/edges in the boost voltage, or the LNB output noise will be too high.

#### Boost Electrolytic Capacitor Option

The A8302 can be configured to operate with a low-ESR electrolytic boost capacitor of 100  $\mu\text{F}$   $\pm 25\%$ . The ESR of the boost capacitor must be less than 150 m $\Omega$  or the boost converter will be unstable. General purpose electrolytic capacitors that do not specify an ESR should be avoided. Allegro recommends an

electrolytic capacitor that is rated to support at least 35 V and has an rms current rating to support the maximum LNBx load. Figure 9 can be used to determine the necessary rms current rating of the boost capacitor given the LNBx load current.

Figure 10. Boost capacitor rms current versus  $I_{\text{LNB}}$ 

#### BOOSTx Filtering and LNBx Noise

The LNBx output noise depends on the amount of high-frequency noise at the BOOSTx pin. To minimize the high-frequency noise at the BOOSTx pin, the ceramic capacitors should be placed as close as possible to the BOOSTx pin.

#### Surge Components

Set-top-box suppliers have increased their surge specifications to require surge to failure of the TVS, or  $\pm 4000$  V, whichever

occurs first. These increased surge voltages produce significantly more current in both the external circuitry and the A8302. Allegro surge testing has shown that the SMDJ20A and LNBTVS6-221 usually fail at approximately 43 V, so all of the LNBR output components (ceramic capacitors, diodes, and so forth) should support at least 50 V.

To protect at these higher voltage/current levels three modifications must be made:

- For increased positive surge, the shunting diode from the LNBx pin to the BOOSTx pin (D3, 3 A/40 V) is no longer adequate to protect the body diode of the output stage. This diode must be increased to a 3 A/50 V device and be located so that it is in series with the BOOSTx pin as shown in application schematics 3 and 4. In this position D3 will block surge current to the majority of the boost capacitance, but the 1  $\mu$ F ceramic capacitor will still filter the high frequency switching noise.
- For increased negative surge, the relatively small clamping diode (D2) from the LNBx pin to ground is no longer adequate. This diode must be increased from a 1 A / 40 V, SOD123 device to a 3 A / 50 V, SMA.
- For a DiSEqC 1.0 application, a 0.47  $\Omega$  / 1% / 0.25 W series resistor must be added as shown in the application schematics. The 0.47  $\Omega$  rating could be reduced if there is enough equivalent resistance in any series output components such as jumpers, inductors, or PCB traces. Every application will have its own surge requirements and the surge solution can be changed. However, Allegro strongly recommends incorporating a form of surge protection to prevent any pin of the A8302 from exceeding its Absolute Maximum voltage ratings shown in this datasheet.



any time during a data transfer. If either a Start or Stop condition is encountered during a data transfer, the A8302 will respond by resetting the data transfer sequence.

#### *I<sup>2</sup>C™ Write Sequence Description*

Writing to the A8302 Control register requires transmission of a total of 27 bits: three 8-bit bytes of data plus an AK bit after each byte. The Write sequence to the A8302 Control registers is shown in figure 10a. Writing to the A8302 Control registers requires: an I<sup>2</sup>C™ Start condition, a chip address with the R/W bit set to 0, the Control register address, the control data, and an I<sup>2</sup>C™ Stop condition as follows:

- The Chip Address cycle consists of a total of nine bits: seven bits of chip address (A6 to A0) plus one R/W bit (set to 0 to indicate a Write) from the master, followed by an AK bit (set to 0 to indicate reception of a valid chip address) from the slave. The cycle begins with a Start condition. The chip address must be transmitted MSB (A6) first. The first five bits of the A8302 chip address (A6 to A2) are fixed as 00010. The remaining two bits (A1 and A0) are used to select one of four possible A8302 chip addresses. The DC voltage on the ADD pin programs the chip address. See the Electrical Characteristics table for the ADD pin voltages and the corresponding chip addresses.
- The Control Register Address cycle consists of a total of nine bits: eight bits of Control register address (RC7 to RC0) from the master followed by an AK bit (set to 0 to indicate reception of a valid register address) from the slave. The Control register address must be transmitted MSB (RC7) first. The A8302 has two Control registers, with register addresses of 0000 0000 and 0000 0001.
- The Control Data cycle consists of a total of nine bits: eight bits of control data (D7 to D0) from the master, followed by an AK bit (set to 0 to indicate reception of eight valid bits) from the slave. The control data must be transmitted MSB (D7) first. The Control registers bits are identified in the Control Registers section of this datasheet. The cycle concludes with a Stop condition.

#### *I<sup>2</sup>C™ Read Sequence Description*

Reading from the A8302 Status register requires transmission of a total of 36 bits: four 8-bit bytes of data, plus an AK bit after each byte. The Read sequence from the A8302 Status register is shown in figure 10b. Reading the A8302 Status register requires: an I<sup>2</sup>C™ Start condition, a chip address with the R/W bit set to 0, the Status register address, an I<sup>2</sup>C™ Stop condition, an I<sup>2</sup>C™ Start condition, a repeat of the chip address with the R/W bit set to 1, the status data, and an I<sup>2</sup>C™ Stop condition, as follows:

- The Chip Address cycle is identical to the Chip Address cycle previously described for the Write sequence.
- The Status Register Address cycle consists of a total of nine bits: eight bits of Status register address (RS7 to RS0) from the master, followed by an AK bit from the slave. The Status register address must be transmitted MSB (RS7) first. The A8302 has only one Status register, so the Status register address is fixed at 0000 0000. The cycle concludes with a Stop condition.
- The Repeat Chip Address cycle is identical to the Chip Address cycle previously described for the Write sequence.
- The Status Data cycle consists of a total of nine bits: eight bits of status data (RD7 to RD0) from the slave, followed by an AK bit from the master. The status data is transmitted MSB (RD7) first. The Status register bits are identified in the Status Registers section of this datasheet. The cycle concludes with a Stop condition.

#### **Interrupt Request ( $\overline{\text{IRQ}}$ ) Pin**

The A8302 provides an interrupt request pin,  $\overline{\text{IRQ}}$ , which is an open-drain, active low output. This output may be connected to a common IRQ line with a suitable external pull-up resistor and can be used with other I<sup>2</sup>C™ compatible devices to request attention from the master controller.

The  $\overline{\text{IRQ}}$  output becomes active (logic low) when the A8302 recognizes a fault condition. The fault conditions that will force  $\overline{\text{IRQ}}$  active include Early Power Failure (EPF), undervoltage lockout (UVLO), overcurrent protection (OCP), and thermal



shutdown (TSD). The UVLO, OCP (RSMODE bit set to 0), and TSD (RSMODE bit set to 0) faults are latched in the Status register and are not unlatched until the A8302 Status register is successfully transmitted to the master controller (an AK bit must be received from the master). See the description in the Status Register section and figure 12 for further details.

When the master device receives an interrupt, it should address all slaves connected to the interrupt line in sequence and read

the Status register of each to determine which device is requesting attention.

The LNBx output disable (DISx bit set to 1) and Power Not Good (PNGx bit set to 1) conditions do not cause an interrupt and are not latched in the Status register.

Figures 12, 13, 14, and 15 show the fault handling timing for UVLO in various conditions: startup and shutdown, and relative  $V_{REF}$ ,  $V_{IN}$ , and EPF conditions.

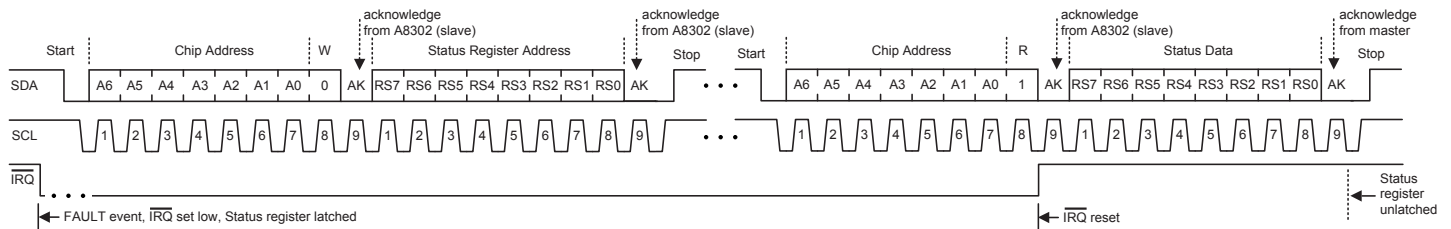


Figure 12. I<sup>2</sup>C™ Interface Read from Status register sequence. The  $\overline{IRQ}$  pin is reset to high when the A8302 acknowledges it is being read. The Status register is unlatched when the master acknowledges the status data from the A8302.

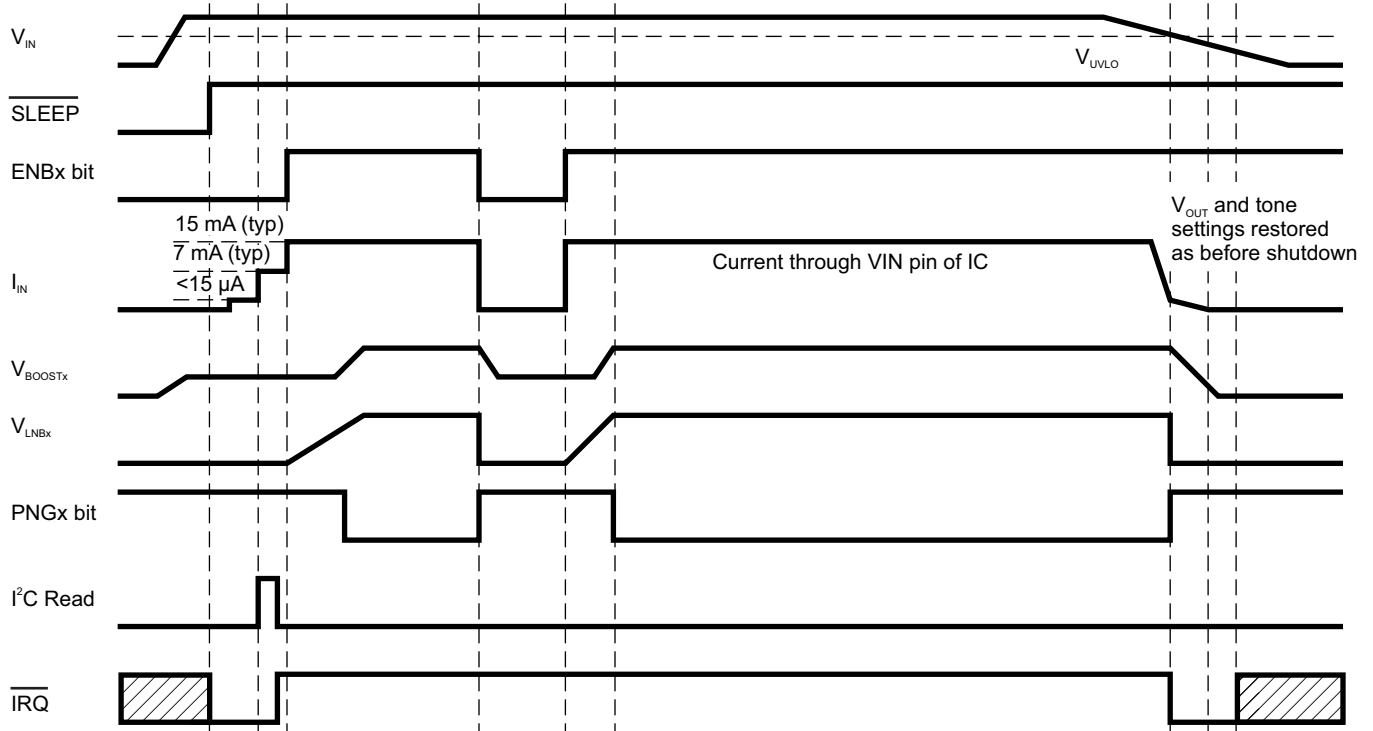


Figure 13. Startup and Shutdown Cases.  $\overline{IRQ}$  and Fault Clearing in Response to Undervoltage at VIN (UVLO). If  $\overline{IRQ}$  transitions low because of a latched fault, the LNBx output does not respond to the ENBx bit. An I<sup>2</sup>C™ Read sequence is required to clear any latched fault and reset the IRQ to logic high. An I<sup>2</sup>C™ Read is required after a UVLO fault.

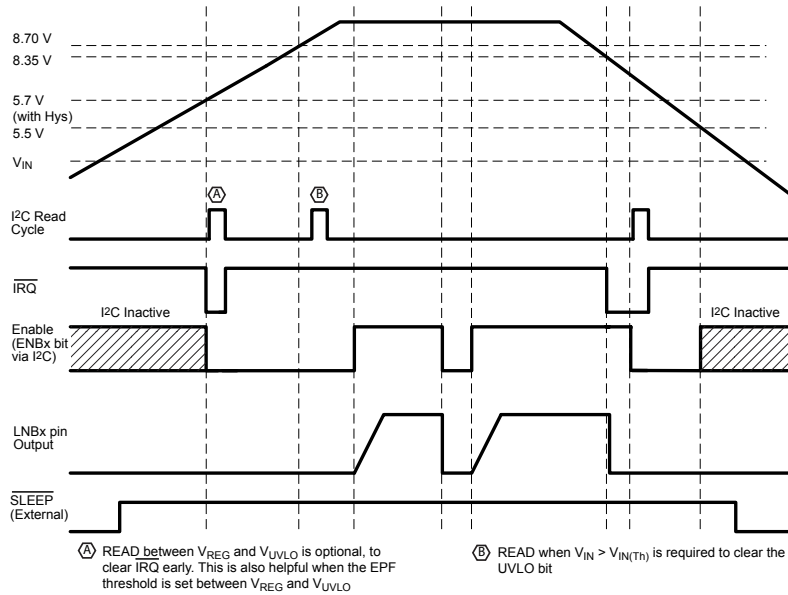


Figure 14a. I<sup>2</sup>C and  $\overline{IRQ}$  operate down to  $V_{IN} > V_{REG}$  ( $V_{REG}$  is 5.25 V typical), LNBx and BOOSTx operate from  $V_{IN(th)}$ . When  $V_{IN}$  exceeds  $V_{REG}$  (5.25 V typical),  $\overline{IRQ}$  transitions low because of the UVLO fault, and an I<sup>2</sup>C Read sequence will clear the  $\overline{IRQ}$  fault. While powering down, when  $V_{IN}$  falls below  $V_{UVLO}$ ,  $\overline{IRQ}$  becomes low, LNBx and BOOSTx turn off, and I<sup>2</sup>C becomes inactive when  $V_{IN}$  falls below  $V_{REG}$ .

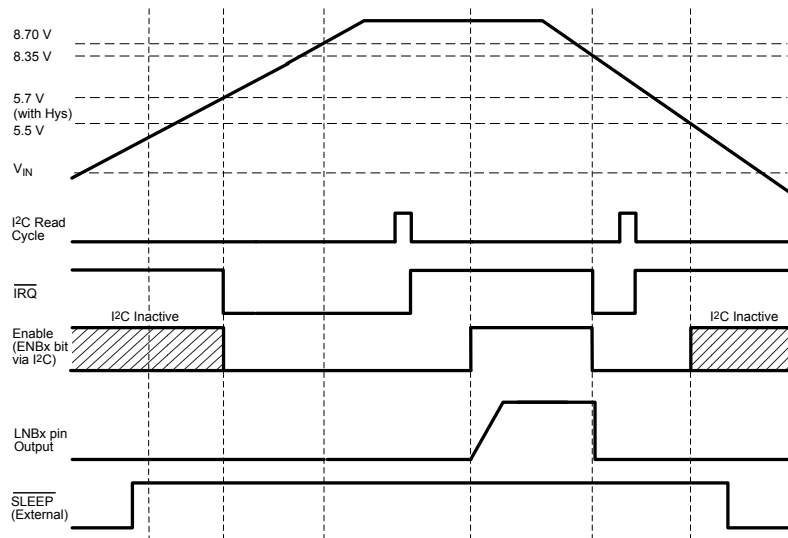


Figure 14b.  $\overline{IRQ}$  is cleared when  $V_{IN}$  is already above  $V_{IN(th)}$ . As the ENBx bit is already set high, LNBx starts rising immediately after an I<sup>2</sup>C Read sequence.