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Mobile Phone Xenon Photoflash Capacitor Charger with IGBT Driver

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: March 4, 2013

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

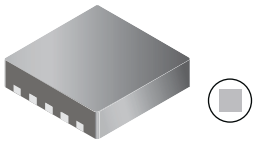
Mobile Phone Xenon Photoflash Capacitor Charger with IGBT Driver

Features and Benefits

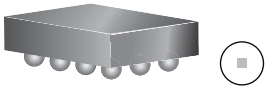
- **Low quiescent current draw (0.1 µA in shutdown mode)**
- **Primary-side output voltage sensing; no resistor divider required**
- **User-adjustable current limit from 0.4 to 1.2 A**
- **1.1 V logic (V_{HI}(min)) compatibility**
- **Integrated IGBT driver with separate sink and source (CG package) or common sink/source (EJ package)**
- **Flash dual trigger with interlock for increased noise immunity**
- Optimized for mobile phone, 1-cell Li+ battery applications
- No primary-side Schottky diode needed
- Zero-voltage switching for lower loss
- >75% efficiency
- Optional regulation feature to maintain the output voltage
- Charge complete indication
- Integrated 40 V DMOS switch

Packages:

10-contact DFN/MLP
3 mm × 3 mm
0.75 nominal overall height
(Package EJ)



12-ball WLCSP
1.205 mm × 1.635 mm
0.5 nominal overall height
(Package CG)



Description

The Allegro® A8437 Xenon photoflash charger IC is designed to meet the needs of ultra-low power, small form factor cameras, particularly camera-phones.

The charge current time is adjustable by setting the charge current limit from 0.4 to 1.2 A maximum. By using primary-side voltage sensing, the need for a secondary-side resistive voltage divider is eliminated. This has the additional benefit of reducing leakage currents on the secondary side of the transformer. To extend battery life, the A8437 features very low supply current draw—typically 0.1 µA in shutdown mode and 10 µA in standby mode.

The A8437 has a flash dual trigger IGBT driver and flash interlock to increase the device noise immunity. The IGBT driver also has separate source and sink connections, for flexibility in controlling IGBT rise and fall times. The charge and trigger voltage logic thresholds are set at 1.1 V_{HI} (min) to support applications implementing low voltage control logic.

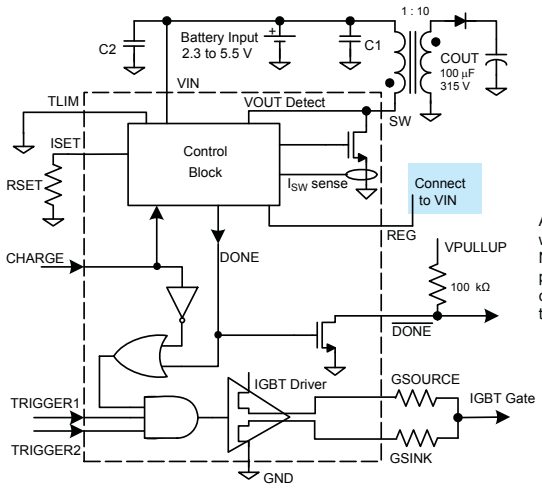
The A8437 is available in a 10-pin, 3 mm × 3 mm DFN/MLP package with exposed pad for enhanced thermal performance. For an even smaller PCB footprint, a wafer-level chip scale package (WLCSP) option is available.

Applications include:

- Mobile phone flash
- Digital and film camera flash

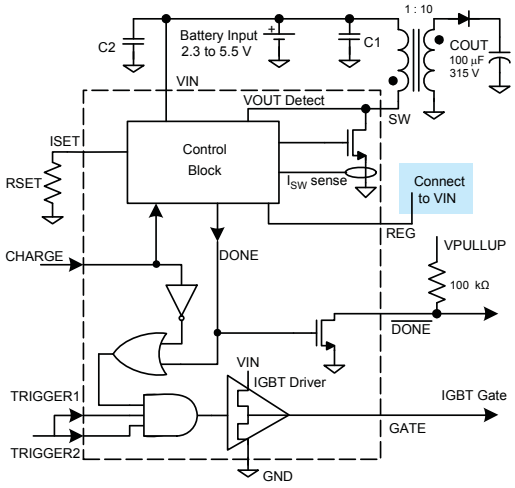
Typical Application

CG Package



Application 1. Typical application without output voltage regulation. Note: Application must periodically restart the charging cycle to recover lost charge on the output capacitor.

EJ Package



Selection Guide

Part Number	Package	Packing
A8437ECGLT*	12-ball WLCSP	Tape and reel, 4000 pieces per reel
A8437EEJTR-T	10-contact DFN/MLP	Tape and reel, 1500 pieces per reel

*Contact Allegro for additional ordering information.

Absolute Maximum Ratings

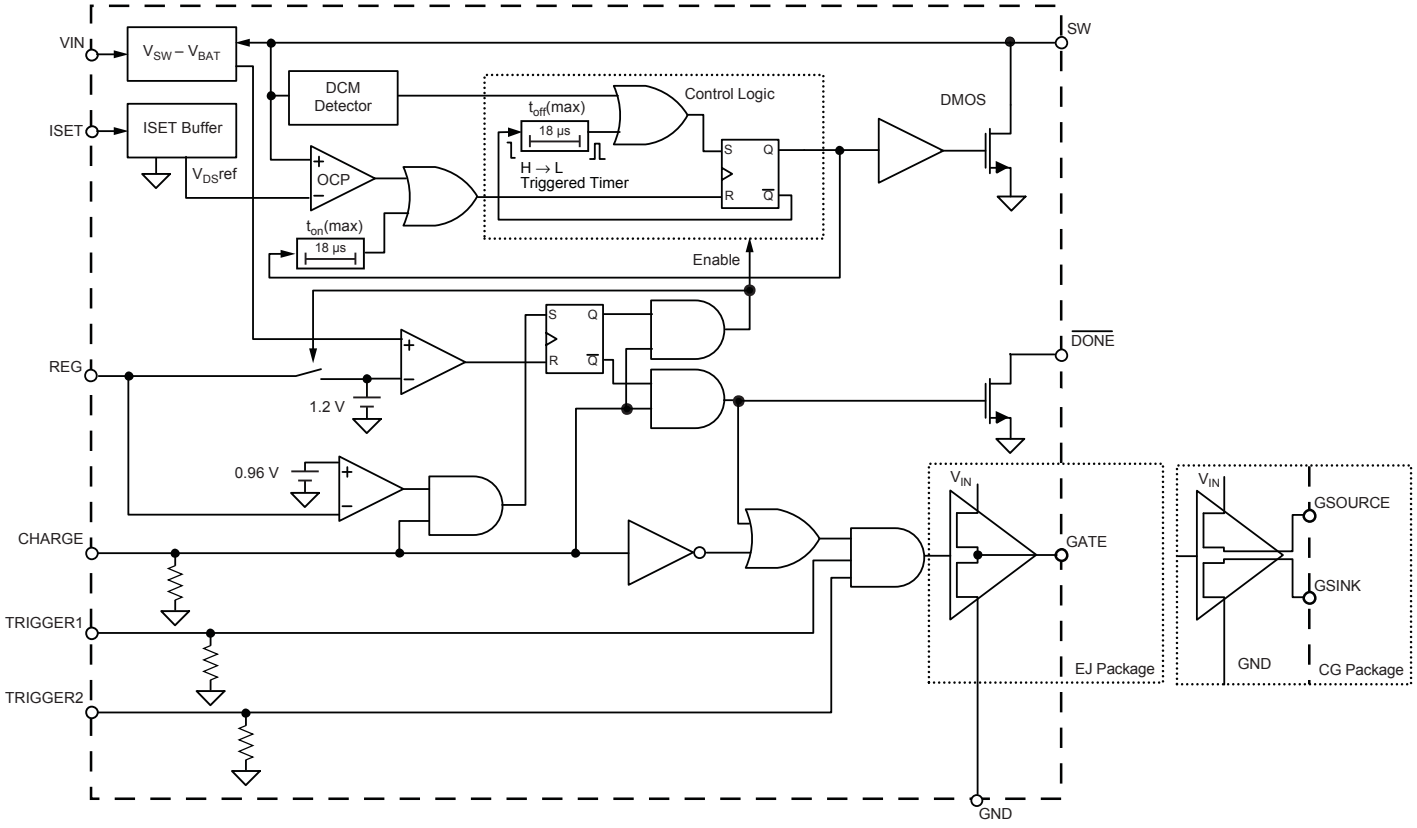
Characteristic	Symbol	Notes	Rating	Units
SW Pin	V_{SW}	DC voltage. (V_{SW} is self-clamped by internal active clamp and is allowed to exceed 40 V during flyback spike durations. Maximum repetitive energy during flyback spike: 0.5 µJ at frequency ≤ 400 kHz.)	–0.3 to 40	V
VIN Pin	V_{IN}		–0.3 to 6.0	V
CHARGE, TRIGGER*x*, $\overline{\text{DONE}}$ Pins		Care should be taken to limit the current when –0.6 V is applied to these pins.	–0.6 to V_{IN} + 0.3 V	V
Remaining Pins			–0.3 to V_{IN} + 0.3 V	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics

Characteristic	Symbol	Test Conditions[1]	Value	Units
Package Thermal Resistance[2]	$R_{\theta JA}$	CG package, on 4-layer PCB based on JEDEC standard	100	ºC/W
		EJ package, on 2-layer PCB with 0.88 in.^{2} area of 2 oz. copper each side, based on JEDEC standard	65	ºC/W
		EJ package, on 4-layer PCB based on JEDEC standard	45	ºC/W

[1]Additional thermal information available on Allegro website.
[2]CG results preliminary.

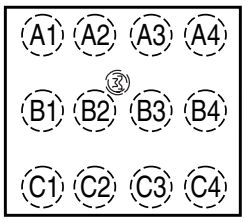
Functional Block Diagram



Pin-out Diagrams

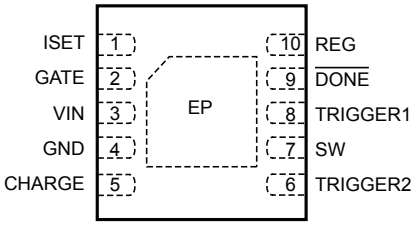
(Contacts Down Views)

CG Package



Orientation mark on ball side

EJ Package



Terminal List Table

Name	Number		Function
	CG	EJ	
ISET	C4	1	Sets the maximum switch current; connect an external resistor to GND to set the desired peak current
GATE	–	2	IGBT gate drive – sink/source
GSOURCE	B3	–	IGBT gate drive – source
GSINK	C3	–	IGBT gate drive – sink
VIN	C2	3	Input voltage; connect to a 2.3 to 5.5 V bias supply
GND	C1	4	Ground connection
CHARGE	B1	5	Pull high to initiate charging; pull low to enter low-power standby mode
TRIGGER2	B2	6	IGBT input trigger 2
SW	A1	7	Drain connection of internal power MOSFET switch; connect to transformer
TRIGGER1	A2	8	IGBT input trigger 1
$\overline{\text{DONE}}$	A3	9	Pulls low when output reaches target value and CHARGE pin is high; goes high during charging or whenever CHARGE pin is low
TLIM	A4	–	For production test only; connect to GND on PCB
REG	B4	10	Output voltage regulation pin; connect to external resistor and capacitor to regulate output voltage, or connect to VIN pin to disable regulation (see Output Regulation section for details)
EP	n.a.	–	Exposed pad for enhanced thermal dissipation; not connected electrically

ELECTRICAL CHARACTERISTICS typical values valid at V_{IN} = 3.6 V, R_{SET} = 33 kΩ, I_{SWlim} = 1.0 A, and T_A=25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VIN Voltage Range	V_{IN}		2.3	–	5.5	V
UVLO Enable Threshold	V_{INUV}	V_{IN} rising	–	2.05	2.2	V
UVLO Hysteresis	$V_{INUVhys}$		–	150	–	mV
VIN Supply Current	I_{IN}	Shutdown (CHARGE = 0 V, TRIGGER1 and TRIGGER2 = 0 V)	–	0.01	0.5	µA
		Charging complete, regulation disabled (REG = VIN)	–	10	50	µA
		Charging complete, regulation enabled	–	0.5	–	mA
		Charging (CHARGE = VIN, TRIGGER1 and TRIGGER2 = 0 V)	–	2	–	mA
Current Limits						
Switch Current Limit[1]	$I_{SWlimMAX}$	Maximum, R_{SET} = 26.7 kΩ	1.08	1.2	1.32	A
	$I_{SWlimMIN}$	Minimum, R_{SET} = 85 kΩ	–	0.4	–	A
SW / ISET Current Ratio	I_{SW}/I_{SET}	R_{SET} = 33 kΩ, CHARGE = high	–	28	–	kA/A
ISET Pin Voltage While Charging	V_{SET}	R_{SET} = 33 kΩ, CHARGE = high	–	1.2	–	V
ISET Pin Internal Resistance	$R_{SET(INT)}$		–	1000	–	Ω
Switch On-Resistance	$R_{SWDS(on)}$	V_{IN} = 3.6 V, I_D = 800 mA, T_A = 25°C	–	0.25	–	Ω
Switch Leakage Current[2]	I_{SWlk}	V_{SW} = V_{IN}(max), over temperature range	–	–	2	µA
		Combined V_{IN} and SW leakage current at T_A=25°C V_{IN}= 5.5 V in Shutdown	–	–	0.5	µA
CHARGE Input Current	I_{CHARGE}	V_{CHARGE} = V_{IN}	–	36	–	µA
CHARGE Input Voltage[2]	V_{CHARGE}	High, over input supply range	1.1	–	–	V
		Low, over input supply range	–	–	0.4	V
CHARGE Pull-Down Resistor Value	R_{CHPD}		–	100	–	kΩ
CHARGE ON/OFF Delay	t_{CH}		–	20	–	us
Maximum Switch-Off Timeout	t_{offMAX}		–	18	–	µs
Maximum Switch-On Timeout	t_{onMAX}		–	18	–	µs
$\overline{\text{DONE}}$ Output Leakage Current[2]	I_{DONElk}		–	–	1	µA
$\overline{\text{DONE}}$ Output Low Voltage[2]	V_{DONEL}	32 µA into $\overline{\text{DONE}}$ pin	–	–	100	mV
Output Comparator Trip Voltage[2]	$V_{OUTTRIP}$	Measured as $V_{SW} - V_{IN}$	31	31.5	32	V
Output Comparator Overdrive	V_{OUTOV}	Pulse width = 200 ns (90% to 90%)	–	200	400	mV
Minimum dV/dt for ZVS Comparator	dV/dt	Measured at SW pin	–	20	–	V/µs
Regulation						
REG Voltage When Charging Completes	$V_{REG(H)}$	CHARGE = high, at $\overline{\text{DONE}}$ → low transition	1.15	1.2	1.25	V
REG Voltage Threshold for Regulation	$V_{REG(L)}$	CHARGE = high, at $\overline{\text{DONE}}$ = low	–	0.96	–	V
REG Output Current Drive Capability	I_{REG}	CHARGE = high, at $\overline{\text{DONE}}$ = high, $V_{SW} - V_{IN}$ = 30 V, V_{REG} = 1.0 V	–	50	–	µA
REG Leakage Current While Not Charging	I_{REGlk}	CHARGE = high, at $\overline{\text{DONE}}$ = low, V_{REG} = 1.2 V	–	0.1	–	µA
IGBT Driver						
TRIGGER, TRIGGER2 Input Voltage[2]	$V_{TRIG(H)}$	Input = logic high, over input supply range	1.1	–	–	V
	$V_{TRIG(L)}$	Input = logic low, over input supply range	–	–	0.4	V
TRIGGER, TRIGGER2 Pull-Down Resistor	R_{TRIGPD}		–	100	–	kΩ
GSOURCE Resistance to VIN[3]	$R_{SrcDS(on)}$	V_{IN} = 3.6 V, $V_{GSOURCE}$ =1.8 V	–	5	–	Ω
GSINK Resistance to GND[3]	$R_{SnkDS(on)}$	V_{IN} = 3.6 V, V_{GSINK} = 1.8 V	–	6	–	Ω
Propagation Delay (Rising)	t_{Dr}	GSOURCE and GSINK tied together, measurement taken at pin; R_{GATE} = 12 Ω, C_L = 6500 pF, V_{IN} = 3.6 V	–	30	–	ns
Propagation Delay (Falling)	t_{Df}		–	30	–	ns
Output Rise Time	t_r		–	70	–	ns
Output Fall Time	t_f		–	70	–	ns

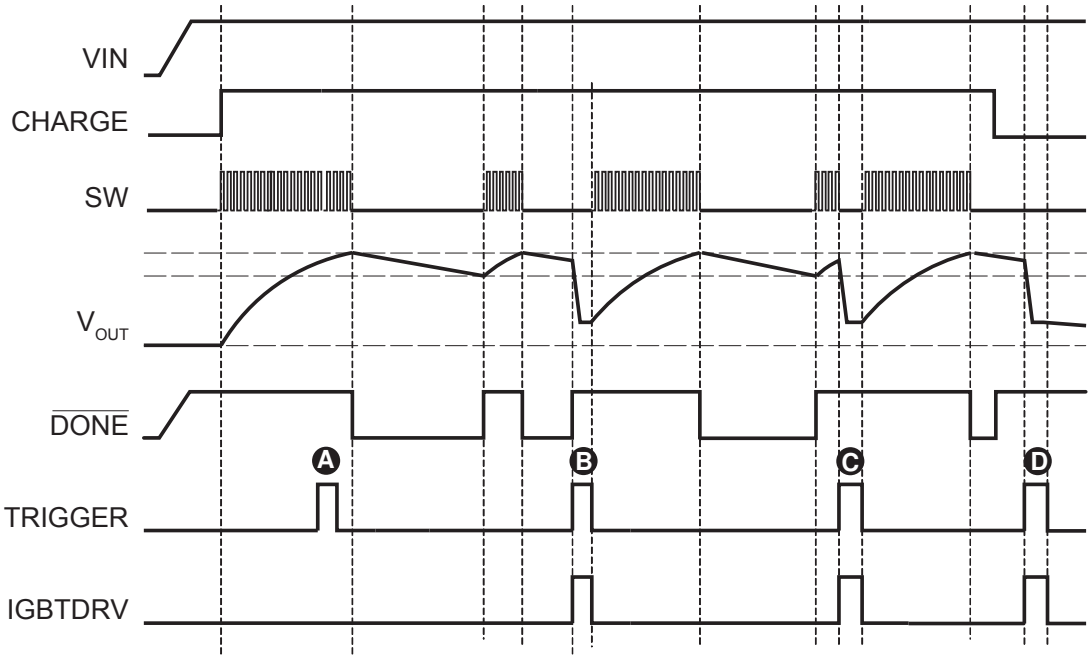
[1]Current limit guaranteed by design and correlation to static test. Refer to application section for peak current in actual circuits.

[2]Specifications over the range T_A= –40°C to 85°C; guaranteed by design and characterization.

[3]GSOURCE and GSINK tied together (GATE pin) in EJ package.

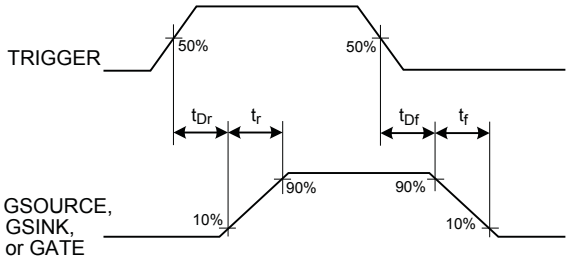
Timing and IGBT Interlock Function

The two TRIGGER signals are internally ANDed together. As shown in the timing diagram, below, triggering is prohibited during the initial charging process. This prevents premature firing of the flash before the output capacitor has been charged to its target voltage. Refer to the section IGBT Gate Driver Interlock for details.



Case	Description
A	$\overline{TRIGGER}$ pulse arrives before first charging process is finished (CHARGE and $\overline{DONE}$ pins are both high). IGBTDRV is disabled in this case.
B	Arrives during regulation mode, while not refreshing. IGBTDRV is enabled. Charging resumes once TRIGGER is low again.
C	Arrives during regulation mode, while refreshing. Charging is stopped after present cycle. IGBTDRV is enabled. Charging resumes after TRIGGER is low again.
D	Arrives while IC is in low-power Standby mode (CHARGE pin is low). IGBTDRV is always enabled in this case.

IGBT Drive Timing Definition

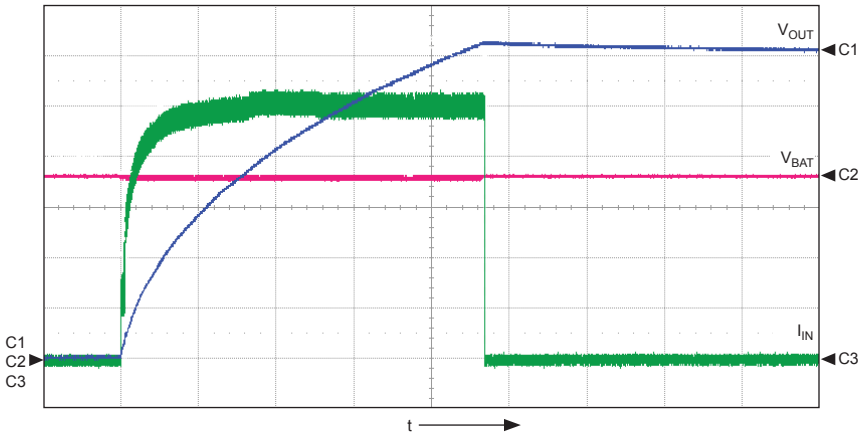


Performance Characteristics

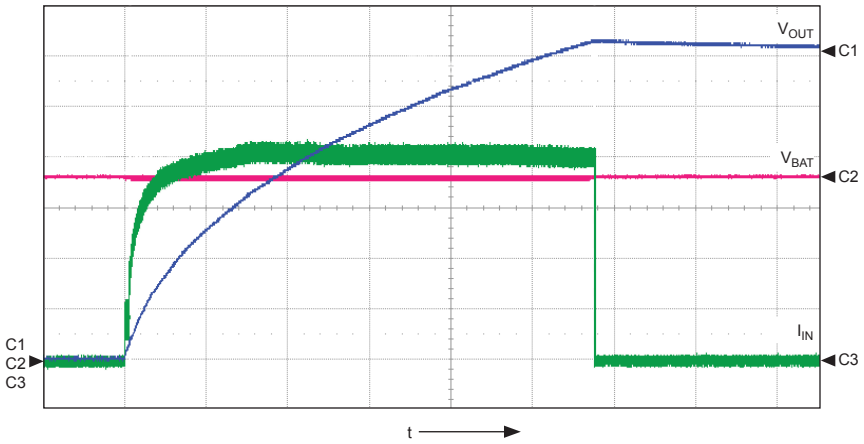
Charging Time at Various Peak Current Levels

Common Parameters		
Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	V_{BAT}	1 V
C3	I_{IN}	100 mA
t	time	200 ms
Conditions	Parameter	Value
	V_{BATT}	3.6 V
	C_{OUT}	20 µF

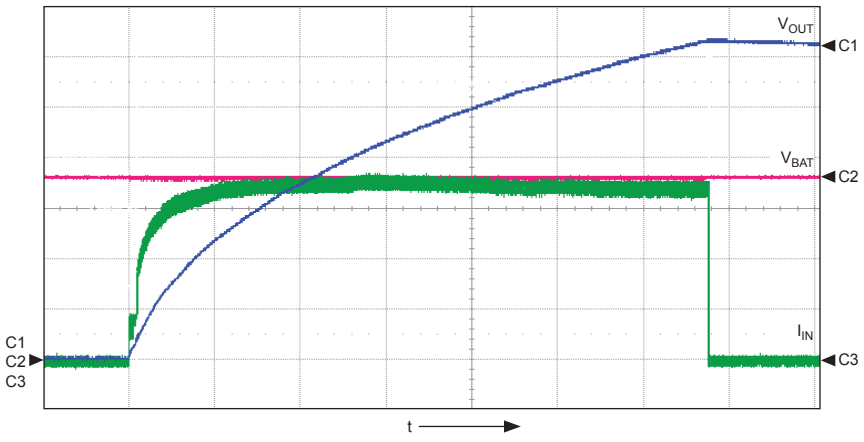
Conditions	Parameter	Value
	R_{SET}	26.7 kΩ
	I_{SWlim}	≈1.2 A

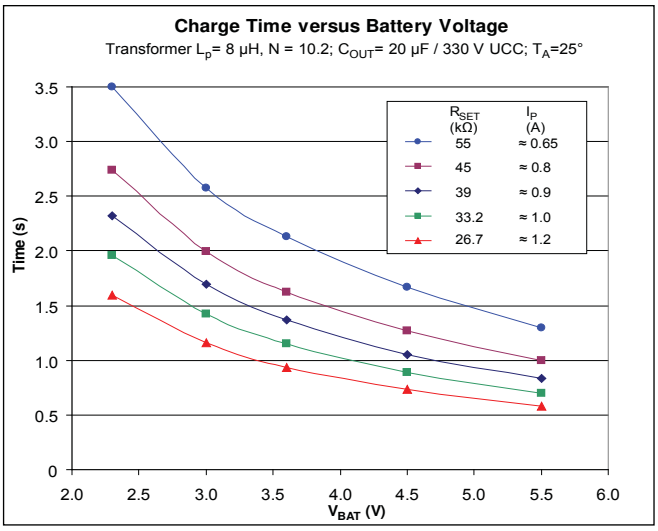


Conditions	Parameter	Value
	R_{SET}	33.2 kΩ
	I_{SWlim}	≈1.0 A

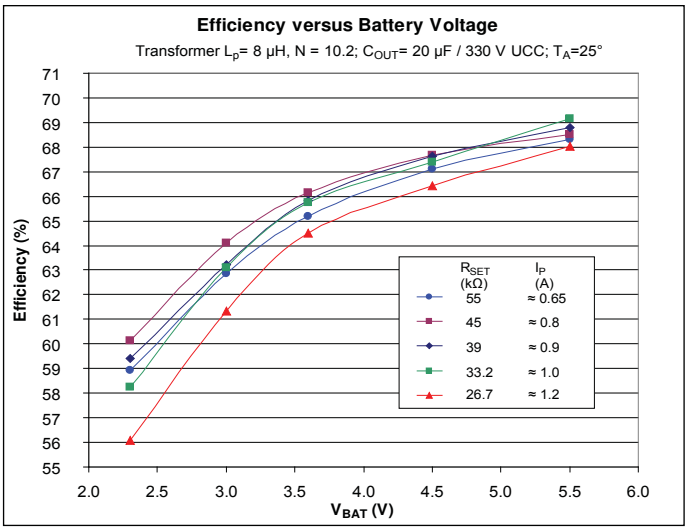


Conditions	Parameter	Value
	R_{SET}	39 kΩ
	I_{SWlim}	≈0.9 A

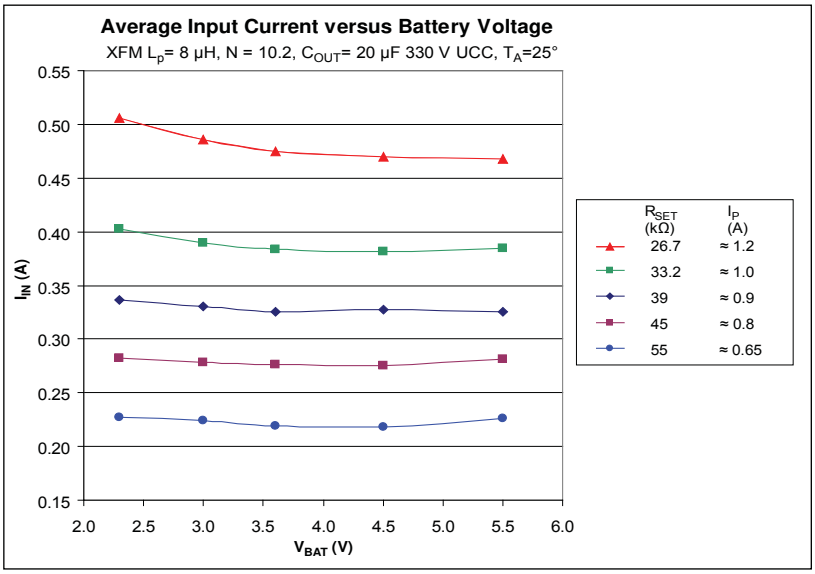




C_{OUT}= 20 µF. For larger or smaller capacitances, charging time scales proportionally.



Special low-profile transformer with relatively low inductance (Lp= 8 µH) and high winding resistance (Rp = 0.37 Ω). Higher efficiency can be achieved by using transformers with higher Lp, which reduces switching frequency and therefore switching loses, and lower resistance, which reduces conduction losses.



An increase in I_{SWlim} with respect to V_{BAT} actually keeps the average input current roughly constant throughout the battery voltage range. Normally, if I_{SWlim} is kept constant, the average current will drop as V_{BAT} goes higher.

Application Information

General Operation Overview

The CHARGE pin enables the part and starts charging. The $\overline{\text{DONE}}$ open-drain indicator is pulled low when CHARGE is high and target output voltage is reached. Charging is reinitiated when the REG pin voltage falls below the regulation threshold. Pulling the CHARGE pin low stops charging and forces the chip into low-power standby mode.

Output Voltage Regulation

When the REG pin is connected to VIN, the A8437 stops charging the output voltage after the reflected voltage ($V_{SW} - V_{IN}$) reaches 31.5 V. In this mode, charging can be reinitiated by cycling the CHARGE signal through a low to high transition.

The A8437 can also be used to regulate output voltage within a predetermined window. In this mode, connect a capacitor, CREG, and resistor, RREG, from the REG pin to GND (refer to the figure Application 3). When CHARGE is held high, the voltage monitoring circuit of the A8437 is always active, irrespective of the REG pin voltage level.

Voltage Regulation Using Predicitive Droop The A8437 uses a technique called *Predictive Droop* for regulating the output capacitor voltage after the completion of a charging cycle. When the target output voltage is reached, the converter stops charging and output capacitor voltage droops due to leakage current. An external resistor and capacitor connected from the REG pin to ground will provide an RC discharge time constant. This time constant can be selected to mirror the droop rate of the output capacitor. When voltage at the REG pin drops to 80% of the reference value, the converter starts charging again and brings the output capacitor back to target voltage again.

The time required for an RC network to discharge from V_0 to V_T is given by:

$$T = R \times C \times \ln(V_0 / V_T) . \quad (1)$$

For example, if C = 10 µF, R = 10 MΩ and V_0/V_T = 1.25, then T = 22 seconds. Assuming that the RC-discharge characteristic of the output capacitor matches that at the REG pin, we can predict that the output voltage has drooped 20%, and therefore it is time to recharge the output capacitor.

By implementing a Predictive Droop technique, no additional leakage paths are introduced on the secondary side, which helps to keep power losses to a minimum. By intentionally making the RC discharge time constant of the REG pin shorter than that of the output capacitor, we can regulate the output voltage to a window tighter than the default 20% hysteresis.

Voltage Regulation Using Direct Sensing If direct sensing from the secondary side is desired, connect the REG pin to a resistor divider network across the output capacitor to enable output regulation. In this case, the charging cut-off is still controlled by primary side sensing (charging stops when reflected voltage reaches 31.5 V), but the regulation threshold is controlled by the secondary side sensing. When the CHARGE pin is high, and the sensed output voltage falls below the lower V_{REG} threshold, the flyback converter charges the output capacitor again until the primary side sensing stops further charging. This cycle repeats till the CHARGE pin is pulled low.

The benefit of this method is that a lower output voltage can be selected independently, simply by changing the resistor divider ratio. For example, given R_1=10 MΩ, R_2= 33.2 kΩ, and $V_{REG(L)}$= 0.96 V, then:

$$V_{OUT}(\text{Low}) = V_{REG(L)} \times (R_1/R_2 + 1) = 290 \text{ V} . \quad (2)$$

Selection of Switching Current Limit

The A8437 features continuously adjustable peak switching current between 0.4 and 1.2A. This is done

by selecting the value of an external resistor RSET, connected from the ISET pin to GND, which determines the ISET bias current, and therefore the switching current limit, I_{SWlim}.

To the first order approximation, I_{SWlim} is related to I_{SET} and R_{SET} according to the following equations:

$$I_{SWlim} = I_{SET} \times K = V_{SET} / R_{SET} \times K , \quad (3)$$

where K = 28000 when battery voltage is 3.6 V.

In real applications, the actual switching current limit is affected by input battery voltage, and also the transformer primary inductance, Lp. If necessary, the following expressions can be used to determine I_{SWlim} more accurately:

$$I_{SET} = V_{SET} / (R_{SET} + R_{SET(INT)} - K \times R_{GND(INT)}), \quad (4)$$

where:

$R_{SET(INT)}$ is the internal resistance of the I_{SET} pin (1 kΩ typical),

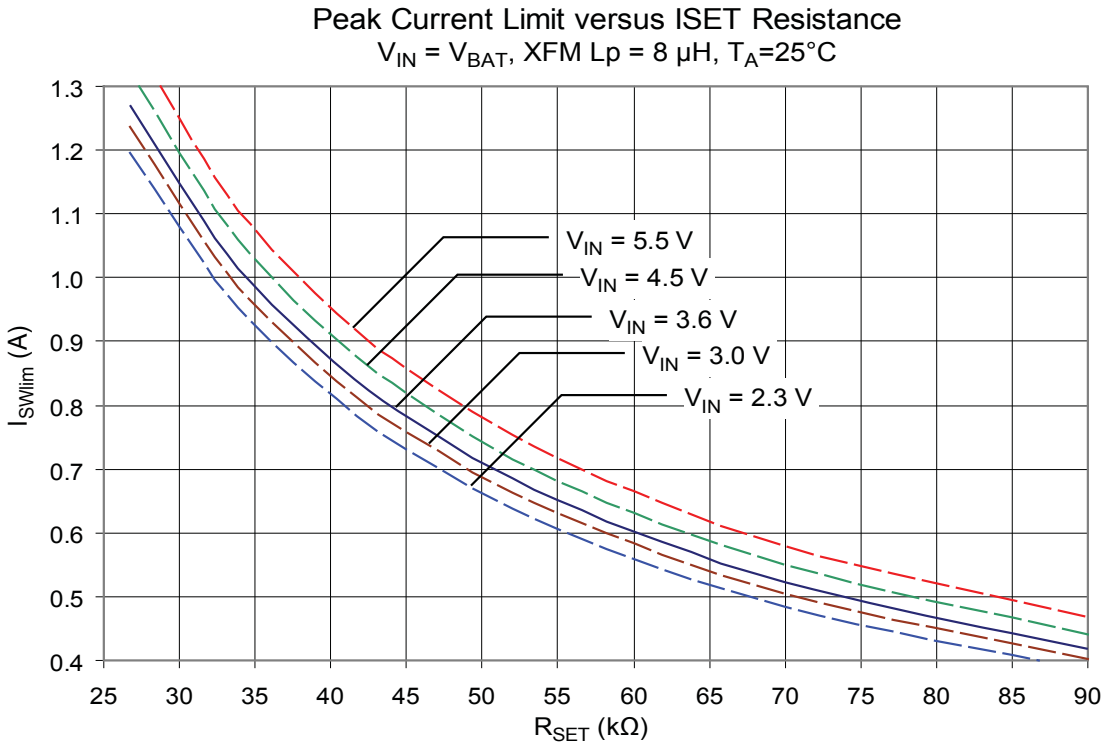
$R_{GND(INT)}$ is the internal resistance of the bonding wire for the GND pin (27 mΩ typical), and

$K = (K' + V_{IN} \times K'')$, with $K' = 24350$ and $K'' \approx 1040$ at $T_A = 25°C$. Then,

$$I_{SWlim} = I_{SET} \times K + V_{BAT} / L_P \times t_D , \quad (5)$$

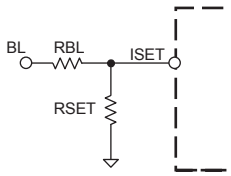
where t_D is the delay in SW turn-off (0.1 µs typical).

The chart at the bottom of the page can be used to determine the relationship between R_{SET} and I_{SWlim} at various battery voltages.



Smart Current Limit (Optional)

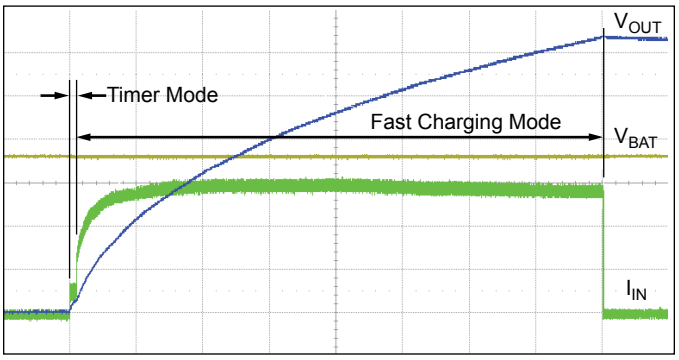
With the help of some simple external logic, the user can change the charging current according to the battery voltage. For example, assume that I_{SET} is normally 36 µA (for I_{SWlim} = 1.0 A). Referring to the following illustration, when the battery voltage drops



below 2.5 V, the signal at BL (battery-low) goes high. The resistor RBL, connecting BL to the ISET pin, then injects 10 µA into RSET. This effectively reduces ISET current to 26 µA (for I_{SWLIM} = 0.73 A). A disadvantage of the above method is that the 10 µA current is always flowing whenever the BL signal goes high.

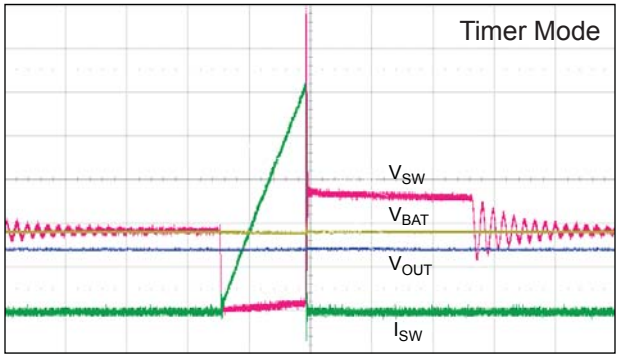
Timer Mode and Fast Charging Mode

The A8437 achieves fast charging times and high efficiency by operating in discontinuous conduction mode (DCM) through most of the charging process. The relationship of Timer Mode and Fast Charging Mode is shown in the following figure.



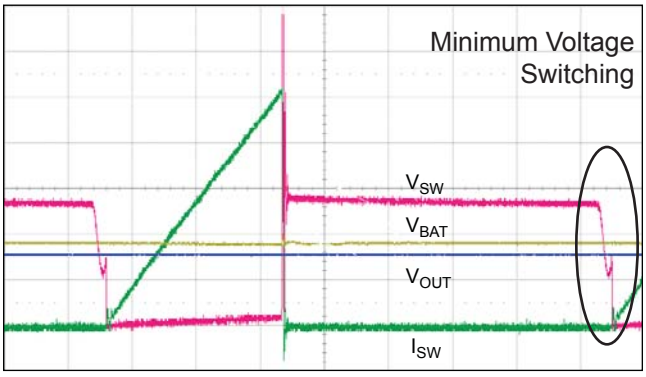
t =200 ms/div; V_{OUT} =50 V/div; V_{BAT} =1 V/div.; I_{IN} =100 mA/div. V_{BAT} =3.6 V; C_{OUT} =20 µF/330 V; R_{SET}=46 kΩ (I_{SWlim}≈0.75 A)

The IC operates in Timer Mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 15 to 20 V. Timer Mode is a fixed period, 18 µs, off-time control. One advantage of having Timer Mode is that it limits the initial battery current surge and thus acts as a "soft-start." A time-expanded view of a Timer Mode interval is shown in the following figure.



V_{OUT}≤ 14 V; t =2 µs/div; V_{BAT} =3.6 V; R_{SET}=33.2 kΩ

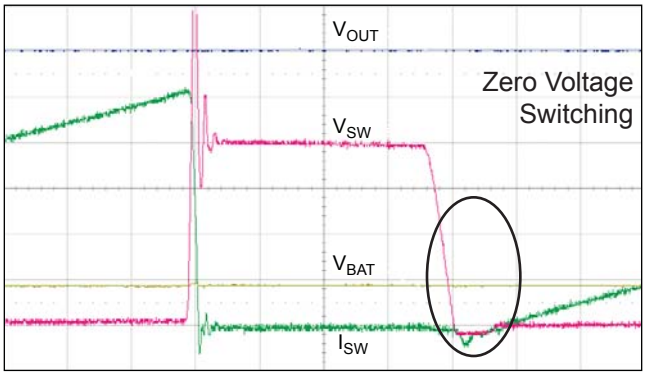
As soon as a sufficient voltage has built up at the output capacitor, the IC enters Fast-Charging Mode. In this mode, the next switching cycle starts after the secondary side current has stopped flowing, and the switch voltage has dropped to a minimum value. A proprietary circuit is used to allow minimum-voltage switching, even if the SW pin voltage does not drop to 0 V. This enables Fast-Charging Mode to start earlier than previously possible, thereby reducing the overall charging time. Minimum-voltage switching is shown in the following figure.



V_{OUT}≥ 15 V; t =1 µs/div; V_{BAT} =3.6 V; R_{SET}=33.2 kΩ

During Fast-Charging Mode, when V_{OUT} is high enough (over 50 V), true zero-voltage switching

(ZVS) is achieved. This further improves efficiency as well as reduces switching noise. A ZVS interval is shown in the following figure.



V_{OUT} = 120 V; t =0.2 µs/div; V_{BAT} =3.6 V; R_{SET}=33.2 kΩ

IGBT Gate Driver Interlock

The TRIGGER1and TRIGGER2 pins are ANDed together inside the IC to control the IGBT gate driver. If only one trigger signal is needed, tie both trigger pins together and use as a single input.

Triggering is disabled (locked) during charging. This is to prevent switching noise from interfering with the IGBT driver. After the CHARGE pin goes high (at the start of a charging cycle), the IC must wait for completion of the charging cycle ($\overline{\text{DONE}}$ goes low) before triggering can be enabled, according to the following chart:

Conditions		Resulting State
CHARGE	$\overline{\text{DONE}}$	IGBT Gate Driver
Low	Don't Care	Enabled
High	High	Disabled
High	Low	Enabled

After completion of the charging cycle, if the charge pin is kept high and REG is enabled, the IC will periodically recharge the output. If a trigger signal comes in during a recharge cycle, charging will be halted immediately and the IGBT gate driver will be allowed to fire after a delay of less than 1 µs. Charging resumes after the trigger signal is removed.

Red Eye Reduction

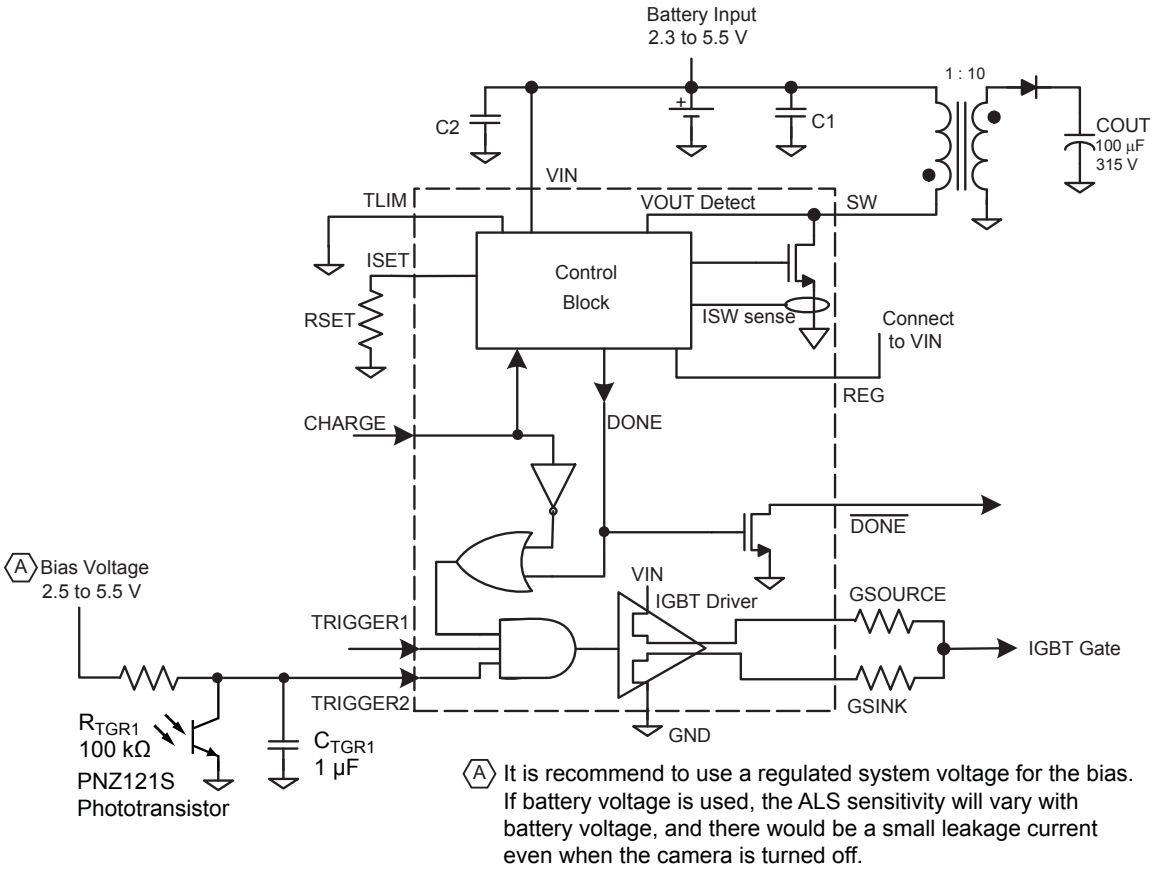
The IGBT gate driver is always enabled when CHARGE is low. If the charge pin is disabled before sufficient voltage has built up on the output capacitor, the flash may not fire. In the case of red-eye reduction flashes, it is recommended to keep the CHARGE pin low until completion of triggering pulses. This ensures that the IGBT gate driver will remain enabled regardless of the $\overline{\text{DONE}}$ state.

Ambient Light Sensing

Ambient Light Sensing (ALS) can be easily implemented for the A8437 using the TRIGGER2 pin plus three external components. This configuration is shown in the figure below.

The phototransistor current is proportional to the intensity of the light that it receives. When there is sufficient ambient light (for example, during daylight outdoor photographing), a current of about 30 µA can flow through the phototransistor. This forces the voltage at TRIGGER2 pin to fall to 0.8 V or lower, so it prohibits TRIGGER1 from firing the flash. The exact threshold of ambient light required to prohibit flash firing can be adjusted by R_{TGR1}. The smaller this resistance, the brighter the ambient light must be to prohibit flash firing.

When ambient conditions are dark, the current flowing through the phototransistor is in less than 1 µA. Because the TRIGGER2 pin is biased at 1.4 V or



ALS typical application (CG package shown)

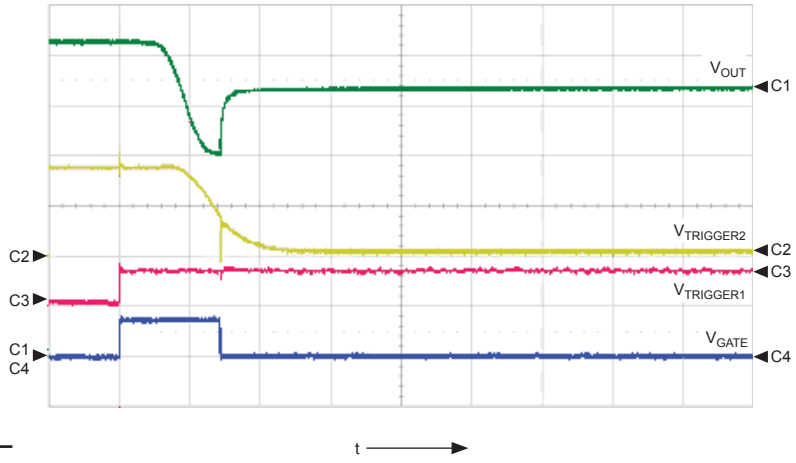
higher, TRIGGER1 is allowed to activate the IGBT gate driver (and thereby fire the flash).

The capacitor CTGR1 and resistor RTGR1 form an integrator for light exposure. When the flash fires, bright light bounces back from subject and enters the phototransistor. In example A below, the flash terminates after just 30 µs, without fully discharging the photoflash capacitor.

If the subject is far away, the reflected light intensity is lower, so the phototransistor current is also lower. In example B below, the flash stays on for longer time (60 µs) and discharges more energy from the photoflash capacitor.

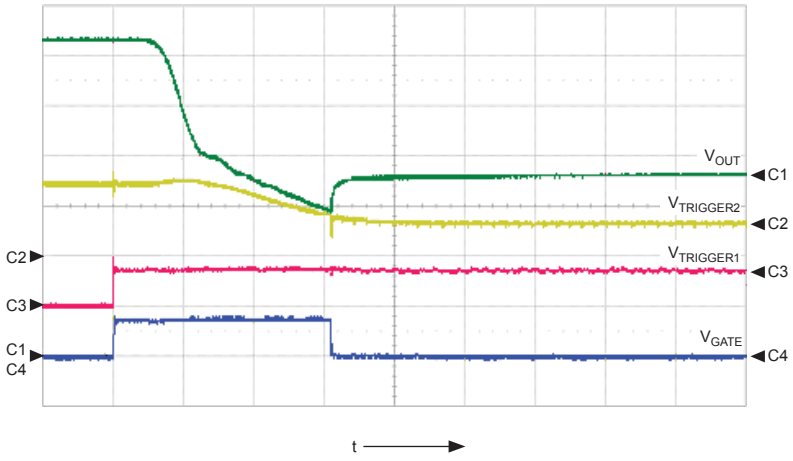
Using a larger C_{TGR1} causes the time constant of the integrator to increase, so a longer pulse is required before the flash is terminated.

Example A



Common Parameters		
Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	$V_{TRIGGER2}$	1 V
C3	$V_{TRIGGER1}$	5 V
C4	V_{GATE}	5 V
t	time	20 µs

Example B



Transformer Selection

1. The transformer turns ratio, N, determines the output voltage:

$$N = N_S / N_P$$

$$V_{OUT} = 31.5 \times N - V_d \ ,$$

where 31.5 is the typical value of $V_{OUTTRIP}$, and V_d is the forward drop of the output diode.

2. The primary inductance, L_P, determines the on-time of the switch:

$$t_{on} = (-L_P / R) \times \ln(1 - I_{SWlim} \times R / V_{IN}) \ ,$$

where R is the total resistance in the primary current path (including $R_{SWDS(on)}$ and the DC resistance of the transformer).

If V_{IN} is much larger than $I_{SWlim} \times R$, then t_{on} can be approximated by:

$$t_{on} = I_{SWlim} \times L_P / V_{IN} \ .$$

3. The secondary inductance, L_S, determines the off-time of the switch. Given:

$$L_S / L_P = N \times N \text{, then}$$

$$t_{off} = (I_{SWlim} / N) \times L_S / V_{OUT}$$

$$= (I_{SWlim} \times L_P \times N) / V_{OUT} \ .$$

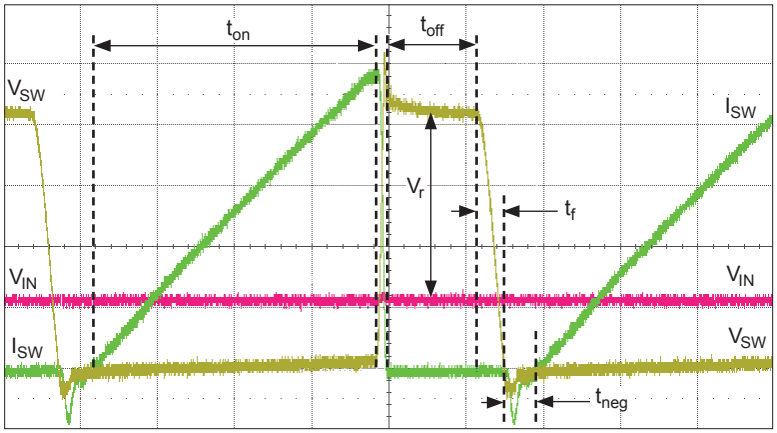
The minimum pulse width for t_{off} determines what is the minimum L_P required for the transformer. For example, if I_{SWlim} = 0.7 A, N = 10, and V_{OUT} = 315 V, then L_P must be at least 9 µH in order to keep t_{off} at 200 ns or longer. These relationships are illustrated in the figure at the bottom of the page.

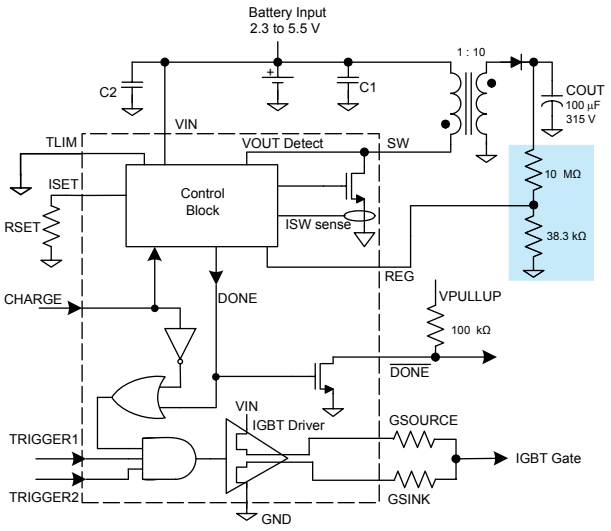
In general, choosing a transformer with a larger L_P results in higher efficiency (because a larger L_P means lower switch frequency and hence lower switching loss). But transformers with a larger L_P also require more windings and larger magnetic cores. Therefore, a trade-off must be made between transformer size and efficiency.

Component Selection

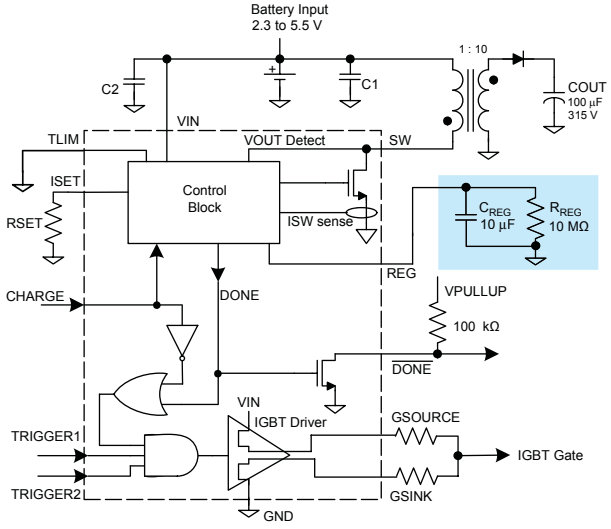
Selection of the flyback transformer should be based on the peak current, according to the following table:

I_{Peak} Range (A)	Supplier	Part Number	L_P (µH)
0.4 to 1.0	TDK	LDT565630T-002	14.5
0.6 to 1.2	TDK	LDT565630T-003	10.5
0.75 to 1.0	TDK	LDT565620ST-203	8.2



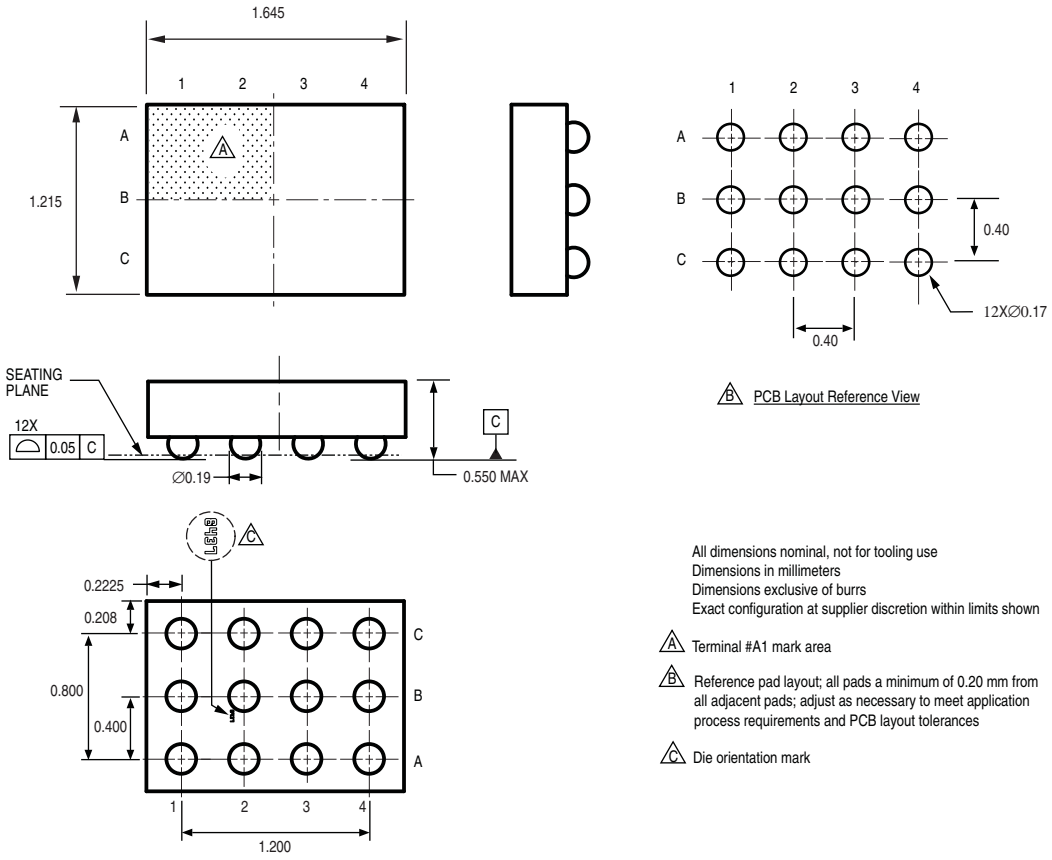


Application 2. Maintaining output target voltage by directly monitoring the output voltage (REG pin connected to a secondary-side resistor divider). CG package shown.



Application 3. Maintaining output voltage by *predicting* the output voltage droop (REG pin connected to primary-side RC network). CG package shown.

Package CG, 12-Ball WLCSP



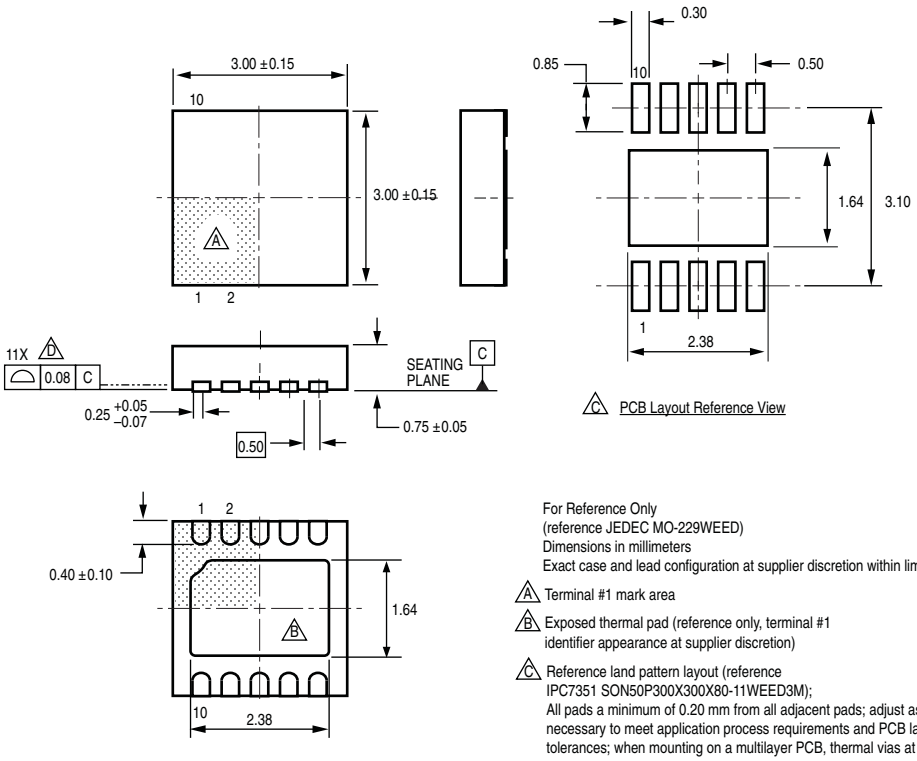
All dimensions nominal, not for tooling use
Dimensions in millimeters
Dimensions exclusive of burrs
Exact configuration at supplier discretion within limits shown

A Terminal #A1 mark area

B Reference pad layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Die orientation mark

Package EJ, 3 mm x 3 mm 10-Contact DFN/MLP



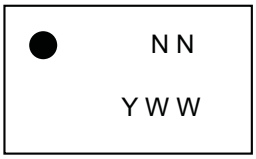
For Reference Only
(reference JEDEC MO-229WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

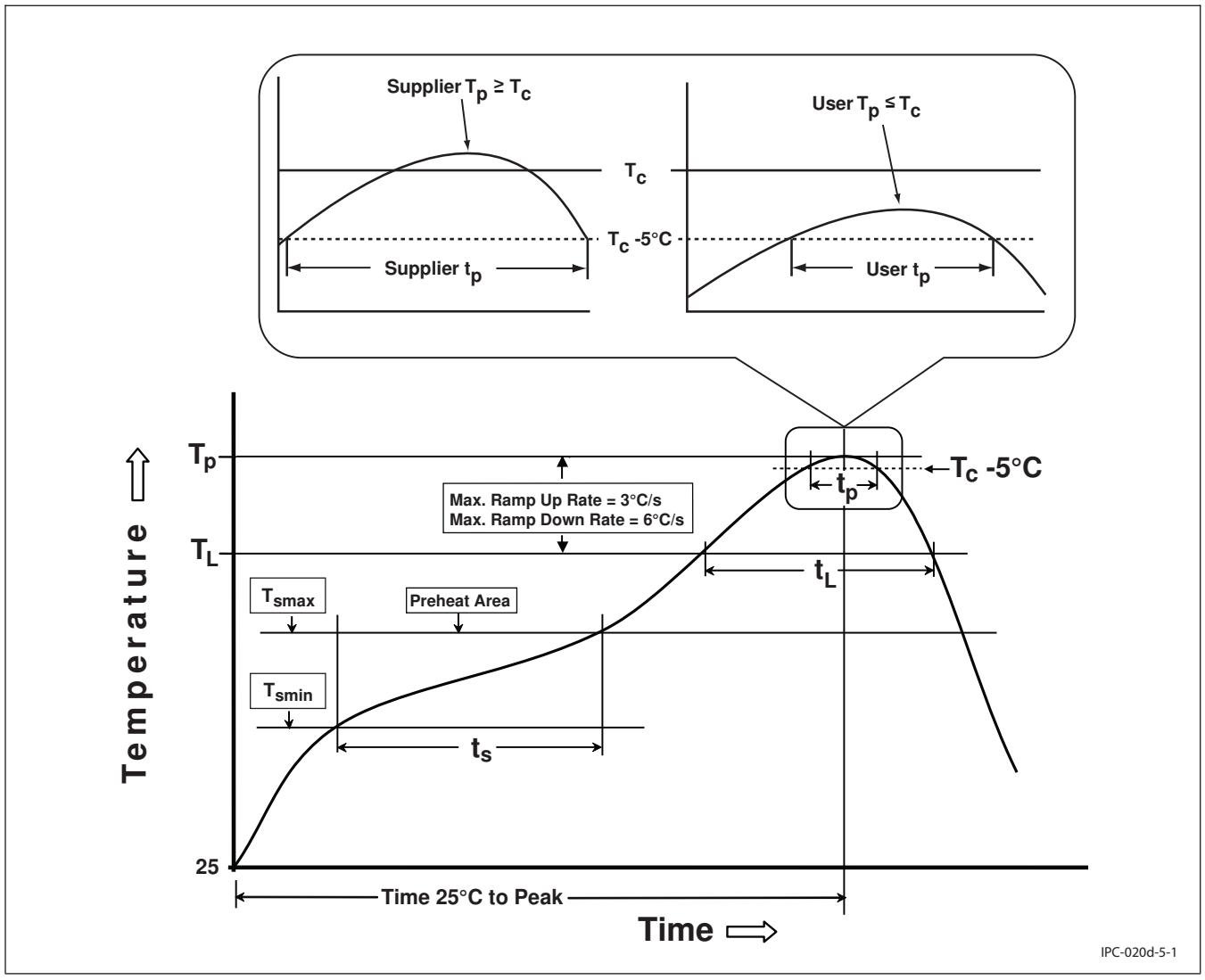
CG Package Marking



Line 1:
Bump A1 mark
NN – last two digits of the device number (37)
Line 2: Date code
Y – last digit of year of manufacture
WW – week of manufacture

(Marks on substrate side, exact appearance at supplier discretion)

Typical Reflow Profile per J-STD-020D



JSTD020D-01, Figure 5-1 Classification Profile (Not to scale)

Typical Reflow Profile per J-STD-020D

JSTD020D-01 Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-1. For suppliers T_p must equal or exceed the Classification temp in Table 4-1.	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.		

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), T_p **shall** be within ± 2 °C of the live-bug T_p and still meet the T_c requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 5-2.

For example, if T_c is 260 °C and time t_p is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.