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Ultra-Small Mobile Adjustable Xenon Photoflash Capacitor Charger with IGBT Driver

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 3, 2013

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

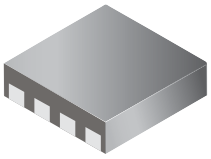
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Ultra-Small Mobile Adjustable Xenon Photoflash Capacitor Charger with IGBT Driver

Features and Benefits

- Primary-side output voltage sensing; no resistor divider required
- Adjustable switch peak current limit up to 1.5 A with single-wire programming through the CHARGE pin
- Option to fine-tune target voltage
- Ultra-small 2 × 2 DFN/MLP-8 package
- Integrated IGBT driver with internal gate resistors
- Low quiescent current draw (0.5 µA max. in shutdown mode)
- 1V logic (V_{HI}(min)) compatibility
- Zero-voltage switching for lower loss
- >75% efficiency
- Charge complete indication
- Integrated 50 V DMOS switch

Package: 8-pin DFN/MLP (suffix EE)



2 mm × 2 mm, 0.60 mm height

Not to scale

Description

The Allegro™ A8739 is a Xenon photoflash charger IC designed to provide an ultra-small solution with flexibility to adjust both charging current limit and output voltage target. By using primary-side voltage sensing, the need for a secondary-side resistive voltage divider is eliminated. This has the additional benefit of reducing leakage currents on the secondary side of the transformer. Target output voltage is primarily determined by the transformer turns ratio, but it can be further adjusted (in steps of –5 V each) using an external resistor. This enables better output accuracy, as well as greater flexibility in the selection of transformers.

To extend battery life, the A8739 features very low supply current draw (0.5 µA max in shutdown mode and 10 µA in standby mode). The switch current limit can be programmed from 0.45 to 1.5 A in 16 steps with single wire interface, through the CHARGE pin.

The IGBT driver also has internal gate resistors for minimum external component count. The charge and trigger voltage logic thresholds are set at 1 V_{HI}(min) to support applications implementing low-voltage control logic.

The A8739 is available in an 8-contact 2 mm × 2 mm DFN/MLP package with a 0.60 maximum overall package height, and an exposed pad for enhanced thermal performance. It is lead (Pb) free with 100% matte tin leadframe plating.

Typical Applications

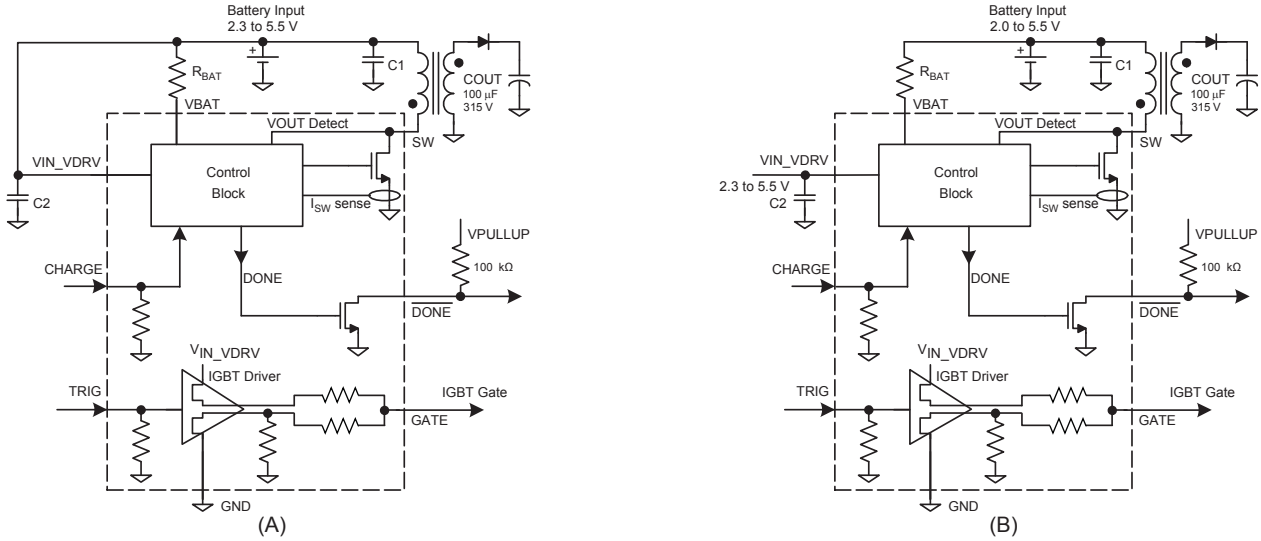


Figure 1. Typical applications: (A) with single battery supply and (B) with separate bias supply

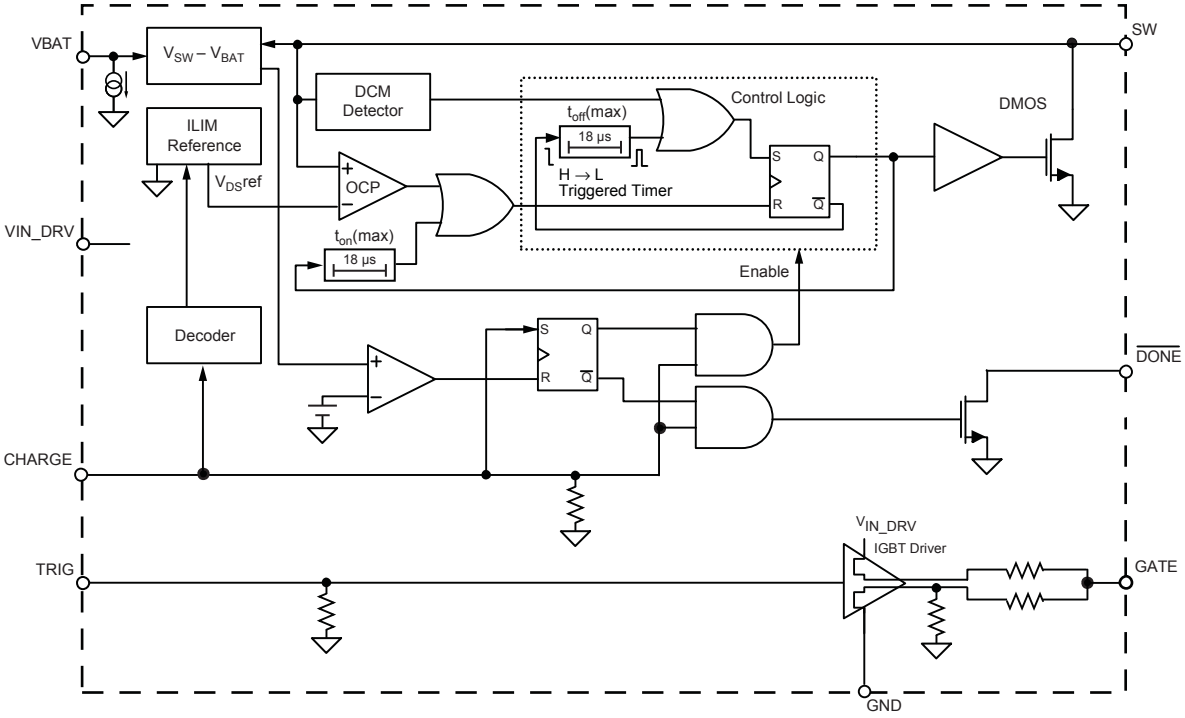
Selection Guide

Part Number	Packing	Package
A8739EEETR-T	1500 pieces per reel	8-contact DFN/MLP with exposed thermal pad

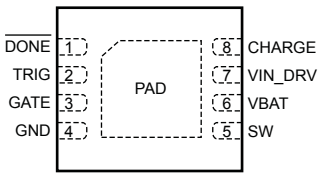
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
SW Pin	V_{SW}	DC voltage. (V_{SW} is self-clamped by internal active clamp and is allowed to exceed 50 V during flyback spike durations. Maximum repetitive energy during flyback spike: 0.5 µJ at frequency ≤ 400 kHz.)	–0.3 to 50	V
VIN_DRV, VBAT Pins	V_{IN}		–0.3 to 6.0	V
CHARGE, TRIG, $\overline{\text{DONE}}$ Pins		Care should be taken to limit the current when –0.6 V is applied to these pins.	–0.6 to V_{IN} + 0.3 V	V
Remaining Pins			–0.3 to V_{IN} + 0.3 V	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Functional Block Diagram



Pin-out Diagram



(Top View)

Terminal List

Number	Name	Function
1	$\overline{\text{DONE}}$	Open collector output, pulls low when output reaches target value and CHARGE is high. Goes high during charging or whenever CHARGE is low.
2	TRIG	IGBT trigger input.
3	GATE	IGBT gate drive output.
4	GND	Ground connection.
5	SW	Drain connection of internal DMOS switch. Connect to transformer primary winding.
6	VBAT	Connect to battery voltage; directly to select the default output voltage, or through a series resistor to select a lower output voltage step.
7	VIN_DRV	Input voltage. Connect to 3 to 5.5 V bias supply. Decouple V_{IN} voltage with 0.1 µF ceramic capacitor placed close to this pin.
8	CHARGE	Charge enable and current limit serial programming pin. Set this pin low to shut down the chip.
–	PAD	Exposed pad for enhanced thermal dissipation. Connect to ground plane.

ELECTRICAL CHARACTERISTICS Typical values are valid at V_{IN} = V_{BAT} = 3.6 V; T_A = 25°C, except ● indicates specifications guaranteed from −40°C to 85°C ambient, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
VBAT Voltage Range	V_{BAT}		●	2.0	–	5.5	V
VIN_DRV Voltage Range	V_{IN}		●	2.3	–	5.5	V
UVLO Enable Threshold	V_{INUV}	V_{IN} rising		–	2.05	2.2	V
UVLO Hysteresis	$V_{INUV(hys)}$			–	150	–	mV
V_{IN} Supply Current	I_{IN}	Shutdown (CHARGE = 0 V, TRIG = 0 V)		–	0.02	0.5	µA
		Charging complete		–	50	100	µA
		Charging (CHARGE = V_{IN}, TRIG = 0 V)		–	2	–	mA
VBAT Pin Supply Current	I_{BAT}	Shutdown (CHARGE = 0 V, TRIG = 0 V)		–	0.01	1	µA
		Charging done (CHARGE = V_{IN}, $\overline{DONE}$ = 0 V)		–	–	5	µA
		Charging (CHARGE = V_{IN}, TRIG = 0 V)		–	50	–	µA
Current Limit							
Primary-Side Current Limit[1]	I_{SWLIM}	100% setting		1.35	1.50	1.65	A
Switch Current Limit (ILIM Programming Input on CHARGE Pin)	I_{SWLIM1}	Default setting		–	100	–	%
	I_{SWLIM2}	One pulse applied to CHARGE pin		–	95	–	%
	I_{SWLIM3}	Two pulses applied to CHARGE pin		–	90	–	%
	I_{SWLIM4}	Three pulses applied to CHARGE pin		–	86	–	%
	I_{SWLIM5}	Four pulses applied to CHARGE pin		–	81	–	%
	I_{SWLIM6}	Five pulses applied to CHARGE pin		–	76	–	%
	I_{SWLIM7}	Six pulses applied to CHARGE pin		–	71	–	%
	I_{SWLIM8}	Seven pulses applied to CHARGE pin		–	67	–	%
	I_{SWLIM9}	Eight pulses applied to CHARGE pin		–	62	–	%
	$I_{SWLIM10}$	Nine pulses applied to CHARGE pin		–	57	–	%
	$I_{SWLIM11}$	Ten pulses applied to CHARGE pin		–	52	–	%
	$I_{SWLIM12}$	Eleven pulses applied to CHARGE pin		–	48	–	%
	$I_{SWLIM13}$	Twelve pulses applied to CHARGE pin		–	43	–	%
	$I_{SWLIM14}$	Thirteen pulses applied to CHARGE pin		–	38	–	%
	$I_{SWLIM15}$	Fourteen pulses applied to CHARGE pin		–	33	–	%
	$I_{SWLIM16}$	Fifteen pulses applied to CHARGE pin		–	29	–	%
Switch On-Resistance	$R_{SWDS(on)}$	V_{IN_DRV} = 3.6 V, I_D = 800 mA, T_A = 25°C		–	0.4	–	Ω
Switch Leakage Current[2]	I_{SWLK}	V_{SW} = 5.5, over full temperature range		–	–	2	µA
CHARGE Pull-down Resistance	R_{CHGPD}			–	100	–	kΩ
CHARGE Input Voltage[2]	V_{CHARGE}	High, over input supply range	●	1.0	–	–	V
		Low, over input supply range	●	–	–	0.4	V

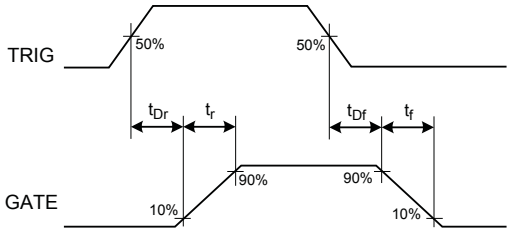
Continued on the next page…

ELECTRICAL CHARACTERISTICS (Continued) Typical values are valid at $V_{IN} = V_{BAT} = 3.6$ V; $T_A = 25°C$, except ● indicates specifications guaranteed from −40°C to 85°C ambient, unless otherwise noted

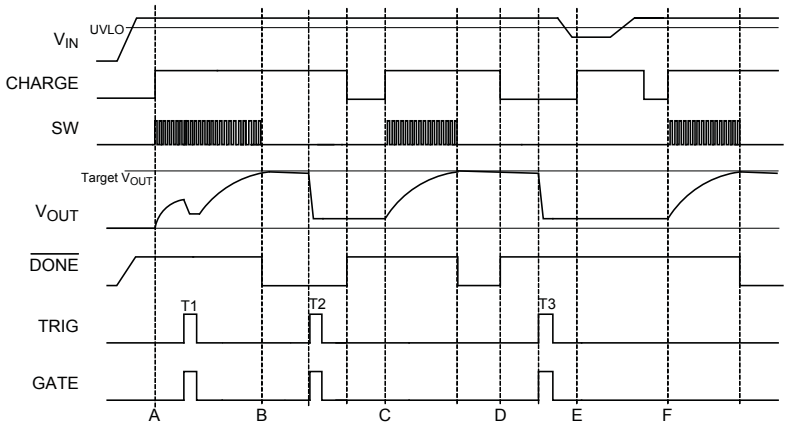
Charge Pin Programming							
ILIM Programming High at CHARGE pin 2	$t_{ILIM(H)init}$	Initial Pulse		15	–	–	µs
	$t_{ILIM(H)}$	Subsequent Pulses		0.2	–	–	µs
ILIM Programming Low at CHARGE pin 2	$t_{ILIM(L)}$			0.2	–	–	µs
Total ILIM Setup Time at CHARGE pin 2	$t_{ILIM(SU)}$			–	200	–	µs
Switch-Off Timeout	$t_{off(max)}$			–	18	–	µs
Switch-On Timeout	$t_{on(max)}$			–	18	–	µs
Output Comparator Trip Voltage	$V_{OUTTRIP1}$	Measured as $V_{SW} – V_{BAT}$ (R_{BAT} = 0 Ω)	●	31	31.5	32	V
	$V_{OUTTRIP2}$	Measured as $V_{SW} – V_{BAT}$ (R_{BAT} = 845 Ω)	●	–	31.0	–	V
	$V_{OUTTRIP3}$	Measured as $V_{SW} – V_{BAT}$ (R_{BAT} = 2.32 kΩ)	●	–	30.5	–	V
	$V_{OUTTRIP4}$	Measured as $V_{SW} – V_{BAT}$ (R_{BAT} = 4.87 kΩ)	●	–	30.0	–	V
	$V_{OUTTRIP5}$	Measured as $V_{SW} – V_{BAT}$ (R_{BAT} = 9.09 kΩ)	●	–	29.5	–	V
$\overline{DONE}$ Leakage Current[2]	I_{DONELK}		●	–	–	1	µA
Output Low Voltage[2]	V_{DONEL}	32 µA into $\overline{DONE}$ pin	●	–	–	100	mV
Output Voltage Overdrive	V_{OUTOV}	Pulse width = 200 ns (90% to 90%)		–	200	400	mV
dV/dt Threshold for ZVS Comparator	dV/dt	Measured at SW pin		–	20	–	V/µs
IGBT Driver							
TRIG Input Voltage[2]	$V_{TRIG(H)}$	Input = logic high, over input supply range	●	1	–	–	V
	$V_{TRIG(L)}$	Input = logic low, over input supply range	●	–	–	0.4	V
TRIG Pull-Down Resistor	R_{TRIGPD}			–	100	–	kΩ
GATE Resistance to VIN_DRV	$R_{SrcDS(on)}$	V_{GATE} = 1.8 V		–	21	–	Ω
GATE Resistance to GND	$R_{SnkDS(on)}$	V_{GATE} = 1.8 V		–	27	–	Ω
Propagation Delay (Rising)[3]	t_{Dr}	Measurement taken at GATE pin, C_L = 6500 pF		–	25	–	ns
Propagation Delay (Falling)[3]	t_{Df}			–	60	–	ns
Output Rise Time[3]	t_r			–	290	–	ns
Output Fall Time[3]	t_f			–	380	–	ns
GATE Pull-Down Resistor	R_{GTPD}			–	20	–	kΩ

[1]Current limit guaranteed by design and correlation to static test.
[2]Specifications throughout the range T_A = –40°C to 85°C guaranteed by design and characterization.
[3]See IGBT Drive Timing Definition diagram for further information.

IGBT Drive Timing Definition



Operation Timing Diagram



Explanation of Events

A: Start charging by pulling CHARGE to high, provided that V_{IN} is above UVLO level.

B: Charging stops when V_{OUT} reaches the target voltage

C: Start a new charging process with a low-to-high transition at the CHARGE pin.

D: Pull CHARGE to low to put the controller in low-power standby mode.

E: Charging does not start, because V_{IN} is below UVLO level when CHARGE goes high.

F: After V_{IN} goes above UVLO, another low-to-high transition at the CHARGE pin is required to start the charging.

T1, T2, T3 (Trigger instances): IGBT driver output pulled high whenever the TRIG pin is at logic high. It is recommended to avoid applying any trigger pulses during charging.

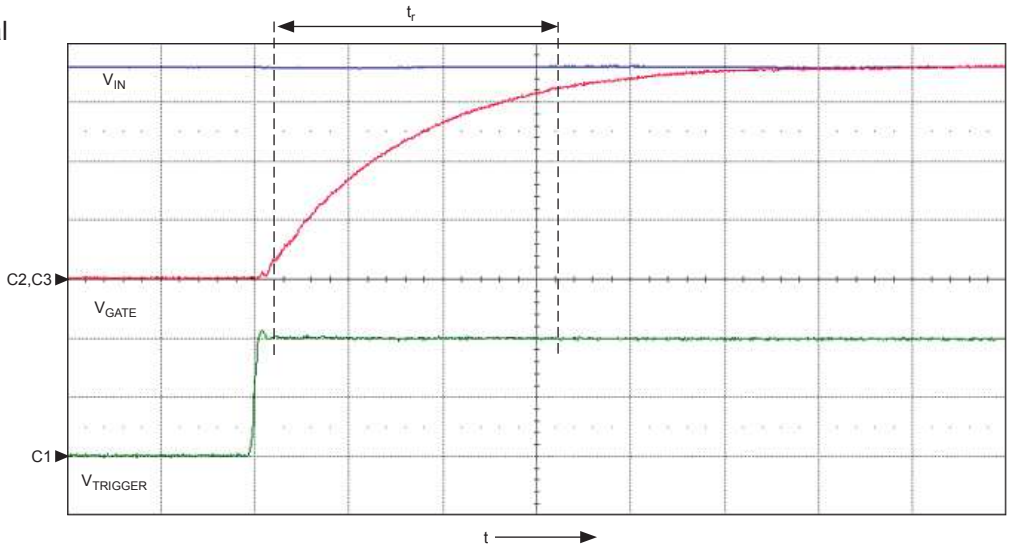
Characteristic Performance

IGBT Drive Performance

IGBT drive waveforms are measured at pin, with capacitive load of 6800 pF

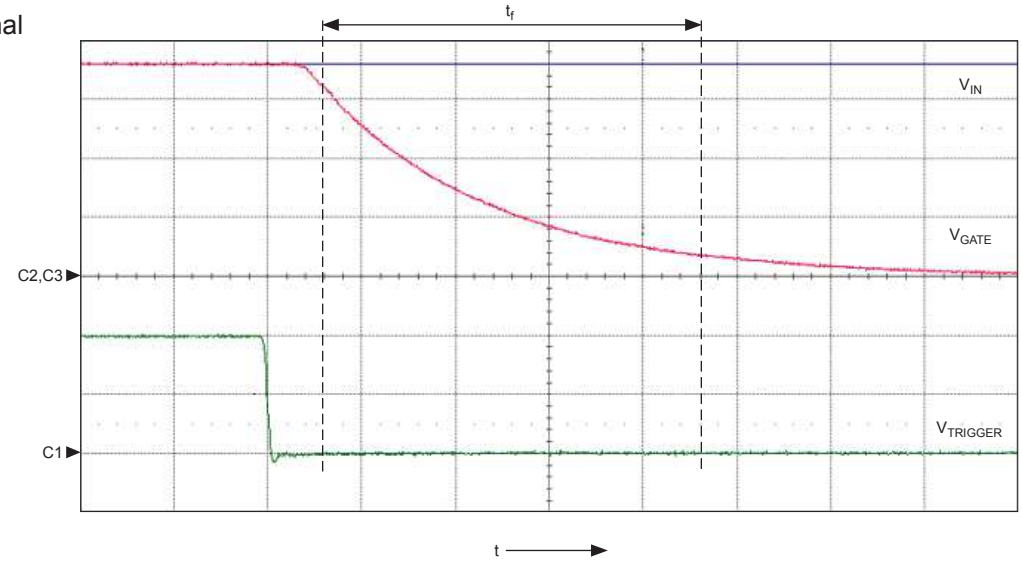
Rising Signal

Symbol	Parameter	Units/Division
C1	$V_{TRIGGER}$	1 V
C2	V_{GATE}	1 V
C3	V_{IN}	1 V
t	time	100 ns
Conditions	**Parameter**	**Value**
	t_{Dr}	23 ns
	t_r	320 ns
	C_{LOAD}	6.8 nF



Falling Signal

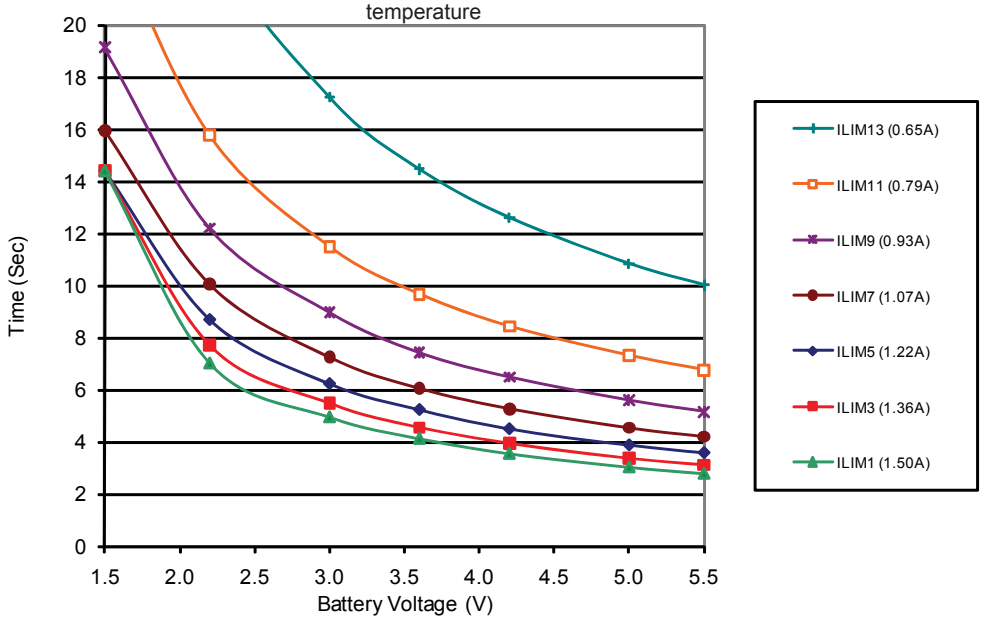
Symbol	Parameter	Units/Division
C1	$V_{TRIGGER}$	1 V
C2	V_{GATE}	1 V
C3	V_{IN}	1 V
t	time	100 ns
Conditions	**Parameter**	**Value**
	t_{Dr}	58 ns
	t_r	402 ns
	C_{LOAD}	6.8 nF



Characteristic Performance

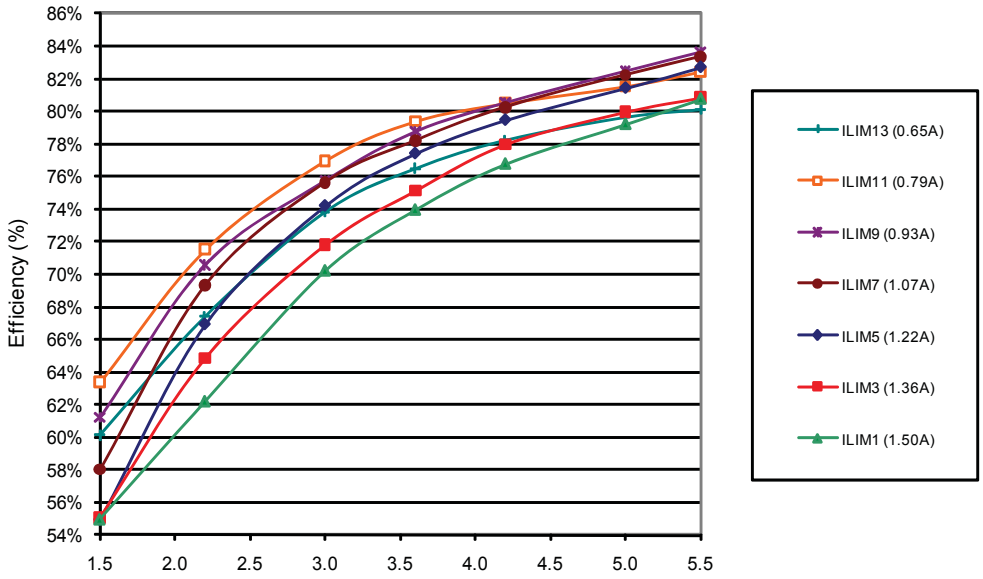
Charge Time versus Battery Voltage at Various ILIM

R_{BAT} = 0 Ω, Transformer $L_{PRIMARY}$ = 12.8 µH, N =10.25, V_{IN} =3.6 V, C_{OUT} = 100 µF / 330 V UCC, at room temperature



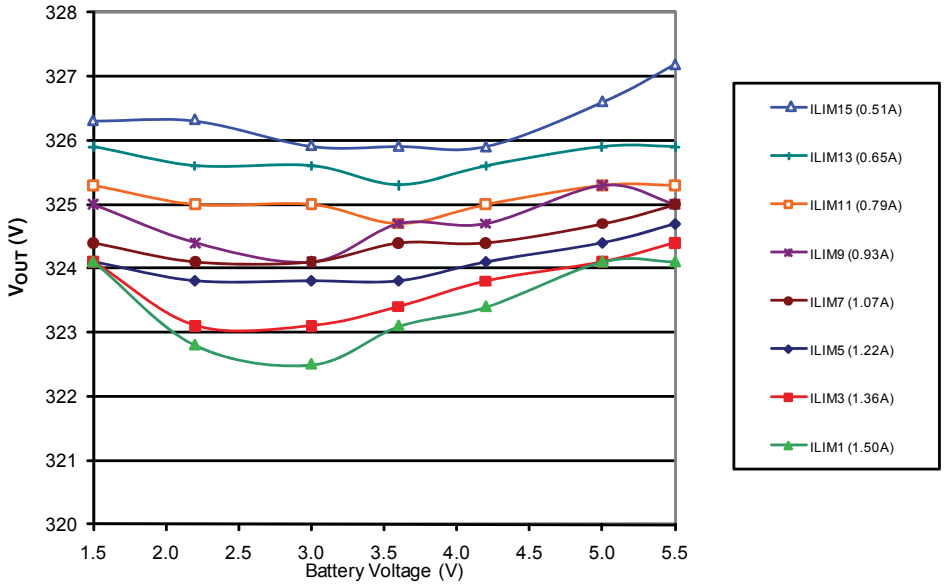
Efficiency versus Battery Voltage at Various ILIM

R_{BAT} = 0 Ω, Transformer $L_{PRIMARY}$ = 12.8 µH, N =10.25, V_{IN} =3.6 V, at room temperature



Final Output Voltage versus Battery Voltage at Various ILIM

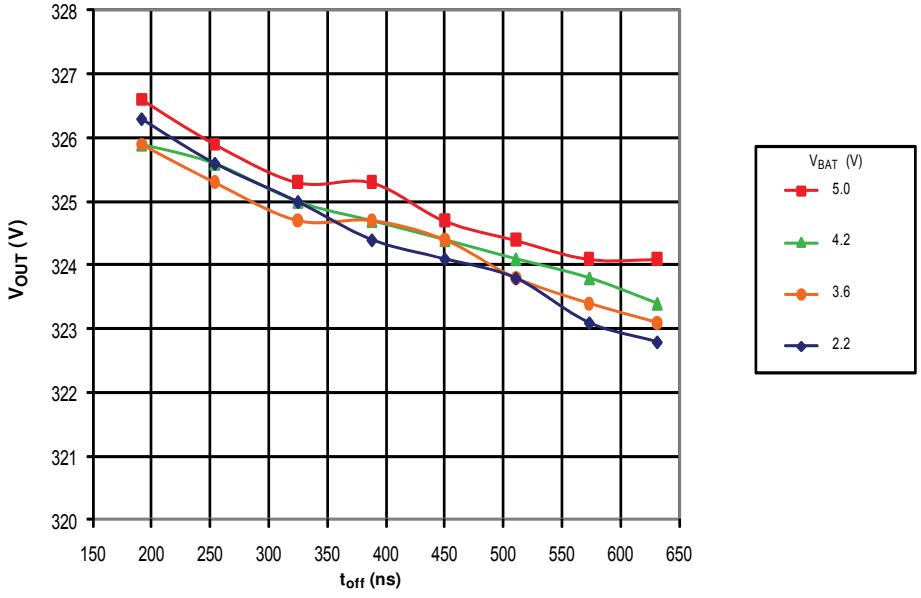
R_{BAT} = 0 Ω, Transformer $L_{PRIMARY}$ = 12.8 µH, N =10.25, V_{IN} =3.6 V, at room temperature



Note: Output voltage is sensed from the primary side winding when the switch turns off. This duration, t_{off} , has to be long enough (>200 ns) in order to obtain an accurate measurement. The value of t_{off} depends on I_{SWlim}, primary inductance, $L_{Primary}$, and the turns ratio, N, as given by: $t_{off} = (I_{SWlim} \times L_{PRIMARY} \times N) / V_{OUT}$.

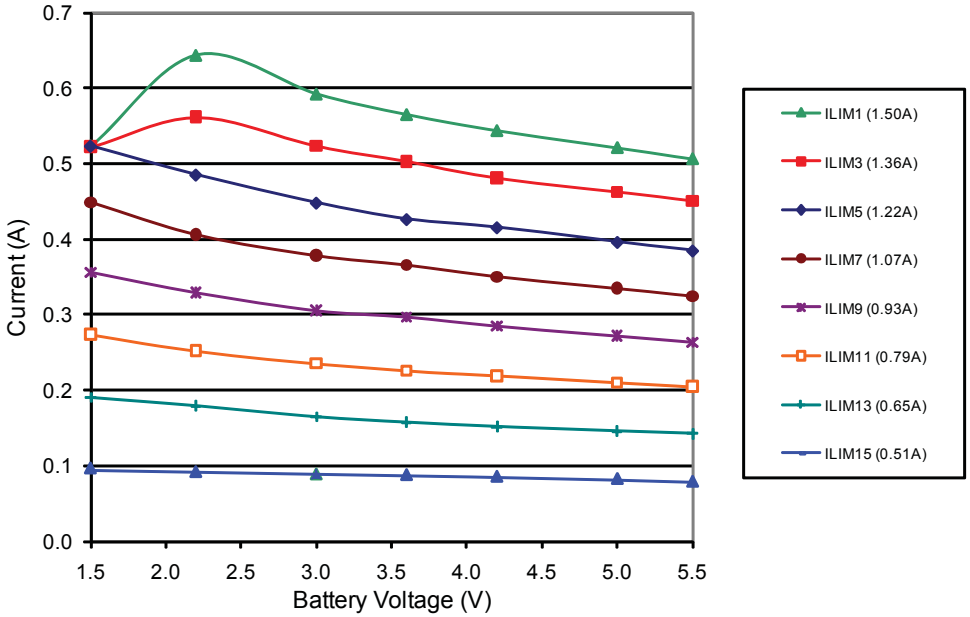
Final Output Voltage versus Secondary Side Conduction Time at Various Battery Voltages

R_{BAT} = 0 Ω, Transformer $L_{PRIMARY}$ = 12.8 µH, N =10.25, V_{IN} =3.6 V, at room temperature



Average Input Current versus Battery Voltage at Various ILIM

R_{BAT} = 0 Ω, Transformer $L_{PRIMARY}$ = 12.8 µH, N =10.25, V_{IN} =3.6 V, at room temperature



Note: Peak switch current is limited by the maximum on-time and di/dt of the transformer primary current; therefore, average input current drops at very low battery voltage.

Charging Waveforms

Output Capacitor Charging at Various Peak Current Limits

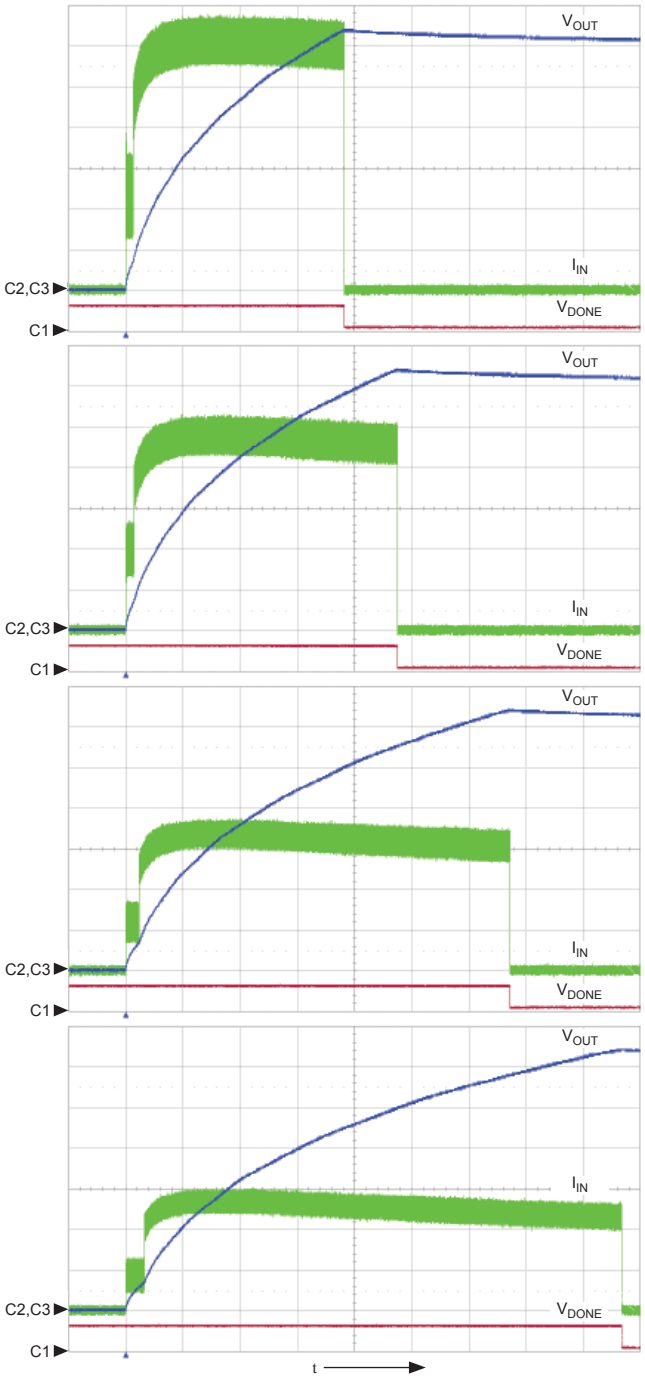
Test conditions: V_{IN} = 3.0 V, V_{BAT} = 3.7 V, C_{OUT} = 100 µF / 330 V UCC, transformer = T-16-024A ($L_{PRIMARY}$ =12.8 µH, N = 10.25), at room temperature
Oscilloscope settings: Ch1 = $\overline{DONE}$ (5 V / div), Ch2 = Output Voltage (50 V / div), Ch3 = Input Current (100 mA / div), Time scale = 1 sec / div

ILIM1 (1.5 A)

ILIM5 (1.22 A)

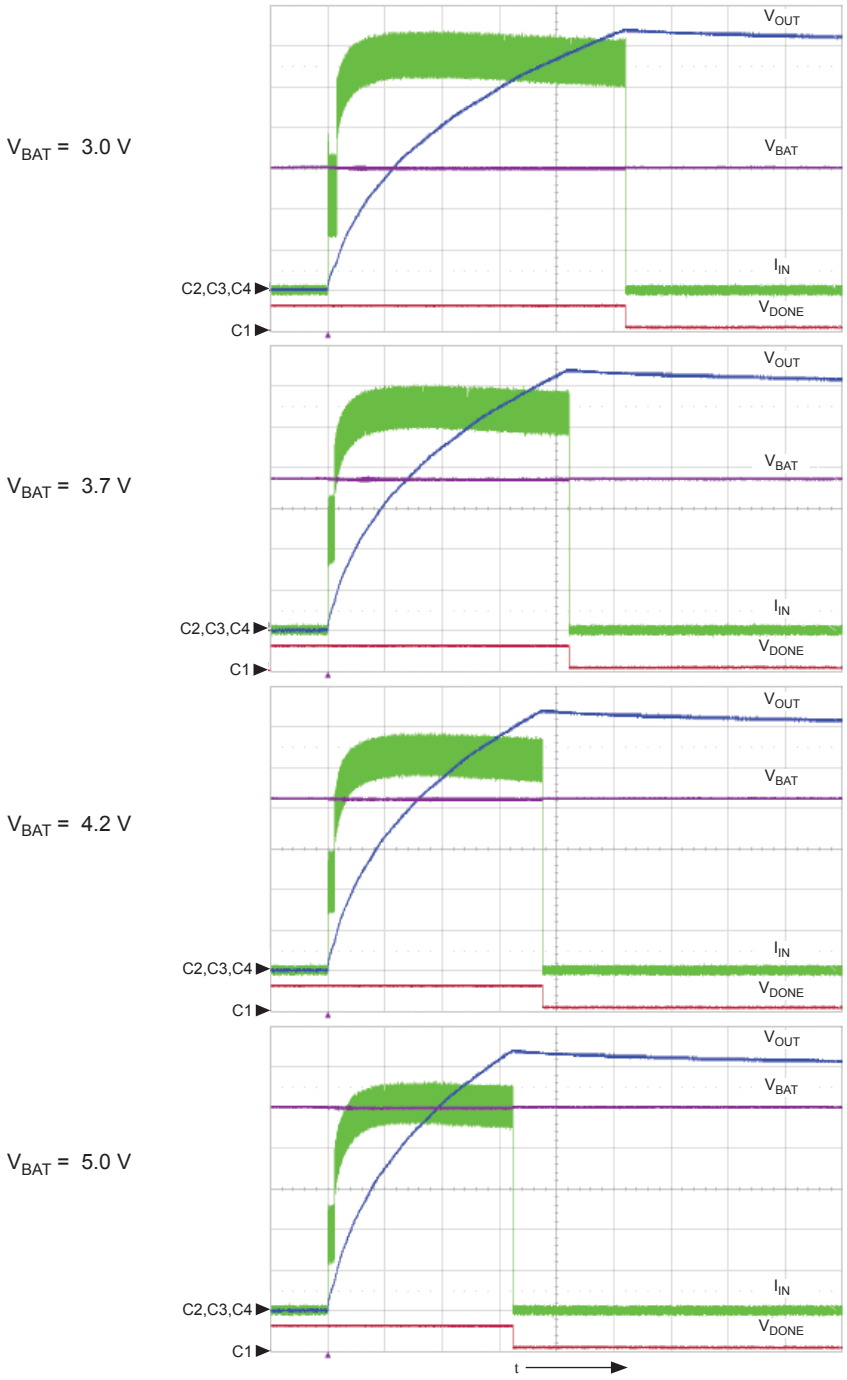
ILIM9 (0.93 A)

ILIM11 (0.79 A)



Output Capacitor Charging at Various Battery Voltages

Test conditions: V_{IN} = 3.0 V, I_{LIM3} (1.36 A), C_{OUT} = 100 µF / 330 V UCC, transformer = T-16-024A ($L_{PRIMARY}$ =12.8 µH, N = 10.25), at room temperature
Oscilloscope settings: Ch1 = $\overline{DONE}$ (5 V / div), Ch2 = Battery Voltage (1 V / div), Ch3 = Output Voltage (50 V / div), Ch4 = Input Current (100 mA V / div), Time scale = 1 sec / div



Functional Description

General Operation Overview

The charging operation is started by a low-to-high signal on the CHARGE pin, provided that V_{IN} is above the V_{UVLO} level. It is strongly recommended to keep the CHARGE pin at logic low during power-up. After V_{IN} exceeds the UVLO level, a low-to-high transition on the CHARGE pin is required to start the charging.

The $\overline{\text{DONE}}$ open-drain indicator is pulled low when CHARGE is high and target output voltage is reached. The primary peak current is set to 1.5 A by default, but it can be programmed from 1.5 A down to approximately 0.44 A in 15 steps. See the ILIM Programming section for details.

When a charging cycle is initiated, the transformer primary side current, $I_{PRIMARY}$, ramps-up linearly at a rate determined by the combined effect of the battery voltage, V_{BAT}, and the primary side inductance, $L_{PRIMARY}$. When $I_{PRIMARY}$ reaches the current limit, I_{SWLIM}, the internal MOSFET is turned off immediately, allowing the energy to be pushed into the photoflash capacitor, C_{OUT}, from the secondary winding. The secondary side current drops linearly as C_{OUT} charges. The switching cycle starts again, either after the transformer flux is reset, or after a predetermined time period, t_{OFF}(max) (18 µs), whichever occurs first.

The A8739 senses output voltage indirectly on primary side. This eliminates the need for high voltage feedback resistors required for secondary sensing. Flyback converter stops switching when output voltage reaches:

$$V_{OUT} = K \times N - V_d ,$$

Where:

K = 31.5 V typically,

V_d is the forward drop of the output diode (approximately 2 V), and

N is transformer turns ratio.

Switch On-Time and Off-Time Control

The A8739 implements an adaptive on-time/off-time control. On-time duration, t_{on}, is approximately equal to

$$t_{on} = I_{SWlim} \times L_{PRIMARY} / V_{BAT} .$$

Off-time duration, t_{off}, depends on the operating conditions during switch off-time. The A8739 applies two charging modes: Fast Charging mode and Timer mode, according to the conditions described in the next section.

Timer Mode and Fast Charging Mode

The A8739 achieves fast charging times and high efficiency by operating in discontinuous conduction mode (DCM) through most of the charging process. The relationship of Timer mode and Fast Charging mode is shown in figure 2.

The IC operates in Timer mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 30 V (depending on transformer used). Timer mode is a fixed period, 18 µs, off-time control. One advantage of having Timer mode is that it limits the initial battery current surge and thus acts as a "soft-start." A time-expanded view of a Timer mode interval is shown in figure 3.

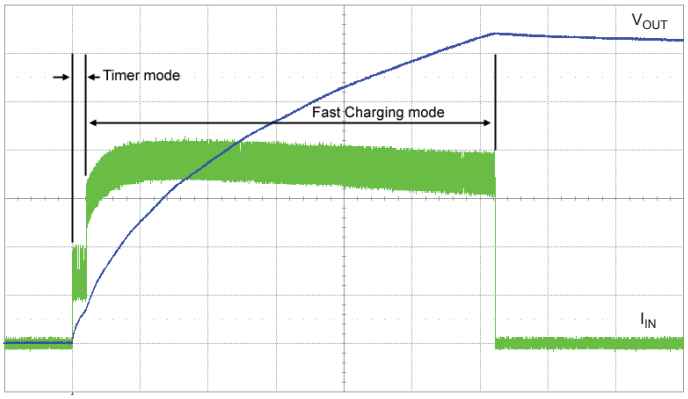


Figure 2. Timer mode and Fast Charging mode: V_{OUT} = 50 V/div, I_{IN} = 100 mA/div., V_{IN} = V_{BAT} = 3.6 V, C_{OUT} = 100 µF/330 V, ILIM = 1.0 A, and t = 1 s/div.

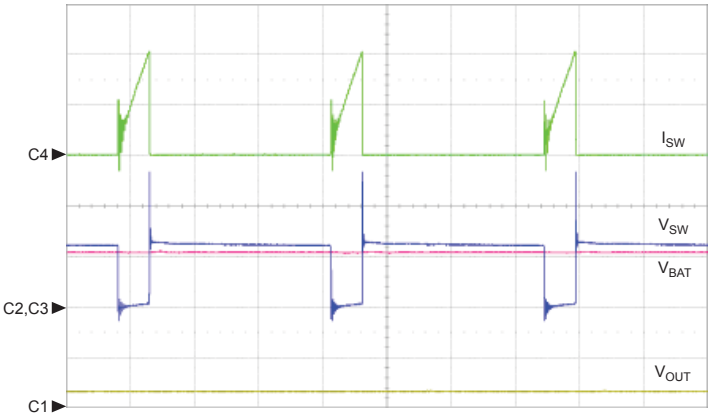


Figure 3. Expanded view of Timer mode: V_{OUT} ≤ 10 V, V_{BAT} = 5.5 V, Ch1: V_{OUT} = 20 V/div., Ch2: V_{BAT} = 5 V/div., Ch3: V_{SW} = 5 V/div., Ch4: I_{SW} = 500 mA/div., t = 5 µs / div.

As soon as a sufficient voltage has built up at the output capacitor, the IC enters Fast-Charging mode. In this mode, the next switching cycle starts after the secondary side current has stopped flowing, and the switch voltage has dropped to a minimum value. A proprietary circuit is used to allow minimum-voltage switching, even if the SW pin voltage does not drop to 0 V. This enables Fast-Charging mode to start earlier, thereby reducing the overall charging time. Minimum-voltage switching is shown in figure 4.

During Fast-Charging mode, when V_{OUT} is high enough (over 50 V), true zero-voltage switching (ZVS) is achieved. This further improves efficiency as well as reduces switching noise. A ZVS interval is shown in figure 5.

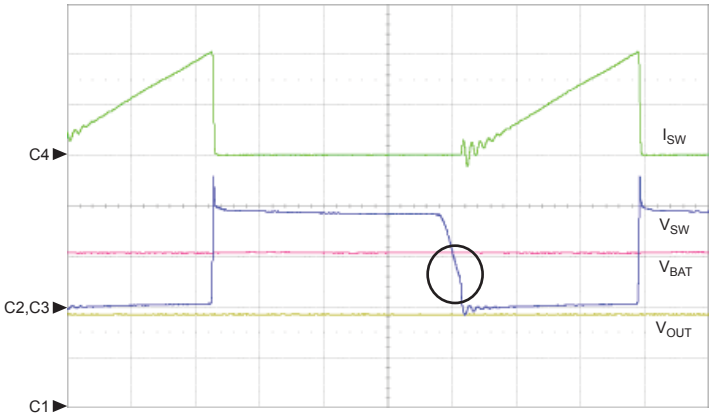


Figure 4. Minimum-voltage switching: $V_{OUT} \geq 35$ V, $V_{BAT} = 5.5$ V, Ch1: $V_{OUT} = 20$ V/div., Ch2: $V_{BAT} = 5$ V/div., Ch3: $V_{SW} = 5$ V/div., Ch4: $I_{SW} = 500$ mA/div., t = 1 µs / div.

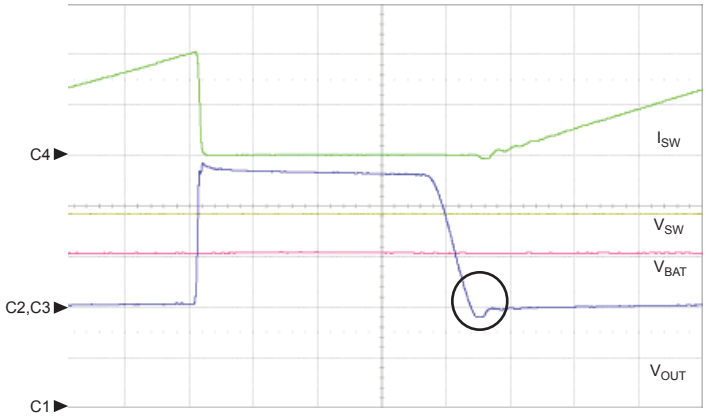


Figure 5. True zero-voltage switching (ZVS): $V_{OUT} = 75$ V, $V_{BAT} = 5.5$ V, Ch1: $V_{OUT} = 20$ V/div., Ch2: $V_{BAT} = 5$ V/div., Ch3: $V_{SW} = 5$ V/div., Ch4: $I_{SW} = 500$ mA/div., t = 0.5 µs / div.

ILIM Programming

The peak current limit can be programmed to sixteen different levels, from 100% to 29%, with programming through the CHARGE pin. An internal digital circuit decodes the input clock signals, which sets the switch current limit. This flexible scheme allows the user to operate the A8739 at required current limits. The battery life can be effectively extended by setting a lower current limit at low battery voltages. Figure 6 shows the ILIM clock timing scheme protocol. The total ILIM setup time, $t_{ILIM(SU)}$, denotes the time needed for the decoder circuit to receive ILIM inputs and set I_{SWLIM}, and has a typical duration of 200 µs.

Figure 7 shows the timing definition of the primary current limiting circuit. At the end of the setup period, $t_{ILIM(SU)}$, primary current starts to ramp up to the set I_{SWLIM}. The I_{SWLIM} setting remains in effect as long as the CHARGE pin is high. To reset the ILIM decoder, pull the CHARGE pin low before clocking-in the new setting.

After the first start-up or an ILIM decoder reset, each new current limit can be set by sending a burst of pulses to the CHARGE pin. The first rising edge starts the ILIM decoder, and up to 16 rising edges will be counted to set the ISWLIM level. The first pulse width, $t_{ILIM1(H)}$, must be at least 15 µs long. Subsequent pulses (up to 15 more) can be as short as 0.2 µs. The last low-to-high edge must arrive within 200 µs from the first edge. The CHARGE pin will stay high afterwards.

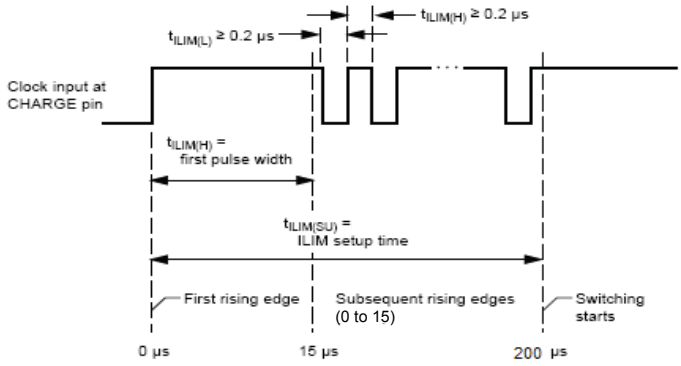


Figure 6. ILIM programming timing definition

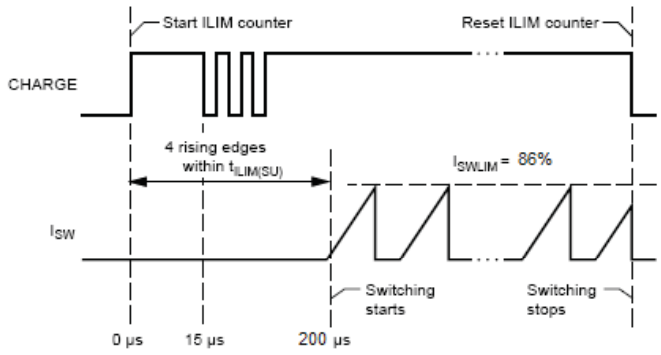


Figure 7. Current limit timing example (I_{SWLIM4} selected)

Output Voltage Adjustment

The target output voltage of the A8739 is primarily determined by the transformer turns ratio, N:

$$V_{OUT} = 31.5\ (V) \times N$$

Typically N = 10, so the output voltage is approximately 315 V. This output voltage can be further programmed in 5 V decrements down to 295 V, by using an external resistor at the VBAT pin. This enables fine-tuning to achieve better accuracy, and provides greater flexibility in the selection of transformers. Refer to figure 8 for example: An external resistor R_{BAT} = 2.32 kΩ is used to set the target output voltage at two steps lower, or 305 V when the transformer turns ratio = 10. Capacitor C3 is needed in case excessive switching noises is coupled into the VBAT pin, which may affect accuracy of target voltage.

The relationship of output voltage and VBAT resistance is shown in figure 9. To ensure proper voltage selection, use only 1% resistors. If C3 is used, make sure the RC filter time constant (R_{BAT} × C3) is less than 1 µs approximately.

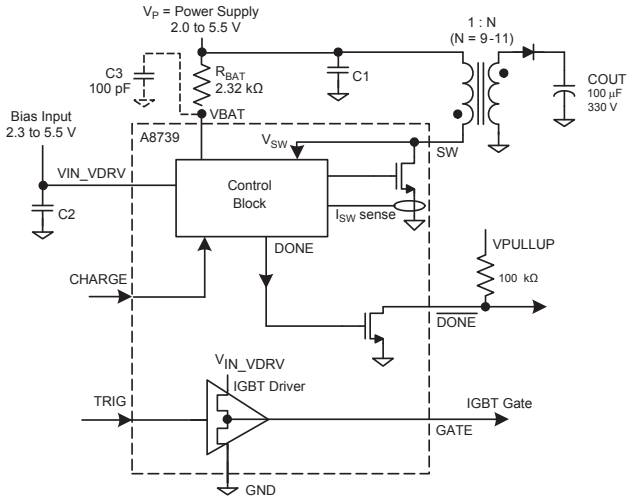
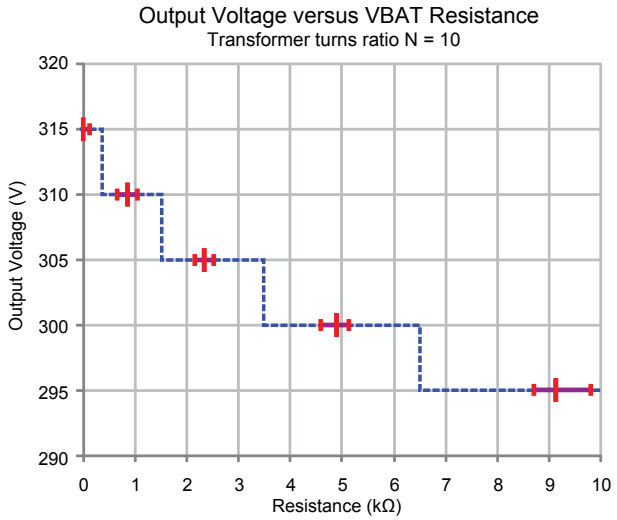


Figure 8. Adjustment of V_{OUT} using a series resistor at the VBAT pin (V_{OUT} = 30.5 × N).



Resistance, R_{BAT} (kΩ)	Output Voltage, V_{OUT} (V)	Recommended 1% Resistor Values (kΩ)	Recommended C3 capacitance (pF)
0 to 0.10	31.5 × N	0	Optional
0.65 to 1.03	31.0 × N	0.845	100
2.15 to 2.49	30.5 × N	2.32	100
4.58 to 5.08	30.0 × N	4.87	100
8.68 to 9.76	29.5 × N	9.09	47

Figure 9. Relationship of V_{OUT} and a series resistor at the VBAT pin

Applications Information

Transformer Design

1. The transformer turns ratio, N, determines the output voltage:

$$N = N_S / N_P$$

$$V_{OUT} = 31.5 \times N - V_d \ ,$$

where 31.5 is the typical value of $V_{OUTTRIP}$, and V_d is the forward drop of the output diode.

2. The primary inductance, $L_{PRIMARY}$, determines the on-time of the switch:

$$t_{on} = (-L_{PRIMARY}/R) \times \ln(1 - I_{SWlim} \times R/V_{IN}) \ ,$$

where R is the total resistance in the primary current path (including $R_{SWDS(on)}$ and the DC resistance of the transformer).

If V_{IN} is much larger than $I_{SWlim} \times R$, then t_{on} can be approximated by:

$$t_{on} = I_{SWlim} \times L_{PRIMARY} / V_{IN} \ .$$

3. The secondary inductance, $L_{SECONDARY}$, determines the off-time of the switch. Given:

$$L_{SECONDARY}/L_{PRIMARY} = N \times N \text{ , then}$$

$$t_{off} = (I_{SWlim}/N) \times L_{SECONDARY}/V_{OUT}$$

$$= (I_{SWlim} \times L_{PRIMARY} \times N)/V_{OUT} \ .$$

The minimum pulse width for t_{off} determines what is the minimum $L_{PRIMARY}$ required for the transformer. For example, if ILIM8 = 1.0 A, N = 10, and V_{OUT} = 315 V, then $L_{PRIMARY}$ must be at least 6.3 µH in order to keep t_{off} at 200 ns or longer. These relationships are illustrated in figure 10.

In general, choosing a transformer with a larger $L_{PRIMARY}$ results in higher efficiency (because a larger $L_{PRIMARY}$ corresponds to a lower switch frequency and hence lower switching loss). But transformers with a larger $L_{PRIMARY}$ also require more windings and larger magnetic cores. Therefore, a trade-off must be made between transformer size and efficiency.

Leakage Inductance and Secondary Capacitance

The transformer design should minimize the leakage inductance to ensure the turn-off voltage spike at the SW node does not exceed the absolute maximum specification on the SW pin (refer to the Absolute Maximum Ratings table). An achievable minimum leakage inductance for this application, however, is usually compromised by an increase in parasitic capacitance. Furthermore, the transformer secondary capacitance should be minimized. Any secondary capacitance is multiplied by N^2 when reflected to the primary, leading to high initial current swings when the switch turns on, and to reduced efficiency.

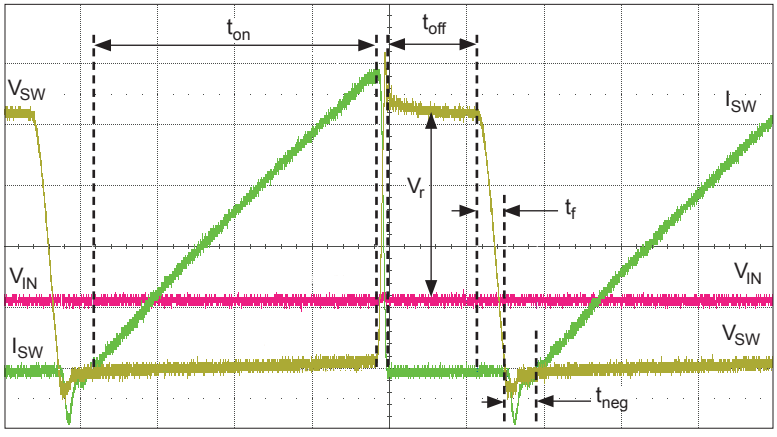


Figure 10. Transformer Selection Relationships

Input Capacitor Selection

Ceramic capacitors with X5R or X7R dielectrics are recommended for the input capacitor, C_{IN}. During initial Timer mode the device operates with 18 µs off-time. The resonant period caused by input filter inductor and capacitor should be at least 2 times greater or smaller than the 18 µs Timer period, to reduce input ripple current during this period. The typical input LC filter is shown in figure 11.

The resonant period is given by:

$$T_{res} = 2\,\pi\,(L \times C_{IN})^{1/2}\ .$$

The effects of input filter components are shown in figures 12, 13, and 14. It is recommended to use at least 10 µF / 6.3 V to decouple the battery input, VBAT , at the primary of the transformer. Decouple the VIN pin using 0.1 µF / 6.3 V bypass capacitor.

Output Diode Selection

Choose rectifying diodes, D1, to have small parasitic capacitance (short reverse recovery time) while satisfying the reverse voltage and forward current requirements. The peak reverse voltage of the diodes, V_{DPeak} , occurs when the internal MOSFET switch is closed. It can be calculated as:

$$V_{DPeak} = V_{OUT} + N \times V_{BAT}\ .$$

The peak current of the rectifying diode, I_{DPeak}, is calculated as:

$$I_{DPeak} = I_{PRIMARY\_Peak} / N\ .$$

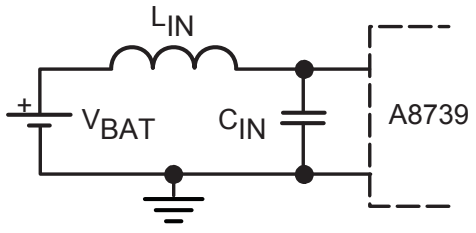


Figure 11. Typical input section with input inductance (inductance, L_{IN}, may be an input filter inductor or inductance due to long wires in test setup)

Effects of Input Filters

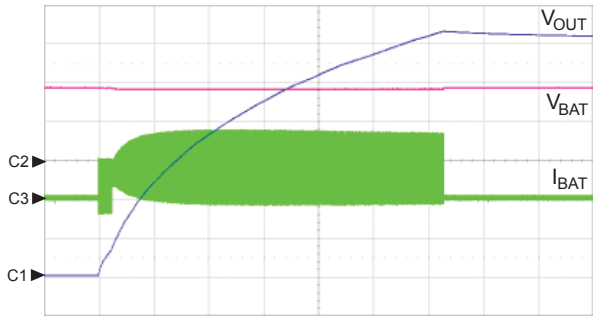


Figure 12. Input current waveforms with Li+ battery connected by 5-in. wire and decoupled by 4.7 µF capacitor, C_{OUT} = 100 µF, V_{IN} = V_{BAT} = 3.6 V, Ch1: V_{OUT} = 50 V/div, Ch2: V_{BAT} = 2 V/div, Ch3: I_{BAT} = 500 mA/div, t = 1 s/div

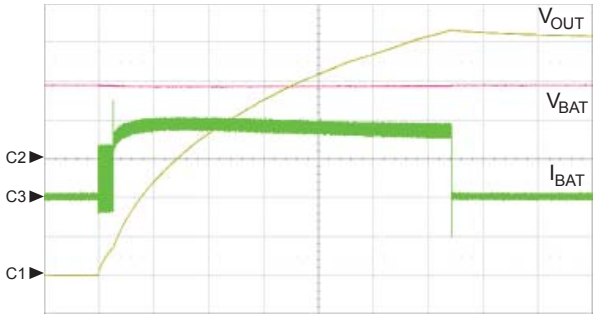


Figure 13. Input current waveforms with Li+ battery connected through 4.7 µH inductor and 4.7 µF capacitor, C_{OUT} = 100 µF, V_{IN} = V_{BAT} = 3.6 V, Ch1: V_{OUT} = 50 V/div, Ch2: V_{BAT} = 2 V/div, Ch3: I_{BAT} = 200 mA/div, t = 1 s/div

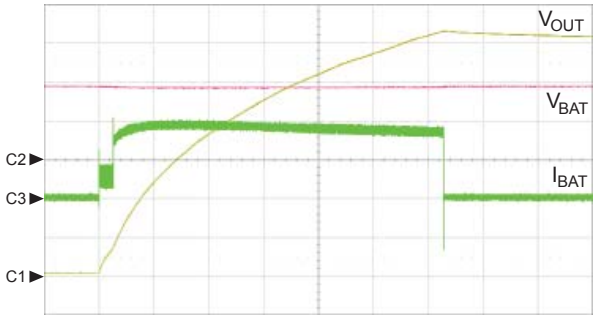


Figure 14. Input current waveforms with Li+ battery connected through 4.7 µH inductor and 10 µF capacitor, C_{OUT} = 100 µF, V_{IN} = V_{BAT} = 3.6 V, Ch1: V_{OUT} = 50 V/div, Ch2: V_{BAT} = 2 V/div, Ch3: I_{BAT} = 200 mA/div, t = 1 s/div

Layout Guidelines

Key to a good layout for the photoflash capacitor charger circuit is to keep the parasitics minimized on the power switch loop (transformer primary side) and the rectifier loop (secondary side). Use short, thick traces for connections to the transformer primary and SW pin. It is important that the $\overline{\text{DONE}}$ signal trace and other signal traces be routed away from the transformer and other switching traces, in order to minimize noise pickup. In addition, high voltage isolation rules must be followed carefully to avoid breakdown failure of the circuit board.

Avoid placing any ground plane area underneath the transformer secondary and diode, to minimize parasitic capacitance.

For low threshold logic (<1.2 V) add 1 nF capacitors across the CHARGE and TRIGGER pins to GND to avoid malfunction due to noise.

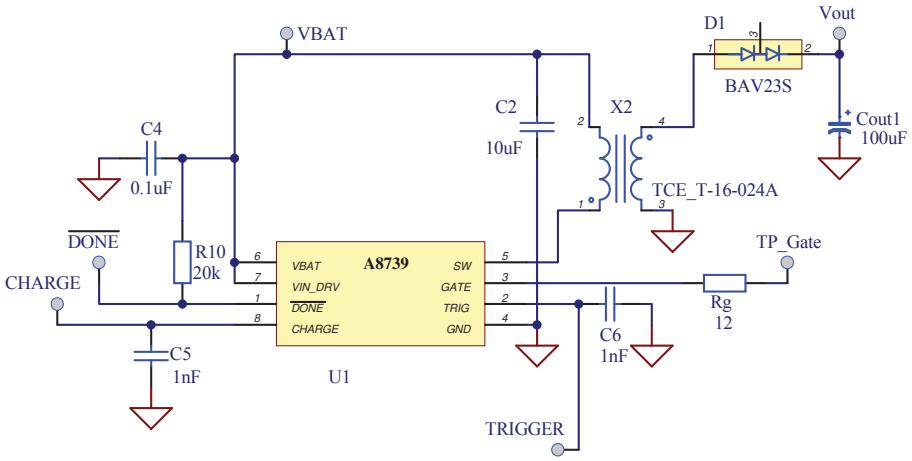
Connect the EE package PAD to the ground pad for better thermal performance. Use ground planes on the top and bottom layers below the IC and connect them through multiple thermal vias. Refer to the figures on page 20 for recommended layout.

Recommended Components

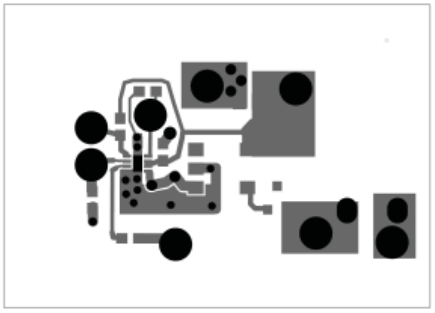
Component	Rating	Part Number	Source
C1, Input Capacitor	10 µF, ±10%, 6.3 V, X5R ceramic capacitor (0805)	JMK212BJ106K	Taiyo Yuden
C2	0.1uF, 6.3V X5R ceramic capacitor		
C_{OUT}, Photoflash Capacitor	100 µF / 330 V	EPH-31ELL101B131S	Chemi-Con
D1, Output Diode	2 x 250 V, 225 mA, 5 pF	BAV23S	Philips Semiconductor, Fairchild Semiconductor
T1, Transformer	$L_{PRIMARY}$ = 12.8 µH, N= 10.25, 6.5 × 8 × 4 mm	T-16-024A	Tokyo Coil Electric

Recommended layout:

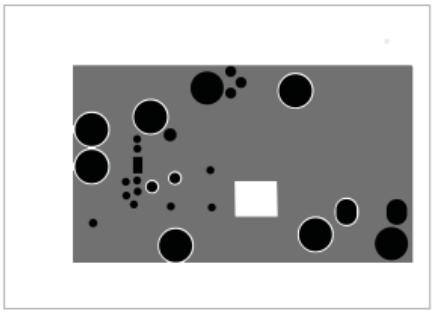
Schematic



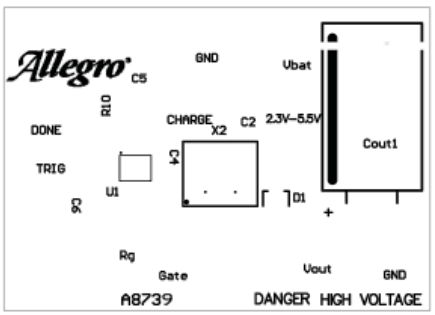
Top side



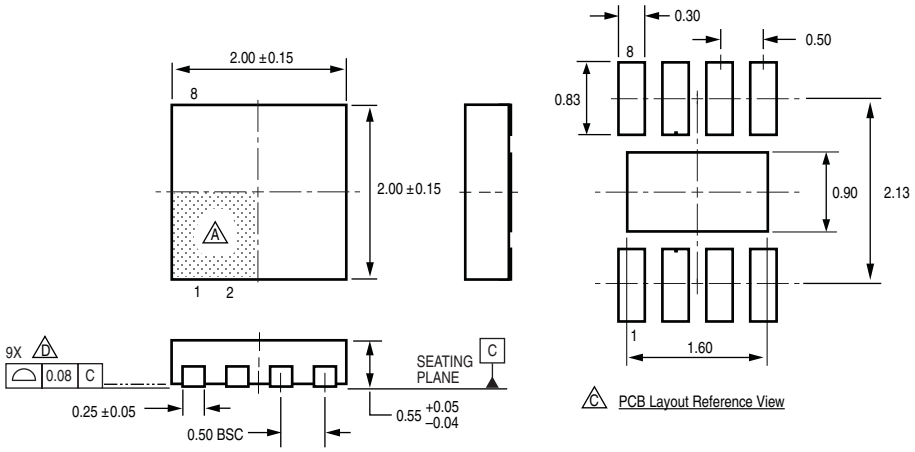
Bottom side

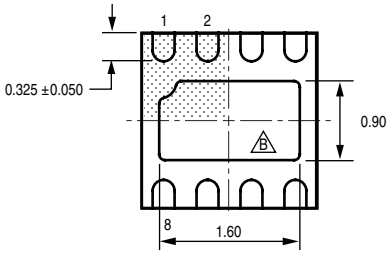


Top components



Package EE 8-Contact DFN/MLP with Exposed Thermal Pad





All dimensions nominal, not for tooling use
(reference JEDEC MO-229UCCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals