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Structure Silicon Monolithic Integrated Circuit
Function Voltage Regulated Charge Pump IC

Product BU90030G

Function
- Input voltage range 2.0V～4.0V
- PFM operation
- Output voltage 4.0V (typ)
- 1.5MHz(typ) switching frequency.
- SSOP6 package

Absolute Maximum rating（Ta=25c）

Item	Symbol	Rating	Unit
Maximum input power supply voltage	VCC	-0.3 ～ 7	V
Maximum input voltage	CP, CN, SHD, VOUT	-0.3 ～ 7	V
Power dissipation	Pd	675 (*1)	mW
Operating temperature range	Topr	-35～+85	C
Storage temperature range	Tstg	-55～+125	C
Junction temperature	Tjmax	+125	C

*1 When mounted on the specified PCB (70mm×70mm×1.6mm glass epoxy).
Deducted by 6.75mW/c when used over Ta=25c.

Operating range (Ta=25c)

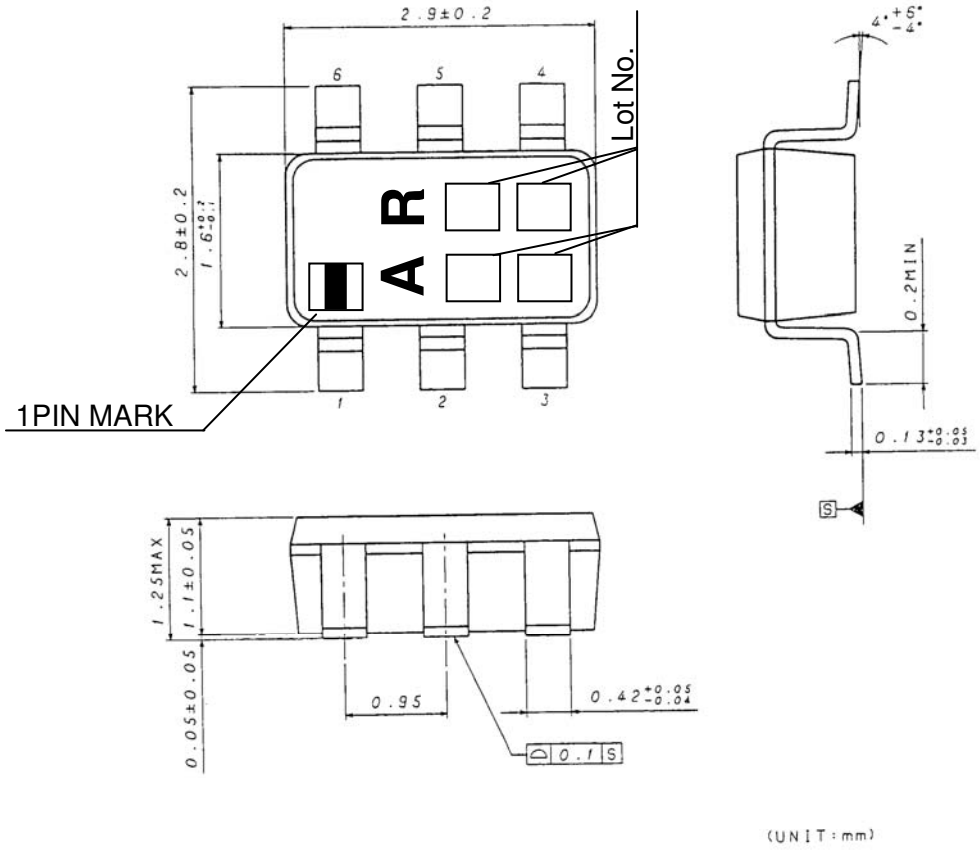
Item	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage	VBAT	2.0	-	4.0	V	
Flying Capacitor	Cfly	0.1	-	1.0	uF	
Output Capacitor	CCPOUT	1.0	-	10	uF	
Maximum Output Current	IOMAX	-	-	80	mA	VCC=2.5V, Cfly=1.0uF, COUT=1.0uF

Electrical characteristics (unless otherwise specified VBAT=2.5[v], Ta=25[c])

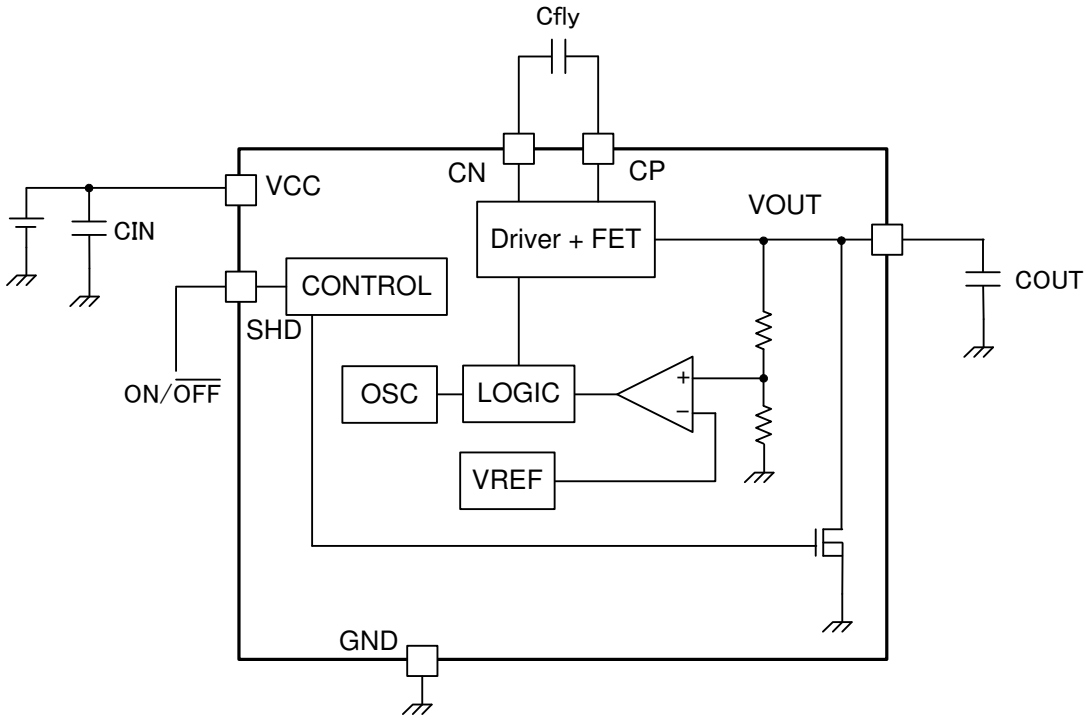
Item		Symbol	Rating			Unit	Condition
			Min.	Typ.	Max.		
【Voltage Control part】							
Output voltage 1		Vcpout1	3.8	4.0	4.2	V	Cfly=COUT=1uF
Output voltage 2		Vcpout2	3.6	-	-	V	VCC=2.0V, IOUT=40mA, Cfly=COUT=1.0uF
【Oscillator circuit】							
MaximumOscillator frequency		Fosc	1.0	1.5	2.0	MHz	VCC=2.0V, VOUT=3.8V, VOUT=40mA
【Output discharge circuit】							
Discharge resistor		RDIS	300	600	900	Ω	VCC=2.5V, VOUT=4.0V
【SHD part】							
SHD pin pull down resistor		RSHD	100	200	400	kΩ	
SHD pin control voltage	Operation	VSHDH	1.4	-	4.0	V	
	Non operation	VSHDL	0	-	0.4	V	
【Circuit current】							
Circuit current at shutdown		ISHD	-	0	5	uA	

* No design for durability against radiation

External dimention/Pin layout



Block diagram



Pin number/name/function

Pin nr	Name	Function
1	VOUT	Starting charge pump output pin
2	GND	GND pin
3	SHD	Shutdown pin
4	CN	Flying Capacitor L side input pin
5	VCC	Power supply input pin
6	CP	Flying Capacitor H side input pin

Operation Notes

1.) Absolute maximum ratings

An excess in the absolute maximum rating, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit.
If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2.) GND voltage

The potential of GND pin must be minimum potential in all condition. As an exception, the circuit design allows voltages up to -0.3 V to be applied to the IC pin.

3.) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions

4.) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

5.) Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction

6.) Mutual impedance

Power supply and ground wiring should reflect consideration of the need to lower mutual impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

7.) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, as shown in the figures below, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

8.) Thermal shutdown Circuit (TSD Circuit)

This model IC has a built-in TSD circuit. This circuit is only to cut off the IC from thermal runaway, and has not been design to protect or guarantee the IC. Therefore, the user should not plan to activate this circuit with continued operation in mind.

9.) External Component

Use a small ESR ceramic capacitor for the external capacitor (CIN,COUT,Cfly) and set them nearby IC.
Use the CIN capacitor's value that meets this condition (CIN≧COUT).
And Use the Cfly capacitor's value that meets this condition (Cfly≦COUT).
There may be a case that it doesn't achieve the objective characteristic because the capacity come down lower than the normal capacitor because of the bias voltage and the temperature when using a small layered ceramic capacitor.
Therefore, the user should use it after checking the DC bias capacity and other characteristics.

Notes

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