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PIC16LF1904/6/7

28/40/44-Pin 8-Bit Flash Microcontrollers with XLP Technology

High-Performance RISC CPU:

- C Compiler Optimized Architecture
- Only 49 Instructions
- Up to 14 Kbytes Self-Write/Read Flash Program Memory Addressing
- Up to 256 Bytes Data Memory Addressing
- Operating Speed:
  - DC – 20 MHz clock input @ 3.6V
  - DC – 16 MHz clock input @ 1.8V
  - DC – 200 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Memory

- Up to 14 Kbytes Self-Write/Read Flash Program Memory Addressing
- Up to 256 Bytes Data Memory Addressing
- High-Endurance Flash Data Memory (HEF)
  - 128B of nonvolatile data storage
  - 100K erase/write cycles

Flexible Oscillator Structure:

- 16 MHz Internal Oscillator Block:
  - Accuracy to ± 3%, typical
  - Software selectable frequency range from 16 MHz to 31.25 kHz
- 31 kHz Low-Power Internal Oscillator
- Three External Clock modes up to 20 MHz
- Two-Speed Oscillator Start-up
- Low-Power RTC Implementation via LPT1OSC

Special Microcontroller Features:

- Operating Voltage Range:
  - 1.8V-3.6V
- Self-Programmable under Software Control
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Low-Power Brown-Out Reset (LPBOR)
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Programmable Code Protection
- Power-Saving Sleep mode

eXtreme Low-Power (XLP) Features (PIC16LF1904/6/7):

- Sleep Current:
  - 30 nA @ 1.8V, typical
- Watchdog Timer Current:
  - 300 nA @ 1.8V, typical
- Secondary Oscillator:
  - 500 nA @ 32 kHz, 1.8V, typical

Analog Features:

- Analog-to-Digital Converter (ADC):
  - 10-bit resolution, up to 14 channels
  - Conversion available during Sleep
  - Dedicated ADC RC oscillator
  - Fixed Voltage Reference (FVR) as channel
- Integrated Temperature Indicator
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V and 2.048V output levels

Peripheral Highlights:

- Up to 36 I/O Pins and 1 Input-only Pin:
  - High current 25 mA sink/source
  - Individually programmable weak pull-ups
  - Individually programmable interrupt-on-change (IOC) pins
- Integrated LCD Controller:
  - At least 19 segment pins and as many as 116 total segments
  - Variable clock input
  - Contrast control
  - Internal voltage reference selections
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler

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- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Dedicated low-power 32 kHz oscillator driver
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on start

PIC16LF190X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High-Endurance Flash (bytes)	I/O's(2)	10-bit ADC (ch)	Timers (8/16-bit)	EUSART	LCD			Debug(1)	XLP
									Common Pins	Segment Pins	Total Segments		
PIC16LF1902	(1)	2048	128	128	25	11	1/1	—	4	19	72(3)	H	Y
PIC16LF1903	(1)	4096	256	128	25	11	1/1	—	4	19	72(3)	H	Y
PIC16LF1904	(2)	4096	256	128	36	14	1/1	1	4	29	116	I/H	Y
PIC16LF1906	(2)	8192	512	128	25	11	1/1	1	4	19	72(3)	I/H	Y
PIC16LF1907	(2)	8192	512	128	36	14	1/1	1	4	29	116	I/H	Y

Note 1: Debugging Methods: (I) – Integrated on Chip; (H) – using Debug Header; (E) – using Emulation Header.

2: One pin is input-only.

3: COM3 and SEG15 share a pin, so the total segments are limited to 72 for 28-pin devices.

Data Sheet Index: (Unshaded devices are described in this document.)

1: DS40001455 PIC16LF1902/3 Data Sheet, 28-Pin Flash, 8-bit Microcontrollers.

2: DS40001569 PIC16LF1904/6/7 Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers.

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

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FIGURE 1: 28-PIN PDIP, SOIC, SSOP PACKAGE DIAGRAM FOR PIC16LF1906

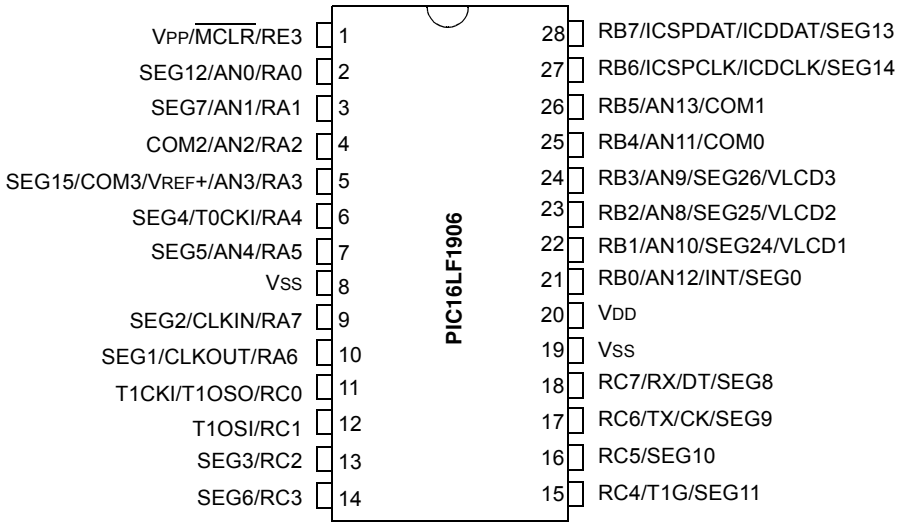

FIGURE 2: 28-PIN UQFN PACKAGE DIAGRAM FOR PIC16LF1906

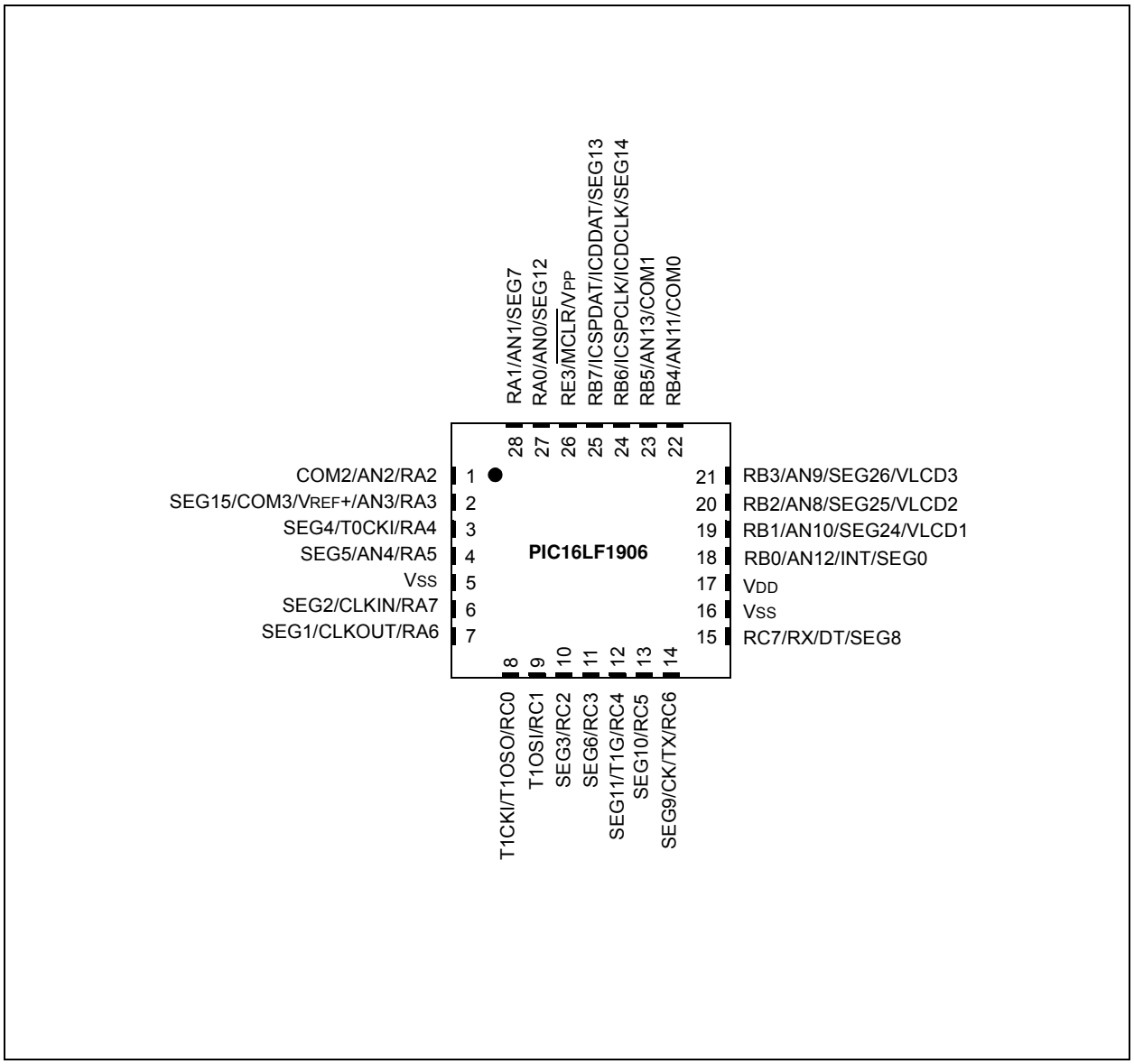

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FIGURE 3: 40-PIN PDIP PACKAGE DIAGRAM FOR PIC16LF1904/7

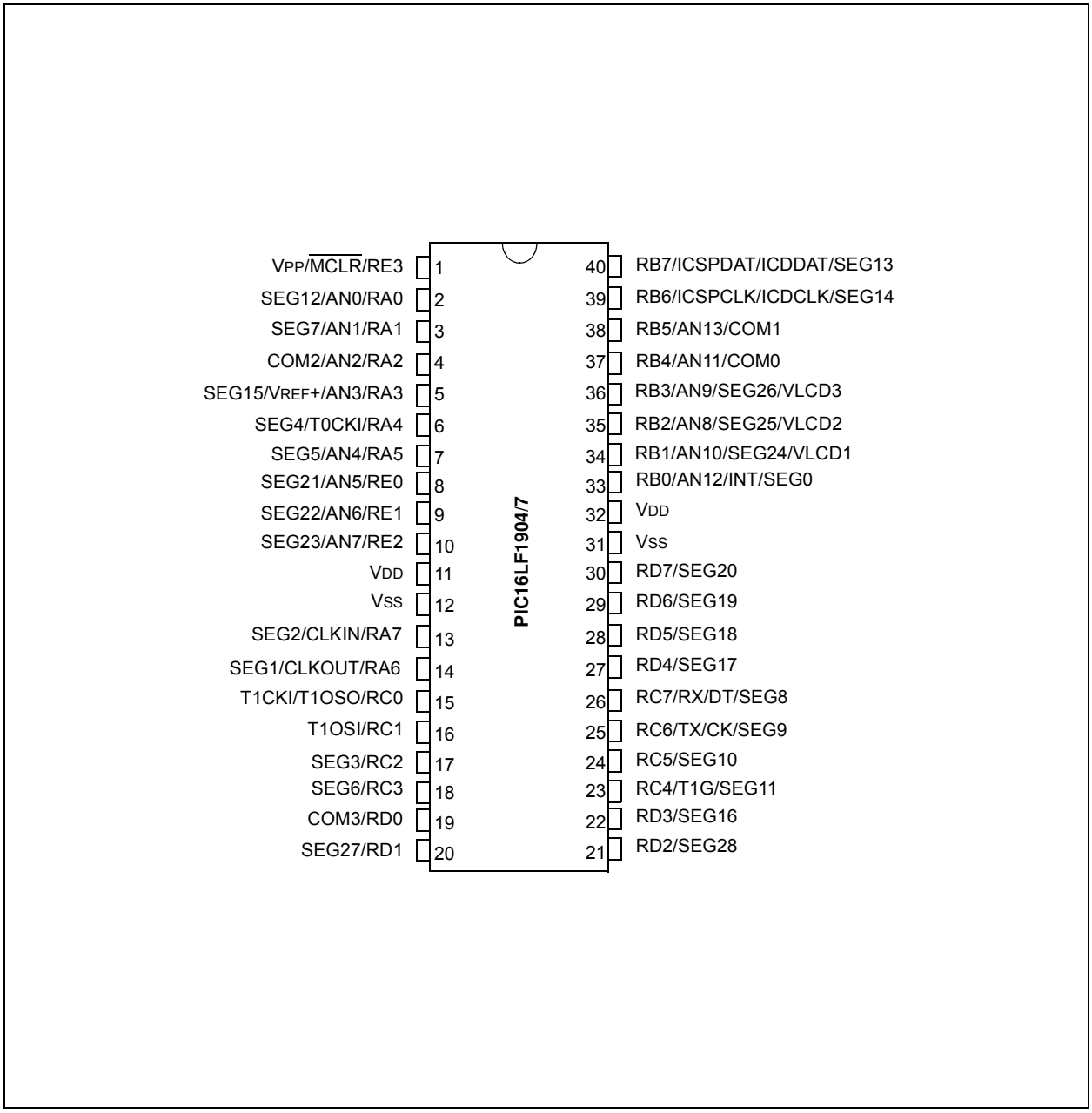

FIGURE 4: 44-PIN TQFP (10X10) PACKAGE DIAGRAM FOR PIC16LF1904/7

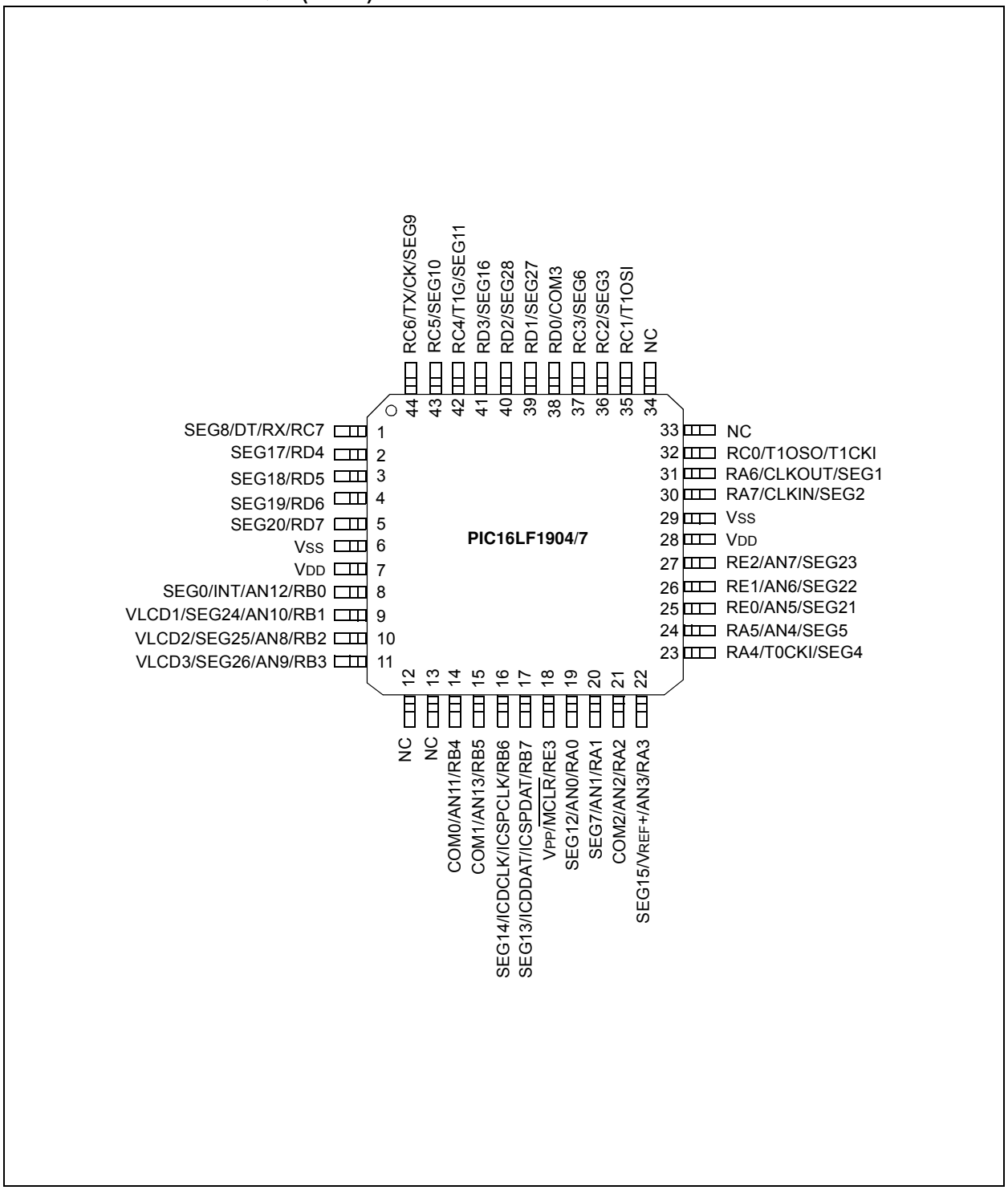

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FIGURE 5: 40-PIN UQFN (5X5) PACKAGE DIAGRAM FOR PIC16LF1904/7

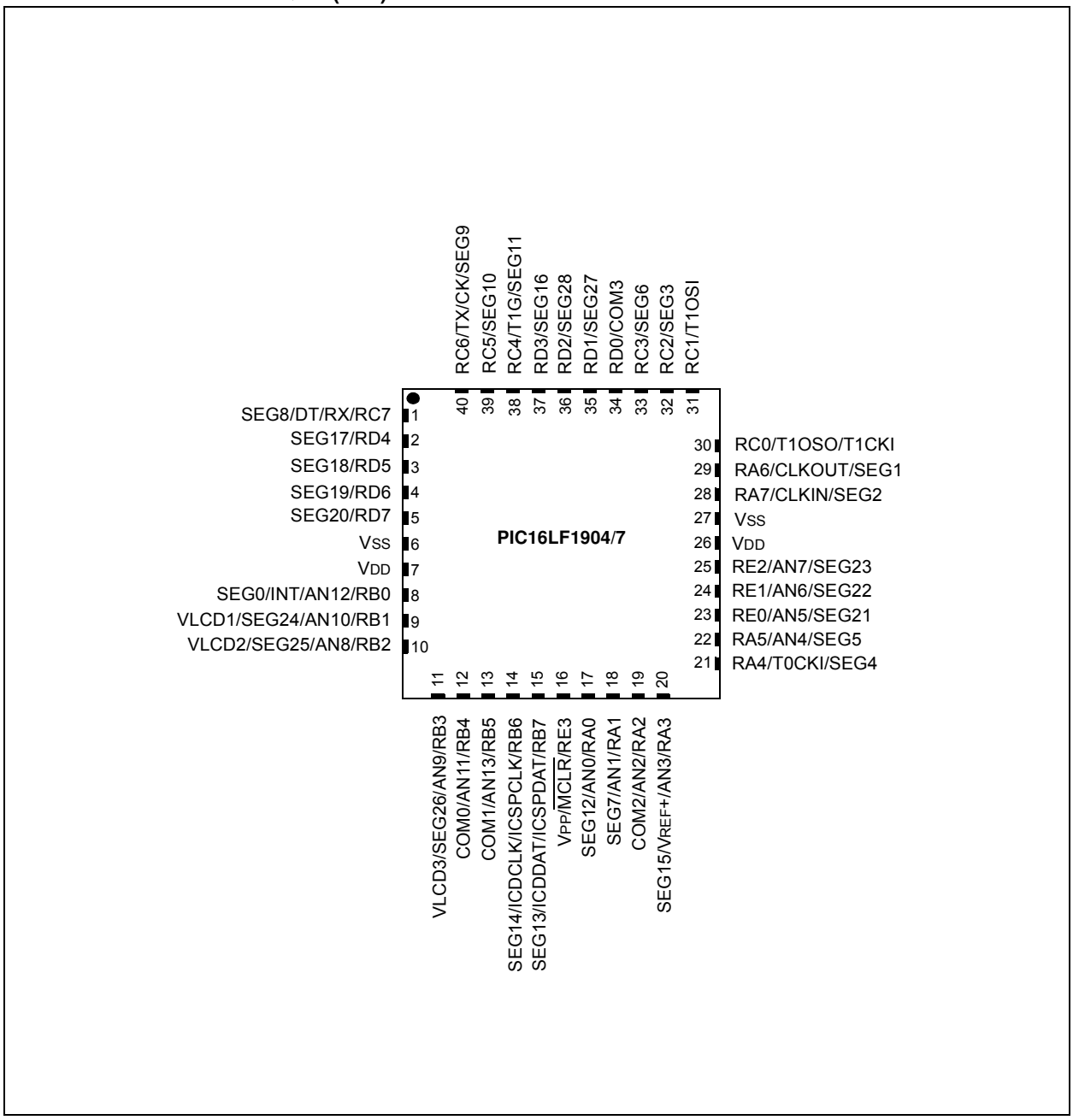

TABLE 1: 28/40/44-PIN ALLOCATION TABLE (PIC16LF1904/6/7)

I/O	28-Pin PDIP/ SOIC/SSOP	28-Pin UQFN	40-Pin PDIP	44-Pin TQFP	40-Pin UQFN	A/D	Timers	EUSART	LCD	Interrupt	Pull-up	Basic
RA0	2	27	2	19	17	AN0	—	—	SEG12	—	—	—
RA1	3	28	3	20	18	AN1	—	—	SEG7	—	—	—
RA2	4	1	4	21	19	AN2	—	—	COM2	—	—	—
RA3	5	2	5	22	20	AN3/ VREF+	—	—	SEG15/ COM3(2)	—	—	—
RA4	6	3	6	23	21	—	T0CKI	—	SEG4	—	—	—
RA5	7	4	7	24	22	AN4	—	—	SEG5	—	—	—
RA6	10	7	14	31	29	—	—	—	SEG1	—	—	CLKOUT
RA7	9	6	13	30	28	—	—	—	SEG2	—	—	CLKIN
RB0	21	18	33	8	8	AN12	—	—	SEG0	INT/ IOC	Y	—
RB1	22	19	34	9	9	AN10	—	—	VLCD1/ SEG24	IOC	Y	—
RB2	23	20	35	10	10	AN8	—	—	VLCD2/ SEG25	IOC	Y	—
RB3	24	21	36	11	11	AN9	—	—	VLCD3/ SEG26	IOC	Y	—
RB4	25	22	37	14	12	AN11	—	—	COM0	IOC	Y	—
RB5	26	23	38	15	13	AN13	—	—	COM1	IOC	Y	—
RB6	27	24	39	16	14	—	—	—	SEG14	IOC	Y	ICSPCLK/ ICDCLK
RB7	28	25	40	17	15	—	—	—	SEG13	IOC	Y	ICSPDAT/ ICDDAT
RC0	11	8	15	32	30	—	T1OSO/ T1CKI	—	—	—	—	—
RC1	12	9	16	35	31	—	T1OSI	—	—	—	—	—
RC2	13	10	17	36	32	—	—	—	SEG3	—	—	—
RC3	14	11	18	37	33	—	—	—	SEG6	—	—	—
RC4	15	12	23	42	38	—	T1G	—	SEG11	—	—	—
RC5	16	13	24	43	39	—	—	—	SEG10	—	—	—
RC6	17	14	25	44	40	—	—	TX/CK	SEG9	—	—	—
RC7	18	15	26	1	1	—	—	RX/DT	SEG8	—	—	—
RD0	—	—	19	38	34	—	—	—	COM3(3)	—	—	—
RD1	—	—	20	39	35	—	—	—	SEG27	—	—	—
RD2	—	—	21	40	36	—	—	—	SEG28	—	—	—
RD3	—	—	22	41	37	—	—	—	SEG16	—	—	—
RD4	—	—	27	2	2	—	—	—	SEG17	—	—	—
RD5	—	—	28	3	3	—	—	—	SEG18	—	—	—
RD6	—	—	29	4	4	—	—	—	SEG19	—	—	—
RD7	—	—	30	5	5	—	—	—	SEG20	—	—	—
RE0	—	—	8	25	23	AN5(4)	—	—	SEG21	—	—	—
RE1	—	—	9	26	24	AN6(4)	—	—	SEG22	—	—	—
RE2	—	—	10	27	25	AN7(4)	—	—	SEG23	—	—	—
RE3	1	26	1	18	16	—	—	—	—	—	Y(1)	$\overline{MCLR}$/VPP
VDD	20	17	11,32	7,28	7, 26	—	—	—	—	—	—	VDD
Vss	8,19	5,16	12,31	6,29	6, 27	—	—	—	—	—	—	Vss
NC	—	—	—	12,13, 33,34	—	—	—	—	—	—	—	VDD

Note 1: Weak pull-up always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.
2: 28-pin only pin location (PIC16LF1906). Location different on 40/44-pin device.
3: 40/44-pin only pin location (PIC16LF1904/7). Location different on 28-pin device.
4: ADC channel is reserved on the PIC16LF1906 28-pin devices.

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1.0 DEVICE OVERVIEW

The PIC16LF1904/6/7 are described within this data sheet. They are available in 28, 40 and 44-pin packages. Figure 1-1 shows a block diagram of the PIC16LF1904/6/7 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16LF1906	PIC16LF1904/7
ADC		•	•
EUSART		•	•
Fixed Voltage Reference (FVR)		•	•
LCD		•	•
Temperature Indicator		•	•
Timers			
	Timer0	•	•
	Timer1	•	•

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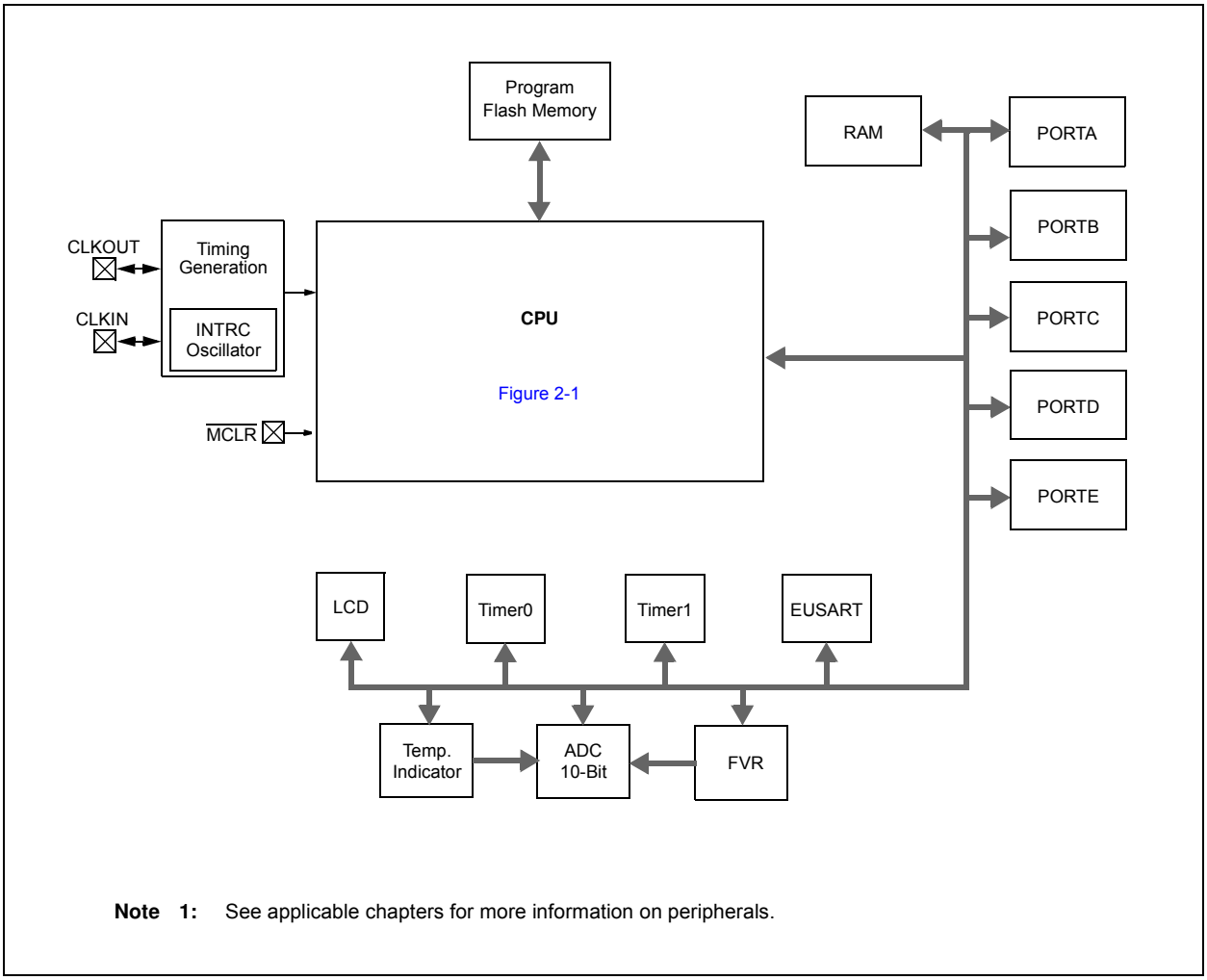
FIGURE 1-1: PIC16LF1904/6/7 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

TABLE 1-2: PIC16LF1904/6/7 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/SEG12	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	SEG12	—	AN	LCD Analog output.
RA1/AN1/SEG7	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
	SEG7	—	AN	LCD Analog output.
RA2/AN2/COM2	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
	COM2	—	AN	LCD Analog output.
RA3/AN3/VREF+/COM3(2)/ SEG15	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel 3 input.
	VREF+	AN	—	A/D Voltage Reference input.
	COM3	—	AN	LCD Analog output.
	SEG15	—	AN	LCD Analog output.
RA4/T0CKI/SEG4	RA4	TTL	CMOS	General purpose I/O.
	T0CKI	ST	—	Timer0 clock input.
	SEG4	—	AN	LCD Analog output.
RA5/AN4/SEG5	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	SEG5	—	AN	LCD Analog output.
RA6/CLKOUT/SEG1	RA6	TTL	CMOS	General purpose I/O.
	CLKOUT	—	CMOS	FOSC/4 output.
	SEG1	—	AN	LCD Analog output.
RA7/CLKIN/SEG2	RA7	TTL	CMOS	General purpose I/O.
	CLKIN	CMOS	—	External clock input (EC mode).
	SEG2	—	AN	LCD Analog output.
RB0/AN12/INT/SEG0	RB0	TTL	CMOS	General purpose I/O.
	AN12	AN	—	A/D Channel 12 input.
	INT	ST	—	External interrupt.
	SEG0	—	AN	LCD Analog output.
RB1(1)/AN10/SEG24/VLCD1	RB1	TTL	CMOS	General purpose I/O.
	AN10	AN	—	A/D Channel 10 input.
	SEG24	—	AN	LCD Analog output.
	VLCD1	AN	—	LCD analog input.
RB2(1)/AN8/SEG25/VLCD2	RB2	TTL	CMOS	General purpose I/O.
	AN8	AN	—	A/D Channel 8 input.
	SEG25	—	AN	LCD Analog output.
	VLCD2	AN	—	LCD analog input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: These pins have interrupt-on-change functionality.
2: PIC16LF1906/7 only.

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TABLE 1-2: PIC16LF1904/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB3(1)/AN9/SEG26/VLCD3	RB3	TTL	CMOS	General purpose I/O.
	AN9	AN	—	A/D Channel 9 input.
	SEG26	—	AN	LCD Analog output.
	VLCD3	AN	—	LCD analog input.
RB4(1)/AN11/COM0	RB4	TTL	CMOS	General purpose I/O.
	AN11	AN	—	A/D Channel 11 input.
	COM0	—	AN	LCD Analog output.
RB5(1)/AN13/COM1	RB5	TTL	CMOS	General purpose I/O.
	AN13	AN	—	A/D Channel 13 input.
	COM1	—	AN	LCD Analog output.
RB6(1)/ICSPCLK/ICDCLK/ SEG14	RB6	TTL	CMOS	General purpose I/O.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
	SEG14	—	AN	LCD Analog output.
RB7(1)/ICSPDAT/ICDDAT/ SEG13	RB7	TTL	CMOS	General purpose I/O.
	ICSPDAT	ST	—	Serial Programming Clock.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.
	SEG13	—	AN	LCD Analog output.
RC0/T1OSO/T1CKI	RC0	TTL	CMOS	General purpose I/O.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
RC1/T1OSI	RC1	TTL	CMOS	General purpose I/O.
	T1OSI	XTAL	XTAL	Timer1 oscillator connection.
RC2/SEG3	RC2	TTL	CMOS	General purpose I/O.
	SEG3	—	AN	LCD Analog output.
RC3/SEG6	RC3	TTL	CMOS	General purpose I/O.
	SEG6	—	AN	LCD Analog output.
RC4/T1G/SEG11	RC4	TTL	CMOS	General purpose I/O.
	T1G	XTAL	XTAL	Timer1 oscillator connection.
	SEG11	—	AN	LCD Analog output.
RC5/SEG10	RC5	TTL	CMOS	General purpose I/O.
	SEG10	—	AN	LCD Analog output.
RC6/TX/CK/SEG9	RC6	TTL	CMOS	General purpose I/O.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
	SEG9	—	AN	LCD Analog output.
RC7/RX/DT/SEG8	RC7	TTL	CMOS	General purpose I/O.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	SEG8	—	AN	LCD Analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: These pins have interrupt-on-change functionality.
2: PIC16LF1906/7 only.

TABLE 1-2: PIC16LF1904/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RD0(2)/COM3	RD0	TTL	CMOS	General purpose I/O.
	COM3	—	AN	LCD Analog output.
RD1(2)/SEG27	RD1	TTL	CMOS	General purpose I/O.
	SEG27	—	AN	LCD Analog output.
RD2(2)/SEG28	RD2	TTL	CMOS	General purpose I/O.
	SEG28	—	AN	LCD Analog output.
RD3(2)/SEG16	RD3	TTL	CMOS	General purpose I/O.
	SEG16	—	AN	LCD Analog output.
RD4(2)/SEG17	RD4	TTL	CMOS	General purpose I/O.
	SEG17	—	AN	LCD Analog output.
RD5(2)/SEG18	RD5	TTL	CMOS	General purpose I/O.
	SEG18	—	AN	LCD Analog output.
RD6(2)/SEG19	RD6	TTL	CMOS	General purpose I/O.
	SEG19	—	AN	LCD Analog output.
RD7(2)/SEG20	RD7	TTL	CMOS	General purpose I/O.
	SEG20	—	AN	LCD Analog output.
RE0(2)/AN5/SEG21	RE0	TTL	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	SEG21	—	AN	LCD Analog output.
RE1(2)/AN6/SEG22	RE1	TTL	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
	SEG22	—	AN	LCD Analog output.
RE2(2)/AN7/SEG23	RE2	TTL	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
	SEG23	—	AN	LCD Analog output.
RE3/$\overline{MCLR}$/VPP	RE3	TTL	CMOS	General purpose I/O.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: These pins have interrupt-on-change functionality.
2: PIC16LF1906/7 only.

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2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"**, for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have an external stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a software Reset. See **Section 3.4 "Stack"** for more details.

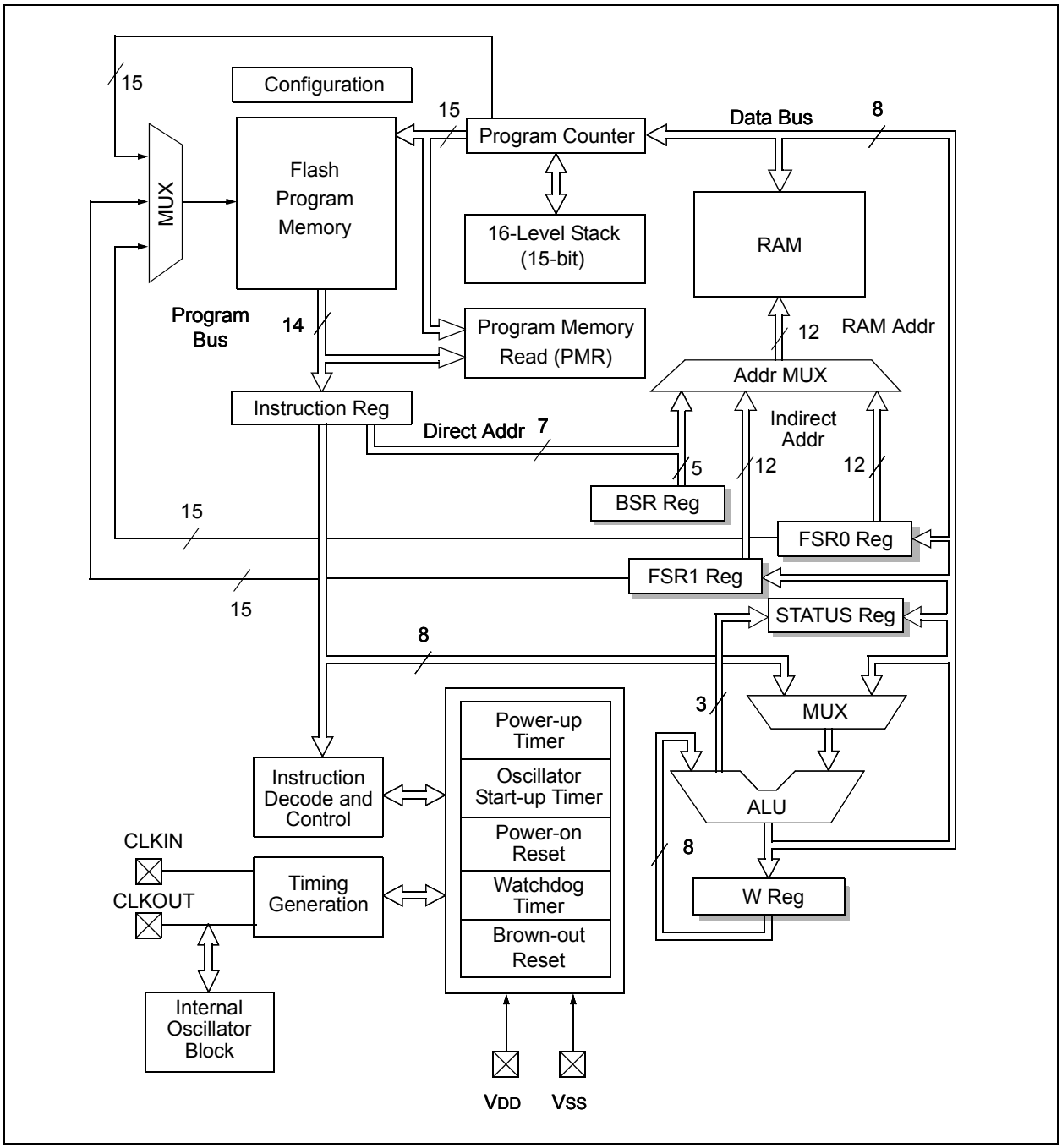
2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.5 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 21.0 "Instruction Set Summary"** for more details.

FIGURE 2-1: CORE BLOCK DIAGRAM



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3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16LF1904/6/7 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 3-1, and 3-2).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address	High-Endurance Flash Memory Address Range (1)
PIC16LF1904	4,096	0FFFh	0F80h-0FFFh
PIC16LF1906/7	8,192	1FFFh	1F80h-1FFFh

Note 1: High-endurance Flash applies to low byte of each address in the range.

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16LF1904

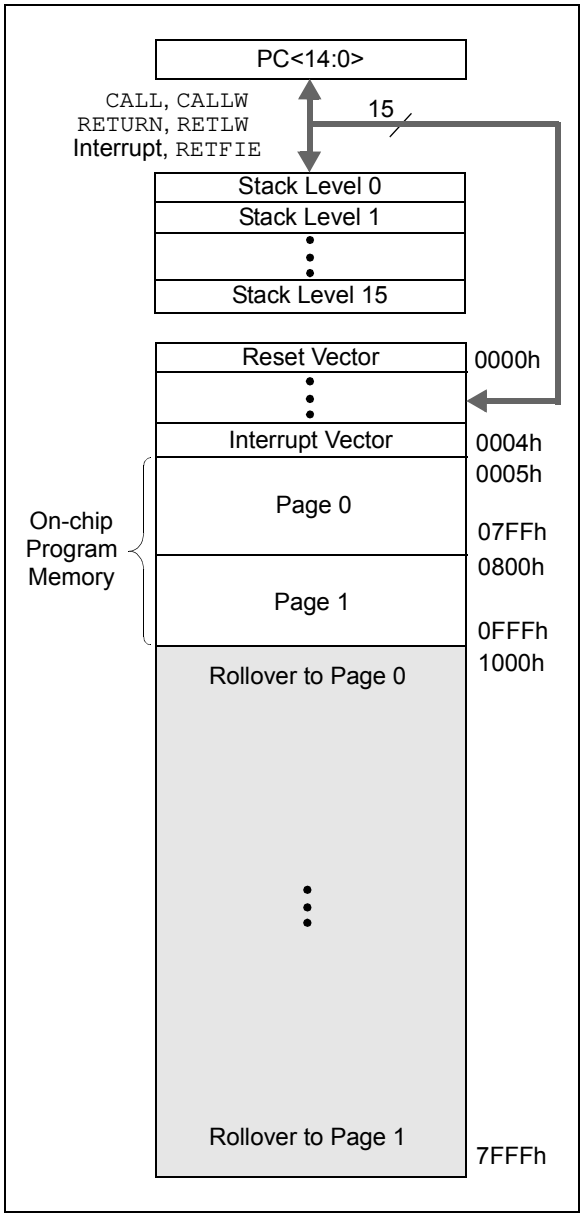
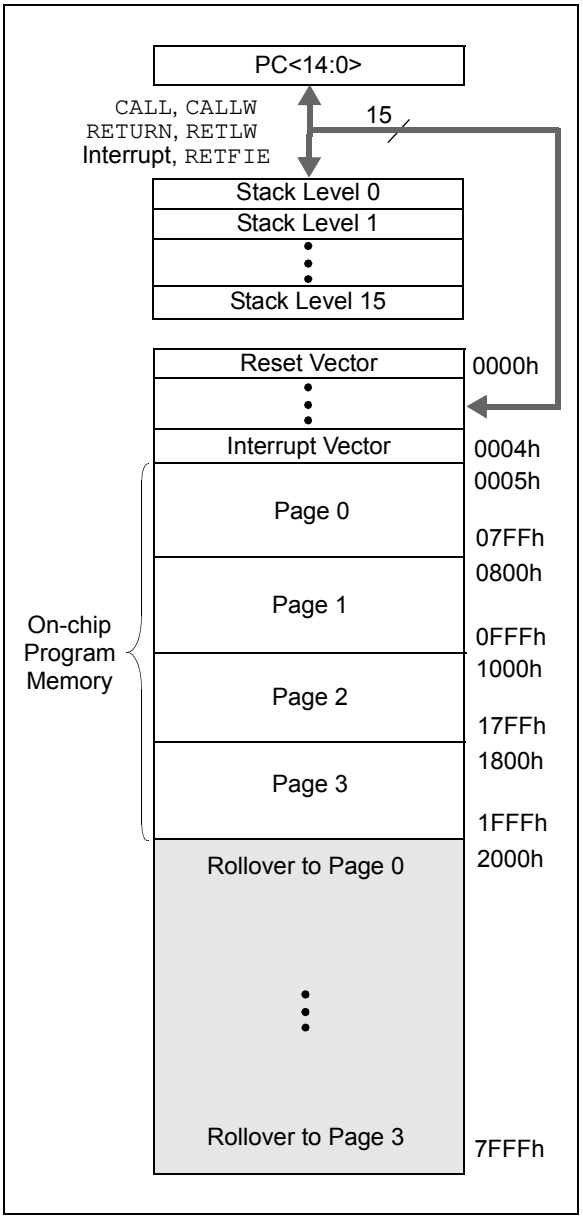


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16LF1906/7



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3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constants
    MOVWF   FSR1H
    MOVIW 0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.5 "Indirect Addressing"** for more information.

Data memory uses a 12-bit address. The upper seven bits of the address define the Bank Address and the lower five bits select the registers/RAM in that bank.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-4.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

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3.2.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '`000u u1uu`' (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 21.0 "Instruction Set Summary"**).

Note: The C and DC bits operate as $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bits, respectively, in subtraction.

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Digit\ Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

3.2.2 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.2.3 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

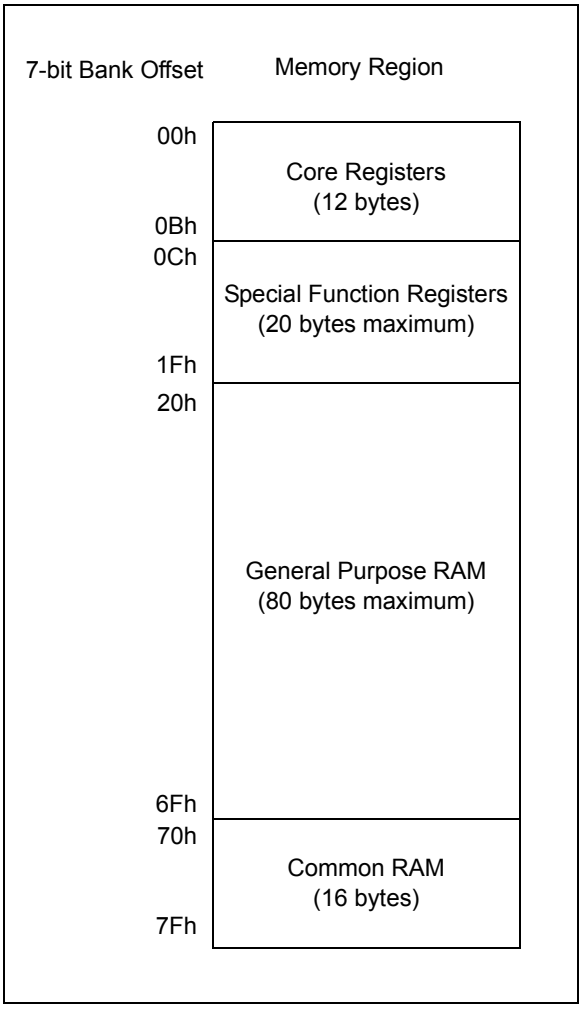
3.2.3.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.5.2 "Linear Data Memory"** for more information.

3.2.4 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-3: BANKED MEMORY PARTITIONING



3.2.5 DEVICE MEMORY MAPS

The memory maps for PIC16LF1904/6/7 are as shown in Table 3-3.

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TABLE 3-3: PIC16LF1904/6/7 MEMORY MAP

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	—	28Ch	—	30Ch	—	38Ch	—
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	—	30Dh	—	38Dh	—
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	—	20Eh	—	28Eh	—	30Eh	—	38Eh	—
00Fh	PORTD(1)	08Fh	TRISD(1)	10Fh	LATD(1)	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	PORTE	090h	TRISE(1)	110h	LATE(1)	190h	ANSELE(1)	210h	WPUE	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	—	191h	PMADRL	211h	—	291h	—	311h	—	391h	—
012h	PIR2	092h	PIE2	112h	—	192h	PMADRH	212h	—	292h	—	312h	—	392h	—
013h	—	093h	—	113h	—	193h	PMDATL	213h	—	293h	—	313h	—	393h	—
014h	—	094h	—	114h	—	194h	PMDATH	214h	—	294h	—	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	—	195h	PMCON1	215h	—	295h	—	315h	—	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	—	296h	—	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	—	217h	—	297h	—	317h	—	397h	—
018h	T1CON	098h	—	118h	—	198h	—	218h	—	298h	—	318h	—	398h	—
019h	T1GCON	099h	OSCCON	119h	—	199h	RCREG	219h	—	299h	—	319h	—	399h	—
01Ah	—	09Ah	OSCSTAT	11Ah	—	19Ah	TXREG	21Ah	—	29Ah	—	31Ah	—	39Ah	—
01Bh	—	09Bh	ADRESL	11Bh	—	19Bh	SPBRG	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	—	09Ch	ADRESH	11Ch	—	19Ch	SPBRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	—	19Dh	RCSTA	21Dh	—	29Dh	—	31Dh	—	39Dh	—
01Eh	—	09Eh	ADCON1	11Eh	—	19Eh	TXSTA	21Eh	—	29Eh	—	31Eh	—	39Eh	—
01Fh	—	09Fh	—	11Fh	—	19Fh	BAUDCON	21Fh	—	29Fh	—	31Fh	—	39Fh	—
020h	General Purpose Register 96 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes(2)	220h	General Purpose Register 80 Bytes(2)	2A0h	General Purpose Register 80 Bytes(2)	320h	General Purpose Register 32 Bytes(2)	3A0h	Unimplemented Read as '0'
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		36Fh	Unimplemented Read as '0'	3EFh	
070h		0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	370h	Accesses 70h – 7Fh	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: PIC16LF1904/7 only.

2: PIC16LF1906/7 only.

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TABLE 3-3: PIC16LF1904/6/7 MEMORY MAP (CONTINUED)

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14	
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)
40Bh		48Bh		50Bh		58Bh		60Bh		68Bh		70Bh	
40Ch	Unimplemented Read as '0'	48Ch	Unimplemented Read as '0'	50Ch	Unimplemented Read as '0'	58Ch	Unimplemented Read as '0'	60Ch	Unimplemented Read as '0'	68Ch	Unimplemented Read as '0'	70Ch	Unimplemented Read as '0'
46Fh		4EFh		56Fh		5EFh		66Fh		6EFh		76Fh	
470h	Common RAM (Accesses 70h – 7Fh)	4F0h	Common RAM (Accesses 70h – 7Fh)	570h	Common RAM (Accesses 70h – 7Fh)	5F0h	Common RAM (Accesses 70h – 7Fh)	670h	Common RAM (Accesses 70h – 7Fh)	6F0h	Common RAM (Accesses 70h – 7Fh)	770h	Common RAM (Accesses 70h – 7Fh)
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh	

BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23	
800h	Core Registers (Table 3-2)	880h	Core Registers (Table 3-2)	900h	Core Registers (Table 3-2)	980h	Core Registers (Table 3-2)	A00h	Core Registers (Table 3-2)	A80h	Core Registers (Table 3-2)	B00h	Core Registers (Table 3-2)	B80h	Core Registers (Table 3-2)
80Bh		88Bh		90Bh		98Bh		A0Bh		A8Bh		B0Bh		B8Bh	
80Ch	Unimplemented Read as '0'	88Ch	Unimplemented Read as '0'	90Ch	Unimplemented Read as '0'	98Ch	Unimplemented Read as '0'	A0Ch	Unimplemented Read as '0'	A8Ch	Unimplemented Read as '0'	B0Ch	Unimplemented Read as '0'	B8Ch	Unimplemented Read as '0'
86Fh		8EFh		96Fh		9EFh		A6Fh		AEFh		B6Fh		BEFh	
870h	Common RAM (Accesses 70h – 7Fh)	8F0h	Common RAM (Accesses 70h – 7Fh)	970h	Common RAM (Accesses 70h – 7Fh)	9F0h	Common RAM (Accesses 70h – 7Fh)	A70h	Common RAM (Accesses 70h – 7Fh)	AF0h	Common RAM (Accesses 70h – 7Fh)	B70h	Common RAM (Accesses 70h – 7Fh)	BF0h	Common RAM (Accesses 70h – 7Fh)
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	

BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30	
C00h	Core Registers (Table 3-2)	C80h	Core Registers (Table 3-2)	D00h	Core Registers (Table 3-2)	D80h	Core Registers (Table 3-2)	E00h	Core Registers (Table 3-2)	E80h	Core Registers (Table 3-2)	F00h	Core Registers (Table 3-2)
C0Bh		C8Bh		D0Bh		D8Bh		E0Bh		E8Bh		F0Bh	
C0Ch	Unimplemented Read as '0'	C8Ch	Unimplemented Read as '0'	D0Ch	Unimplemented Read as '0'	D8Ch	Unimplemented Read as '0'	E0Ch	Unimplemented Read as '0'	E8Ch	Unimplemented Read as '0'	F0Ch	Unimplemented Read as '0'
C6Fh		CEFh		D6Fh		DEFh		E6Fh		EEFh		F6Fh	
C70h	Common RAM (Accesses 70h – 7Fh)	CF0h	Common RAM (Accesses 70h – 7Fh)	D70h	Common RAM (Accesses 70h – 7Fh)	DF0h	Common RAM (Accesses 70h – 7Fh)	E70h	Common RAM (Accesses 70h – 7Fh)	EF0h	Common RAM (Accesses 70h – 7Fh)	F70h	Common RAM (Accesses 70h – 7Fh)
C7Fh		CFFh		D7Fh		DFFh		E7Fh		EFFh		F7Fh	

Legend: = Unimplemented data memory locations, read as '0'

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TABLE 3-3: PIC16LF1904/6/7 MEMORY MAP (CONTINUED)

	BANK 15		BANK 31
780h	Core Registers (Table 3-2)	F80h	Core Registers (Table 3-2)
78Bh		F8Bh	
78Ch	Unimplemented Read as '0'	F8Ch	Unimplemented Read as '0'
790h		FE3h	
791h	LCDCON	FE4h	STATUS_SHAD
792h	LCDPS	FE5h	WREG_SHAD
793h	LCDREF	FE6h	BSR_SHAD
794h	LCDCST	FE7h	PCLATH_SHAD
795h	LCDRL	FE8h	FSR0L_SHAD
796h	—	FE9h	FSR0H_SHAD
797h	—	FEAh	FSR1L_SHAD
798h	LCDSE0	FEBh	FSR1H_SHAD
799h	LCDSE1	FECh	—
79Ah	LCDSE2(1)	FEDh	STKPTR
79Bh	LCDSE3	FEEh	TOSL
79Ch	Unimplemented Read as '0'	FEFh	TOSH
79Fh		FF0h	Common RAM (Accesses 70h – 7Fh)
7A0h	LCDDATA0	FFFh	
7A1h	LCDDATA1		
7A2h	LCDDATA2(1)		
7A3h	LCDDATA3		
7A4h	LCDDATA4		
7A5h	LCDDATA5(1)		
7A6h	LCDDATA6		
7A7h	LCDDATA7		
7A8h	LCDDATA8(1)		
7A9h	LCDDATA9		
7AAh	LCDDATA10		
7ABh	LCDDATA11(1)		
7ACh	LCDDATA12		
7ADh	—		
7AEh	—		
7AFh	LCDDATA15		
7B0h	—		
7B1h	—		
7B2h	LCDDATA18		
7B3h	—		
7B4h	—		
7B5h	LCDDATA21		
7B6h	—		
7B7h	—		
7B8h	Unimplemented Read as '0'		
7EFh			

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: PIC16LF1904/7 only.