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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## 5 Amp Gate Drive Optocoupler in 11-mm SSO8 Package with 100 kV/ $\mu$ s Noise Immunity

### Data Sheet

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#### Description

The Broadcom® ACNU-3430 is a 5A gate drive optocoupler device in the 11-mm SSO8 package designed for high voltage, space-constrained industrial applications, including motor drives and solar inverters. This package platform features wide 11-mm creepage and 10.5-mm clearance, high insulation voltage of  $V_{IORM} = 1414 V_{PEAK}$  and a compact package footprint, 40 percent smaller than the 400-mil DIP-8 package. The ACNU-3430 has common mode transient immunity (CMTI) greater than 100 kV/ $\mu$ s and a propagation delay faster than 150 ns, enabling high frequency switching to improve efficiency in driving IGBT and SiC/GaN MOSFET.

**CAUTION** Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that might be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

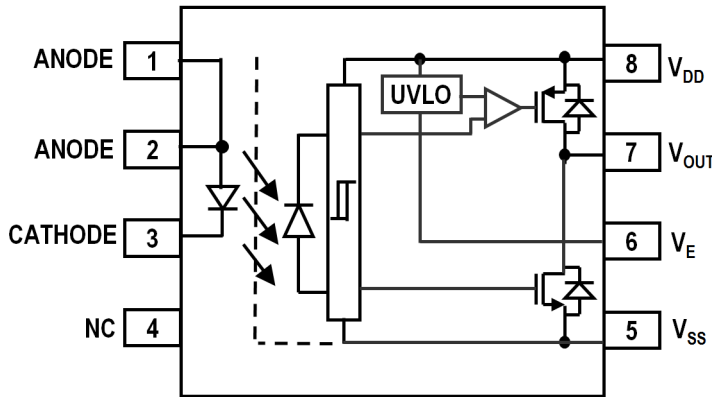
#### Features

- 5.0A maximum peak output current
- 11-mm creepage and 10.5-mm clearance
- Rail-to-rail output voltage
- UVLO with  $V_E$  reference for negative power supply
- 150-ns maximum propagation delay
- 90-ns maximum propagation delay difference
- LED current input with hysteresis
- 100-kV/ $\mu$ s minimum Common Mode Rejection (CMR) at  $V_{CM} = 1500V$
- $I_{DD} = 5.0$  mA maximum supply current
- Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- Wide operating  $V_{DD}$  range: 15V to 30V
- Industrial temperature range:  $-40^{\circ}C$  to  $110^{\circ}C$
- Pending safety approvals:
  - UL Recognized 5000  $V_{RMS}$  for 1min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5  $V_{IORM} = 1414 V_{peak}$

#### Applications

- IGBT/MOSFET gate drives
- AC and brushless DC motor drives
- Renewable energy inverters
- Industrial inverters
- Switching power supplies

**Figure 1 Functional Diagram**



**Design Notes:** A 1- $\mu$ F bypass capacitor must be connected between pins  $V_{DD}$  and  $V_{SS}$ .

**Table 1 Truth Table – ACNU-3430**

LED	$V_{DD} - V_{SS}$ POSITIVE GOING (i.e., TURN-ON)	$V_{DD} - V_{SS}$ NEGATIVE GOING (i.e., TURN-OFF)	VO
OFF	0V to 30V	0V to 30V	LOW
ON	0V to 11.9V	0V to 10.9V	LOW
ON	11.9V to 13.2V	10.9V to 12.2V	TRANSITION
ON	13.2V to 30V	12.2V to 30V	HIGH

## Ordering Information

ACNU-3430 is UL Recognized with 5000  $V_{RMS}$  for 1 minute per UL1577.

**Table 2 Ordering Information**

Part Number	Option	Package	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant				
ACNU-3430	-000E	11-mm SSO8		X	80 per tube
	-500E		X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

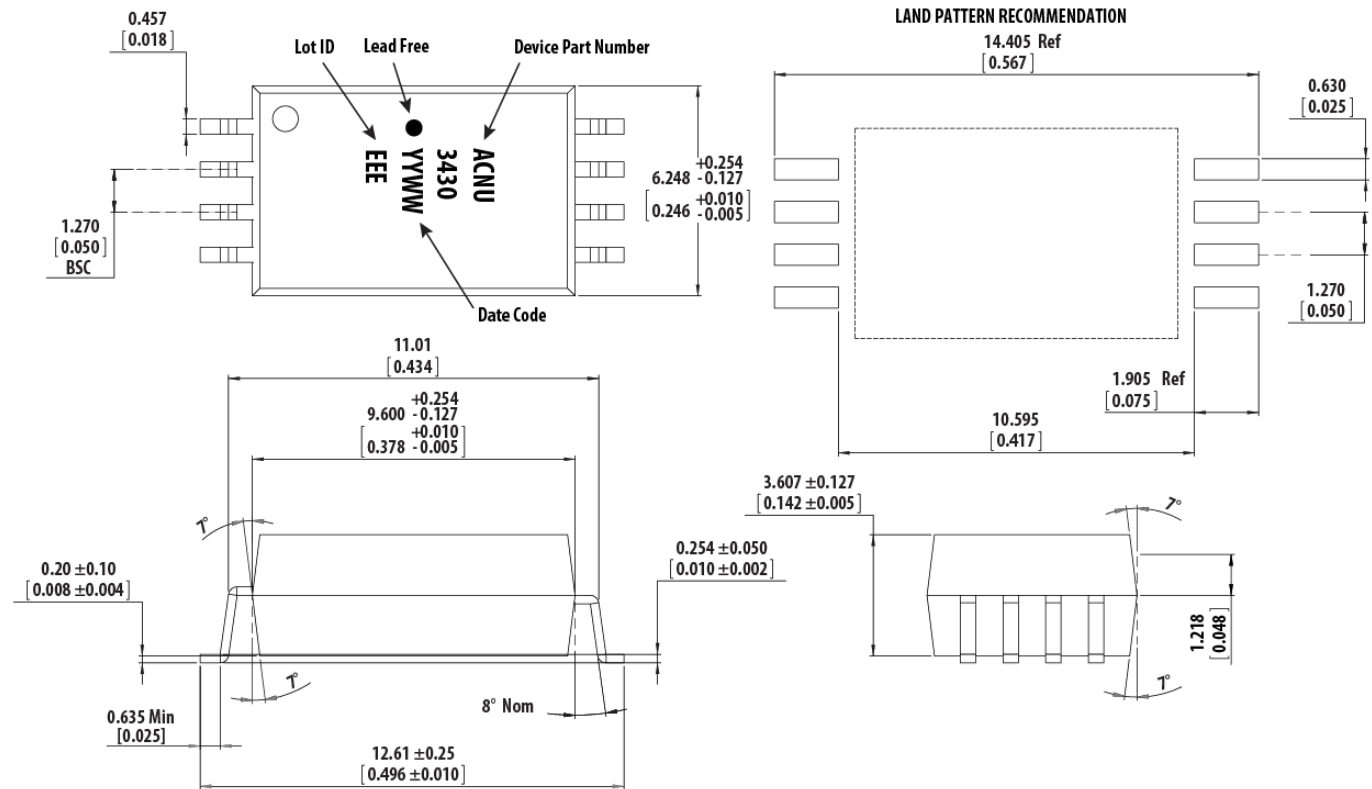
Example:

ACNU-3430-500E to order the product in tape and reel packaging with IEC/EN/DIN EN 60747-5-5 safety approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

## Package Outline Drawings

Figure 2 ACNU-3430 Outline Drawing (11-mm SSO8 Package)



Lead Coplanarity = 0.10mm (0.004 inches)  
 Dimensions in mm [inch]  
 Maximum mold flash on each side 0.127mm [0.005]  
 Note: Floating lead protrusion is 0.15mm [0.006] Max if applicable

## Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

## Regulatory Information

The ACNU-3430 is pending approval by the following organizations.

<b>UL</b>	Recognized under UL 1577, component recognition program up to $V_{ISO} = 5000 V_{RMS}$ , File E55361
<b>CSA</b>	CSA Component Acceptance Notice #5, File CA 88324
<b>IEC/EN/DIN EN 60747-5-5</b>	Maximum Working Insulation Voltage $V_{IORM} = 1414 V_{peak}$



## Insulation Characteristics

**Table 3 IEC/EN/DIN EN 60747-5-5 Insulation Characteristics**

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage $\leq 600 V_{RMS}$ for rated mains voltage $\leq 1000 V_{RMS}$		I – IV I – III	
Climatic Classification		40/110/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	1414	$V_{peak}$
Input to Output Test Voltage, Method b <sup>a</sup> $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial discharge $< 5$ pC	$V_{PR}$	2652	$V_{peak}$
Input to Output Test Voltage, Method a <sup>a</sup> $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10$ sec, Partial discharge $< 5$ pC	$V_{PR}$	2262	$V_{peak}$
Highest Allowable Overvoltage <sup>a</sup> (Transient Overvoltage $t_{ini} = 60$ sec)	$V_{IOTM}$	8000	$V_{peak}$
Safety-Limiting Values – maximum values allowed in the event of a failure <sup>b</sup> (see Note 2). Case Temperature Input Current Output Power	$T_S$ $I_{S, INPUT}$ $P_{S, OUTPUT}$	175 230 600	$^{\circ}C$ mA mW
Insulation Resistance at $T_S, V_{IO} = 500V$	$R_S$	$>10^9$	$\Omega$

- a. Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the *Avago Regulatory Guide to Isolation Circuits*, AV02-2041EN for a detailed description of Method a and Method b partial discharge test profiles.
- b. These optocouplers are suitable for *safe electrical isolation* only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

## Insulation and Safety-Related Specifications

**Table 4 Insulation and Safety Related Specifications**

Parameter	Symbol	ACNU-3430	Unit	Conditions
Minimum External Air Gap (Clearance)	L(101)	10.5	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	11.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>300	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1).

**NOTE** All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended Land Pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques, such as grooves and ribs, that may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors, such as pollution degree and insulation level.

## Absolute Maximum Ratings

**Table 5 Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	$T_S$	-55	125	°C	
Operating Temperature	$T_A$	-40	110	°C	
Average Input Current	$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (<1 ms pulse width, 300pps)	$I_{F(TRAN)}$	—	1	A	
Reverse Input Voltage	$V_R$	—	5	V	
High Peak Output Current	$I_{OH(PEAK)}$	—	5.0	A	b
Low Peak Output Current	$I_{OL(PEAK)}$	—	5.0	A	b
Total Output Supply Voltage	$(V_{DD} - V_{SS})$	-0.5	35	V	
Negative Output Supply Voltage	$(V_E - V_{SS})$	-0.5	15	V	
Positive Output Supply Voltage	$(V_{DD} - V_E)$	-0.5	$35 - (V_E - V_{SS})$	V	
Output Voltage	$V_{O(PEAK)}$	-0.5	$V_{DD}$	V	
Output IC Power Dissipation	$P_O$	—	500	mW	c
Total Power Dissipation	$P_T$	—	550	mW	d

- a. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.
- b. Maximum pulse width = 10  $\mu$ s. This value is intended to allow for component tolerances for designs with  $I_O$  peak minimum = 4A. See the [Application Information](#) section for additional details on limiting  $I_{OH}$  peak.
- c. Derate linearly above 85°C free-air temperature at a rate of 12.5 mW/°C.
- d. Derate linearly above 85°C free-air temperature at a rate of 13.75 mW/°C. The maximum LED junction temperature should not exceed 125°C.

## Recommended Operating Conditions

**Table 6 Recommended Operating Conditions**

Parameter	Symbol	Min	Max.	Unit	Note
Operating Temperature	$T_A$	-40	110	°C	
Output Supply Voltage	$(V_{DD} - V_{SS})$	15	30	V	
Negative Output Supply Voltage	$(V_E - V_{SS})$	0	15	V	
Positive Output Supply Voltage	$(V_{DD} - V_E)$	15	$30 - (V_E - V_{SS})$	V	
Input Current (ON)	$I_{F(ON)}$	7	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.5	V	

## Electrical Specifications (DC)

All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} - V_E = 15\text{V}$ ,  $V_E - V_{SS} = 15\text{V}$ . All minimum and maximum specifications are at recommended operating conditions ( $T_A = -40^\circ\text{C}$  to  $110^\circ\text{C}$ ,  $I_{F(ON)} = 7\text{ mA}$  to  $12\text{ mA}$ ,  $V_{F(OFF)} = -3.6\text{ V}$  to  $0.5\text{ V}$ ,  $V_{DD} - V_E = 15\text{V}$ ,  $V_E - V_{SS} = 15\text{V}$ ), unless otherwise noted.

**Table 7 Electrical Specifications (DC)**

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Peak Output Current	$I_{OH}$	-4.0	-7.5	—	A	$V_{DD} - V_O = 15$	4, 5	a
Low Level Peak Output Current	$I_{OL}$	4.0	6.2	—	A	$V_O - V_{SS} = 15$	7, 8	a
High Output Transistor RDS(ON)	$R_{DS,OH}$	0.5	0.9	2.1	$\Omega$	$I_{OH} = 4\text{ A}$	9	b
Low Output Transistor RDS(ON)	$R_{DS,OL}$	0.2	0.65	1.3	$\Omega$	$I_{OL} = -4\text{ A}$	10	b
High Level Output Voltage	$V_{OH}$	$V_{DD} - 0.3$	$V_{DD} - 0.08$	—	V	$I_O = -100\text{ mA}$	3	c, d
High Level Output Voltage	$V_{OH}$	—	$V_{DD}$	—	V	$I_O = 0\text{ mA}$ , $I_F = 10\text{ mA}$		
Low Level Output Voltage	$V_{OL}$	—	0.05	0.25	V	$I_O = 100\text{ mA}$	6	
High Level Output Supply Current ( $V_{DD}$ )	$I_{DDH}$	—	3	5	mA	$I_F = 10\text{ mA}$	11	
Low Level Output Supply Current ( $V_{DD}$ )	$I_{DDL}$	—	3	5	mA	$V_F = 0\text{V}$	11	
$V_E$ High Level Output Supply Current	$I_{EH}$	-1.3	-0.7	—	mA	$I_F = 10\text{ mA}$	12	
$V_E$ Low Level Output Supply Current	$I_{EL}$	-1.0	-0.65	—	mA	$V_F = 0\text{V}$	12	
Threshold Input Current Low to High	$I_{FLH}$	0.50	2	6	mA	$V_O > 5\text{V}$	13	
Threshold Input Voltage High to Low	$V_{FHL}$	0.5	—	—	V			
Input Forward Voltage	$V_F$	1.20	1.45	1.85	V	$I_F = 10\text{ mA}$	17	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F / \Delta T_A$	—	-1.5	—	mV/ $^\circ\text{C}$	$I_F = 10\text{ mA}$		
Input Reverse Breakdown Voltage	$BV_R$	5	—	—	V	$I_R = 100\text{ mA}$		
Input Capacitance	$C_{IN}$	—	23	—	pF	$f = 1\text{ MHz}$ , $V_F = 0\text{V}$		
UVLO Threshold	$V_{UVLO+}$	11.9	12.6	13.2	V	$V_O > 5\text{V}$ , $I_F = 10\text{ mA}$		
	$V_{UVLO-}$	10.9	11.6	12.2				
UVLO Hysteresis	$UVLO_{HYS}$	—	1.0	—	V			

- Maximum pulse width = 10 ms.
- Output is sourced at  $-4.0\text{A}/4.0\text{A}$  with a maximum pulse width = 10  $\mu\text{s}$ .
- In this test,  $V_{OH}$  is measured with a DC load current. When driving capacitive loads,  $V_{OH}$  approaches  $V_{DD}$  as  $I_{OH}$  approaches zero amps.
- Maximum pulse width = 1 ms.



## Switching Specifications (AC)

All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} - V_E = 15\text{V}$ ,  $V_E - V_{SS} = 15\text{V}$ . All minimum and maximum specifications are at recommended operating conditions ( $T_A = -40^\circ\text{C}$  to  $110^\circ\text{C}$ ,  $I_{F(ON)} = 7\text{ mA}$  to  $12\text{ mA}$ ,  $V_{F(OFF)} = -3.6\text{V}$  to  $0.5\text{V}$ ,  $V_{DD} - V_E = 15\text{V}$ ,  $V_E - V_{SS} = 15\text{V}$ ), unless otherwise noted.

**Table 8 Switching Specifications (AC)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	$t_{PLH}$	50	75	150	ns	$R_G = 7.5\ \Omega$ , $C_G = 25\ \text{nF}$ , $f = 10\ \text{kHz}$ , Duty Cycle = 50%, $I_F = 10\ \text{mA}$ ,	14, 15, 18	
Propagation Delay Time to Low Output Level	$t_{PHL}$	50	70	150	ns			
Pulse Width Distortion	PWD	—	—	80	ns		18	a
Propagation Delay Difference Between Any Two Parts	PDD ( $t_{PHL} - t_{PLH}$ )	-90	—	90	ns		18	b
Propagation Delay Skew	$t_{PSK}$	—	—	80	ns		18	c
Rise Time	$t_R$	—	20	50	ns		16, 18	
Fall Time	$t_F$	—	10	30	ns			
Output High Level Common Mode Transient Immunity	$ CM_H $	100	—	—	kV/ $\mu\text{s}$	$T_A = 25^\circ\text{C}$ , $I_F = 10\ \text{mA}$ , $V_{CM} = 1500\text{V}$ ,	19	d, e
Output Low Level Common Mode Transient Immunity	$ CM_L $	100	—	—	kV/ $\mu\text{s}$	$T_A = 25^\circ\text{C}$ , $V_E = 0\text{V}$ , $V_{CM} = 1500\text{V}$		d, f

- Pulse Width Distortion (PWD) is defined as  $|t_{PHL} - t_{PLH}|$  for any given device.
- The difference between  $t_{PHL}$  and  $t_{PLH}$  between any two ACNU-3430 parts under the same test condition.
- $t_{PSK}$  is equal to the worst-case difference in  $t_{PHL}$  or  $t_{PLH}$  that will be seen between units at any given temperature and specified test conditions.
- Pin 1 and 4 need to be connected to LED common. Split resistor network in the ratio 1:1.5 with  $150\ \Omega$  at the anode and  $200\ \Omega$  at the cathode.
- Common mode transient immunity in the high state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output remains in the high state (i.e.,  $V_O > 15.0\text{V}$ ).
- Common mode transient immunity in a low state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output remains in a low state (i.e.,  $V_O < 1.0\text{V}$ ).

## Package Characteristics

All typical values are at  $T_A = 25^\circ\text{C}$ . All minimum/maximum specifications are at recommended operating conditions, unless otherwise noted.

**Table 9 Package Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	$V_{ISO}$	5000	—	—	$V_{RMS}$	$RH < 50\%$ , $t = 1\ \text{min.}$ , $T_A = 25^\circ\text{C}$		a, b
Input-Output Resistance	$R_{I-O}$	—	$10^{12}$	—	$\Omega$	$V_{I-O} = 500\ \text{V}_{DC}$		b
Input-Output Capacitance	$C_{I-O}$	—	0.5	—	pF	$f = 1\ \text{MHz}$		

- In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 6000\ \text{V}_{RMS}$  for 1 second (leakage detection current limit,  $I_{I-O} \leq 5\ \mu\text{A}$ ).
- The device is considered to be a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

Figure 3  $V_{OH}$  vs. Temperature

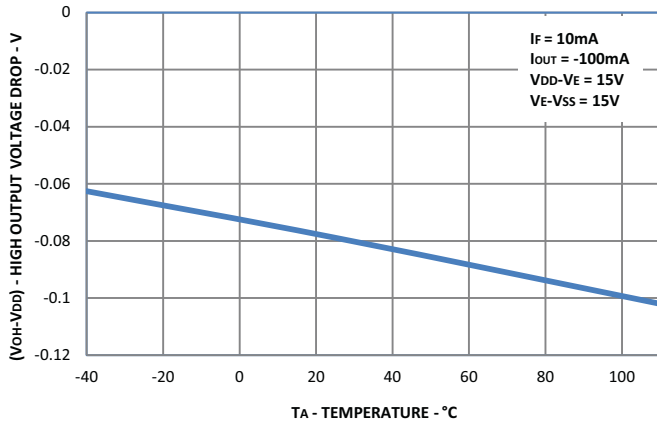


Figure 4  $I_{OH}$  vs. Temperature

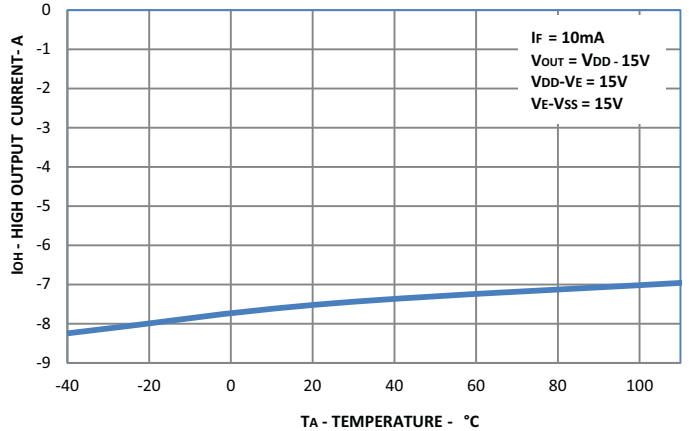


Figure 5  $I_{OH}$  vs.  $V_{OH}$

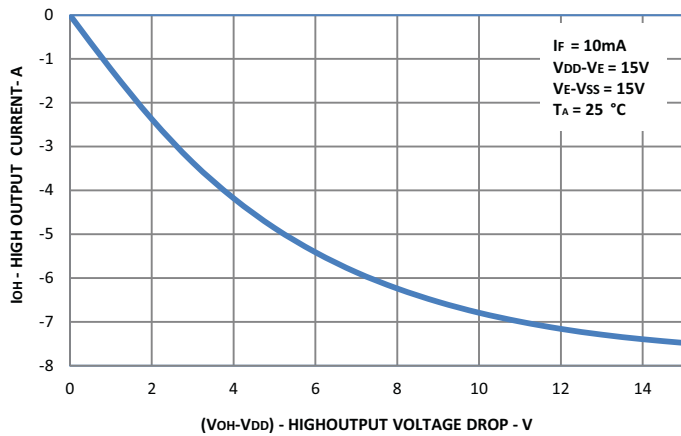


Figure 6  $V_{OL}$  vs. Temperature

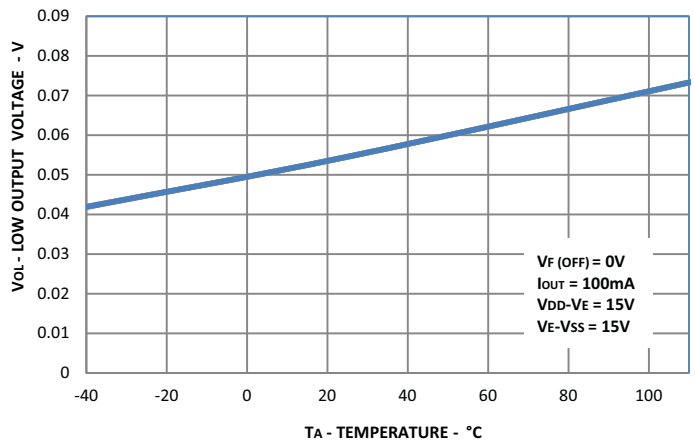


Figure 7  $I_{OL}$  vs. Temperature

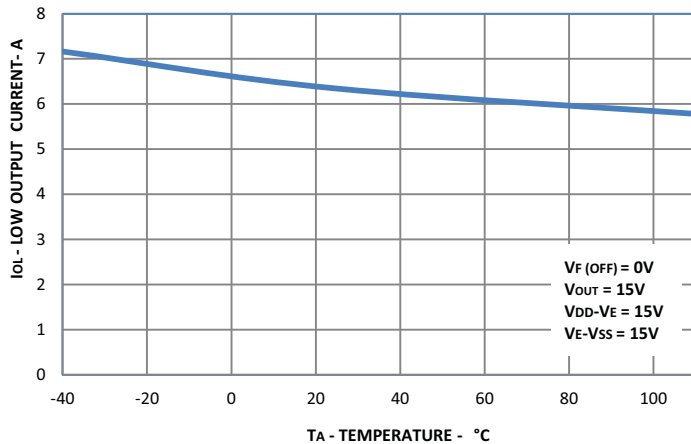


Figure 8  $I_{OL}$  vs.  $V_{OL}$

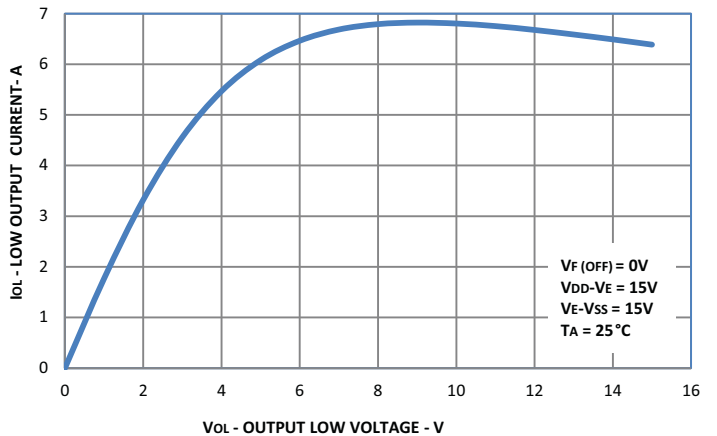


Figure 9  $R_{DS,OH}$  vs. Temperature

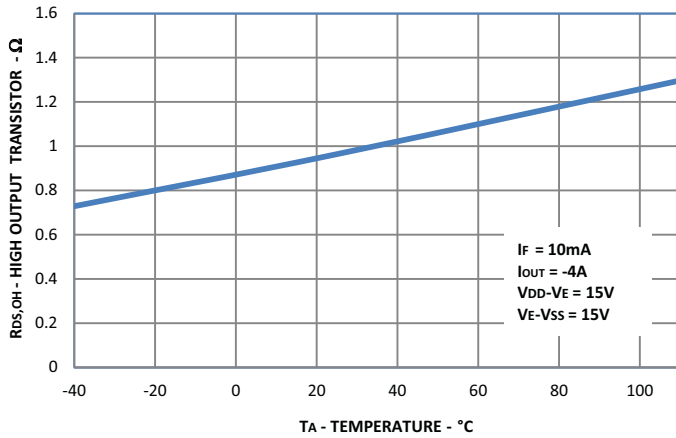


Figure 10  $R_{DS,OL}$  vs. Temperature

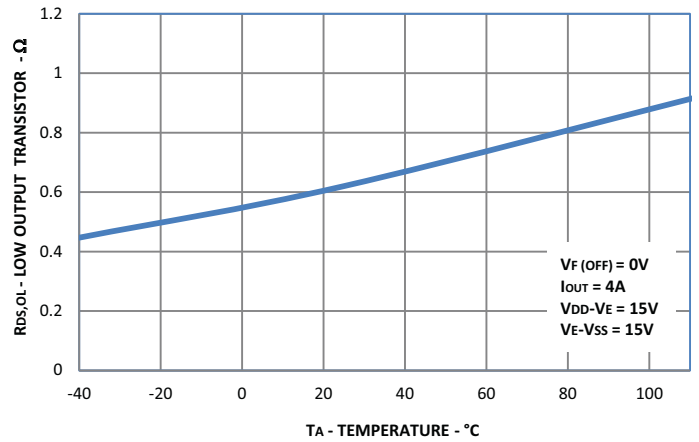


Figure 11  $I_{DD}$  vs. Temperature

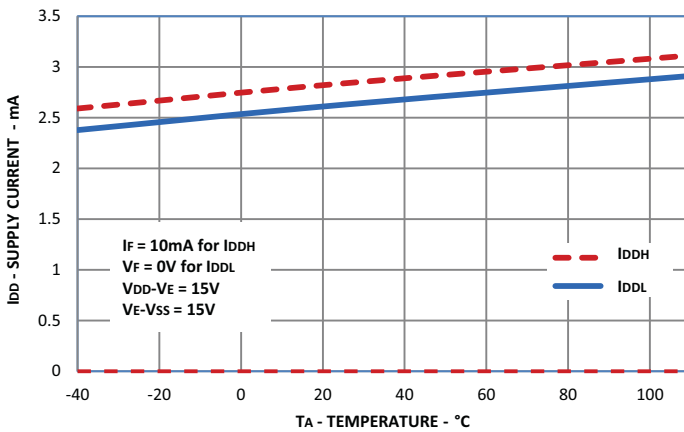


Figure 12  $I_E$  vs. Temperature

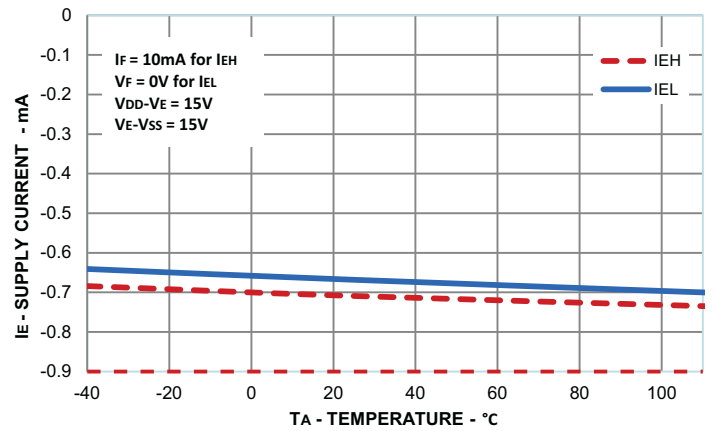


Figure 13  $I_{FLH}$  vs. Temperature

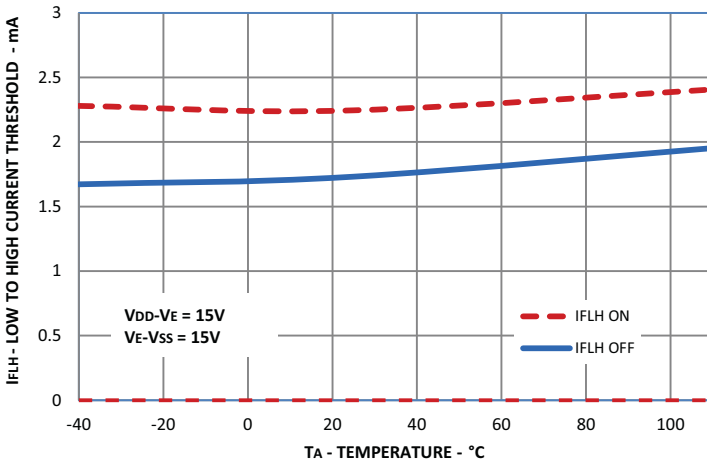


Figure 14 Propagation Delay vs.  $I_F$

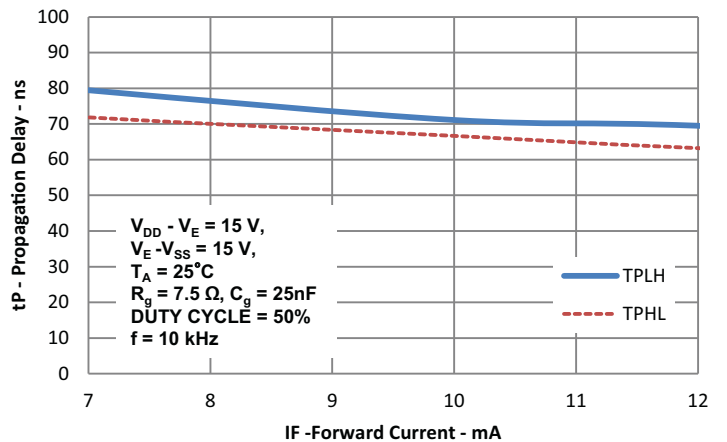


Figure 15 Propagation Delay vs. Temperature

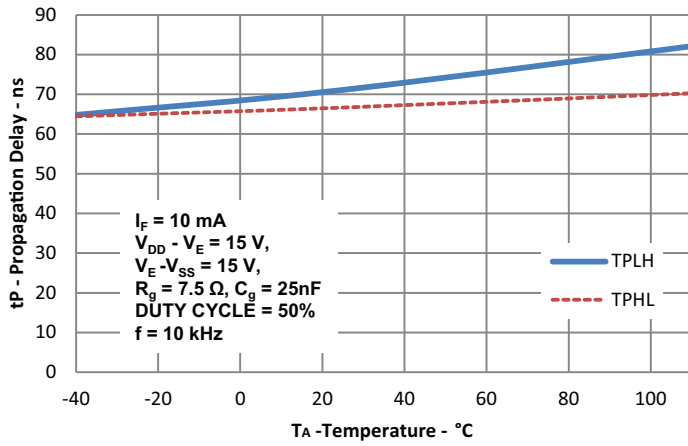


Figure 16 Rise and Fall Time vs. Temperature

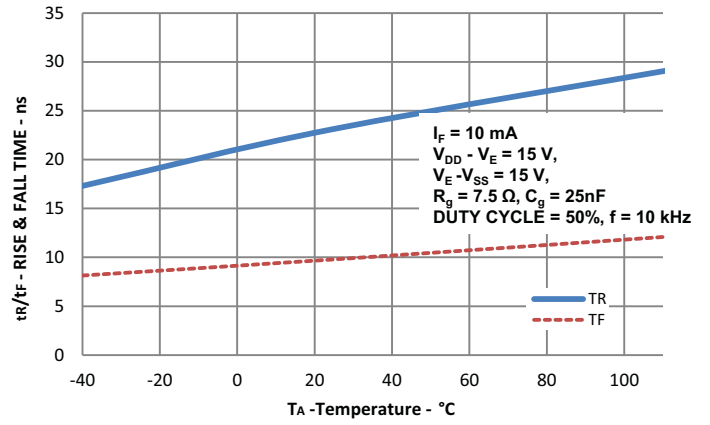
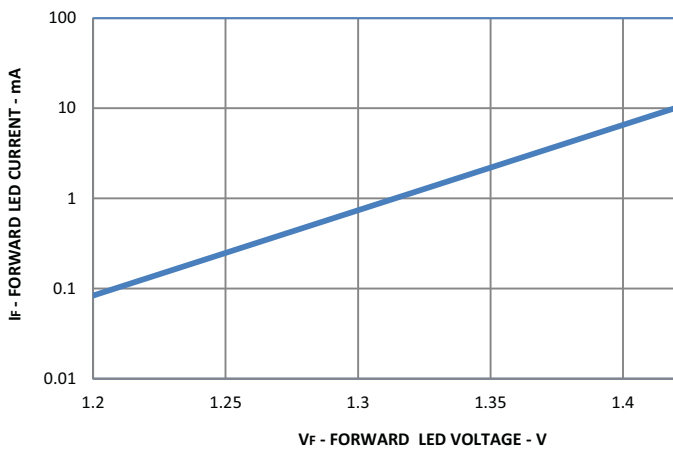
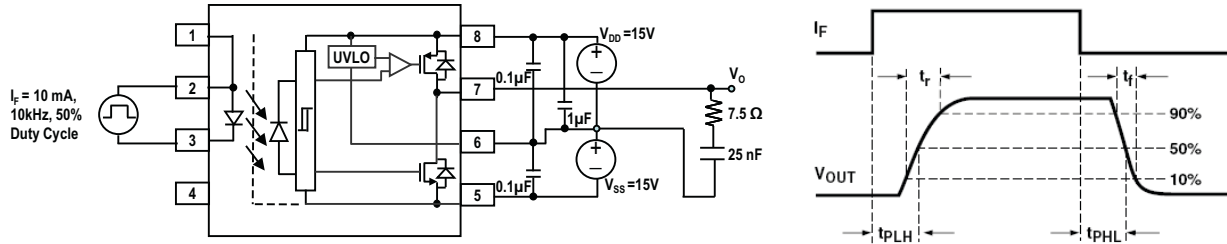


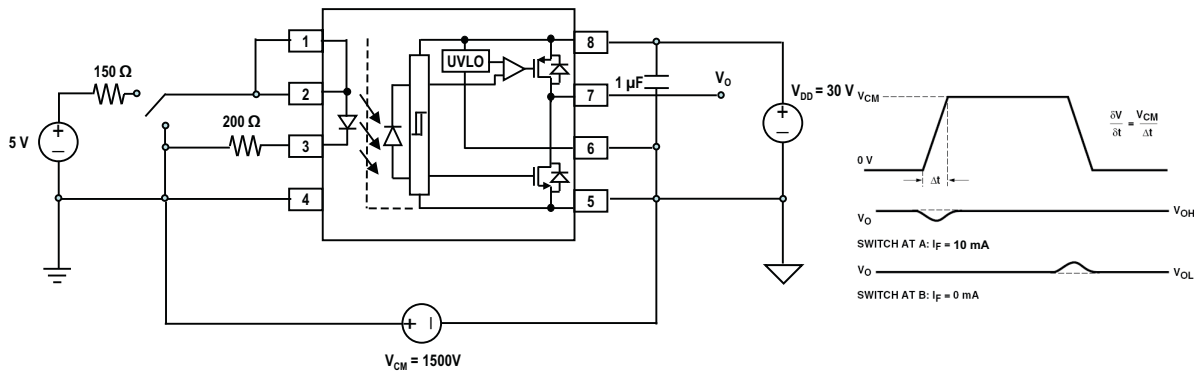
Figure 17 Input Current vs. Forward Voltage



**Figure 18**  $t_{PLH}$ ,  $t_{PHL}$ , PWD PDD,  $t_{PSK}$ ,  $t_r$ , and  $t_f$  Test Circuit and Waveforms



**Figure 19** CMR Test Circuit with Split Resistors Network and Waveforms



## Application Information

### Product Overview Description

The ACNU-3430 is an optically isolated power output stage capable of driving IGBT or power MOSFET. Based on BCDMOS technology, this gate drive optocoupler delivers higher peak output current, better rail-to-rail output voltage performance and faster speed than the previous generation products.

The high peak output current and short propagation delay are needed for fast IGBT switching to reduce dead time and improve system overall efficiency. Rail-to-rail output voltage ensures that the MOSFET's gate voltage is driven to the optimum intended level with no power loss across the MOSFET. This helps the designer lower the system power, which is suitable for bootstrap power supply operation.

The ACNU-3430 has a  $V_E$  pin that allows of use negative power supply without affecting the UVLO monitoring the positive power supply. It has very high CMR (common mode rejection) rating which allows the microcontroller and the MOSFET to operate at very large common mode noise found in industrial motor drives and other power switching applications. The input is driven by direct LED current and has a hysteresis that prevents output oscillation if insufficient LED driving current is applied. This eliminates the need of additional Schmitt trigger circuit at the input LED.

### Recommended Application Circuit

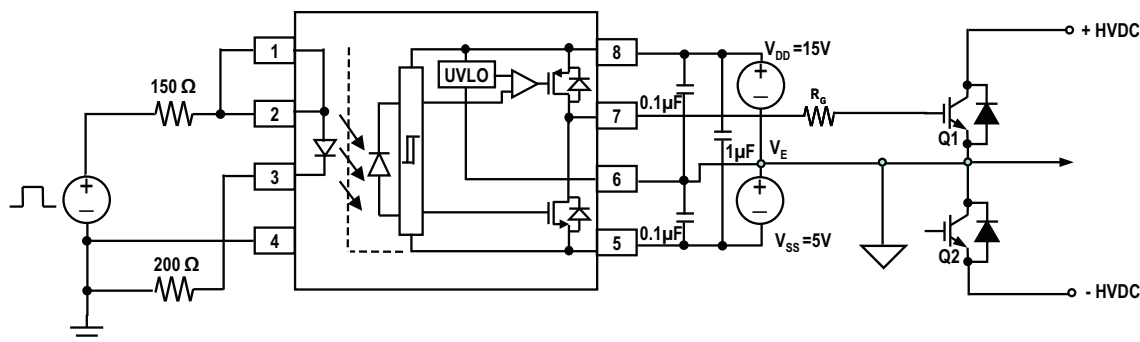
The recommended application circuit shown in [Figure 20](#) illustrates a typical gate drive implementation using the ACNU-3430.

The supply bypass capacitors provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (5.0 mA) power supply will be enough to power the device. The split resistors (in the ratio of 1:1.5) across the LED provide a high CMR response by providing a balanced resistance network across the LED. Connect pin 1 and pin 4 to LED common.

The gate resistor  $R_G$  serves to limit gate charge current and controls the IGBT switching times.

In PC board design, care should be taken to avoid routing the IGBT's collector or emitter traces close to the ACNU-3430 input as this can result in unwanted coupling of transient signals into ACNU-3430 and degrade performance.

**Figure 20 Recommended Application Circuit with Split Resistors LED Drive**





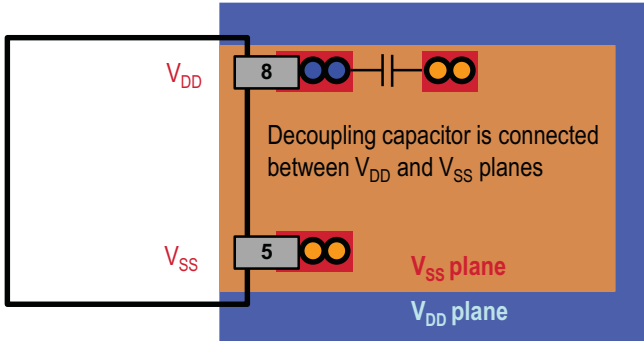
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## Recommended Supply and Ground Planes Layout

At 5A rated high current switching, decoupling capacitor must be close to  $V_{DD}$  and  $V_{SS}$  pins.

And due to the fast switching, large  $V_{DD}$  and  $V_{SS}$  planes are recommended to prevent noise by lowering the parasitic inductance.

**Figure 21 Recommended Supply and Ground Planes Layout**



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