ACNV4506

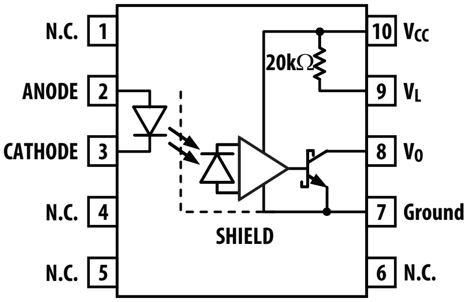
Intelligent Power Module and Gate Drive Interface Optocouplers

Data Sheet

Description

The ACNV4506 device contains a GaAsP LED optically coupled to an integrated high gain photo detector. Minimized propagation delay difference between devices makes these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time. Specifications and performance plots are given for typical IPM applications.

Functional Diagram



Note:
A 0.1 μF bypass capacitor must be connected between pins 7 and 10.

Truth Table

LED	V_O
ON	LOW
OFF	HIGH

Features

- Performance Specified for Common IPM Applications Over Industrial Temperature Range.
- Short Maximum Propagation Delays
- Minimized Pulse Width Distortion (PWD)
- Very High Common Mode Rejection (CMR)
- High CTR.
- Available in Widebody DIP10 and GulWing packages with 13.0 mm creepage and clearance.
- Safety Approval (pending):
  - UL Recognized with 7500 V_{rms} for 1 minute per UL1577.
  - CSA Approved.
  - IEC/EN/DIN EN 60747-5-2 Approved with V_{IORM} = 2262V_{peak}.

Specifications

- Wide operating temperature range: –40°C to 105°C.
- Typical propagation delay t_{PHL} = 200 ns, t_{PLH} = 350 ns
- Typical Pulse Width Distortion (PWD) = 150 ns.
- 30 kV/μs minimum common mode rejection (CMR) at V_{CM} = 1500 V.
- CTR = 90%(typ) at I_F = 10mA

Applications

- IPM Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

ACNV4506 is pending UL recognition with 7500Vrms for 1 minute per UL1577.

	Option							
Part number	**RoHS Compliant**	**Package**	**Surface Mount**	**Gull Wing**	**Tape &Reel**	**UL 7500Vrms/ 1 Minute rating**	**IEC/EN/DIN EN 60747-5-2**	**Quantity**
ACNV4506	-000E	500 mil DIP-10				X	X	35 per tube
	-300E		X	X		X	X	35 per tube
	-500E		X	X	X	X	X	500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

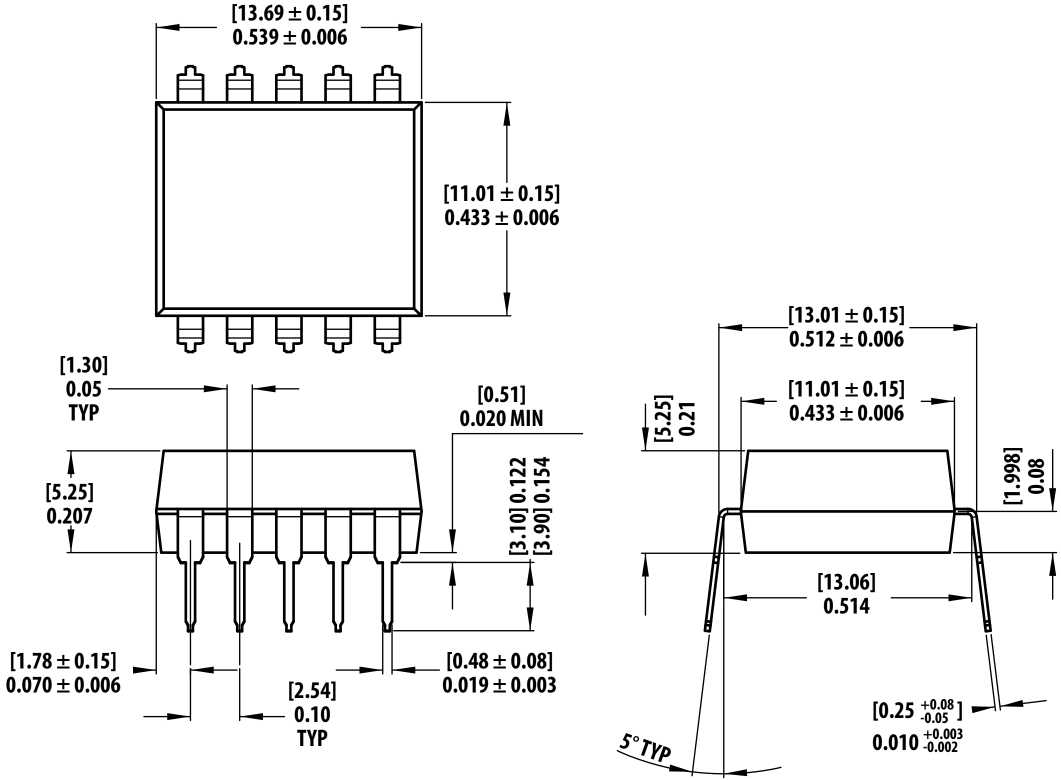
Example 1:

ACNV4506-500E to order product of 500mil DIP-10 Widebody with Gull Wing Surface Mount package in Tape and Reel packaging with both UL 7500Vrms/1min and IEC/EN/DIN EN60747-5-2 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

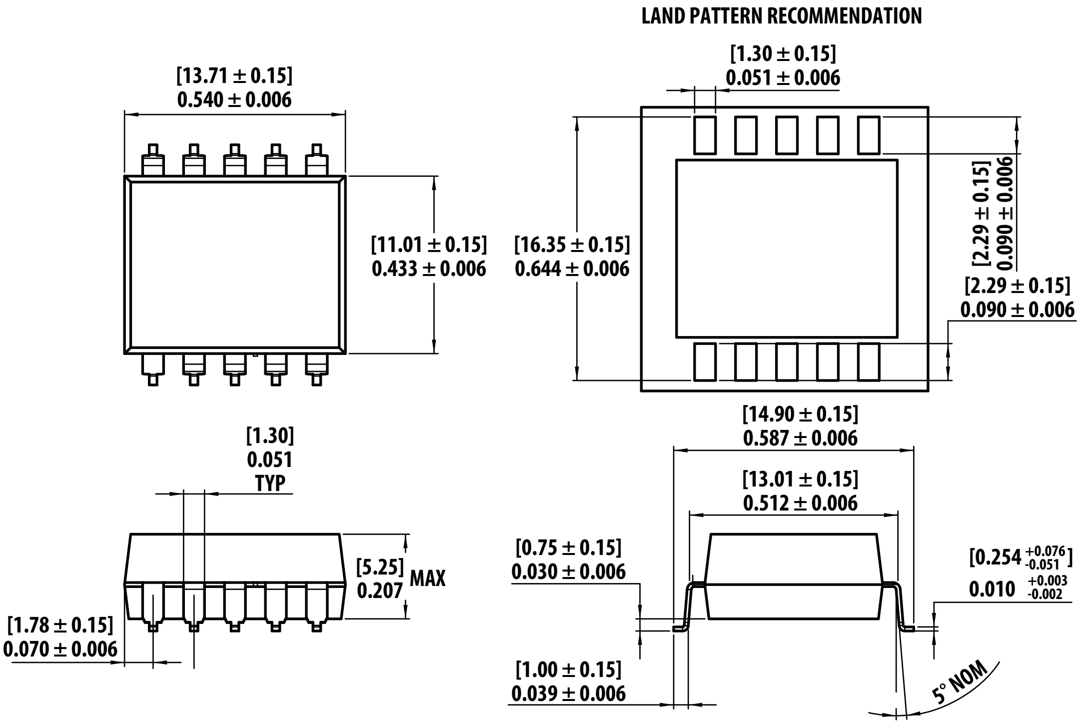
Package Outline Drawings

ACNV4506 Widebody 500Mils DIP10 Package, 13.0 mm clearance



Dimensions in Inches [Millimeters]

ACNV4506 Widebody 500Mils GulWing Tape & Reel Package, 13.0 mm clearance



Dimension in Inches [Millimeter]

Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACNV4506 is pending approval from the following organizations:

IEC

IEC/EN/DIN EN 60747-5-2:2009

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 7500 V_{RMS}. File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 1. IEC/EN/DIN EN 60747-5-2 Insulation Characteristics* (ACNV4506)

Description	Symbol	Characteristic	Unit
Climatic Classification (IEC 68 Part I)		55/105/21	
Maximum Working Insulation Voltage	V_{IORM}	2262	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	4242	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6=VPR, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	3619	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	12000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure (also see Figure 13). Case Temperature Input Current Output Power	T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$	115 400 1	°C mA W
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACNV4506	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	13.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	13.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		2	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Minimum Internal Tracking (Internal Creepage)		NA	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	$T_{storage}$	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Average Input Current	$I_{F(avg)}$		25	mA	1
Peak Input Current (50% duty cycle, <1 ms pulse width)	$I_{F(peak)}$		50	mA	2
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(tran)}$		1.0	A	
Reverse Input Voltage (Pin 3-2)	V_R		5	V	
Average Output Current (Pin 8)	$I_{O(avg)}$		15	mA	
Output Voltage (Pin 8-7)	V_O	-0.5	30		
Supply Voltage (Pin 10-7)	V_{CC}	-0.5	30		
Output Power Dissipation	P_O		100	mW	3
Total Power Dissipation	P_T		145	mW	4
Infrared and Vapor Phase Reflow Temperature	See Reflow Thermal Profile.				

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply Voltage	V_{CC}	4.5	30	V	
Output Voltage	V_O	0	30	V	
Input Current (ON)	$I_{F(on)}$	10	20	mA	
Input Voltage (OFF)	$V_{F(off)}$	-5	0.8	V	
Operating Temperature	T_A	-40	105	°C	

Table 5. Electrical Specifications

Over recommended operating conditions unless otherwise specified:
T_A = -40°C to +105°C, V_{CC} = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	44	90		%	I_F = 10 mA, V_O = 0.6 V		5
Low Level Output Current	I_{OL}	4.4	9.0		mA	I_F = 10 mA, V_O = 0.6 V	1, 2	
Low Level Output Voltage	V_{OL}		0.3	0.6	V	I_O = 2.4 mA		
Input Threshold Current	I_{TH}		1.0	5.0	mA	V_O = 0.8 V, I_O = 0.75 mA	1	9
High Level Output Current	I_{OH}		5	50	µA	V_F = 0.8 V	3	
High Level Supply Current	I_{CCH}		0.6	1.3	mA	V_F = 0.8 V, V_O = Open		9
Low Level Supply Current	I_{CCL}		0.6	1.3	mA	I_F = 10 mA, V_O = Open		9
Input Forward Voltage	V_F		1.5	1.85	V	I_F = 10 mA	4	
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		

* All typical values at 25°C, VCC = 15 V.

Table 6. Switching Specifications (RL = 20 kΩ)

Over recommended operating conditions unless otherwise specified.
T_A = -40°C to +105°C, V_{CC} = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Low Output Level	t_{PHL}	95	200	400	ns	C_L = 100 pF	$I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8 V, V_{CC} = 15.0 V, V_{THLH} = 2.0 V, V_{THHL} = 1.5 V	5, 7, 9-11	8, 9
			110		ns	C_L = 10 pF			
Propagation Delay Time to High Output Level	t_{PLH}	250	350	550	ns	C_L = 100 pF			
			200		ns	C_L = 10 pF			
Pulse Width Distortion	PWD		150	450	ns	C_L = 100 pF			13
Propagation Delay Difference Between Any 2 Parts	t_{PLH}-t_{PHL}	-150	150	450	ns				10
Output High Level Common Mode Transient immunity	$\lvert CM_H \rvert$	30	35		kV/µs	I_F = 0 mA, V_O > 3.0 V	V_{CC} = 15.0 V, C_L = 100 pF, V_{CM} = 1500 V_{P-P}, T_A = 25°C	6	11
Output Low Level Common Mode Transient immunity	$\lvert CM_L \rvert$	30	35		kV/µs	I_F = 10 mA, V_O < 1.0 V			12

* All typical values at 25°C, VCC = 15 V.

Table 7. Switching Specifications (RL = Internal Pull-up)

Over recommended operating conditions unless otherwise specified.
T_A = -40°C to +105°C, V_{CC} = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Low Output Level	t_{PHL}	95	200	400	ns		$I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8 V, V_{CC} = 15.0 V, V_{THLH} = 2.0 V, V_{THHL} = 1.5 V	8	8, 9
Propagation Delay Time to High Output Level	t_{PLH}	200	365	550	ns				
Pulse Width Distortion	PWD		165	500	ns				13
Propagation Delay Difference Between Any 2 Parts	t_{PLH}-t_{PHL}	-150	165	500	ns				10
Output High Level Common Mode Transient immunity	$\lvert CM_H \rvert$	30	35		kV/μs	I_F = 0 mA, V_O > 3.0 V	V_{CC} = 15.0 V, C_L = 100 pF, V_{CM} = 1500 V_{P-P}, T_A = 25°C	6	11
Output Low Level Common Mode Transient immunity	$\lvert CM_L \rvert$	30	35		kV/μs	I_F = 10 mA, V_O < 1.0 V			12

* All typical values at 25°C, VCC = 15 V.

Table 8. Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	7500			V_{rms}	RH < 50%, t = 1 min, T_A = 25°C		6, 7
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		6
Input-Output Capacitance	C_{I-O}		0.6		pF	Freq=1 MHz		6

Notes:

1. Derate linearly above 90°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 90°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 90°C free-air temperature at a rate of 3.0 mW/°C.
4. Derate linearly above 90°C free-air temperature at a rate of 4.2 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current (I_O) to the forward LED input current (I_F) times 100.
6. Device considered a two-terminal device: Pins 1-5 shorted together and Pins 6-10 shorted together.
7. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 7500 V_{RMS} for 1 minute (leakage detection current limit, $I_{I-O} \leq 5$ μA).
8. Pulse: f = 20 kHz, Duty Cycle = 10%.
9. Use of a 0.1 μF bypass capacitor connected between pins 7 and 10 can improve performance by filtering power supply line noise.
10. The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)
11. Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 3.0 V).
12. Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 1.0 V).
13. Pulse Width Distortion (PWD) is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.

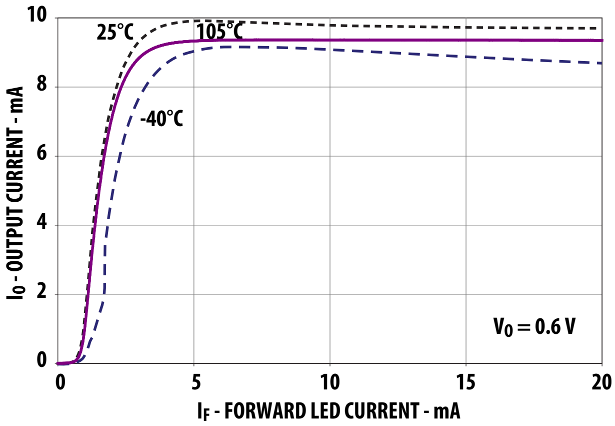


Figure 1. Typical Transfer Characteristics

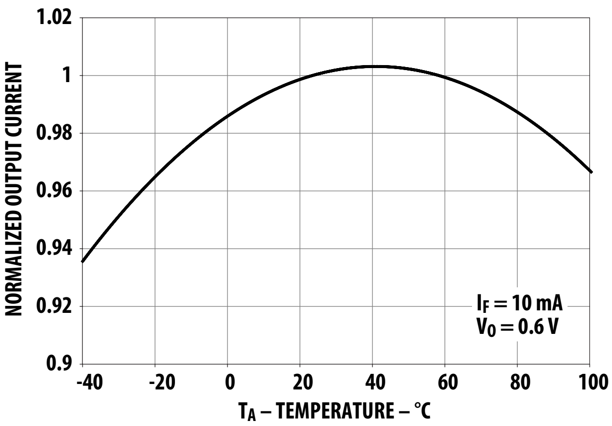


Figure 2. Normalized Output Current vs. Temperature

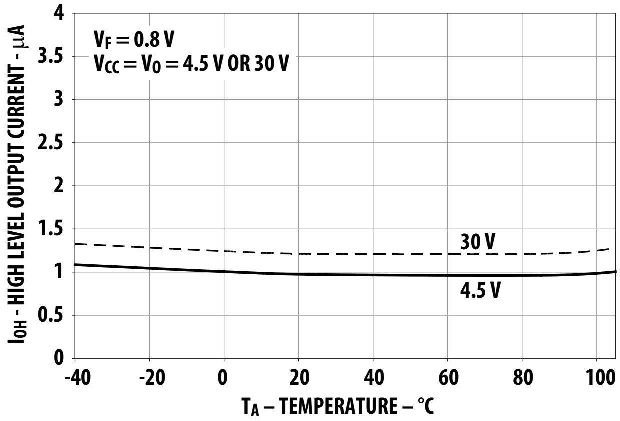


Figure 3. High Level Output Current vs. Temperature

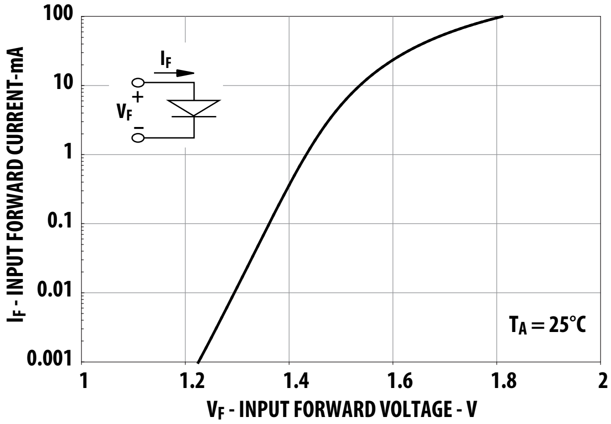


Figure 4. Input Current vs. Forward Voltage

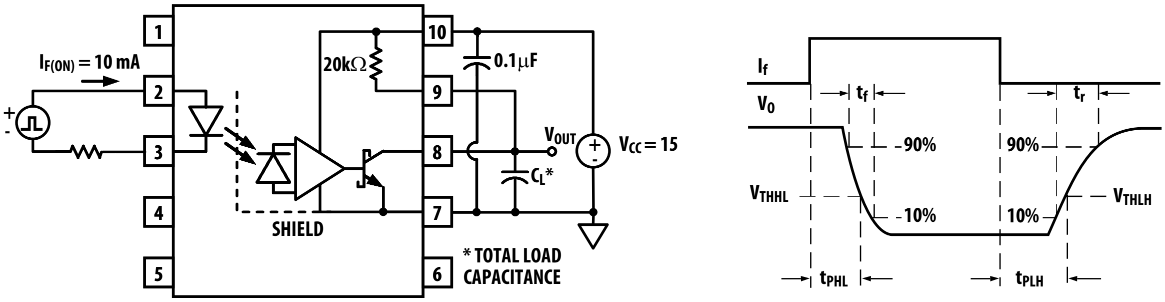


Figure 5. Propagation Delay Test Circuit

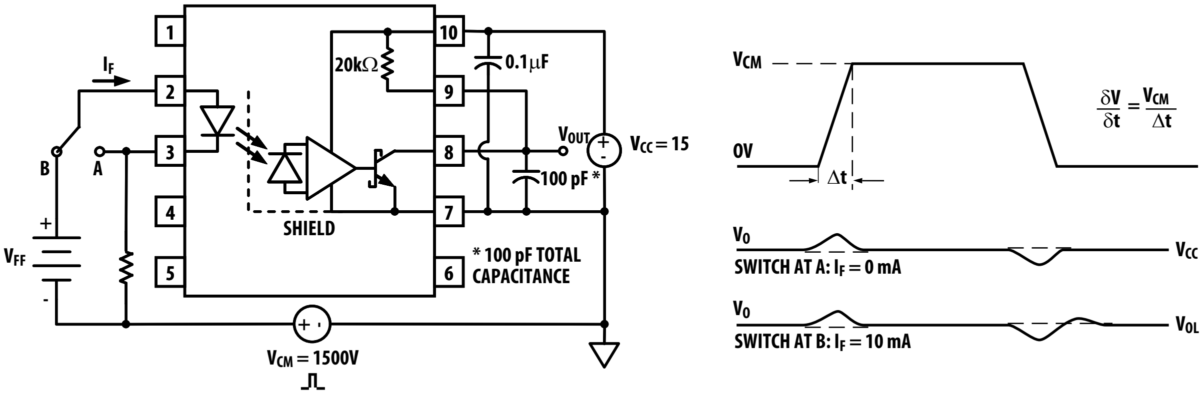


Figure 6. CMR Test Circuit and Waveforms

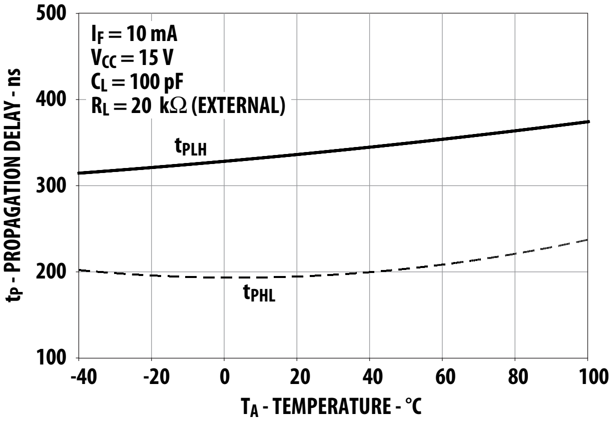


Figure 7. Propagation Delay with External 20 kΩ RL vs. Temperature

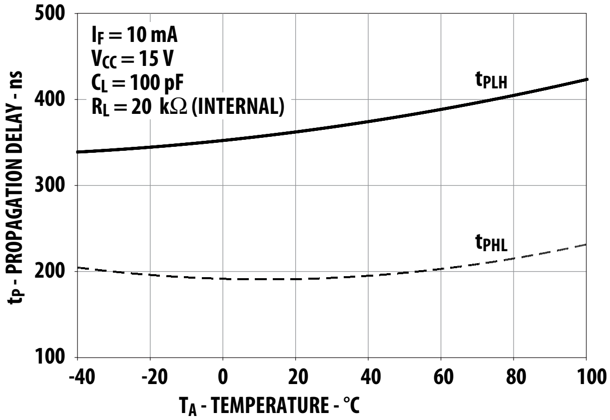


Figure 8. Propagation Delay with Internal 20 kΩ RL vs. Temperature

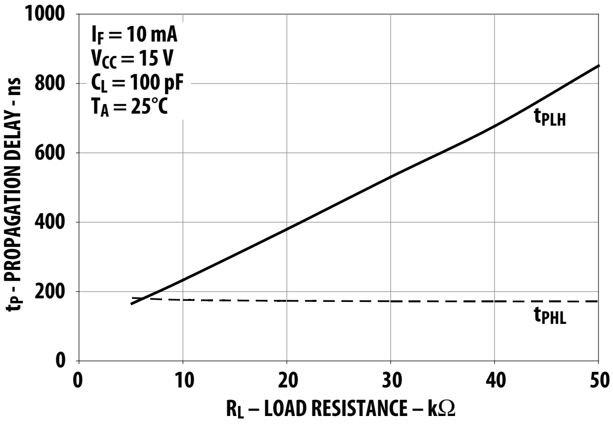


Figure 9. Propagation Delay vs. Load Resistance

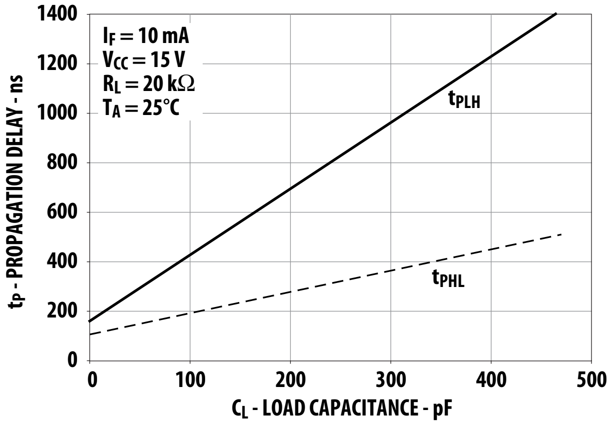


Figure 10. Propagation Delay vs. Load Capacitance

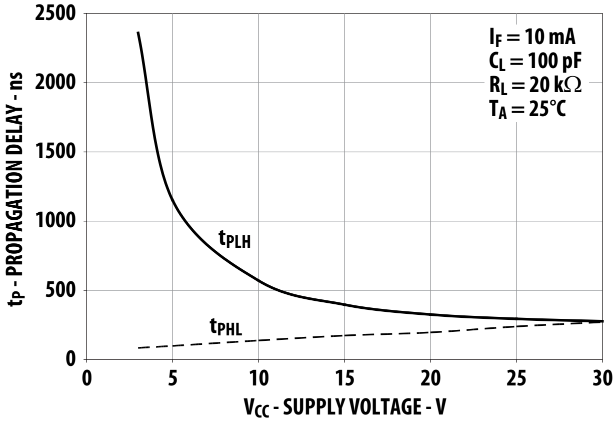


Figure 11. Propagation Delay vs. Supply Voltage

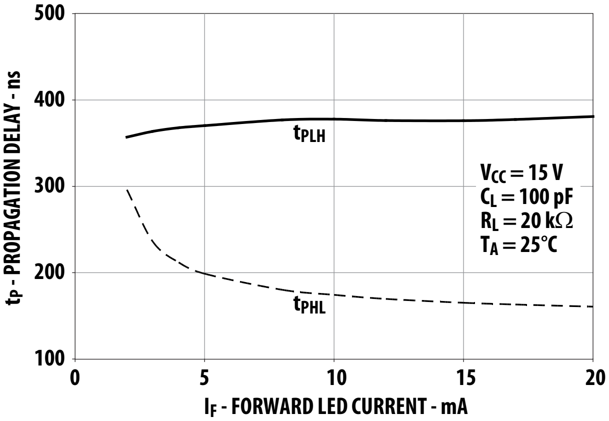


Figure 12. Propagation Delay vs. Input Current

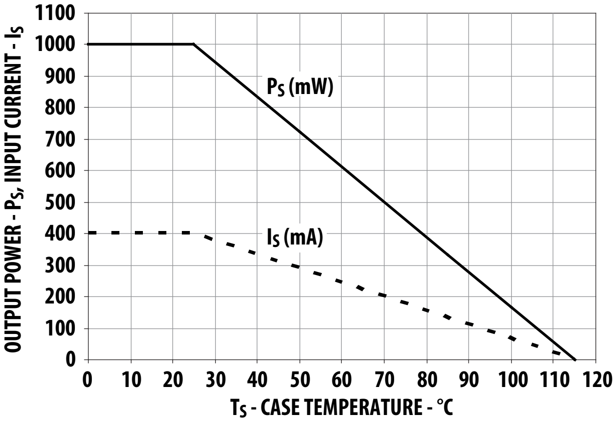


Figure 13. Dependence of Safety Limiting Values on Temperatures (Thermal Derating Curves)

Applications Information

LED Drive Circuit Considerations For Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 15. The ACNV4506 improve CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and the optocoupler output pin and output ground as shown in Figure 16. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 14), can achieve 30 kV/µs CMR while minimizing component complexity. Note that a CMOS gate is recommended in Figure 14 to keep the LED off when the gate is in the high state.

Another cause of CMR failure for a shielded optocoupler is direct coupling to the optocoupler output pins through C_{LEDO1} in Figure 16. Many factors influence the effect and magnitude of the direct coupling including: the position of the LED current setting resistor and the value of the capacitor at the optocoupler output (C_L).

CMR With The LED On (CMR_L)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. The recommended minimum LED current of 10 mA provides adequate margin over the maximum I_{TH} of 5.0 mA (see Figure 1) to achieve 30 kV/µs CMR.

The placement of the LED current setting resistor effects the ability of the drive circuit to keep the LED on during transients and interacts with the direct coupling to the optocoupler output. For example, the LED resistor in Figure 17 is connected to the anode. Figure 18 shows the AC equivalent circuit for Figure 17 during common mode transients. During a $+dV_{CM}/dt$ in Figure 18, the current available at the LED anode (I_{total}) is limited by the series resistor. The LED current (I_F) is reduced from its DC value by an amount equal to the current that flows through C_{LEDP} and C_{LEDO1}. The situation is made worse because the current through C_{LEDO1} has the effect of trying to pull the output high (toward a CMR failure) at the same time the LED current is being reduced. For this reason, the recommended LED drive circuit (Figure 14) places the current setting resistor in series with the LED cathode. Figure 19

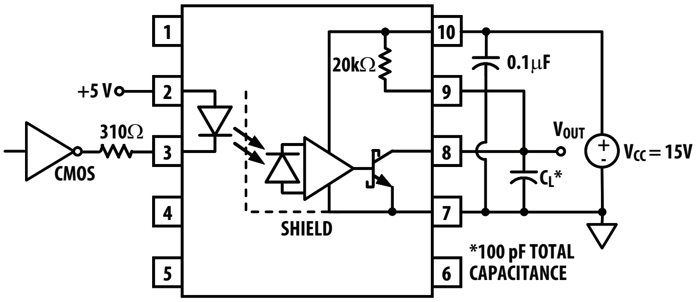


Figure 14. Recommended LED Drive Circuit

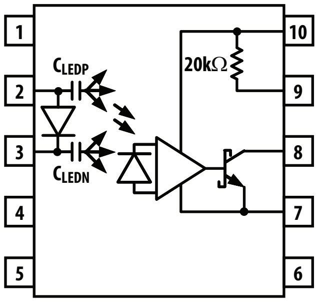


Figure 15. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers

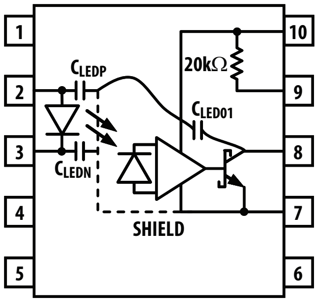


Figure 16. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers

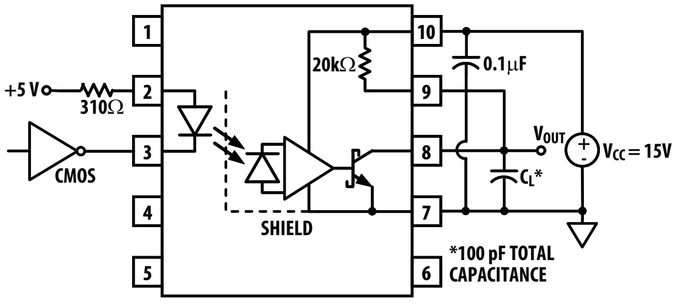


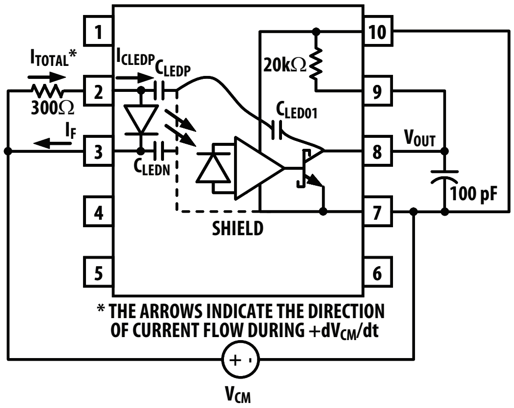
Figure 17. LED Drive Circuit with Resistor Connected to LED Anode (Not Recommended)

is the AC equivalent circuit for Figure 14 during common mode transients. In this case, the LED current is not reduced during a $+dV_{CM}/dt$ transient because the current flowing through the package capacitance is supplied by the power supply. During a $-dV_{CM}/dt$ transient, however, the LED current is reduced by the amount of current flowing through C_{LEDN}. But, better CMR performance is achieved since the current flowing in C_{LEDO1} during a negative transient acts to keep the output low.

CMR With The LED Off (CMR_H)

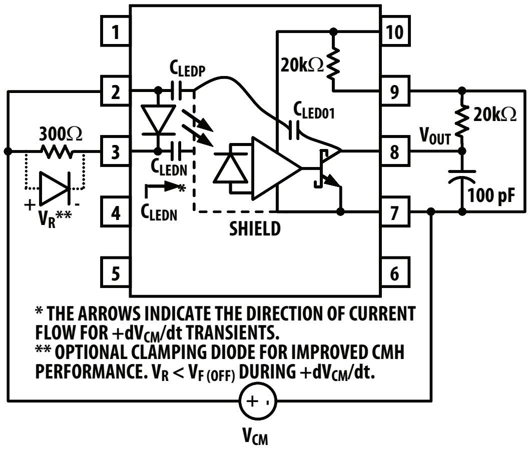
A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $+dV_{CM}/dt$ transient in Figure 19, the current flowing through C_{LEDN} is supplied by the parallel combination of the LED and series resistor. As long as the voltage developed across the resistor is less than $V_{F(OFF)}$ the LED will remain off and no common mode failure will occur. Even if the LED momentarily turns on, the 100 pF capacitor from pins 8-7 will keep the output from dipping below the threshold. The recommended LED drive circuit (Figure 14) provides about 10 V of margin between the lowest optocoupler output voltage and a 3 V IPM threshold during a 30 kV/µs transient with V_{CM} = 1500 V. Additional margin can be obtained by adding a diode in parallel with the resistor, as shown by the dashed line connection in Figure 19, to clamp the voltage across the LED below $V_{F(OFF)}$.

Since the open collector drive circuit, shown in Figure 20, cannot keep the LED off during a $+dV_{CM}/dt$ transient, it is not desirable for applications requiring ultra high CMR_H performance. Figure 21 is the AC equivalent circuit for Figure 20 during common mode transients. Essentially all the current flowing through C_{LEDN} during a $+dV_{CM}/dt$ transient must be supplied by the LED. CMR_H failures can occur at dv/dt rates where the current through the LED and C_{LEDN} exceeds the input threshold. Figure 22 is an alternative drive circuit which does achieve ultra high CMR performance by shunting the LED in the off state.



* THE ARROWS INDICATE THE DIRECTION OF CURRENT FLOW DURING $+dV_{CM}/dt$

Figure 18. AC Equivalent Circuit for Figure 17 during Common Mode Transients



* THE ARROWS INDICATE THE DIRECTION OF CURRENT FLOW FOR $+dV_{CM}/dt$ TRANSIENTS.
** OPTIONAL CLAMPING DIODE FOR IMPROVED CMH PERFORMANCE. $V_R < V_{F(OFF)}$ DURING $+dV_{CM}/dt$.

Figure 19. AC Equivalent Circuit for Figure 14 during Common Mode Transients

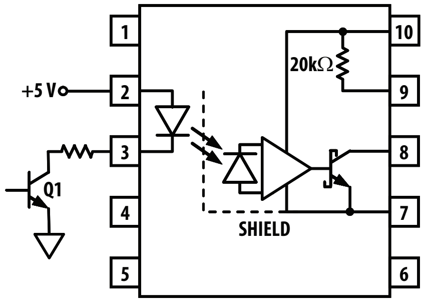
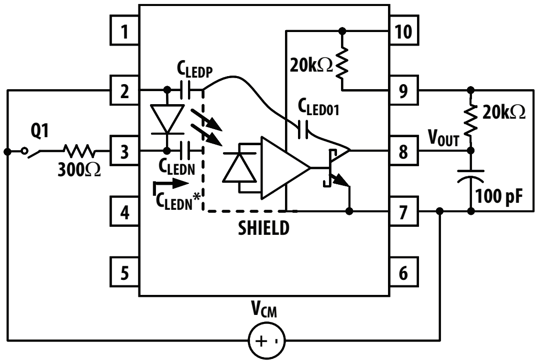


Figure 20. Not Recommended Open Collector LED Drive Circuit



* THE ARROWS INDICATE THE DIRECTION OF CURRENT FLOW FOR $+dV_{CM}/dt$ TRANSIENTS.

Figure 21. AC Equivalent Circuit for Figure 20 during Common Mode Transients

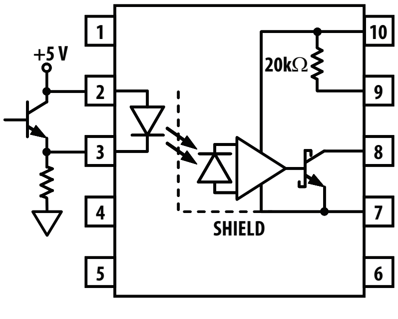


Figure 22. Recommended LED Drive Circuit for Ultra High CMR

IPM Dead Time and Propagation Delay Specifications

The ACNV4506 includes a Propagation Delay Difference specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 23) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time the designer must consider the propagation delay characteristics of the optocoupler as well as the characteristics of the IPM IGBT gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the IPM IGBT gate drive circuit can be analyzed in the same way) it is important to know the minimum and maximum turn on (t_{PHL}) and turn-off (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range.

The limiting case of zero dead time occurs when the input to Q1 turns off at the same time that the input to Q2 turns on. This case determines the minimum delay between LED1 turn-off and LED2 turn-on, which is related to the worst case optocoupler propagation delay waveforms, as shown in Figure 24. A minimum dead time of zero is achieved in Figure 24 when the signal to turn on LED2 is delayed by (t_{PLH} max - t_{PHL} min) from the LED1 turn off. Note that the propagation delays used to calculate PDD are taken at equal temperatures since the optocouplers under consideration are typically mounted in close proximity to each other. (Specifically, previous equation are not the same as the t_{PLH} max and t_{PHL} min, over the full operating temperature range, specified in the data sheet.) This delay is the maximum value for the propagation delay difference specification which is specified at 450 ns for the ACNV4506 over an operating temperature range of -40°C to 105°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time occurs in the highly unlikely case where one optocoupler with the fastest t_{PLH} and another with the slowest t_{PHL} are in the same inverter leg. The maximum dead time in this case becomes the sum of the spread in the t_{PLH} and t_{PHL} propagation delays as shown in Figure 25. The maximum dead time is also equivalent to the difference between the maximum and minimum propagation delay difference specifications. The maximum dead time (due to the optocouplers) for the ACNV4506 are 600 ns (= 450 ns - (-150 ns)) over an operating temperature range of -40°C to 105°C.

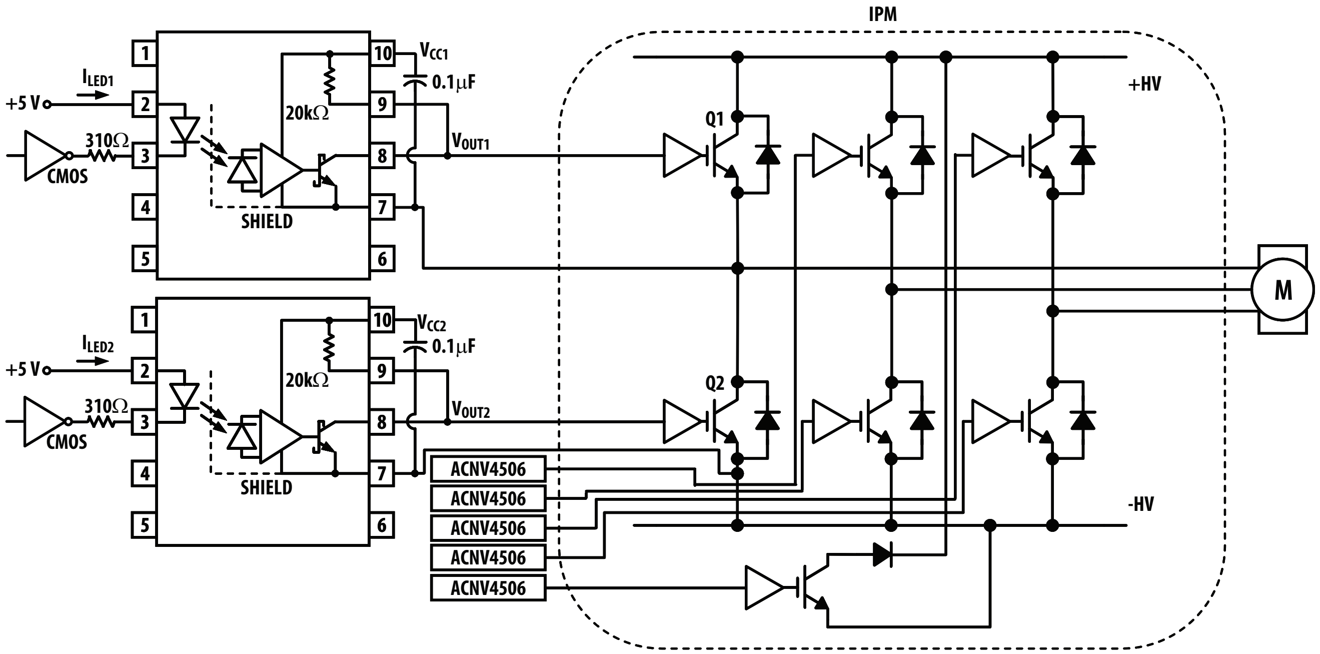
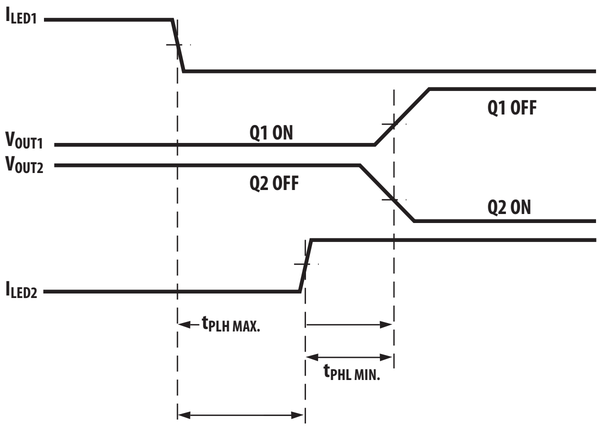


Figure 23. Typical Application Circuit

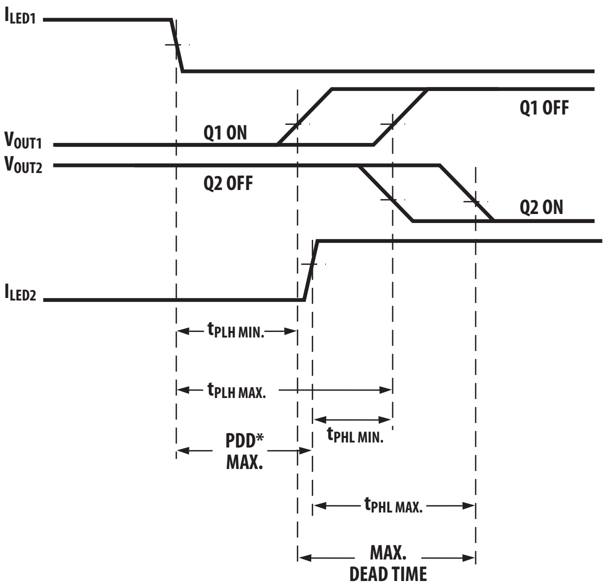


PDD* MAX. =
$(t_{PLH}-t_{PHL})$ MAX. = $t_{PLH\ MAX.} - t_{PHL\ MIN.}$

*PDD = PROPAGATION DELAY DIFFERENCE

Note: The propagation delays used to calculate
PDD are taken at equal temperatures.

Figure 24. Minimum LED Skew for Zero Dead Time



MAXIMUM DEAD TIME (DUE TO OPTOCOUPLER)
$= (t_{PLH\ MAX.} - t_{PLH\ MIN.}) + (t_{PHL\ MAX.} - t_{PHL\ MIN.})$
$= (t_{PLH\ MAX.} - t_{PHL\ MIN.}) - (t_{PLH\ MIN.} - t_{PHL\ MAX.})$
= PDD* MAX. - PDD* MIN.

*PDD = PROPAGATION DELAY DIFFERENCE

Note: The propagation delays used to calculate the maximum
Dead time are taken at equal temperatures.

Figure 25. Waveforms for Deadtime Calculation

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