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# Automotive 2.5-Amp MOSFET Gate Drive Optocoupler with Integrated Desat Over Current Sensing, Miller Current Clamping and Under Voltage Lock-Out Feedback

## Data Sheet

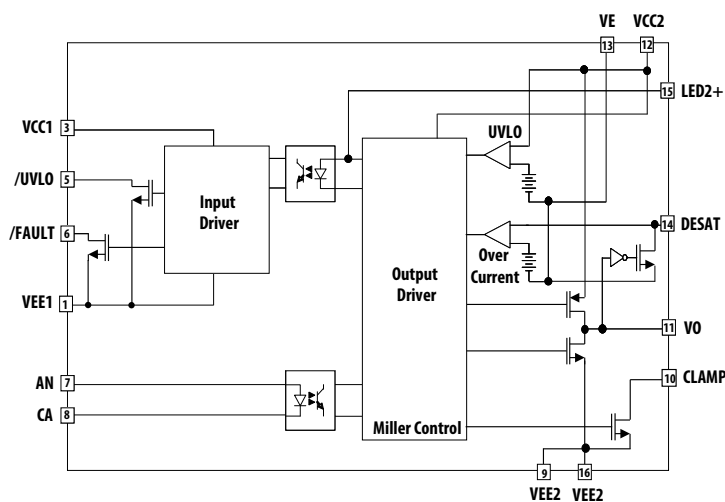
### Description

The Broadcom® automotive 2.5-amp gate drive optocoupler features fast propagation delay with excellent timing skew performance. Smart features that are integrated to protect the MOSFET include desaturation sensing with shutdown protection and fault feedback, under voltage lockout and feedback, and active Miller current clamping. This full-featured and easy-to-implement gate drive optocoupler comes in a compact, surface-mountable SO-16 package for space-savings. It is ideally designed for driving power MOSFETs used in AC-DC and DC-DC converters and satisfies automotive AEC-Q100 semiconductor requirements.

Broadcom R<sup>2</sup>Coupler™ isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

### Functional Diagram

Figure 1 ACPL-31JT Functional Diagram



### Features

- Qualified to AEC-Q100 Grade 1 test guidelines
- Automotive temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Common mode rejection (CMR):  $>50\text{kV}/\mu\text{s}$  at  $V_{\text{CM}} = 1500\text{V}$
- High noise immunity
  - Miller current clamping
  - Direct LED input with low input impedance and low noise sensitivity
  - Negative gate bias
- Peak output current: 2.5A maximum.
- Miller clamp sinking current: 1.9A maximum
- Wide operating voltage: 12V to 20V
- Propagation delay: 250 ns maximum
- Dead time distortion:  $-100$  ns to  $+15$  ns
- Integrated fail-safe MOSFET protection
- Desat sensing, turn-off protection, and fault feedback
- Under voltage lock-out protection (UVLO) with feedback
- SO-16 package with 8-mm clearance and creepage
- Regulatory approvals:
  - UL1577, CSA
  - EC/EN/DIN EN 60747-5-5

### Applications

- Automotive isolated MOSFET gate drive
- Automotive DC-DC converter
- Switching power supplies

### CAUTION

It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

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## Ordering Information

Part Number	Option	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	(RoHS Compliant)					
ACPL-31JT	-000E	SO-16	X		X	45 per tube
ACPL-31JT	-500E		X	X	X	850 per reel

To order, choose a part number from the Part Number column and combine with the desired option from the RoHS Compliant column to form an order entry.

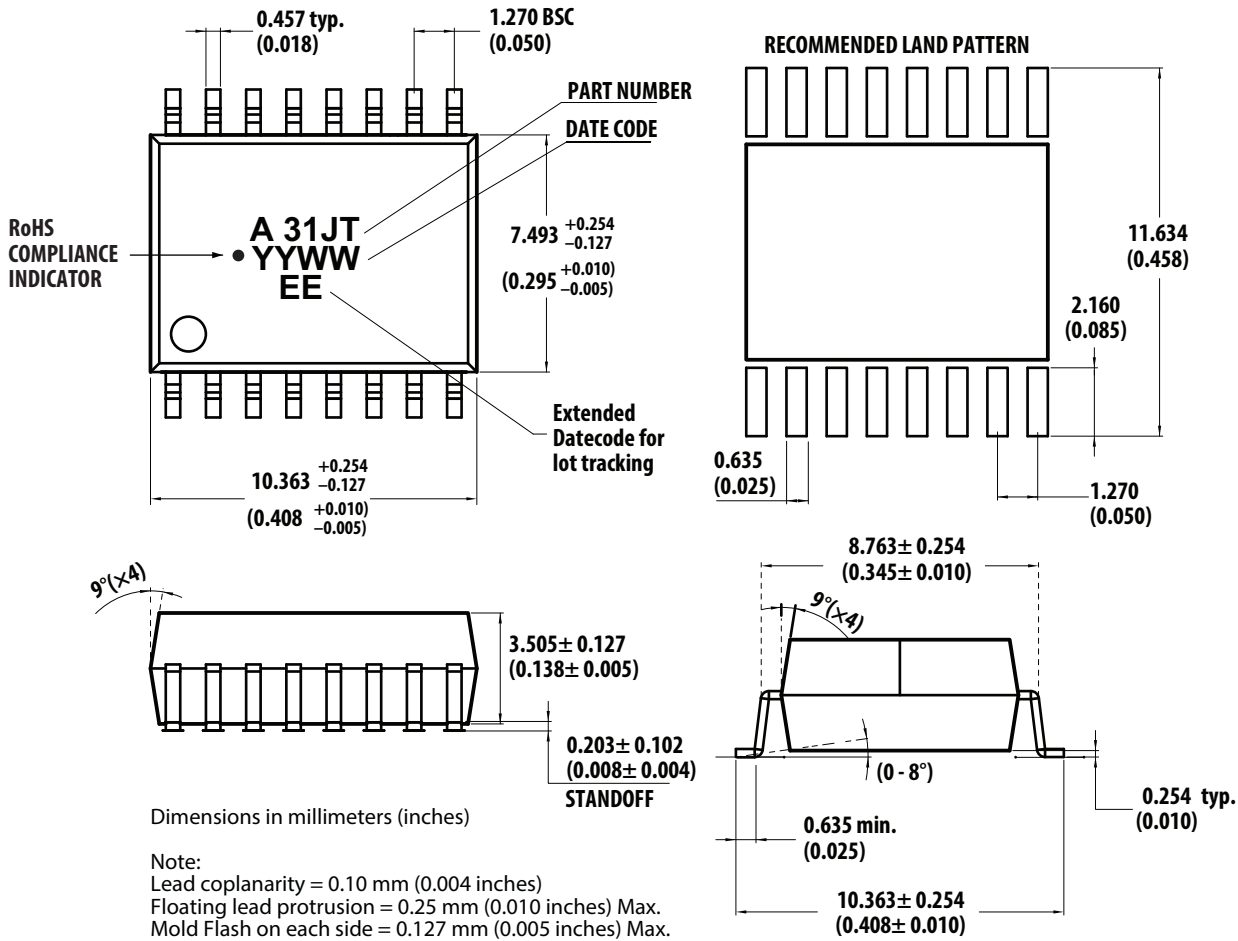
Example 1:

ACPL-31JT-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

## Package Outline Drawings

### 16-Lead Surface Mount



### Recommended Lead-free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

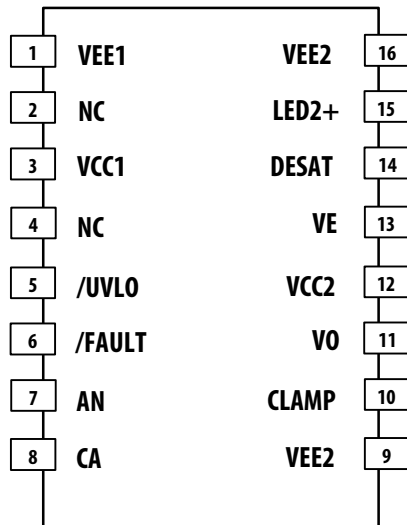
Non-halide flux should be used.

## Product Overview Description

The ACPL-31JT (shown in Figure 1) is a highly integrated power control device that incorporates all the necessary components for a complete, isolated MOSFET gate drive circuit. It features desaturation sensing with shutdown protection and fault feedback, under voltage lock-out and feedback and active Miller current clamping in a SO-16 package. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increased its noise immunity.

## Package Pin Out

Figure 2 Pin Out of ACPL-31JT



## Pin Description

Pin Name	Function	Pin Name	Function
VEE1	Input common	VEE2	Negative power supply
NC	No connection	LED2+	No connection, for testing only
VCC1	Input power supply	DESAT	Desat over current sensing
NC	No connection	VE	MOSFET Source reference
/UVLO	VCC2 under voltage lock-out feedback	VCC2	Positive power supply
/FAULT	Over current fault feedback	VO	Driver output to MOSFET gate
AN	Input LED anode	CLAMP	Miller current clamping output
CA	Input LED cathode	VEE2	Negative power supply

## Regulatory Information

The ACPL-31JT is approved by the following organizations.

<b>UL</b>	Approved under UL 1577, component recognition program up to VISO = 5000 VRMS
<b>CSA</b>	Approved under CSA Component Acceptance Notice #5, File CA 88324.
<b>IEC/EN/DIN EN 60747-5-5</b>	Approved under IEC 60747-5-5, EN 60747-5-5, DIN EN 60747-5-5

## IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Units
Insulation Classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage $\leq 150$ Vrms for rated mains voltage $\leq 300$ Vrms for rated mains voltage $\leq 600$ Vrms for rated mains voltage $\leq 1000$ Vrms		I – IV I – IV I – IV I – III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	1230	$V_{PEAK}$
Input to Output Test Voltage, Method b <sup>a</sup> $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1s$ , Partial discharge $< 5$ pC	$V_{PR}$	2306	$V_{PEAK}$
Input to Output Test Voltage, Method a <sup>a</sup> $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10s$ , Partial Discharge $< 5$ pC	$V_{PR}$	1968	$V_{PEAK}$
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60s$ )	$V_{IOTM}$	8000	$V_{PEAK}$
Safety-Limiting Values – maximum values allowed in the event of a failure Case Temperature Input Power Output Power	$T_S$ $P_{S,INPUT}$ $P_{S,OUTPUT}$	175 400 1200	$^{\circ}C$ mW mW
Insulation Resistance at $T_S$ , $V_{IO} = 500V$	$R_S$	$> 10^9$	Ohm

- a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulation section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

**NOTE** Isolation characteristics are guaranteed only within the safety maximum ratings that must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECC00802.

## Insulation and Safety-Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	$>175$	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110)

## Absolute Maximum Ratings

Unless otherwise specified, all voltages at input IC reference to  $V_{EE1}$ , all voltages at output IC reference to  $V_{EE2}$ .

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	$T_S$	-55	150	°C	
Operating Temperature	$T_A$	-40	125	°C	
IC Junction Temperature	$T_J$	—	150	°C	a
Average Input Current	$I_{F(AVG)}$	—	20	mA	
Peak Transient Input Current (<1- $\mu$ s pulse width, 300 pps)	$I_{F(TRAN)}$	—	1	A	
Reverse Input Voltage	$V_R$	—	6	V	
/Fault Output Current (Sinking)	$I_{/FAULT}$	—	10	mA	
/Fault Pin Voltage	$V_{/FAULT}$	-0.5	6	V	
/UVLO Output Current (Sinking)	$I_{/UVLO}$	—	10	mA	
/UVLO Pin Voltage	$V_{/UVLO}$	-0.5	6	V	
Positive Input Supply Voltage	$V_{CC1}$	-0.5	26	V	
Total Output Supply Voltage	$V_{CC2}$	-0.5	30	V	
Negative Output Supply Voltage	$V_{EE2} - V_E$	-10	0.5	V	b
Positive Output Supply Voltage	$V_{CC2} - V_E$	-0.5	30	V	
Gate Drive Output Voltage	$V_{O(peak)}$	-0.5	$V_{CC2} + 0.5$	V	
Peak Output Current	$ I_{O(peak)} $	—	2.5	A	c
Peak Clamping Sinking Current	$I_{CLAMP}$	—	2	A	c
Miller Clamping Pin Voltage	$V_{CLAMP} - V_{EE2}$	-0.5	$V_{CC2} + 0.5$	V	
Desat Voltage	$V_{DESAT} - V_E$	$V_E - 0.5$	$V_{CC2} + 0.5$	V	d
Desat Discharging Current (Continuous)	$I_{DSCHG}$	—	5	mA	
Output IC Power Dissipation	$P_O$	—	580	mW	a
Input IC Power Dissipation	$P_I$	—	150	mW	

- Output IC power dissipation is derated linearly above 100°C from 580 mW to 260 mW at 125°C based on the thermal characteristic on page 11.
- This supply is optional. Required only when negative gate drive is implemented.
- Maximum pulse width = 1s, maximum duty cycle = 1%.
- Maximum 500-ns pulse width if peak  $V_{DESAT} > 10$  V.

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Temperature	$T_A$	-40	125	°C	
Input Supply Voltage	$V_{CC1} - V_{EE1}$	8	18	V	
Total Output Supply Voltage	$V_{CC2} - V_{EE2}$	12	20	V	a
Negative Output Supply Voltage	$V_{EE2} - V_E$	-8	0	V	b
Positive Output Supply Voltage	$V_{CC2} - V_E$	12	20	V	
Input LED Current	$I_{F(ON)}$	10	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-5.5	0.8	V	
Input pulse width	$t_{ON(LED)}$	500	—	ns	

a. 12V is the recommended minimum operating positive supply voltage ( $V_{CC2} - V_E$ ) to ensure adequate margin in excess of the maximum  $V_{UVLO+}$  threshold of 11.2V.

b. Maximum pulse width = 1s, maximum duty cycle = 1%.

## Electrical and Switching Specifications

Unless otherwise specified, all Minimum/Maximum specifications are at recommended operating conditions. All typical values at  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = 12\text{V}$ ,  $V_{CC2} - V_{EE2} = 13\text{V}$ ,  $V_E - V_{EE2} = 0\text{V}$ . All voltages at input IC reference to  $V_{EE1}$ , all voltages at output IC reference to  $V_{EE2}$ .

**Table 1 Electrical and Switching Specifications**

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
<b>IC Supply Current</b>								
Input Supply Current	$I_{CC1}$	—	3.7	6.0	mA		3	
Output Low Supply Current	$I_{CC2L}$	—	10.5	13.2	mA	$I_F = 0\text{ mA}$	4	
Output High Supply Current	$I_{CC2H}$	—	10.6	13.6	mA	$I_F = 10\text{ mA}$	4	
<b>Logic Input and Output</b>								
LED Forward Voltage	$V_F$	1.25	1.55	1.85	V	$I_F = 10\text{ mA}$	5	
LED Reverse Breakdown Voltage	$V_{BR}$	6	—	—	V	$I_F = -10\text{ A}$		
Input Capacitance	$C_{IN}$	—	90	—	pF			
LED Turn on Current Threshold Low to High	$I_{TH+}$	—	2.7	6.6	mA	$V_O = 5\text{ V}$	6	
LED Turn on Current Threshold High to Low	$I_{TH-}$	—	2.1	6.4	mA	$V_O = 5\text{ V}$	6	
LED Turn on Current Hysteresis	$I_{TH\_HYS}$	—	0.6	—	mA			
/FAULT Logic Low Output Current	$I_{FAULT\_L}$	4.0	9.0	—	mA	$V_{FAULT} = 0.4\text{ V}$		
/FAULT Logic High Output Current	$I_{FAULT\_H}$	—	—	20	$\mu\text{A}$	$V_{FAULT} = 5\text{ V}$		
/UVLO Logic Low Output Current	$I_{UVLO\_L}$	4.0	9.0	—	mA	$V_{UVLO} = 0.4\text{ V}$		
/UVLO Logic High Output Current	$I_{UVLO\_H}$	—	—	20	$\mu\text{A}$	$V_{UVLO} = 5\text{ V}$		



**Table 1 Electrical and Switching Specifications (Continued)**

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
<b>Gate Driver</b>								
High Level Output Current	$I_{OH}$	—	-2.0	-0.75	A	$V_O = V_{CC2} - 3V$	7	a
Low Level Output Current	$I_{OL}$	1.0	2.2	—	A	$V_O = V_{EE2} + 2.5V$	8	a
High Level Output Voltage	$V_{OH}$	$V_{CC2} - 0.5$	$V_{CC2} - 0.2$	—	V	$I_O = -100\text{ mA}$		b, c, d
Low Level Output Voltage	$V_{OL}$	—	0.1	0.5	V	$I_O = 100\text{ mA}$		
VIN to High Level Output Propagation Delay Time	$t_{PLH}$	50	110	250	ns	$V_{source} = 3.3V, R_f = 140\Omega, R_g = 10\Omega, C_{load} = 1\text{ nF}, f = 200\text{ kHz}, \text{Duty Cycle} = 50\%$	9, 12	e
VIN to Low Level Output Propagation Delay Time	$t_{PHL}$	50	150	250	ns		f	
Pulse Width Distortion ( $t_{PHL} - t_{PLH}$ )	PWD	-15	—	100	ns		g, h	
Dead Time Distortion ( $t_{PLH} - t_{PHL}$ )	DTD	-100	—	15	ns		h, i	
10% to 90% Rise Time	$t_R$	—	60	—	ns			
90% to 10% Fall Time	$t_F$	—	50	—	ns			
Output High Level Common Mode Transient Immunity	$ CM_H $	50	>70	—	kV/ $\mu$ s	$T_A = 25^\circ\text{C}, V_{CM} = 1500V, V_{CC2} = 20V$	13	j
Output Low Level Common Mode Transient Immunity	$ CM_L $	50	>70	—	kV/ $\mu$ s	$T_A = 25^\circ\text{C}, V_{CM} = 1500V, V_{CC2} = 20V$	14	k
<b>Active Miller Clamp</b>								
Clamp Threshold Voltage	$V_{TH\_CLAMP}$	—	2.0	3.0	V			
Clamp Low Level Sinking Current	$I_{CLAMP}$	0.75	1.9	—	A	$V_{CLAMP} = V_{EE2} + 2.5V$		
<b>V<sub>CC2</sub> UVLO Protection (UVLO Voltage V<sub>UVLO</sub> Reference to V<sub>E</sub>)</b>								
V <sub>CC2</sub> UVLO Threshold Low to High	$V_{UVLO+}$	8.8	10	11.2	V	$V_O > 5V$		d, l
V <sub>CC2</sub> UVLO Threshold High to Low	$V_{UVLO-}$	7.8	9	10.2	V	$V_O < 5V$		d, m
V <sub>CC2</sub> UVLO Hysteresis	$V_{UVLO\_HYS}$	—	1	—	V			
V <sub>CC2</sub> to UVLO High Delay	$t_{PLH\_UVLO}$	—	10	—	$\mu$ s			n
V <sub>CC2</sub> to UVLO Low Delay	$t_{PHL\_UVLO}$	—	10	—	$\mu$ s			o
V <sub>CC2</sub> UVLO to VOUT High Delay	$t_{UVLO\_ON}$	—	10	—	$\mu$ s			p
V <sub>CC2</sub> UVLO to VOUT Low Delay	$t_{UVLO\_OFF}$	—	10	—	$\mu$ s			q

**Table 1 Electrical and Switching Specifications (Continued)**

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
<b>Desaturation Protection (Desat Voltage <math>V_{DESAT}</math> Reference to <math>V_E</math>)</b>								
Desat Sensing Threshold	$V_{DESAT}$	3.4	3.9	4.4	V		10	d
Desat Discharging Current (Pulsed)	$I_{DSCHG}$	20	53	—	mA	$V_{DESAT} = 5V$	11	
Internal Desat Blanking Time	$t_{DESAT(BLANKING)}$	0.2	0.4	0.6	$\mu s$	Clod = 1 nF	6	r
Desat Sense to 90% VO Delay	$t_{DESAT(90\%)}$	—	0.15	0.5	$\mu s$		6	s
Desat to Low Level FAULT Signal Delay	$t_{DESAT(/FAULT)}$	—	—	7	$\mu s$		6	t
Output Mute Time due to Desat	$t_{DESAT(MUTE)}$	2.3	3.2	5	ms		6	u
Time for Input Kept Low Before Fault Reset to High	$t_{DESAT(RESET)}$	2.3	3.2	5	ms		6	v

- Maximum 500-ns pulse width if peak  $V_{DESAT} > 10V$ .
- For High Level Output Voltage testing,  $V_{OH}$  is measured with a DC load current. When driving capacitive loads,  $V_{OH}$  will approach  $V_{CC}$  as  $I_{OH}$  approaches zero.
- Maximum pulse width = 1.0 ms, maximum duty cycle = 20%.
- Once  $V_O$  of the ACPL-31JT is allowed to go high ( $V_{CC2} - V_E > V_{UVLO}$ ), the DESAT detection feature of the ACPL-31JT will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once  $V_{CC2}$  exceeds  $V_{UVLO+}$  threshold, DESAT will remain functional until  $V_{CC2}$  is below  $V_{UVLO-}$  threshold. Thus, the DESAT detection and UVLO features of the ACPL-31JT work in conjunction to ensure constant IGBT protection.
- $t_{PLH}$  is defined as propagation delay from 50% of LED input  $I_F$  to 50% of High level output.
- $t_{PHL}$  is defined as propagation delay from 50% of LED input  $I_F$  to 50% of Low level output.
- Pulse Width Distortion (PWD) is defined as ( $t_{PHL} - t_{PLH}$ ) of any given unit.
- As measured from  $I_F$  to  $V_O$ .
- Dead Time Distortion (DTD) is defined as ( $t_{PLH} - t_{PHL}$ ) between any two ACPL-31JT parts under the same test conditions.
- Common mode transient immunity in the high state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in the high state (that is,  $V_O > 12V$ ).
- Common mode transient immunity in the low state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a low state (that is,  $V_O < 1.0V$ ).
- This is the "increasing" (that is, turn-on or "positive going" direction) of  $V_{CC2} - V_E$ .
- This is the "decreasing" (that is, turn-off or "negative going" direction) of  $V_{CC2} - V_E$ .
- The delay time when  $V_{CC2}$  exceeds UVLO+ threshold to UVLO High – 50% of UVLO positive-going edge.
- The delay time when  $V_{CC2}$  falls below UVLO- threshold to UVLO Low – 50% of UVLO negative-going edge.
- The delay time when  $V_{CC2}$  exceeds UVLO+ threshold to 50% of High level output.
- The delay time when  $V_{CC2}$  falls below UVLO- threshold to 50% of Low level output.
- The delay time for ACPL-31JT to respond to a DESAT fault condition without any external DESAT capacitor.
- The amount of time from when DESAT threshold is exceeded to 90% of VGATE at mentioned test conditions.
- The amount of time from when DESAT threshold is exceeded to FAULT output Low – 50% of  $V_{CC1}$  voltage.
- The amount of time when DESAT threshold is exceeded, Output is mute to LED input.
- The amount of time when DESAT Mute time is expired, LED input must be kept Low for Fault status to return to High.

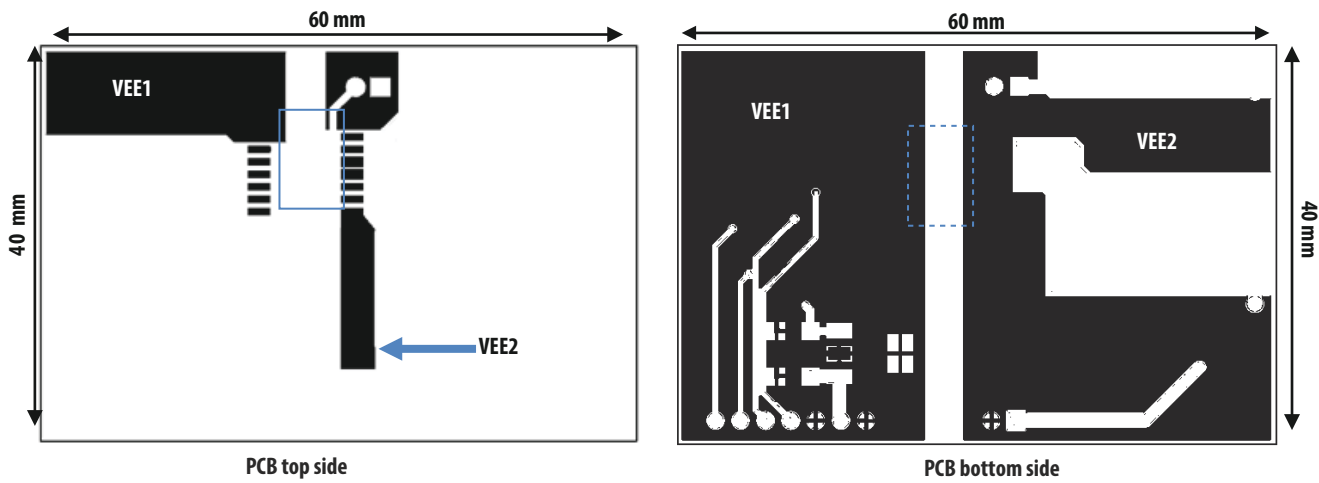
## Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	$V_{ISO}$	5000	—	—	$V_{RMS}$	RH < 50%, t = 1 min., $T_A = 25^\circ\text{C}$	a, b, c
Resistance (Input-Output)	$R_{I-O}$	—	1014	—	$\Omega$	$V_{I-O} = 500 V_{DC}$	c
Capacitance (Input-Output)	$C_{I-O}$	—	1.3	—	pF	f = 1 MHz	
Thermal coefficient between LED and input IC	$A_{EI}$	—	35.4	—	$^\circ\text{C}/\text{W}$		
Thermal coefficient between LED and output IC	$A_{EO}$	—	33.1	—	$^\circ\text{C}/\text{W}$		
Thermal coefficient between input IC and output IC	$A_{IO}$	—	25.6	—	$^\circ\text{C}/\text{W}$		
Thermal coefficient between LED and Ambient	$A_{EA}$	—	176.1	—	$^\circ\text{C}/\text{W}$		
Thermal coefficient between input IC and Ambient	$A_{IA}$	—	92	—	$^\circ\text{C}/\text{W}$		
Thermal coefficient between output IC and Ambient	$A_{OA}$	—	76.7	—	$^\circ\text{C}/\text{W}$		

- In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 6000 V_{RMS}$  for 1 second.
- The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.
- Device considered a two terminal device: pins 1–8 shorted together and pins 9–16 shorted together.

## Thermal Characteristics

Thermal characteristics are based on the ground planes layout of the evaluation PCB.



### Notes on Thermal Calculation

Application and environmental design for ACPL-31JT needs to ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 150°C. The following equations calculate the maximum power dissipation and corresponding effect on junction temperatures and can only be used as a reference for thermal performance comparison under specified PCB layout as shown above. The thermal resistance model shown here is not meant to and will not predict the performance of a package in an application-specific environment.

$$\begin{aligned} \text{LED Junction Temperature} &= A_{EA} \times P_E + A_{EI} \times P_I + A_{EO} \times P_O + T_A \\ \text{Input IC Junction Temperature} &= A_{EI} \times P_E + A_{IA} \times P_I + A_{IO} \times P_O + T_A \\ \text{Output IC Junction Temperature} &= A_{EO} \times P_E + A_{IO} \times P_I + A_{OA} \times P_O + T_A \end{aligned}$$

$P_E$  – LED Power Dissipation  
 $P_I$  – Input IC Power Dissipation  
 $P_O$  – Output IC Power Dissipation

#### Calculation of LED Power Dissipation

LED Power Dissipation,  $P_E = I_{F(\text{LED})}$  (Recommended Max)  $\times V_{F(\text{LED})}$  (125°C)  $\times$  Duty Cycle  
 Example:  $P_E = 16 \text{ mA} \times 1.25 \times 50\% \text{ duty cycle} = 10 \text{ mW}$

#### Calculation of Input IC Power Dissipation

Input IC Power Dissipation,  $P_I = I_{CC1}$  (Max)  $\times V_{CC1}$  (Recommended Max)  
 Example:  $P_I = 6 \text{ mA} \times 18\text{V} = 108 \text{ mW}$

#### Calculation of Output IC Power Dissipation

Output IC Power Dissipation,  $P_O = V_{CC2}$  (Recommended Max)  $\times I_{CC2}$  (Max) +  $P_{HS}$  +  $P_{LS}$

$P_{HS}$  – High Side Switching Power Dissipation  
 $P_{LS}$  – Low Side Switching Power Dissipation

$$\begin{aligned} P_{HS} &= (V_{CC2} \times Q_G \times f_{PWM}) \times R_{OH(\text{MAX})} / (R_{OH(\text{MAX})} + R_{GH}) / 2 \\ P_{LS} &= (V_{CC2} \times Q_G \times f_{PWM}) \times R_{OL(\text{MAX})} / (R_{OL(\text{MAX})} + R_{GL}) / 2 \end{aligned}$$

- $Q_G$  – Gate Charge at Supply Voltage  
 $f_{PWM}$  – LED Switching Frequency  
 $R_{OH(MAX)}$  – Maximum High Side Output Impedance -  $V_{OH(MIN)} / I_{OH(MIN)}$   
 $R_{GH}$  – Gate Charging Resistance  
 $R_{OL(MAX)}$  – Maximum Low Side Output Impedance -  $V_{OL(MIN)} / I_{OL(MIN)}$   
 $R_{GL}$  – Gate Discharging Resistance

Example:

$$R_{OH(MAX)} = (V_{CC2} - V_{OH(MIN)}) / I_{OH(MIN)} = 3V / 0.75A = 4\Omega$$

$$R_{OL(MAX)} = V_{OL(MIN)} / I_{OL(MIN)} = 2.5V / 1A = 2.5\Omega$$

$$P_{HS} = (20V \times 100 \text{ nC} \times 200 \text{ kHz}) \times 4\Omega / (4\Omega + 10\Omega) / 2 = 57.14 \text{ mW}$$

$$L_S = (20V \times 100 \text{ nC} \times 200 \text{ kHz}) \times 2.5 \Omega / (2.5\Omega + 10\Omega) / 2 = 40 \text{ mW}$$

$$P_O = 20V \times 13.6 \text{ mA} + 57.14 \text{ mW} + 40 \text{ mW} = 360.14 \text{ mW}$$

### Calculation of Junction Temperature

$$\text{LED Junction Temperature} = 176.1 \text{ }^\circ\text{C/W} * 10 \text{ mW} + 35.4 \text{ }^\circ\text{C/W} * 108 \text{ mW} + 33.1 * 360.14 \text{ mW} + T_A = 17.5^\circ\text{C} + T_A$$

$$\text{Input IC Junction Temperature} = 35.4 \text{ }^\circ\text{C/W} * 10 \text{ mW} + 92 \text{ }^\circ\text{C/W} * 108 \text{ mW} + 25.6 * 360.14 \text{ mW} + T_A = 19.5^\circ\text{C} + T_A$$

$$\text{Output IC Junction Temperature} = 33.1 \text{ }^\circ\text{C/W} * 10 \text{ mW} + 25.6 \text{ }^\circ\text{C/W} * 108 \text{ mW} + 76.7 * 360.14 \text{ mW} + T_A = 30.7^\circ\text{C} + T_A$$

## Typical Performance Plots

Figure 3  $I_{CC1}$  across Temperature

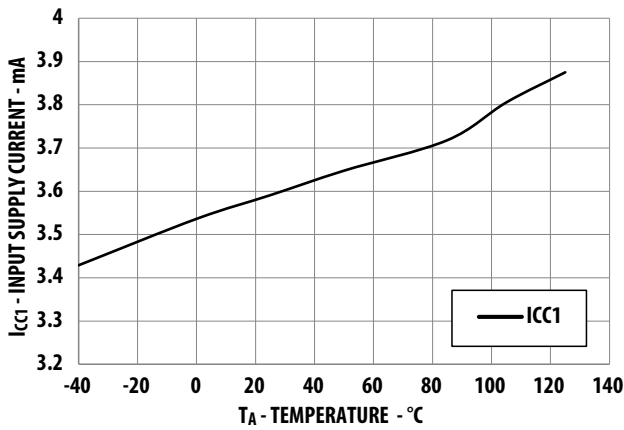


Figure 4  $I_{CC2}$  across Temperature

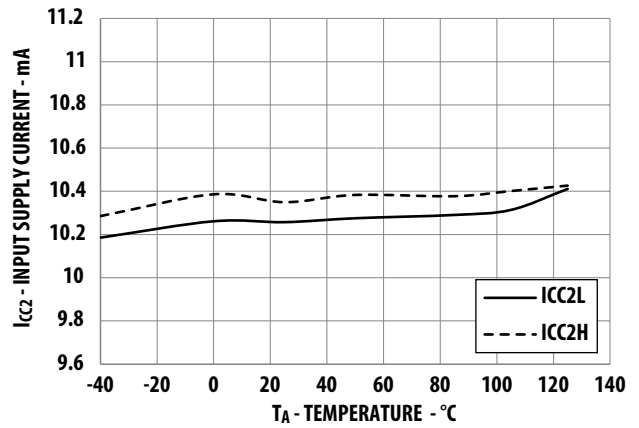


Figure 5  $I_F$  vs.  $V_F$

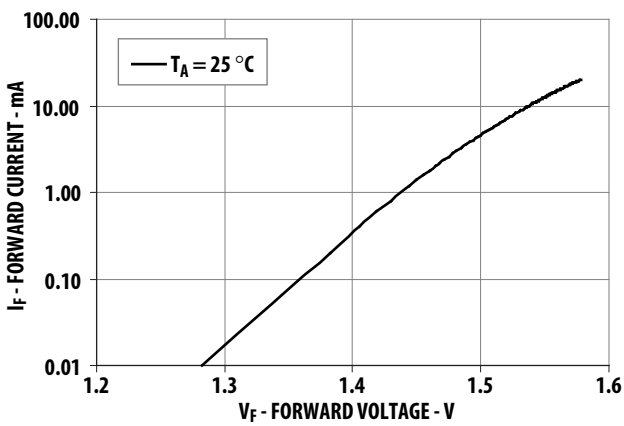


Figure 6  $I_{TH}$  across Temperature

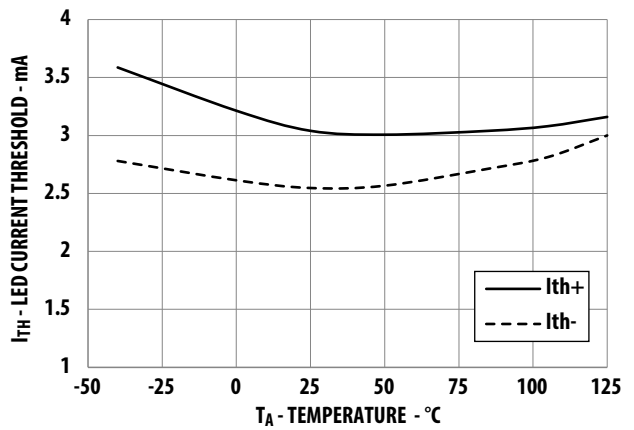


Figure 7  $V_{OH}$  vs.  $I_{OH}$

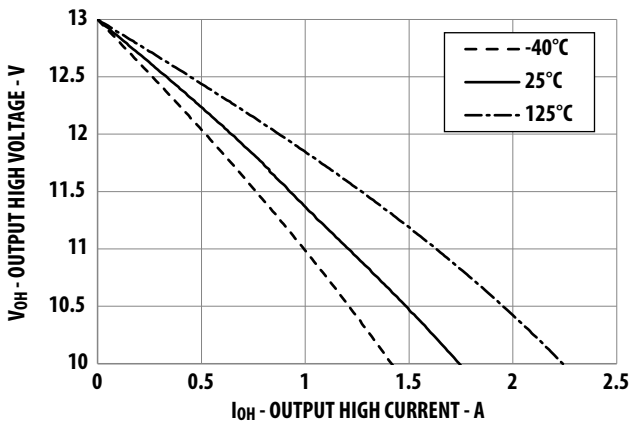


Figure 8  $V_{OL}$  vs.  $I_{OL}$

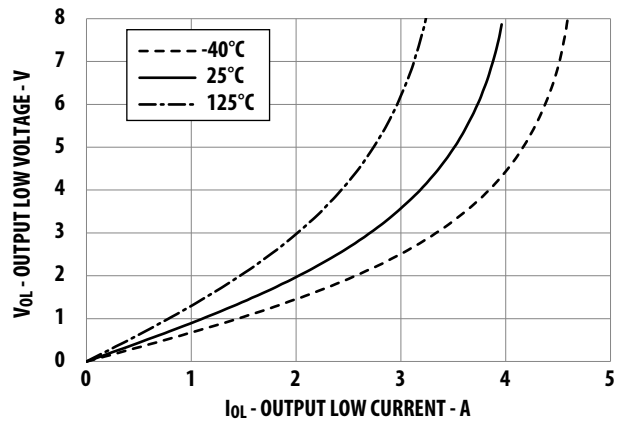


Figure 9  $T_p$  across Temperature

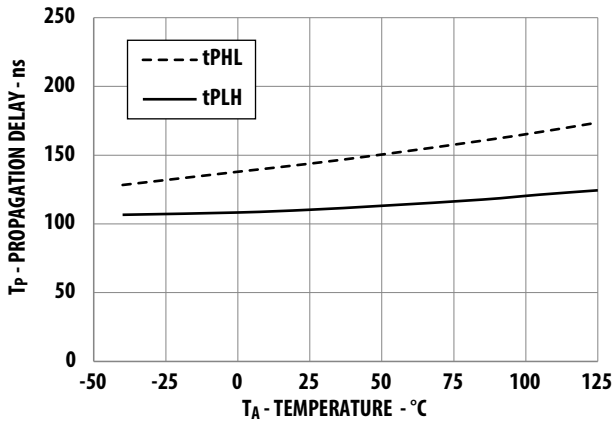


Figure 10  $V_{DESAT}$  Threshold across Temperature

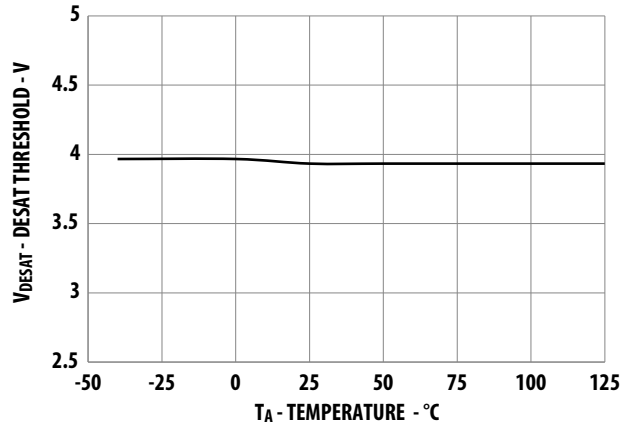
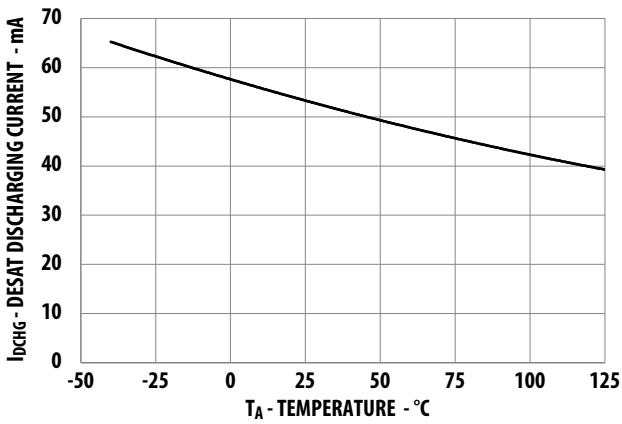
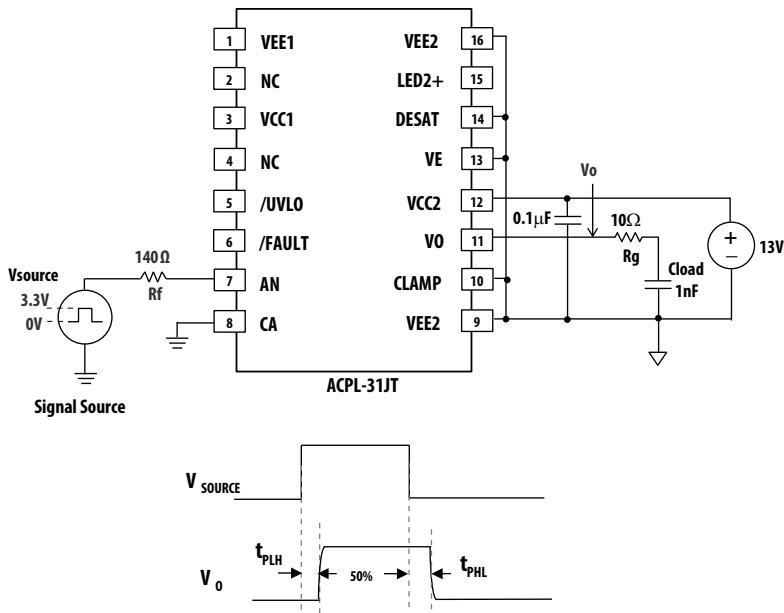


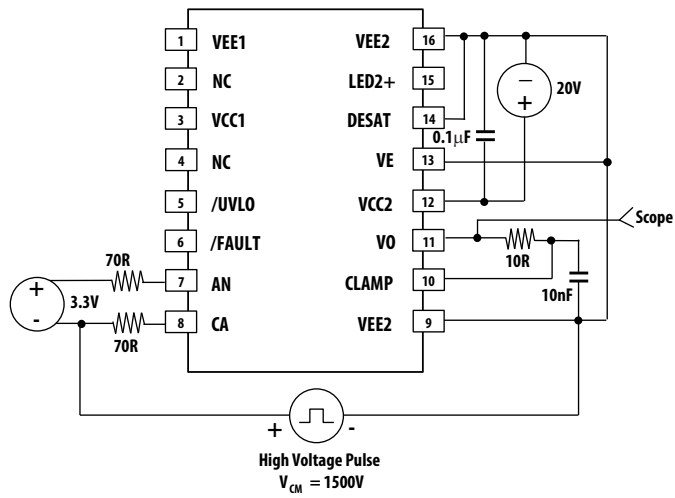
Figure 11  $I_{DCHG}$  across Temperature



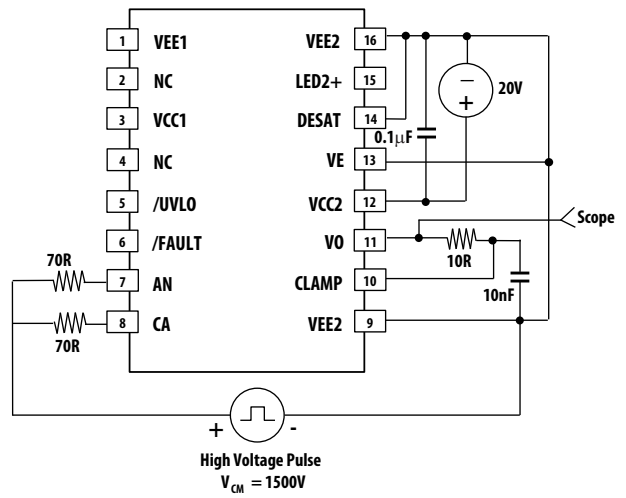
**Figure 12 Propagation Delay Test Circuit and Timing Diagram**



**Figure 13 CMR Vo High Test Circuit**



**Figure 14 CMR Vo Low Test Circuit**







### Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the LED current. When LED current is driven high the output of ACPL-31JT is capable of delivering 2.5-A sourcing current to drive the MOSFET's gate. While LED is switched off the gate driver can provide 2.5-A sinking current to switch the gate off fast. Additional miller clamping pull-down transistor is activated when output voltage reaches about 2V with respect to  $V_{EE2}$  to provide low impedance path to miller current as shown in Figure 17.

### Description of Under Voltage Lock Out

Insufficient gate voltage to MOSFET can increase turn on resistance of MOSFET, resulting in large power loss and MOSFET damage due to high heat dissipation. ACPL-31JT monitors the output power supply constantly. When output power supply is lower than under voltage lockout (UVLO) threshold gate driver output will shut off to protect MOSFET from low voltage bias. During power up, the UVLO feature forces the gate driver output to low to prevent unwanted turn-on at lower voltage.

Figure 17 Gate Drive Signal Behavior

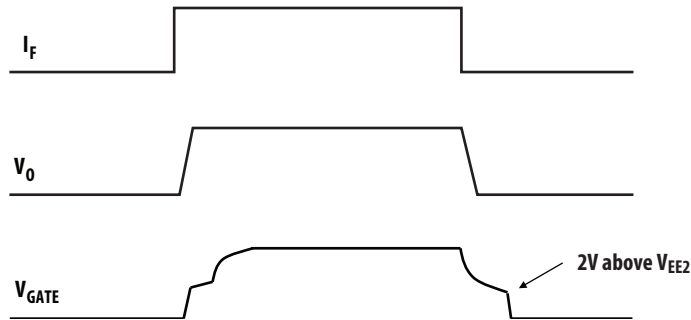
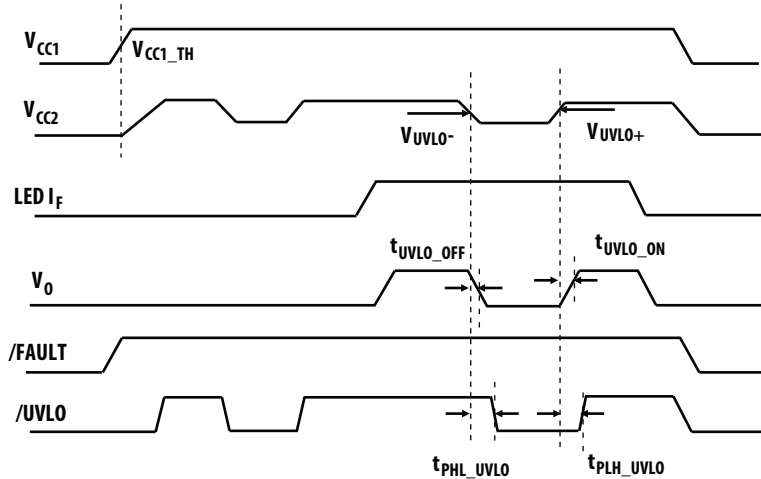


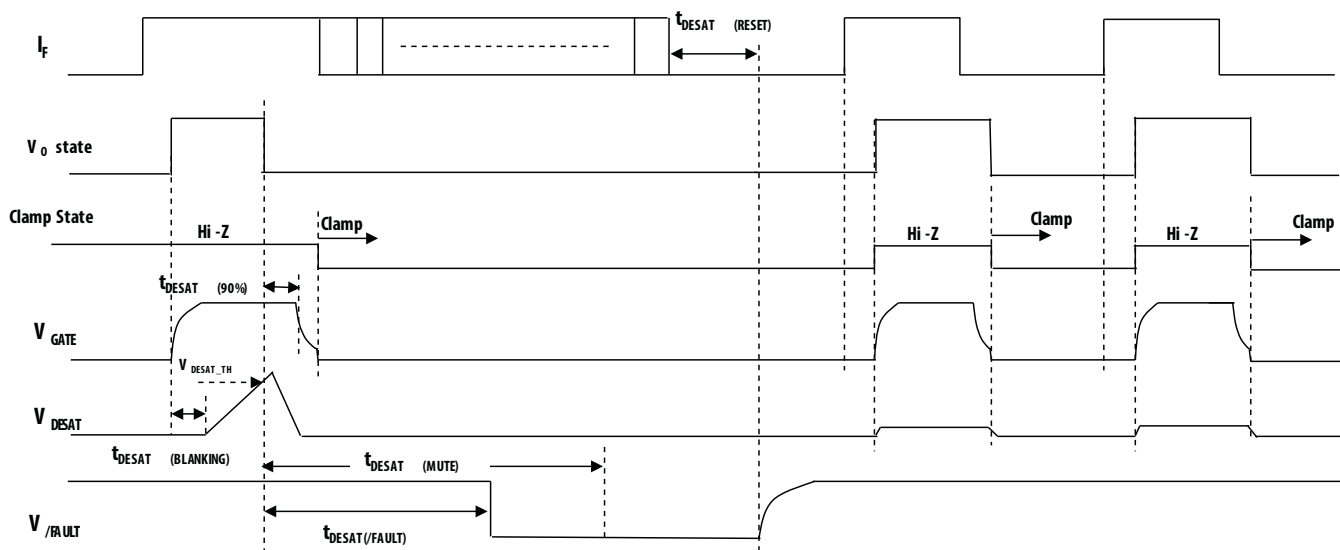
Figure 18 Circuit Behaviors at Power-up and Power-down



## Description of Operation during Over Current Condition

1. DESAT terminal monitors MOSFET's Drain-Source voltage,  $V_{DS}$ .
2. When the voltage on the DESAT terminal exceeds Desat sensing threshold, the output shuts down immediately.
3. FAULT output goes low, notifying the microcontroller of the fault condition.
4. Microcontroller takes appropriate action.
5. When  $t_{DESAT(MUTE)}$  expires LED input need to be kept low for  $t_{DESAT(RESET)}$  before fault condition is cleared. FAULT status will return to high and CLAMP output will return to Hi-Z state.
6. Output ( $V_O$ ) starts to respond to LED input after fault condition is cleared.

Figure 19 Circuit Behaviors during Over Current Event

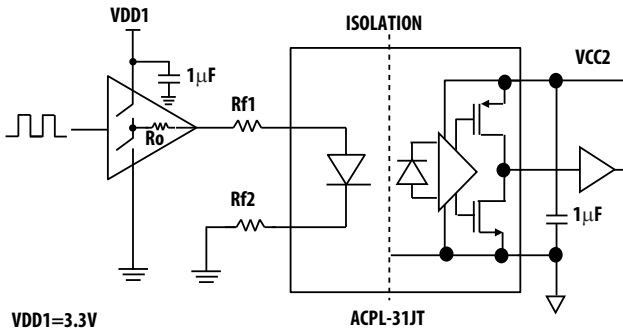


## Recommended LED Drive Circuits

There will be common mode noise whenever there is a difference in the ground level of the optocoupler's input control circuitry and that of the output control circuitry. Figure 20 and Figure 21 show the recommended LED drive circuits that use logic gate (CMOS buffer) for high common mode rejection (CMR) performance of the optocoupler gate driver. Split limiting resistors are used to balance the impedance at both anode and cathode of the input LED for high common mode noise rejection. The output impedance of the CMOS buffer (shown as  $R_O$  in Figure 20 and Figure 21) has to be included in the calculation for LED drive current.

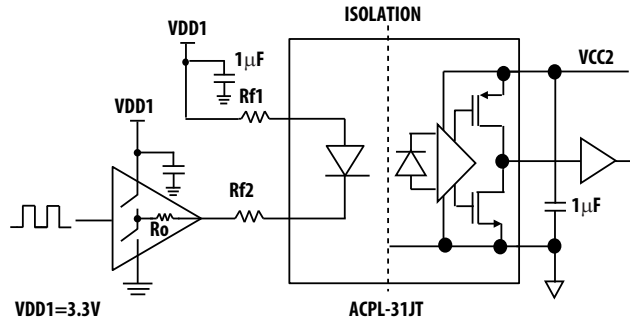
On the other hand, Figure 22 and Figure 23 show the recommended LED drive circuits that use a single transistor. During the LED off state, M1 and Q1 in Figure 22 and Figure 23 will shunt current, which results in greater power consumption. It is not recommended to have open drain and open collector drive circuits, as shown in Figure 24 and Figure 25. This is because during the off state of the MOSFET/transistor, the cathode of the input LED sees high impedance and becomes sensitive to common mode switching noise.

**Figure 20 Recommended Non-inverting Drive Circuit**



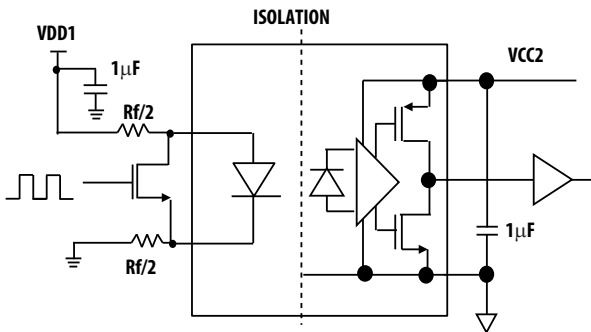
VDD1=3.3V  
 $Rf2 = Rf1 + Ro$   
 Recommended  $Ro + Rf1 + Rf2 = 140\Omega$

**Figure 21 Recommended Inverting Drive Circuit**



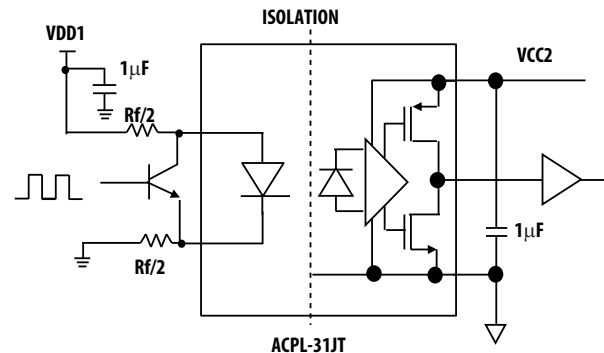
VDD1=3.3V  
 $Rf1 = Rf2 + Ro$   
 Recommended  $Ro + Rf1 + Rf2 = 140\Omega$

**Figure 22 Recommended Single Transistor Drive Circuit**



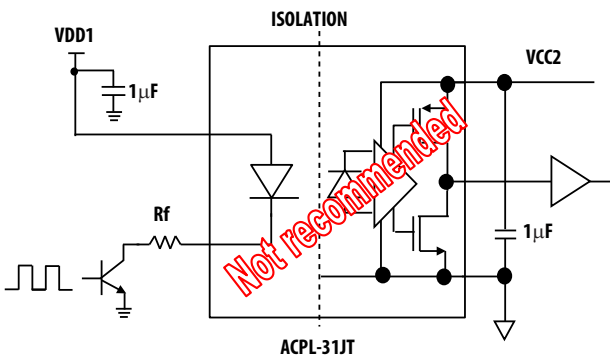
VDD1=3.3V  
 Recommended  $Rf = 140\Omega$

**Figure 23 Recommended Single Transistor Drive Circuit**

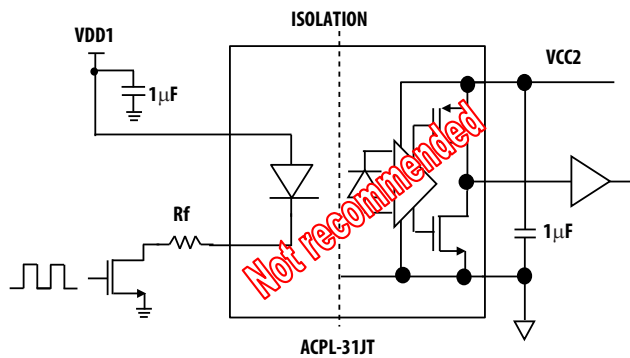


VDD1=3.3V  
 Recommended  $Rf = 140\Omega$

**Figure 24 Not Recommended – Open Drain/Open Collector Drive Circuit**



**Figure 25 Not Recommended – Open Drain/Open Collector Drive Circuit**



### Drive Power

If a CMOS buffer is used to drive the LED, it is recommended that user connect the CMOS buffer at the LED cathode. This is because the sinking capability of the NMOS is usually greater than the driving capability of the PMOS in a CMOS buffer.

### Drive Logic

The designer can configure LED drive circuits for non-inverting and inverting logic as recommended in [Figure 21](#), [Figure 22](#), and [Figure 23](#). For the inverting and non-inverting logic to work, the external power supply VDD1 must be connected to the CMOS buffer. If the VDD1 supply is lost, the LED will be permanently off and output will be low.

### Bypass and Reservoir Capacitors

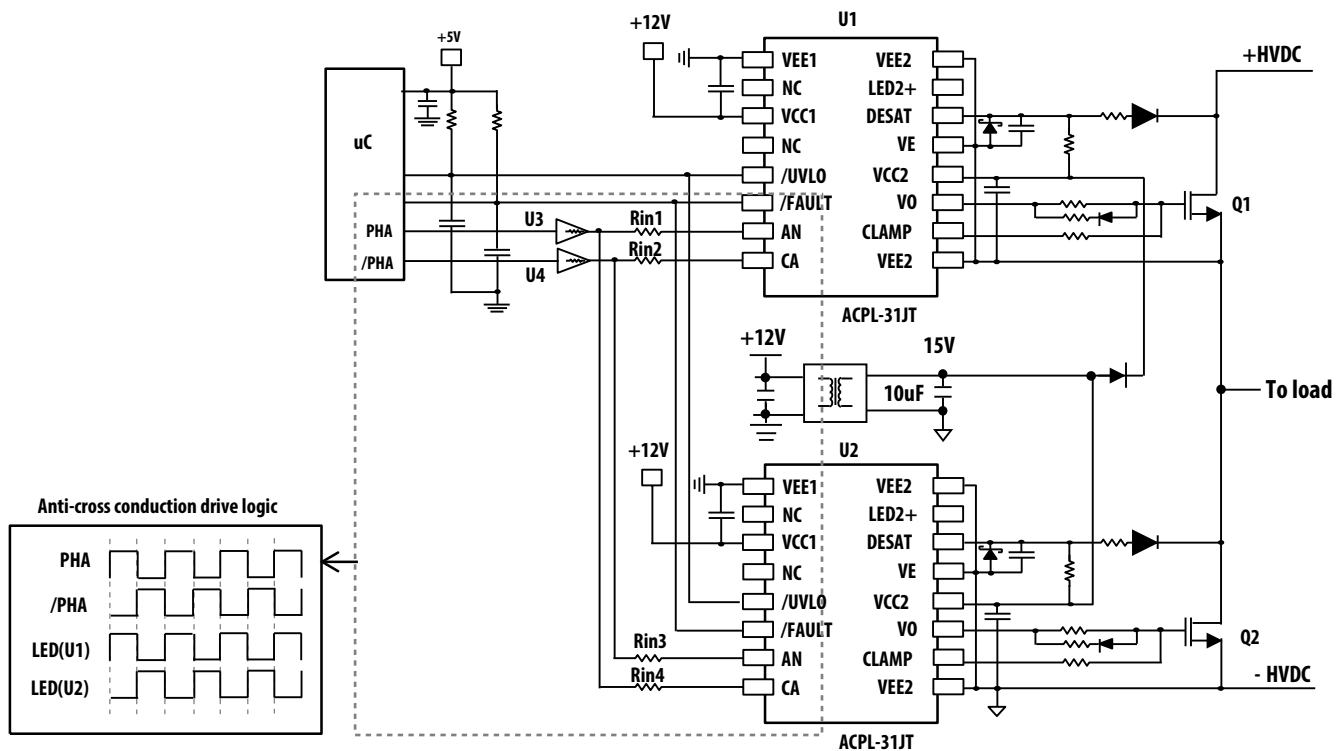
Supply bypass capacitors are necessary at the input buffer and ACPL-31JT output supply pins. A ceramic capacitor with the value of 1 μF is recommended at the input buffer to provide high frequency bypass, which also helps to improve CMR

performance. At the output supply pins, it is recommended to use a 1-μF low ESR and low ESL capacitor across VCC2 – VE, VE – VEE2 and VCC2 – VEE2 pins. These capacitors are used to supply instant driving current to MOSFET at VOUT during switching.

### Anti-Cross Conduction Drive

One of the many benefits of using ACPL-31JT is the ease of implementing anti-cross conduction drive between the high side and the low side gate drivers to prevent a shoot-through event. This safety interlock drive can be realized by interlocking the output of buffer U3 and U4 to both the high and the low side gate drivers, as shown in [Figure 26](#). Due to the difference in propagation delay between optocouplers, however, a certain amount of dead time has to be added to ensure sufficient dead time at the MOSFET gate. For more details, see [Dead Time Distortion and Propagation Delay](#).

**Figure 26 Typical High-Speed MOSFET Gate Drive Circuit**



### Dead Time Distortion and Propagation Delay

Dead time is the period of time during which both high side and low side power transistors (shown as Q1 and Q2 in Figure 26) are off. Originally, the system is required to design in some amount of dead time to compensate for the turnoff delay needed for the MOSFET to discharge the input capacitance after the gate is switched off. In this application note, this amount of dead time is called system original dead time. When an optocoupler is used, the designer has to consider the effect of the optocoupler’s dead time distortion (DTD) toward system original dead time. The optocoupler’s negative DTD decreases system original dead time; on the other hand, the optocoupler’s positive DTD increases system original dead time. Therefore, the designer must add extra dead time to system original dead time to compensate for the optocoupler’s negative DTD. Figure 27 and Figure 28 illustrate the effect of the optocoupler’s DTD to system original dead time.

Here is an example of total dead time calculation for a typical optocoupler drive circuit for MOSFET.

Total dead time required

$$= \text{System original dead time} + |\text{optocoupler's negative DTD}|$$

$$= \text{System original dead time} + |100 \text{ ns}|$$

where system original dead time = MOSFET turn-off delay

**NOTE** The propagation delays used to calculate dead time distortion (DTD) are taken at equal temperatures and test conditions as the optocouplers used under consideration are typically mounted in close proximity to each other and are switching same type of MOSFETs.

### Dead Time and Propagation Delay Waveforms

Figure 27 Negative DTD Reduces Original DT

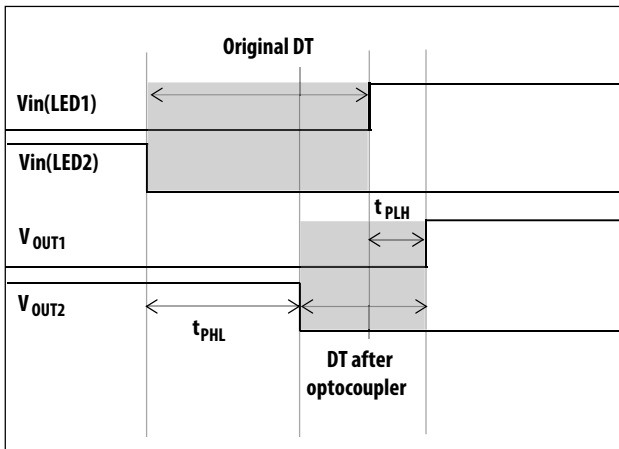
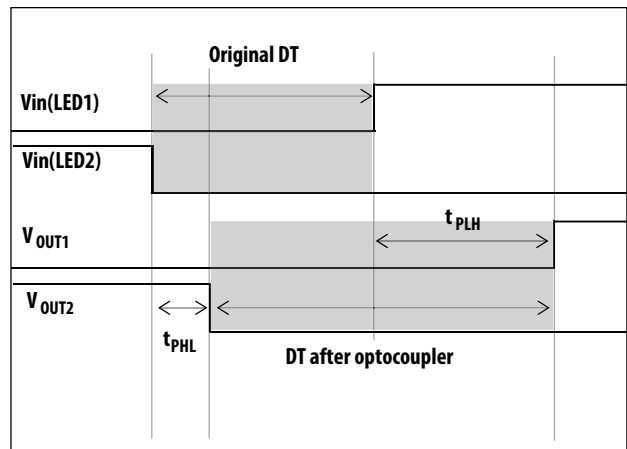


Figure 28 Positive DTD Increases Original DT

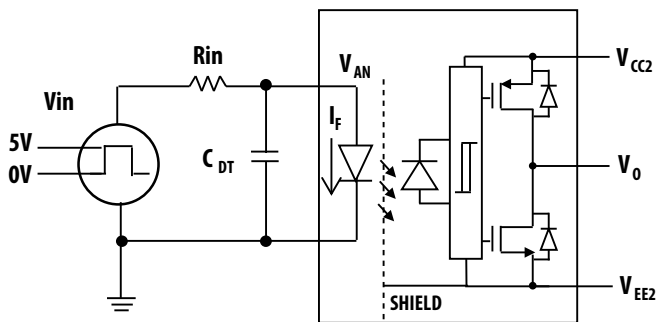


## Programmable Dead Time

Programmable dead time can be introduced to an optocoupler gate driver by adding an external capacitor (C) across the input LED (Anode and Cathode) as shown in Figure 29. This simple circuitry offers you the flexibility to optimize gate drive switching timing for various MOSFETs and applications through hardware configuration.

The value of the external capacitor (CDT) can be calculated based on the minimum dead time requirement for the system, as shown in the following equation. The added dead time will delay the turn-on timing of the gate signal, as shown in Figure 30.

Figure 29 Add CDT for Dead Time Programming



Where

$$C_{DT(MIN)} = - \frac{DT_{(min)}}{R_{in(min)} \ln \left( 1 - \frac{V_{F(min)} - V_{in(off)}}{V_{in(on)} - V_{in(off)}} \right)}$$

DT: Total dead time required for a system, inclusive of original dead time and the optocoupler’s negative DTD

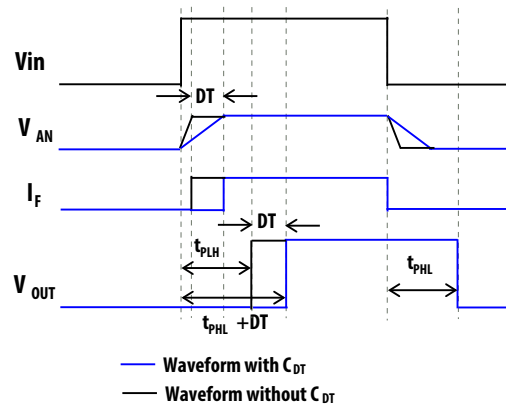
R<sub>in</sub>: Total input LED current-limiting resistor

C<sub>DT</sub>: External Dead time programming capacitor

V<sub>F</sub>: Input LED forward voltage

V<sub>i</sub>n: Input PWM voltage

Figure 30 Timing Diagram with and without C<sub>DT</sub>



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For product information and a complete list of distributors, please go to our web site: [www.broadcom.com](http://www.broadcom.com).

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