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Automotive 2.5 Amp Gate Drive Optocoupler with Integrated Flyback Controller for Isolated DC-DC Converter, Integrated IGBT Desat Over Current Sensing, Miller Current Clamping and UVLO Feedback

Data Sheet

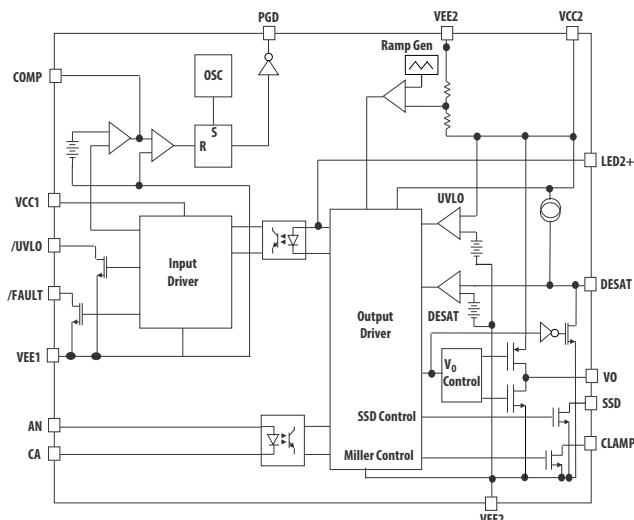
Description

The ACPL-33JT Automotive 2.5 Amp Gate Drive Optocoupler features integrated flyback controller for isolated DC-DC converter, IGBT desaturation sensing and fault feedback, Under-Voltage LockOut (UVLO) with soft-shutdown and fault feedback and active Miller current clamping. The fast propagation delay with excellent timing skew performance enables excellent timing control and efficiency. This full feature optocoupler comes in a compact, surface-mountable SO-16 package for space-savings, is suitable for traction power train inverter, power converter, battery charger, air-conditioner and oil pump motor drives in HEV and EV applications.

Avago R2Coupler® isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

Functional Diagram

Figure 1 ACPL-33JT Functional Diagram



Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: -40°C to +125°C
- Integrated flyback controller for isolated DC-DC converter
- Regulated output voltage: 16V
- Peak output current: 2.5A max.
- Miller clamp sinking current: 2A
- Input supply voltage range: 4.5V to 5.5V
- Common mode rejection (CMR): > 50 kV/μs at V_{CM} = 1500V
- Propagation delay: 250 ns max.
- Integrated fail-safe IGBT protection
 - Desat sensing, “soft” IGBT turn-off and fault feedback
 - Under voltage lock-out (UVLO) protection with feedback
- High noise immunity
 - Miller current clamping
 - Direct LED input with low input impedance and low noise sensitivity
- SO-16 package with 8-mm clearance and creepage
- Regulatory approvals:
 - UL1577, CSA
 - IEC/EN/DIN EN 60747-5-5

Applications

- Automotive isolated IGBT/MOSFET inverter gate drive
- Automotive DC-DC converter
- AC and brushless DC motor drives
- Hybrid and plug-in hybrid power train inverter
- Uninterruptible power supplies (UPSs)

CAUTION Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both, that might be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Table 1 Ordering Information

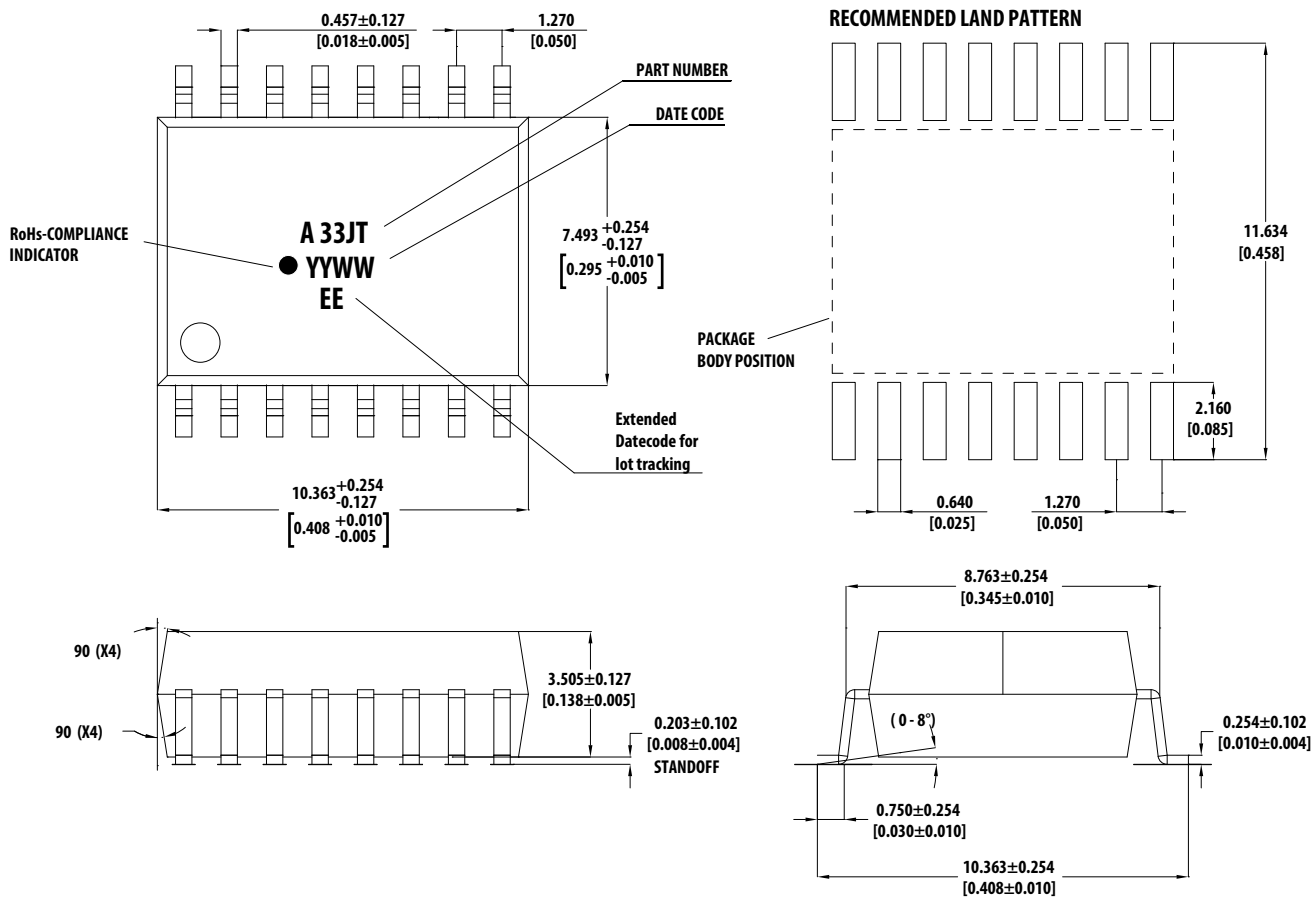
Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-33JT	-500E	SO-16	X	X	X	850 per reel

To order, choose a part number from the Part Number column and combine with the desired option from the Option column to form an order entry.

Example:

ACPL-33JT-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Figure 2 Package Outline Drawings (16-Lead Surface Mount)

Dimensions in millimeters (inches).

NOTE

- Lead coplanarity = 0.10 mm (0.004 inches) max
- Floating lead protrusion = 0.254 mm (0.010 inches) max
- Mold flash on each side = 0.254 mm (0.010 inches) max

Recommended Lead-free IR Profile

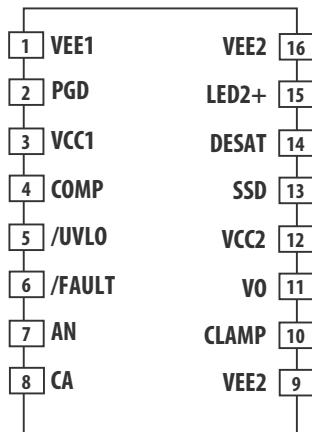
Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Non-halide flux should be used.

Product Overview Description

The ACPL-33JT (shown in [Figure 1](#)) is a highly integrated power control device that incorporates all the necessary components for a complete, reliable, isolated IGBT gate drive circuit. It features a flyback controller for isolated DC-DC converter, a high current gate driver, Miller current clamping, IGBT desaturation sensing, IGBT soft shutdown (SSD), fault feedback and under voltage lock-out (UVLO) protection and feedback in a SO-16 package. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increases its noise immunity.

Package Pinout

Figure 3 Pin out of ACPL-33JT**Table 2 Pin Description**

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	VEE1	Input IC common	16	VEE2	Output IC common and IGBT emitter reference
2	PGD	Primary gate drive for MOSFET	15	LED2+	No connection, for testing only
3	VCC1	Input power supply	14	DESAT	Desaturation over current sensing
4	COMP	Compensation network for Flyback Controller	13	SSD	Soft Shutdown
5	/UVLO	VCC2 Under Voltage Lock-Out feedback	12	VCC2	Output power supply
6	/FAULT	Over current fault feedback	11	VO	Driver output to IGBT gate
7	AN	Input LED anode	10	CLAMP	Miller current clamping output
8	CA	Input LED cathode	9	VEE2	Output IC common and IGBT emitter reference

Regulatory Information

The ACPL-33JT is approved by the following organizations:

Table 3 Regulatory Information

UL	Approved under UL 1577, component recognition program up to VISO = 5000 VRMS.
CSA	Approved under CSA Component Acceptance Notice #5, File CA 88324.
IEC/EN/DIN EN 60747-5-5	Approved under: IEC 60747-5-5, EN 60747-5-5, DIN EN 60747-5-5, IEC/EN/DIN EN60747-5-5

Table 4 IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Insulation Classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage $\leq 150 V_{rms}$ for rated mains voltage $\leq 300 V_{rms}$ for rated mains voltage $\leq 600 V_{rms}$ for rated mains voltage $\leq 1000 V_{rms}$		I – IV I – IV I – IV I – III	
Climatic Classification ^a		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1230	V_{PEAK}
Input to Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ sec, Partial discharge < 5 pC	V_{PR}	2306	V_{PEAK}
Input to Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m = 10$ sec, Partial Discharge < 5 pC	V_{PR}	1968	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60$ sec)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting values – maximum values allowed in the event of a failure Case Temperature Input Power Output Power	T_S $P_{S,INPUT}$ $P_{S,OUTPUT}$	175 400 1200	°C mW mW
Insulation Resistance at T_S , $V_{IO} = 500V$	R_S	$> 10^9$	Ohm

a. Climatic classification denotes minimum operating temperature/ maximum operating temperature/ humidity test duration.

NOTE

1. Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECC00802.
2. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulation section IEC 60747-5-5, EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

Table 5 Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110)

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	150	°C	
Operating Temperature	T_A	-40	125	°C	
Output IC Junction Temperature	T_J		150	°C	a
Average Input Current	$I_{F(AVG)}$		20	mA	
Peak Transient Input Current (<1 μ s pulse width, 300pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	V_R		6.0	V	
Input Supply Voltage ^b	$V_{CC1} - V_{EE1}$	-0.5	6.0	V	
Primary Gate Drive Voltage ^b	$V_{PGD} - V_{EE1}$	-0.5	V_{CC1}	V	
COMP Pin Voltage ^b	$V_{COMP} - V_{EE1}$	-0.5	V_{CC1}	V	
/UVLO Output Current ^c	$I_{/UVLO}$		10	mA	
/UVLO Pin Voltage ^b	$V_{/UVLO} - V_{EE1}$	-0.5	6.0	V	d
/Fault Output Current ^c	$I_{/FAULT}$		10	mA	
/Fault Pin Voltage ^b	$V_{/FAULT} - V_{EE1}$	-0.5	6.0	V	d
Output Supply Voltage ^b	$V_{CC2} - V_{EE2}$	-0.5	25	V	
Peak Output Current ^c	$ I_{O(peak)} $		2.5	A	e
Gate Drive Output Voltage ^b	$V_{O(peak)} - V_{EE2}$	-0.5	$V_{CC2}+0.5$	V	
Miller Clamping Pin Voltage ^b	$V_{CLAMP} - V_{EE2}$	-0.5	$V_{CC2}+0.5$	V	f
Desat Voltage ^b	$V_{DESAT} - V_{EE2}$	-0.5	$V_{CC2}+0.5$	V	g
Soft Shutdown Pin Voltage ^b	$V_{SSD} - V_{EE2}$	-0.5	$V_{CC2}+0.5$	V	
Output IC Power Dissipation	P_O		600	mW	a
Input IC Power Dissipation	P_I		150	mW	a

- a. Input IC power dissipation is derated linearly above 10 0°C from 15 0mW to 100 mW at 125 °C for high effective thermal conductivity board. Output IC power dissipation is derated linearly above 100 °C from 600 mW to 350 mW at 125 °C for high effective thermal conductivity board; see [Figure 6](#). For power derating with low effective thermal conductivity board, see [Figure 5](#).
- b. Absolute maximum voltage ratings imply transistor off state.
- c. Absolute maximum current ratings imply transistor on state.
- d. Duration of absolute maximum voltage applied to /UVLO or /Fault pin during the internal MOS turns ON is limited to maximum 10 μ s with maximum 5% duty cycle.
- e. Maximum pulse width=1 μ s, maximum duty cycle=1%.
- f. When CLAMP pin is turned on, maximum pulse width is limited to 1 μ s, maximum duty cycle=2%.
- g. Maximum pulse width=5 μ s, maximum duty cycle=10%.

Table 7 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Temperature	T_A	-40	125	°C	
Input IC Supply Voltage	V_{CC1}	4.5	5.5	V	a
Total Output IC Supply Voltage	$V_{CC2} - V_{EE2}$	15.2	16.8	V	b
Input LED Turn on Current	$I_{F(ON)}$	10	16	mA	
Input LED Turn off Voltage (VAN-VCA)	$V_{F(OFF)}$	-5.5	0.8	V	
Maximum PWM Duty Cycle	D_{MAX}		50	%	
Input Pulse Width	$t_{ON(LED)}$	500		ns	

- a. In most applications, V_{CC1} will be powered up first (before V_{CC2}) and powered down last (after V_{CC2}). This is desirable for maintaining control of the IGBT gate. In applications where V_{CC2} is powered up first, it is important to ensure that the input remains low until V_{CC1} reaches the proper operating voltage to avoid any momentary instability at the output during V_{CC1} ramp-up or ramp-down).
- b. 15.2V is the recommended minimum operating supply voltage ($V_{CC2} - V_{EE2}$) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 14.5V.

Electrical Specifications

Unless otherwise specified, all Minimum/Maximum specifications are at recommended operating conditions, all voltages at input IC are referenced to V_{EE1} , all voltages at output IC are referenced to V_{EE2} . All typical values at $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - V_{EE2} = 16\text{ V}$.

Table 8 Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
DCDC Flyback Converter								
VCC1 MOS Threshold	V_{CC1_MOSTH}	0.4	1.2	1.7	V	$I_{FAULT} = 2.0\text{ mA}$		
VCC1 Turn on Threshold	V_{CC1_TH}	3.7	4.0	4.3	V			
VCC1 Turn on Threshold Hysteresis	$V_{CC1_TH_HYS}$	0.05	0.3	0.5	V			
PWM Switching Frequency	f_{PWM}	100	150	190	kHz			a
Primary Gate Drive Rise Time	t_{rPGD}	3	16	40	ns	$C_{PGD} = 1\text{ nF}$		
Primary Gate Drive Fall Time	t_{fPGD}	3	14	40	ns	$C_{PGD} = 1\text{ nF}$		
Maximum PWM Duty Cycle	D_{MAX}	50	55	60	%		8	
Regulated VCC2 Voltage	$V_{CC2} - V_{EE2}$	15.2	16.0	16.8	V			
VCC2 Over Voltage Protection Threshold	V_{OV_TH}	18.0	20.5	22.0	V			
VCC2 Over Voltage Protection Threshold Hysteresis	$V_{OV_TH_HYS}$	0.4	0.8	1.2	V			
IC Supply Current								
Input Supply Current	I_{CC1}		4.7	6.2	mA	$V_{COMP} = 0\text{ V}$	10	
Output Supply Current	I_{CC2}	6.5	10.30	14.20	mA	$I_F = 0\text{ mA}$	11	
Logic Input and Output								
LED Forward Voltage	V_F	1.25	1.55	1.85	V	$I_F = 10\text{ mA}$	12	
LED Reverse Breakdown Voltage	V_{BR}	6.0	11		V	$I_F = 10\text{ }\mu\text{A}$		
Input Capacitance	C_{IN}		90		pF			b

Table 8 Electrical Specifications (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
LED Turn on Current Threshold Low-to-High	I_{TH+}	0.5	2.7	7.5	mA	$V_O = 5V$	13	
LED Turn on Current Threshold High-to-Low	I_{TH-}	0.3	2.3	7.0	mA	$V_O = 5V$	13	
LED Turn on Current Hysteresis	I_{TH_HYS}		0.4		mA			
/FAULT Logic Low Output Current	I_{FAULT_L}	4	10	20	mA	$V_{FAULT} = 0.4V$		
/FAULT Logic High Output Current	I_{FAULT_H}		0.01	2	μA	$V_{FAULT} = 5V$		
/UVLO Logic Low Output Current	I_{UVLO_L}	4	10	20	mA	$V_{UVLO} = 0.4V$		
/UVLO Logic High Output Current	I_{UVLO_H}		0.01	2	μA	$V_{UVLO} = 5V$		
Gate Driver								
High Level Output Current	I_{OH}		-1.7	-0.5	A	$V_O = V_{CC2} - 3V$	14	
Low Level Output Current	I_{OL}	0.5	2.4		A	$V_O = V_{EE2} + 2.5V$	15	
High Level Peak Output Current	I_{OH_PEAK}			-2	A	$V_O = V_{CC2} - 14V$		c
Low Level Peak Output Current	I_{OL_PEAK}	2			A	$V_O = V_{EE2} + 14V$		c
High Level Output Voltage	V_{OH}	$V_{CC2}-0.5$	$V_{CC2}-0.2$		V	$I_O = -100\text{ mA}$		d, e
Low Level Output Voltage	V_{OL}		0.1	0.5	V	$I_O = 100\text{ mA}$		
IF to High Level Output Propagation Delay Time	t_{PLH}	50	115	250	ns	$R_g = 10\Omega$ $C_g = 10\text{ nF}$ $f = 10\text{ kHz}$ Duty Cycle = 50%	16, 21	f
IF to Low Level Output Propagation Delay Time	t_{PHL}	50	150	300	ns		16, 21	g
Pulse Width Distortion	PWD	-175	35	230	ns			h, i
Dead Time Distortion	DTD	-230	-35	175	ns			i, j
VO 10% to 90% Rise Time	t_R	10	76	280	ns			
VO 90% to 10% Fall Time	t_F	10	41	280	ns			
Output High Level Common Mode Transient Immunity	$ CM_H $	30	>50		kV/s	$T_A = 25^\circ C$, $I_F = 10\text{ mA}$, $V_{CM} = 1500V$	23	k
Output Low Level Common Mode Transient Immunity	$ CM_L $	30	>50		kV/s	$T_A = 25^\circ C$, $I_F = 0\text{ mA}$, $V_{CM} = 1500V$	24	l
Active Miller Clamp and Soft Shutdown								
Low Level SSD Current During Fault Condition	I_{SSDLF}	90	150	210	mA	$V_{SSD} = 14V$	17	
Clamp Threshold Voltage	V_{TH_CLAMP}	1	2.1	3	V			
Clamp Low Level Sinking Current	I_{CLAMP}	0.5	2		A	$V_{CLAMP} = V_{EE2} + 2.5V$		
V_{CC2} UVLO Protection								
V _{CC2} UVLO Threshold Low to High	V_{UVLO+}	12	13.4	14.5	V	$V_O > 5V$		e, m
V _{CC2} UVLO Threshold High to Low	V_{UVLO-}	10	11.3	12.5	V	$V_O < 5V$		e, n
V _{CC2} UVLO Hysteresis	V_{UVLO_HYS}	1.6	2.1	2.4	V			

Table 8 Electrical Specifications (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
V _{CC2} to UVLO High Delay	t _{PLH_UVLO}		9	20	μs		30	o
V _{CC2} to UVLO Low Delay	t _{PHL_UVLO}		7	20	μs		30	p
V _{CC2} UVLO to VOUT High Delay	t _{UVLO_ON}		5	6.5	μs		30	q
V _{CC2} UVLO to VOUT Low Delay	t _{UVLO_OFF}		1.1	2	μs		30	r
Desaturation Protection								
Desat Sensing Threshold	V _{DESAT}	6.65	7.0	7.35	V		18	
Desat Charging Current	I _{CHG}	0.8	1.0	1.2	mA	V _{DESAT} = 0V, V _{DESAT} = 6V	19	
Desat Discharging Current	I _{DSCHG}	19	60	106	mA	V _{DESAT} = 7.5V	20	
Desat Blanking Time	t _{DESAT(BLANKING)}	0.3	0.6	0.9	μs	RSSD = 0 Ω C _g = 10 nF	30	s
Desat Sense to 90% VGATE Delay	t _{DESAT(90%)}	0.05	0.2	0.5	μs		22, 30	t
Desat Sense to 10% VGATE Delay	t _{DESAT(10%)}	0.5	1.2	2	μs		22, 30	u
Desat to Low Level FAULT Signal Delay	t _{DESAT(FAULT)}		4.4	8	μs			v
Output Mute Time due to Desaturation	t _{DESAT(MUTE)}	3	7.5	12	ms		30	w
Time Input Kept Low Before Fault Reset to High	t _{DESAT(RESET)}	3	7.5	12	ms		30	x

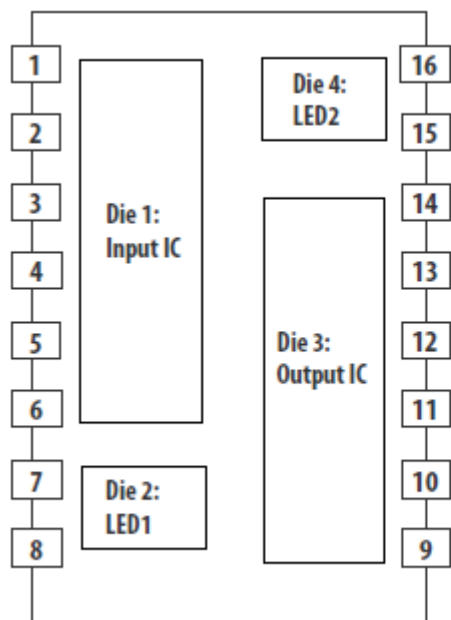
- a. PWM switching frequency of primary gate drive (PGD) is dithered in a range of ±6% typically over 3.3 ms.
- b. C_{IN} is measured between pin 7 and pin 8 of the IC.
- c. Maximum pulse width=1 μs, maximum duty cycle=1%.
- d. Maximum pulse width = 1.0 ms, maximum duty cycle = 1%.
- e. Once V_{OH} of ACPL-33JT is allowed to go high (V_{CC2} – V_{EE2} > V_{UVLO}), the DESAT detection features of the ACPL-33JT will be the primary source of IGBT protection. Once V_{CC2} exceeds V_{UVLO+} threshold, DESAT will remain functional until V_{CC2} is below V_{UVLO-} threshold. Thus, the DESAT detection and UVLO features of the ACPL-33JT work in conjunction to ensure constant IGBT protection.
- f. t_{PLH} is defined as propagation delay from 50% of LED input I_F to 50% of High level output.
- g. t_{PHL} is defined as propagation delay from 50% of LED input I_F to 50% of Low level output.
- h. Pulse Width Distortion (PWD) is defined as (t_{PHL} – t_{PLH}) of any given unit.
- i. As measured from I_F to V_O.
- j. Dead Time Distortion (DTD) is defined as (t_{PLH} – t_{PHL}) between any two ACPL-33JT under the same test conditions.
- k. Common mode transient immunity in the output high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output remains in the high state (that is, V_O > 14V). CM_H specification is guaranteed by design and not subjected to production test.
- l. Common mode transient immunity in the output low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output remains in the low state (that is, V_O < 2.0V). CM_L specification is guaranteed by design and not subjected to production test.
- m. This is the “increasing” (that is, turn-on or “positive going” direction) of V_{CC2} – V_{EE2}.
- n. This is the “decreasing” (that is, turn-off or “negative going” direction) of V_{CC2} – V_{EE2}.
- o. The delay time when V_{CC2} exceeded UVLO+ threshold to 50% of /UVLO positive going edge.
- p. The delay time when V_{CC2} exceeded UVLO- threshold to 50% of /UVLO negative going edge.
- q. The delay time when V_{CC2} exceeded UVLO+ threshold to 50% of High level output.
- r. The delay time when V_{CC2} exceeded UVLO- threshold to 50% of Low level output.
- s. The delay time for ACPL-33JT to respond to a DESAT fault condition without any external DESAT capacitor.
- t. The amount of time from when DESAT threshold is exceeded to 90% of V_{GATE} at mentioned test conditions.
- u. The amount of time from when DESAT threshold is exceeded to 10% of V_{GATE} at mentioned test conditions.
- v. The amount of time from when DESAT threshold is exceeded to /Fault output Low – 50% of V_{CC1} voltage.
- w. The amount of time when DESAT threshold is exceeded, Output is mute to LED input.
- x. The amount of time when DESAT Mute time is expired, LED input must be kept Low for Fault status to return to High.

Table 9 Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary						
Withstand Voltage	V_{ISO}	5000			V_{RMS}	$RH < 50\%$, $t = 1 \text{ min.}$, $T_A = 25^\circ\text{C}$
Resistance (Input-Output)	R_{I-O}	10^9	10^{14}		Ω	$V_{I-O} = 500 \text{ Vdc}$
Capacitance (Input-Output)	C_{I-O}		0.8		pF	$f = 1 \text{ MHz}$

Thermal Resistance Model for ACPL-33JT

The diagram for measurement is shown in [Figure 4](#). This is a multi chip package with four heat sources, the effect of heating of one die due to the adjacent dice are considered by applying the theory of linear superposition. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated and all the dice temperatures are recorded and so on until the 4th die is heated. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4 by 4 matrix for our case of four heat sources.

Figure 4 Diagram of ACPL-33JT for Measurement

$$\begin{vmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{vmatrix} \cdot \begin{vmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{vmatrix}$$

R_{11} : Thermal Resistance of Die1 due to heating of Die1 (C/W)
 R_{12} : Thermal Resistance of Die1 due to heating of Die2 (C/W)
 R_{13} : Thermal Resistance of Die1 due to heating of Die3 (C/W)
 R_{14} : Thermal Resistance of Die1 due to heating of Die4 (C/W)
 R_{21} : Thermal Resistance of Die2 due to heating of Die1 (C/W)
 R_{22} : Thermal Resistance of Die2 due to heating of Die2 (C/W)
 R_{23} : Thermal Resistance of Die2 due to heating of Die3 (C/W)
 R_{24} : Thermal Resistance of Die2 due to heating of Die4 (C/W)
 R_{31} : Thermal Resistance of Die3 due to heating of Die1 (C/W)
 R_{32} : Thermal Resistance of Die3 due to heating of Die2 (C/W)
 R_{33} : Thermal Resistance of Die3 due to heating of Die3 (C/W)
 R_{34} : Thermal Resistance of Die3 due to heating of Die4 (C/W)
 R_{41} : Thermal Resistance of Die4 due to heating of Die1 (C/W)
 R_{42} : Thermal Resistance of Die4 due to heating of Die2 (C/W)
 R_{43} : Thermal Resistance of Die4 due to heating of Die3 (C/W)
 R_{44} : Thermal Resistance of Die4 due to heating of Die4 (C/W)

P_1 : Power dissipation of Die1 (W)
 P_2 : Power dissipation of Die2 (W)
 P_3 : Power dissipation of Die3 (W)
 P_4 : Power dissipation of Die4 (W)

T_1 : Junction temperature of Die1 due to heat from all dice (0 °C)
 T_2 : Junction temperature of Die2 due to heat from all dice (0 °C)
 T_3 : Junction temperature of Die3 due to heat from all dice (0 °C)
 T_4 : Junction temperature of Die4 due to heat from all dice (0 °C)

T_a : Ambient temperature (°C)

ΔT_1 : Temperature difference between Die1 junction and ambient (°C)
 ΔT_2 : Temperature difference between Die2 junction and ambient (°C)
 ΔT_3 : Temperature difference between Die3 junction and ambient (°C)
 ΔT_4 : Temperature difference between Die4 junction and ambient (°C)

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + T_a \text{ ----- (1)}$$


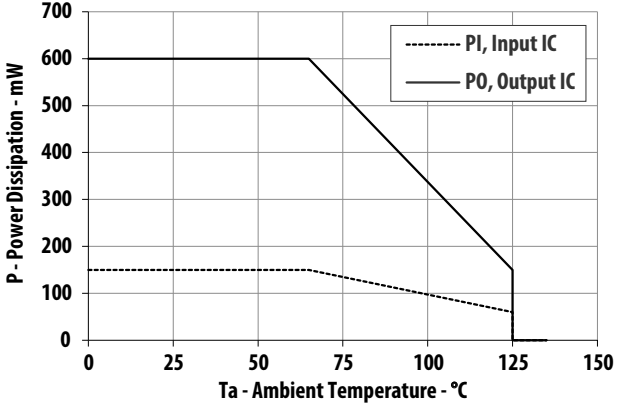

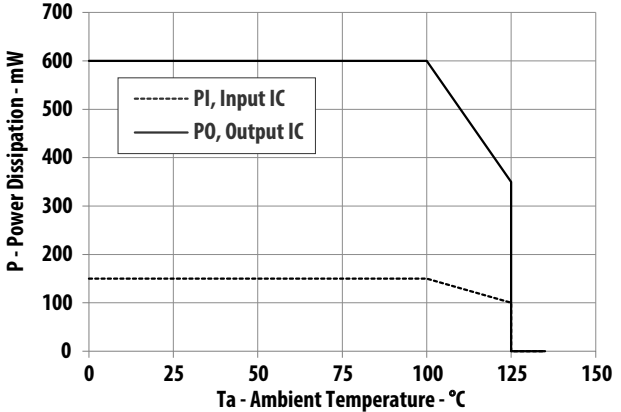
$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + T_a \text{ ----- (2)}$$

$$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + T_a \text{ ----- (3)}$$

$$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + T_a \text{ ----- (4)}$$

Measurement is done on low effective thermal conductivity board according to JEDEC Standard 51-3 and on high effective thermal conductivity board according to JEDEC Standard 51-7.

Table 10 Test Boards

Test Board	Test Board Conditions	Thermal Resistance	Power Dissipation Derating Chart
<p>Low effective thermal conductivity board</p>  <p>76 mm × 76 mm</p>	<p>Single layer board for signal</p> <p>Outer layer: 2 oz. copper thickness</p>	<p>R11 = 138°C/W R12 = 87°C/W R13 = 67°C/W R14 = 87°C/W R21 = 89°C/W R22 = 241°C/W R23 = 81°C/W R24 = 95°C/W R31 = 73°C/W R32 = 92°C/W R33 = 117°C/W R34 = 118°C/W R41 = 86°C/W R42 = 96°C/W R43 = 111°C/W R44 = 225°C/W</p>	<p>Figure 5 PowerDerating Chart Using Low Effective Thermal Conductivity Board</p>  <p>NOTE</p> <ul style="list-style-type: none"> Input IC power dissipation is derated linearly above 65°C from 150 mW to 60 mW at 125°C. Output IC power dissipation is derated linearly above 65°C from 600 mW to 150 mW at 125°C.
<p>High effective thermal conductivity board</p>  <p>76 mm × 76 mm</p>	<p>4-layer board that embodies two signal layers, a power plane and a ground plane</p> <p>Outer layers: 2 oz. copper thickness</p> <p>Inner layers: 1 oz. copper thickness</p>	<p>R11 = 78°C/W R12 = 34°C/W R13 = 23°C/W R14 = 29°C/W R21 = 37°C/W R22 = 165°C/W R23 = 32°C/W R24 = 31°C/W R31 = 24°C/W R32 = 33°C/W R33 = 59°C/W R34 = 48°C/W R41 = 32°C/W R42 = 34°C/W R43 = 51°C/W R44 = 136°C/W</p>	<p>Figure 6 Power Derating Chart Using High Effective Thermal Conductivity Board</p>  <p>NOTE</p> <ul style="list-style-type: none"> Input IC power dissipation is derated linearly above 100°C from 150 mW to 100 mW at 125°C. Output IC power dissipation is derated linearly above 100°C from 600 mW to 350 mW at 125°C.

Notes on Thermal Calculation

Application and environmental design for ACPL-33JT needs to ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 150°C. The following equations calculate the maximum power dissipation and corresponding effect on junction temperatures and can only be used as a reference for thermal performance comparison under specified PCB layout as shown above. The thermal resistance model shown here is not meant to and will not predict the performance of a package in an application-specific environment.

Calculation of Input IC Power Dissipation, P_1

$$\text{Input IC Power Dissipation } (P_1) = P_{I(\text{Static})} + P_{I(\text{PGD})}$$

where

$$P_{I(\text{Static})} - \text{Static power dissipated by the input IC} = I_{CC1} \times V_{CC1}$$

$$P_{I(\text{PGD})} - \text{Switching power dissipated in the PGD pin} = (V_{CC1} \times Q_{G_ExtMOS} \times f_{PWM_DCDC}) \times R_{O(\text{MAX})} / (R_{O(\text{MAX})} + R_{G_PGD})$$

$$Q_{G_ExtMOS} - \text{Gate charge of external MOSFET connected to PGD pin at supply voltage}$$

$$f_{PWM_DCDC} - \text{DC-DC switching frequency}$$

$$R_{O(\text{MAX})} - \text{Maximum PGD pin output impedance} = 0.3V / 50 \text{ mA} = 6$$

$$R_{G_PGD} - \text{Gate resistance connected to PGD pin}$$

Example:

$$P_{I(\text{Static})} = 6 \text{ mA} \times 5.5V = 33 \text{ mW}$$

$$P_{I(\text{PGD})} = (5.5V \times 5 \text{ nC} \times 190 \text{ kHz}) \times 6\Omega / (6\Omega + 10\Omega) = 1.96 \text{ mW}$$

$$P_1 = 33 \text{ mW} + 1.96 \text{ mW} = 34.96 \text{ mW}$$

Calculation of Input LED Power Dissipation, P_2

$$\text{Input LED Power Dissipation } (P_2) = I_F(\text{LED}) (\text{Recommended Max.}) \times V_{F(\text{LED})} (\text{at } 125^\circ\text{C}) \times \text{Duty Cycle}$$

Example:

$$P_2 = 16 \text{ mA} \times 1.25V \times 50\% \text{ duty cycle} = 10 \text{ mW}$$

Calculation of Output IC Power Dissipation, P_3

$$\text{Output IC Power Dissipation } (P_3) = P_{O(\text{Static})} + P_{HS} + P_{LS}$$

where

$$P_{O(\text{Static})} - \text{Static power dissipated by the output IC} = I_{CC2} \times V_{CC2}$$

$$P_{HS} - \text{High side switching power dissipation at } V_O \text{ pin} = (V_{CC2} \times Q_G \times f_{PWM}) \times R_{OH(\text{MAX})} / (R_{OH(\text{MAX})} + R_{GH}) / 2$$

$$P_{LS} - \text{Low side switching power dissipation at } V_O \text{ pin} = (V_{CC2} \times Q_G \times f_{PWM}) \times R_{OL(\text{MAX})} / (R_{OL(\text{MAX})} + R_{GL}) / 2$$

$$Q_G - \text{IGBT gate charge at supply voltage}$$

$$f_{PWM} - \text{Input LED switching frequency}$$

$$R_{OH(\text{MAX})} - \text{Maximum high side output impedance} = (V_{CC2} - V_{OH(\text{MIN})}) / I_{OH(\text{MIN})}$$

$$R_{GH} - \text{Gate charging resistance}$$

$$R_{OL(\text{MAX})} - \text{Maximum low side output impedance} = V_{OL(\text{MAX})} / I_{OL(\text{MIN})}$$

$$R_{GL} - \text{Gate discharging resistance}$$

Example:

$$R_{OH(MAX)} = (V_{CC2} - V_{OH(MIN)}) / I_{OH(MIN)} = 3.0V / 0.5A = 6.0\Omega$$

$$R_{OL(MAX)} = V_{OL(MAX)} / I_{OH(MIN)} = 2.5V / 0.5A = 5.0\Omega$$

$$P_{HS} = (16V \times 1\mu C \times 10 \text{ kHz}) \times 6.0\Omega / (6.0\Omega + 10\Omega) / 2 = 30 \text{ mW}$$

$$P_{LS} = (16V \times 1\mu C \times 10 \text{ kHz}) \times 5.0\Omega / (5.0\Omega + 10\Omega) / 2 = 26.7 \text{ mW}$$

$$P_3 = 14.2 \text{ mA} \times 16V + 30 \text{ mW} + 26.7 \text{ mW} = 283.9 \text{ mW}$$

Calculation of LED2 Power Dissipation, P_4

$$\text{LED2 Power Dissipation } (P_4) = I_{F(LED2)} (\text{Design Max.}) \times V_{F(LED2)} (\text{at } 125^\circ\text{C}) \times \text{Duty Cycle}$$

Example:

$$P_4 = 16 \text{ mA} \times 1.25V \times 50\% \text{ duty cycle} = 10 \text{ mW}$$

Calculation of Junction Temperature for High Effective Thermal Conductivity Board:

$$\text{Input IC Junction Temperature} = (78^\circ\text{C/W} \times P_1 + 34^\circ\text{C/W} \times P_2 + 23^\circ\text{C/W} \times P_3 + 29^\circ\text{C/W} \times P_4) + T_a$$

$$\text{Input LED Junction Temperature} = (37^\circ\text{C/W} \times P_1 + 165^\circ\text{C/W} \times P_2 + 32^\circ\text{C/W} \times P_3 + 31^\circ\text{C/W} \times P_4) + T_a$$

$$\text{Output IC Junction Temperature} = (24^\circ\text{C/W} \times P_1 + 33^\circ\text{C/W} \times P_2 + 59^\circ\text{C/W} \times P_3 + 48^\circ\text{C/W} \times P_4) + T_a$$

$$\text{LED2 Junction Temperature} = (32^\circ\text{C/W} \times P_1 + 34^\circ\text{C/W} \times P_2 + 51^\circ\text{C/W} \times P_3 + 136^\circ\text{C/W} \times P_4) + T_a$$

Printed Circuit Board Layout Considerations

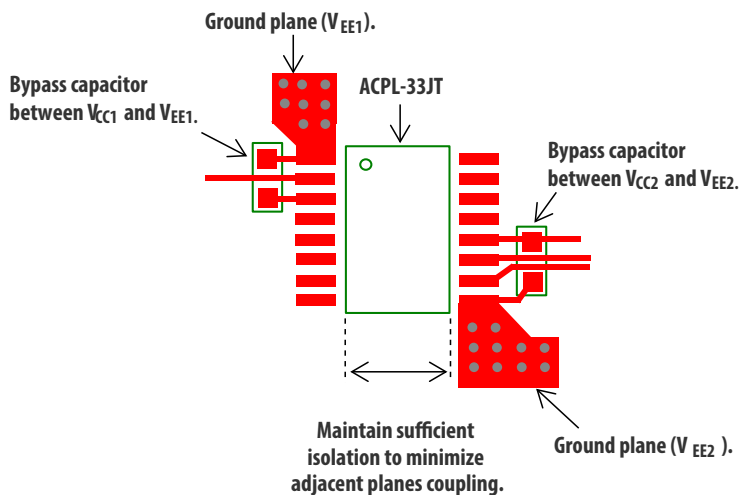
Care must be taken while designing the layout of printed circuit board (PCB) for optimum performance.

Adequate spacing should always be maintained between the high voltage isolated circuitry and any input referenced circuitry. The same minimum spacing between two adjacent high-side isolated regions of the printed circuit board must be maintained as well. Insufficient spacing will reduce the effective isolation and increase parasitic coupling that will degrade CMR performance.

The placement and routing of supply bypass capacitors requires special attention. During switching transients, the majority of the gate charge is supplied by the bypass capacitors. Maintaining short bypass capacitor trace lengths will ensure low supply ripple and clean switching waveforms.

Bypass capacitors should be placed closely in between these pins: V_{CC1} (pin 3) to V_{EE1} (pin 1) and V_{CC2} (pin 12) to V_{EE2} (pin 9). Ground plane connections are necessary for V_{EE1} and V_{EE2} in order to achieve maximum power as the ACPL-33JT is designed to dissipate the majority of heat generated through these pins. Actual power dissipation will depend on the application environment (PCB layout, airflow, part placement, and so on).

Figure 7 PCB Layout Considerations



Typical Performance Plots

Figure 8 PWM Duty Cycle vs. V_{COMP}

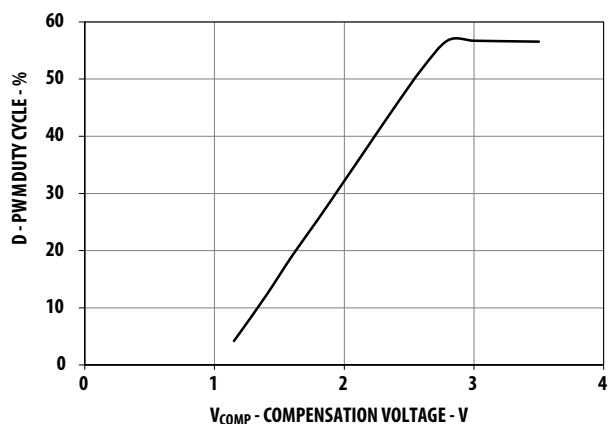


Figure 9 I_{COMP} vs. Supply Voltage

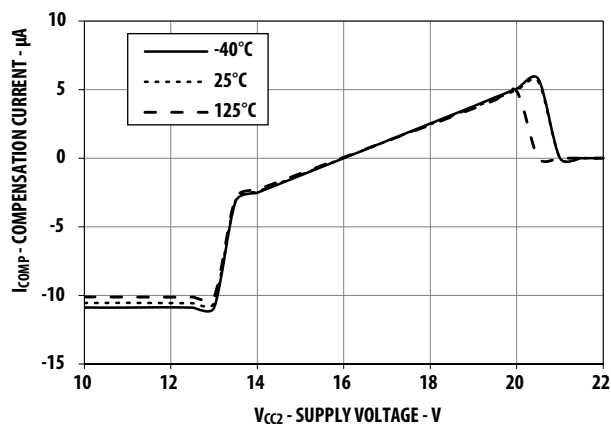


Figure 10 I_{CC1} vs. Temperature

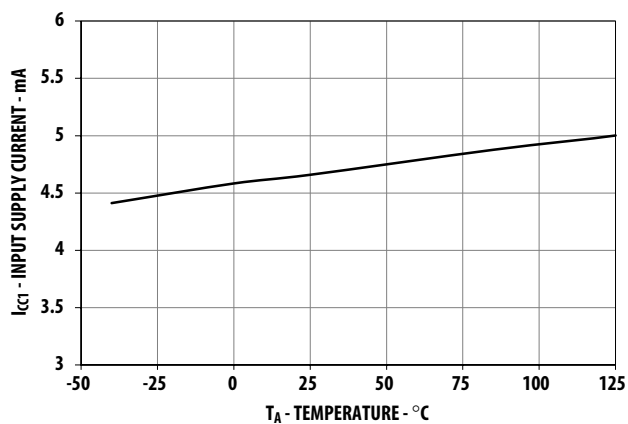


Figure 11 I_{CC2} vs. Temperature

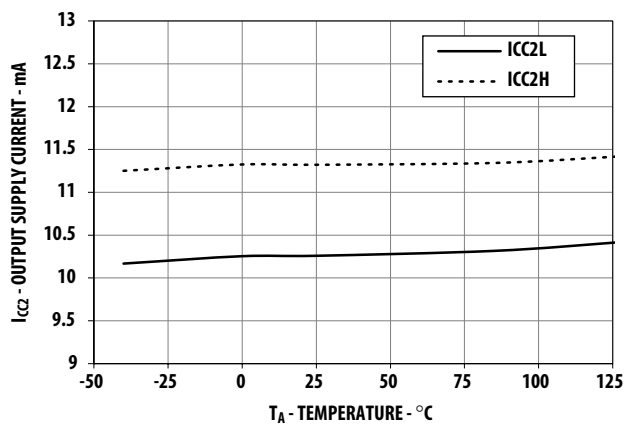


Figure 12 I_F vs. V_F

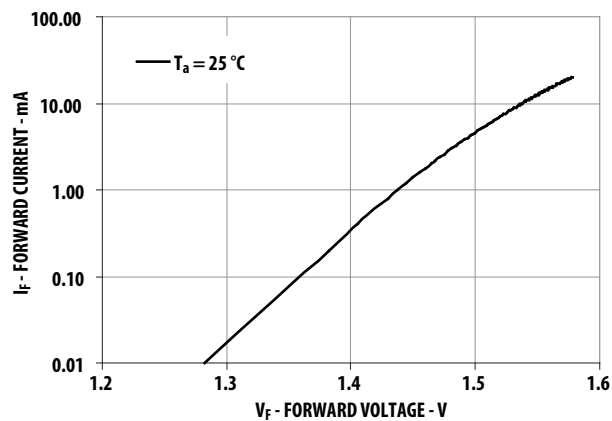


Figure 13 I_{TH} vs. Temperature

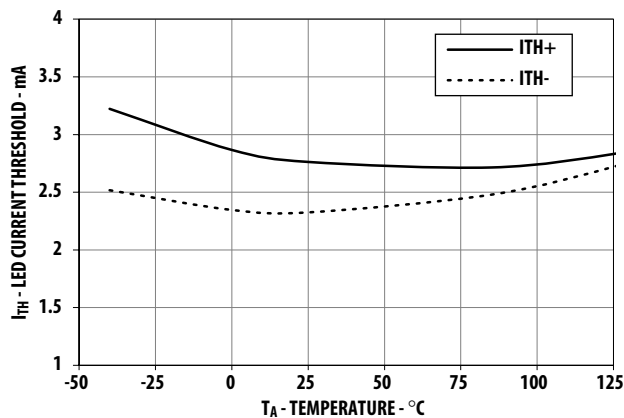


Figure 14 V_{OH} vs. I_{OH}

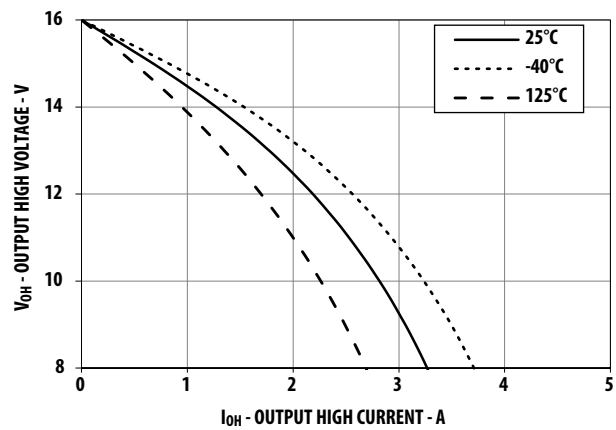


Figure 15 V_{OL} vs. I_{OL}

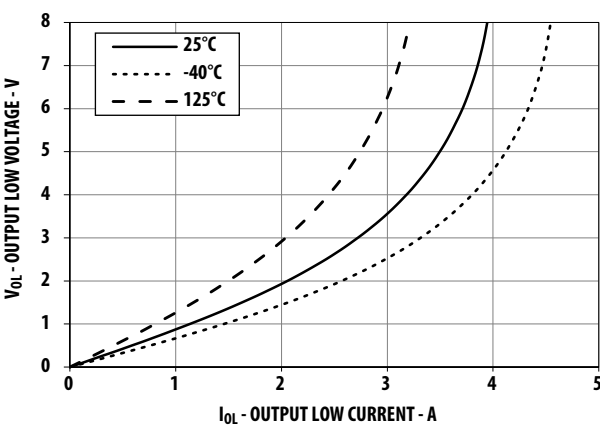


Figure 16 T_P vs. Temperature

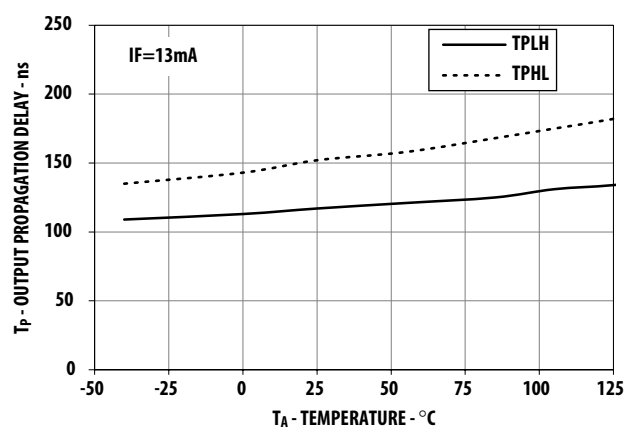


Figure 17 I_{SSD} vs. V_{SSD}

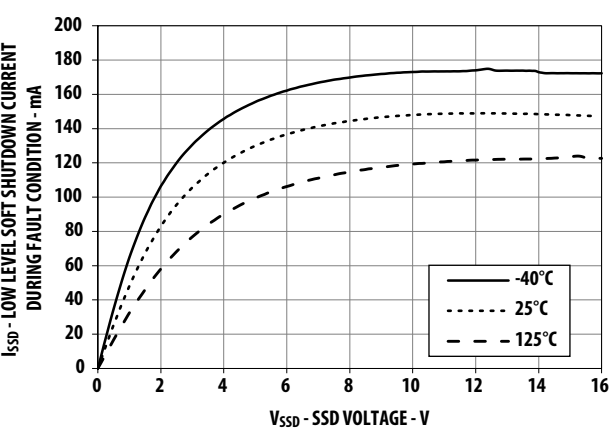


Figure 18 V_{DESAT} Threshold vs. Temperature

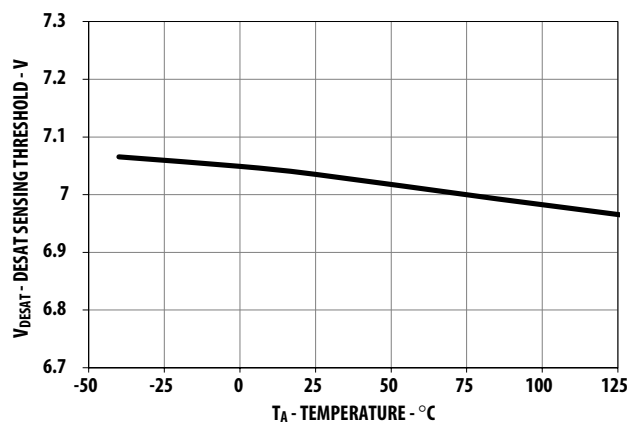


Figure 19 I_{CHG} vs. Temperature

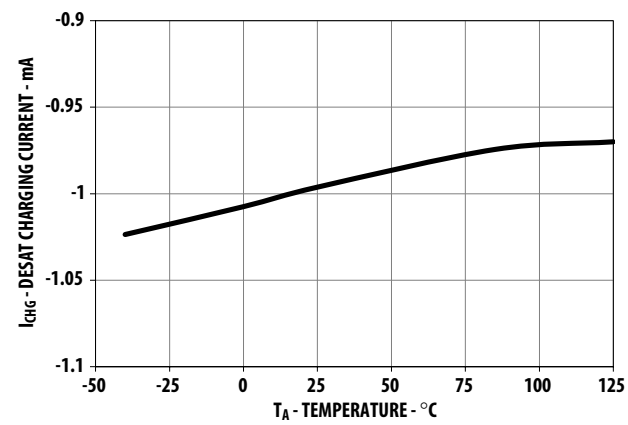


Figure 20 I_{DSCHG} vs. Temperature

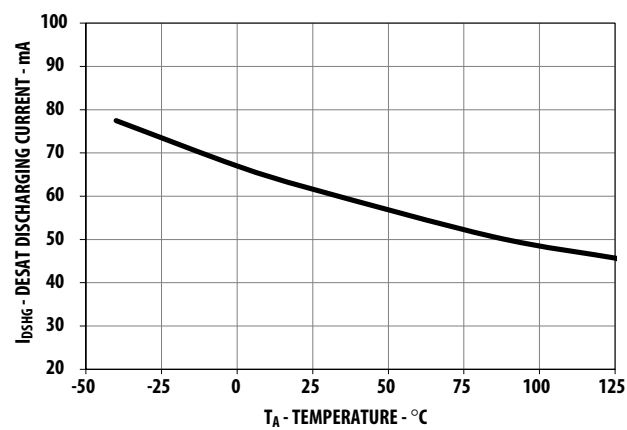


Figure 21 Propagation Delay Test Circuit

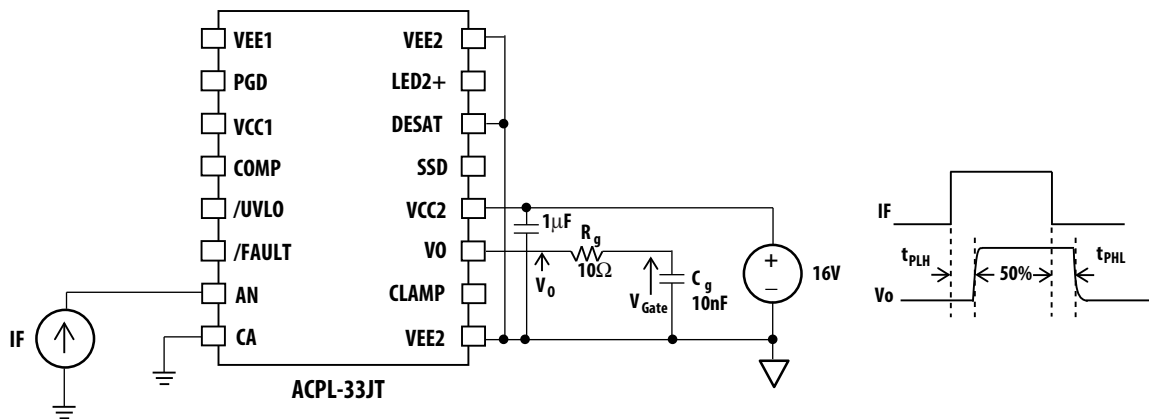


Figure 22 $t_{DESAT(90\%)}$ and $t_{DESAT(10\%)}$ Test Circuit

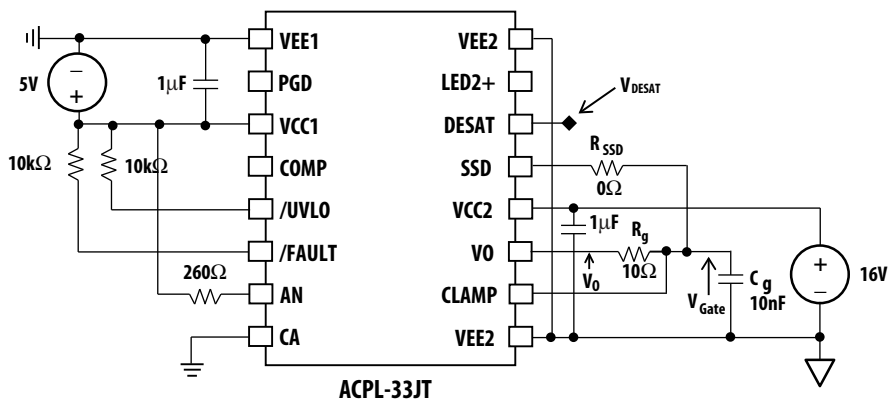


Figure 23 CMR V_O High Test Circuit

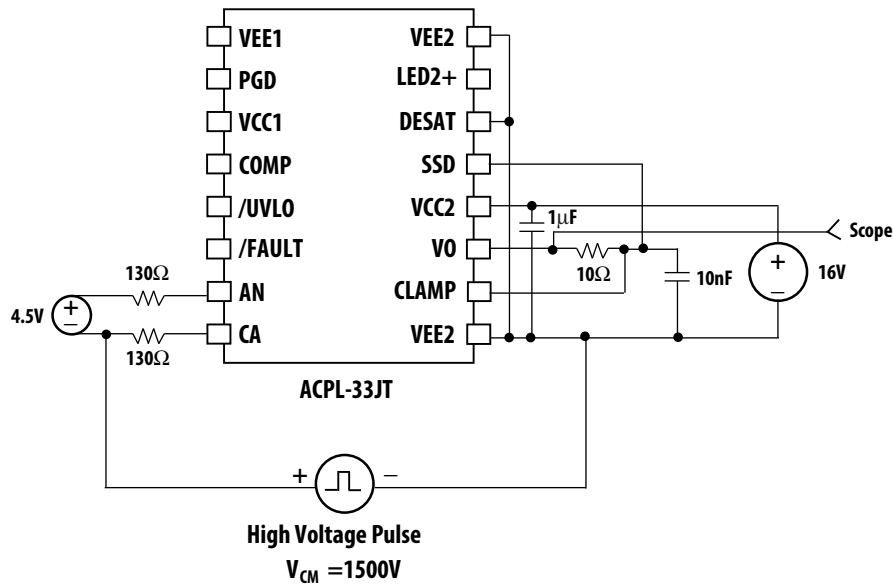


Figure 24 CMR V_O Low Test Circuit

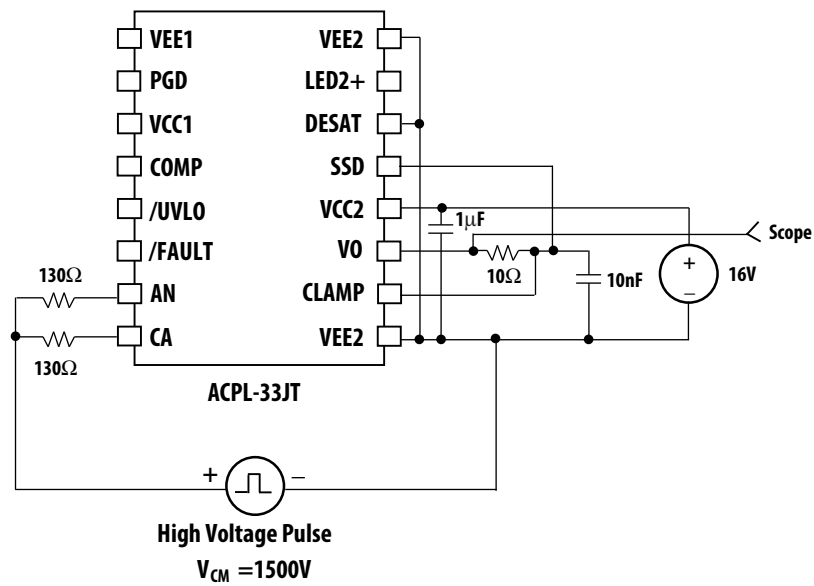


Table 11 Internal Connection Equivalent Circuits

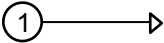
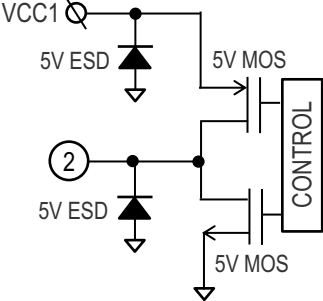
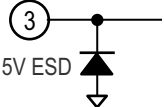
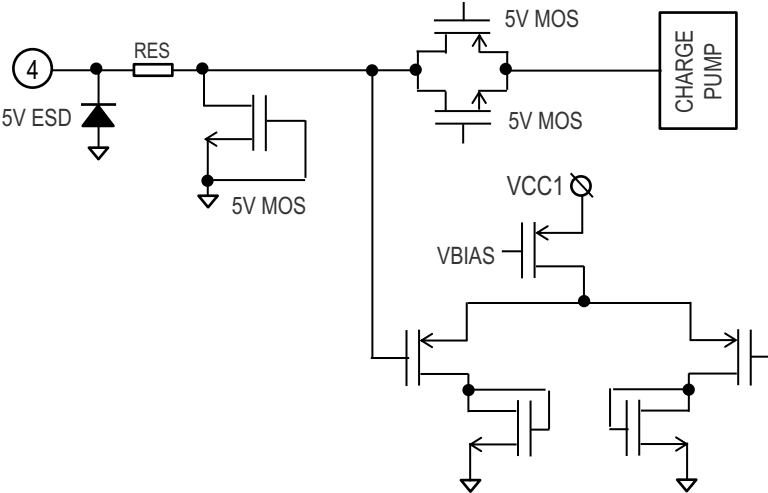
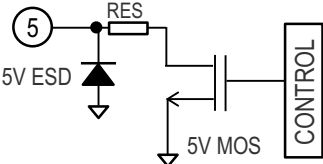
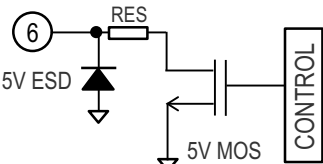
Pin No.	Pin Name	Equivalent Circuits	Note
1	V _{EE1}		Input Common/GND
2	PGD		
3	V _{CC1}		
4	COMP		5
5	/UVLO		
6	/FAULT		

Table 11 Internal Connection Equivalent Circuits (Continued)

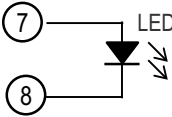
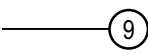
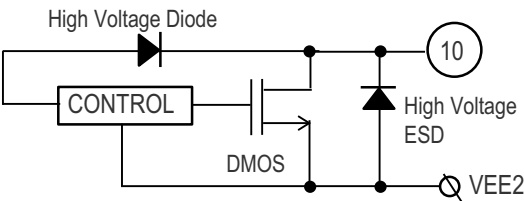
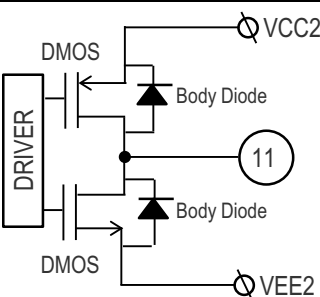
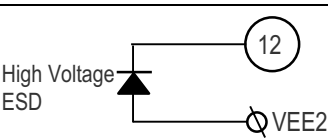
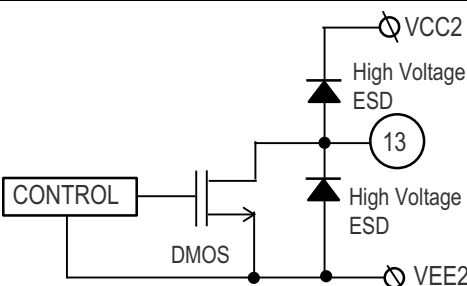
Pin No.	Pin Name	Equivalent Circuits	Note
7, 8	Input LED 7 – Anode 8 – Cathode		
9	V _{EE2}		Output Common
10	CLAMP		
11	V _O		
12	V _{CC2}		
13	SSD		

Table 11 Internal Connection Equivalent Circuits (Continued)

Pin No.	Pin Name	Equivalent Circuits	Note
14	DESAT		
15	LED2+		
16	V _{EE2}		Output Common

Typical Application/Operation

Introduction to Fault Detection and Protection

The power stage of a typical three-phase inverter is susceptible to several types of failures, most of which are potentially destructive to the power IGBTs. These failure modes can be grouped into four basic categories: phase or rail supply short circuits due to user misconnect or bad wiring; control signal failures due to noise or computational errors; overload conditions induced by the load; and component failures in the gate drive circuitry. Under any of these fault conditions, the current through the IGBTs can increase rapidly, causing excessive power dissipation and heating. The IGBTs become damaged when the current load approaches the saturation current of the device, and the collector-to-emitter voltage rises from saturation region to desaturation (active) region. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn off the over current during a fault condition.

A circuit providing fast local fault detection and shutdown is an ideal solution, but the number of required components, board space consumed, cost, and complexity have until now limited its use to high performance drives. The features that this circuit must have are high speed, low cost, low resolution, low power dissipation, and small size.

The ACPL-33JT satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shutdown, and optically isolated fault and UVLO status feedback signal into a single 16-pin surface mount package.

The fault detection method, which the ACPL-33JT has adopted, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off-state of the IGBT, the fault detect circuitry is simply disabled to prevent false 'fault' signals.

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the ACPL-33JT limits the power dissipation in the IGBT, even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly conservative over current threshold is not needed to protect the IGBT.

Typical Application Circuit

The ACPL-33JT has non-inverting gate control inputs, an open collector fault, and UVLO outputs suitable for wired 'OR' applications.

The application circuit shown in [Figure 25](#) illustrates a typical gate drive implementation using the ACPL-33JT.

The two supply bypass capacitors (1 μF and 20 μF) provide filtering and the large transient currents necessary during a switching transition. The Desat diode and 220 pF blanking capacitor are the necessary external components for the fault detection circuitry. The gate resistor (R_{G_ON} and R_{G_OFF}) serves to limit gate charge and discharge current and indirectly controls the IGBT collector voltage rise and fall times. The open collector fault and UVLO outputs have a passive 10 k Ω pull-up resistor and a 330 pF filtering capacitor.

Operation of Integrated Flyback Controller

The average PWM switching frequency of the primary gate drive (PGD) is dithered typically in a range of $\pm 6\%$, typically over 3.3 ms. This frequency dithering feature helps to achieve better EMI performance by spreading the switching and its harmonics over a wider band.

Figure 25 shows a reference circuit for DC-DC flyback conversion including the compensation network at pin 4, COMP. This compensation network is referenced to a nominal transformer of $L_p = 7 \mu\text{H}$, $L_s = 86 \mu\text{H}$. For $V_{in} = 6\text{V}$ to 24V , this circuit will nominally support a secondary-side load of up to 90 mA (including I_{CC2}) at the regulated V_{CC2} voltage.

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