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ACPL-36JV-000E

Automotive Gate Drive Optocoupler with R²Coupler™ Isolation, 2.5 Amp Output Current, Integrated Desaturation (V_{CE}) Detection and Fault Status Feedback

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available; -xxxE denotes a lead-free product

Description

Avago's automotive 2.5 Amp Gate Drive Optocoupler with Integrated Desaturation (V_{CE}) Detection and Fault Status Feedback makes automotive IGBT V_{CE} fault protection compact, affordable, and easy-to-implement while satisfying automotive AEC-Q100 Grade 2 semiconductor requirement.

Avago R²Coupler isolation products provide the reinforced insulation and reliability needed for critical in automotive and high temperature industrial applications

Functional Diagram

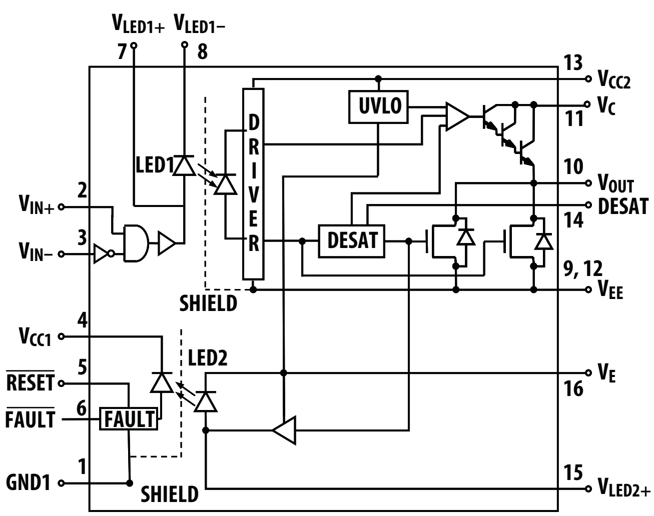


Figure 1. ACPL-36JV Functional Diagram

Features

- 2.5 A maximum peak output current
- Drive IGBTs up to I_C = 150 A, V_{CE} = 1200 V
- Optically isolated, FAULT status feedback
- SO-16 package
- CMOS/TTL compatible
- 500 ns max. switching speeds
- "Soft" IGBT turn-off
- Integrated fail-safe IGBT protection
  - Desat (VCE) detection
  - Under Voltage Lock-Out protection (UVLO) with hysteresis
- User configurable: inverting, noninverting, auto-reset, auto-shutdown
- Wide operating V_{CC} range: 15 to 30 Volts
- -40°C to +105°C operating temperature range
- 15 kV/µs min. Common Mode Rejection (CMR) at V_{CM} = 1500 V
- Qualified to AEC-Q100 Grade 2 Test Guidelines
- Regulatory approvals (Pending):
  - UL1577, CSA
  - IEC/EN/DIN EN 60747-5-5

Applications

- Automotive Isolated IGBT/MOSFET Inverter gate drive
- Automotive DC-DC Converter
- AC and brushless dc motor drives
- Industrial inverters for power supplies and motor controls
- Un-interruptible Power Supplies

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

ACPL-36JV is UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part Number	RoHS Compliant	Package	Surface Mount	Tape & Reel	Quantity
ACPL-36JV	-000E	SO-16	X		45 per tube
	-500E		X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

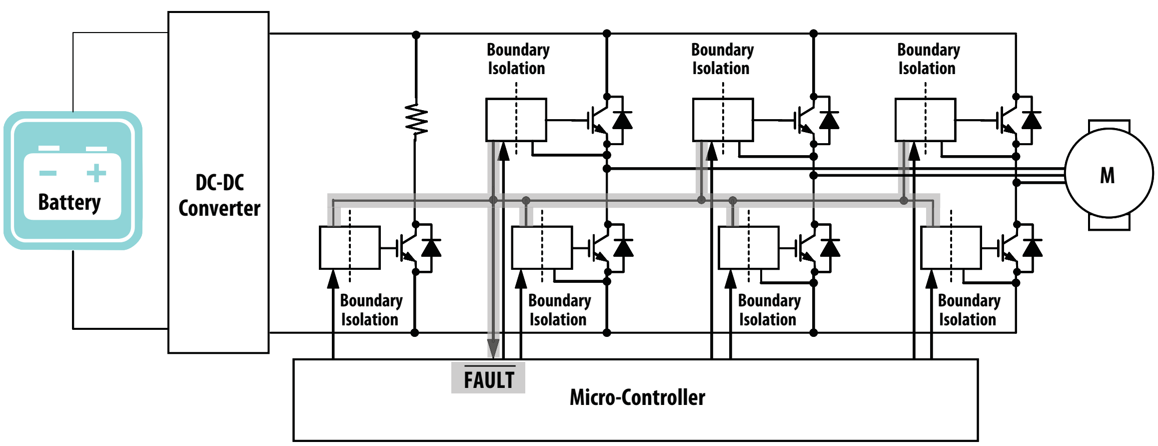
Example 1:

ACPL-36JV-500E to order product of SO-16 Surface Mount RoHS compliant package in Tape and Reel packaging.

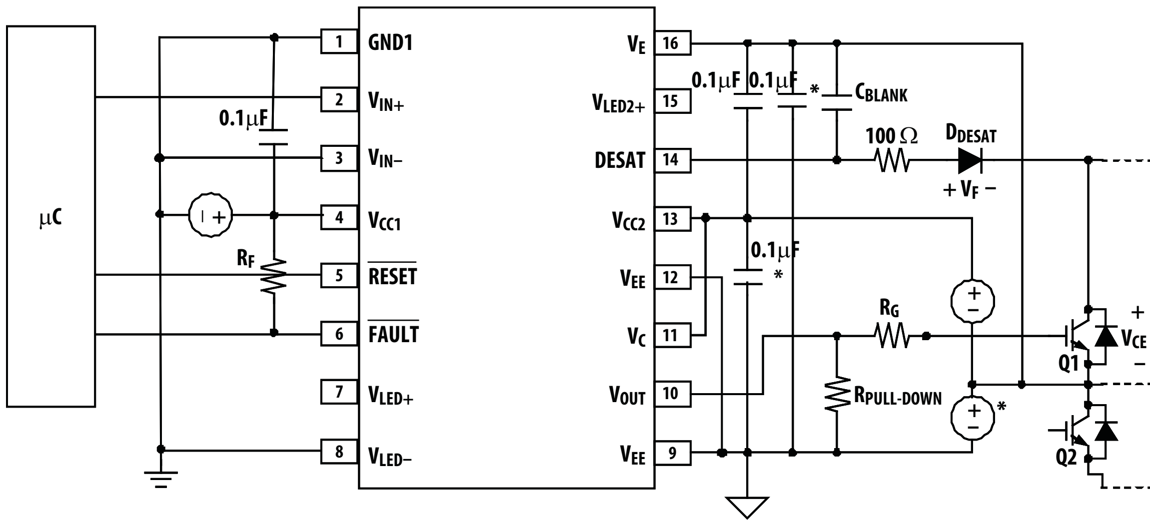
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Typical Fault Protected IGBT Gate Drive Circuit

The ACPL-36JV is an easy-to-use, intelligent gate driver which makes IGBT V_{CE} fault protection compact, affordable, and easy-to-implement. Features such as user configurable inputs, integrated V_{CE} detection, under voltage lockout (UVLO), "soft" IGBT turn-off and isolated fault feedback provide maximum design flexibility and circuit protection.



Typical Application Block Diagram of a motor control system.



Typical de-saturation protected gate drive circuit, non-inverting.

Description of Operation during Fault Condition

1. DESAT terminal monitors the IGBT V_{CE} voltage through D_{DESAT}.
2. When the voltage on the DESAT terminal exceeds 7 volts, the IGBT gate voltage (V_{OUT}) is slowly lowered.
3. FAULT output goes low, notifying the microcontroller of the fault condition.
4. Microcontroller takes appropriate action.

Output Control

The outputs (V_{OUT} and FAULT) of the ACPL-36JV are controlled by the combination of V_{IN}, UVLO and a detected IGBT Desat condition. As indicated in the below table, the ACPL-36JV can be configured as inverting or non-inverting using the V_{IN+} or V_{IN-} inputs respectively. When an inverting configuration is desired, V_{IN+} must be held high and V_{IN-} toggled. When a non-inverting configuration is desired, V_{IN-} must be held low and V_{IN+} toggled. Once UVLO is not active ($V_{CC2} - V_E > V_{UVLO}$), V_{OUT} is allowed to go high, and the DESAT (pin 14) detection feature of the ACPL-36JV will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once $V_{UVLO+} > 11.6$ V, DESAT will remain functional until $V_{UVLO-} < 12.4$ V. Thus, the DESAT detection and UVLO features of the ACPL-36JV work in conjunction to ensure constant IGBT protection.

V_{IN+}	V_{IN-}	UVLO ($V_{CC2} - V_E$)	Desat Condition Detected on Pin 14	Pin 6 (FAULT) Output	V_{OUT}
X	X	Active	X	X	Low
X	X	X	Yes	Low	Low
Low	X	X	X	X	Low
X	High	X	X	X	Low
High	Low	Not Active	No	High	High

Product Overview Description

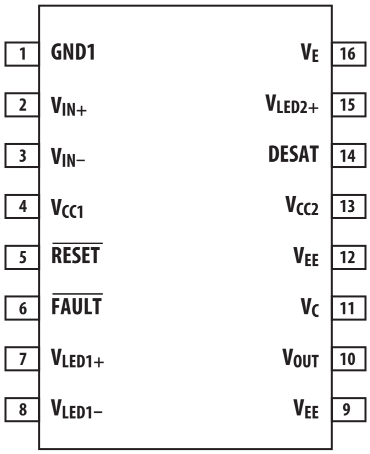
The ACPL-36JV (shown in Figure 1) is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT gate drive circuit with fault protection and feedback into one SO-16 package. TTL input logic levels allow direct interface with a microcontroller, and an optically isolated power output stage drives IGBTs with power ratings of up to 150 A and 1200 V. A high speed internal optical link minimizes the propagation delays between the microcontroller and the IGBT while allowing the two systems to operate at very large common mode voltage differences that are common in industrial motor drives and other power switching applications. An output IC provides local protection for the IGBT to prevent damage during overcurrents, and a second optical link provides a fully isolated fault status feedback signal for the microcontroller. A built in "watchdog" circuit monitors the power stage supply voltage to prevent IGBT caused by insufficient gate drive voltages. This integrated IGBT gate driver is designed to increase the performance and reliability of a motor drive without the cost, size, and complexity of a discrete design.

Two light emitting diodes and two integrated circuits housed in the same SO-16 package provide the input control circuitry, the output power stage, and two optical channels. The input Buffer IC is designed on a bipolar process, while the output Detector IC is designed manufactured on a high voltage BiCMOS/Power DMOS process. The forward optical signal path, as indicated by LED1, transmits the gate control signal. The return optical signal path, as indicated by LED2, transmits the fault status feedback signal. Both optical channels are completely controlled by the input and output ICs respectively, making the internal isolation boundary transparent to the microcontroller.

Under normal operation, the input gate control signal directly controls the IGBT gate through the isolated output detector IC. LED2 remains off and a fault latch in the input buffer IC is disabled. When an IGBT fault is detected, the output detector IC immediately begins a "soft" shutdown sequence, reducing the IGBT current to zero in a controlled manner to avoid potential IGBT damage from inductive over-voltages. Simultaneously, this fault status is transmitted back to the input buffer IC via LED2, where the fault latch disables the gate control input and the active low fault output alerts the microcontroller.

During power-up, the Under Voltage Lockout (UVLO) feature prevents the application of insufficient gate voltage to the IGBT, by forcing the ACPL-36JV's output low. Once the output is in the high state, the DESAT (V_{CE}) detection feature of the ACPL-36JV provides IGBT protection. Thus, UVLO and DESAT work in conjunction to provide constant IGBT protection.

Package Pin Out

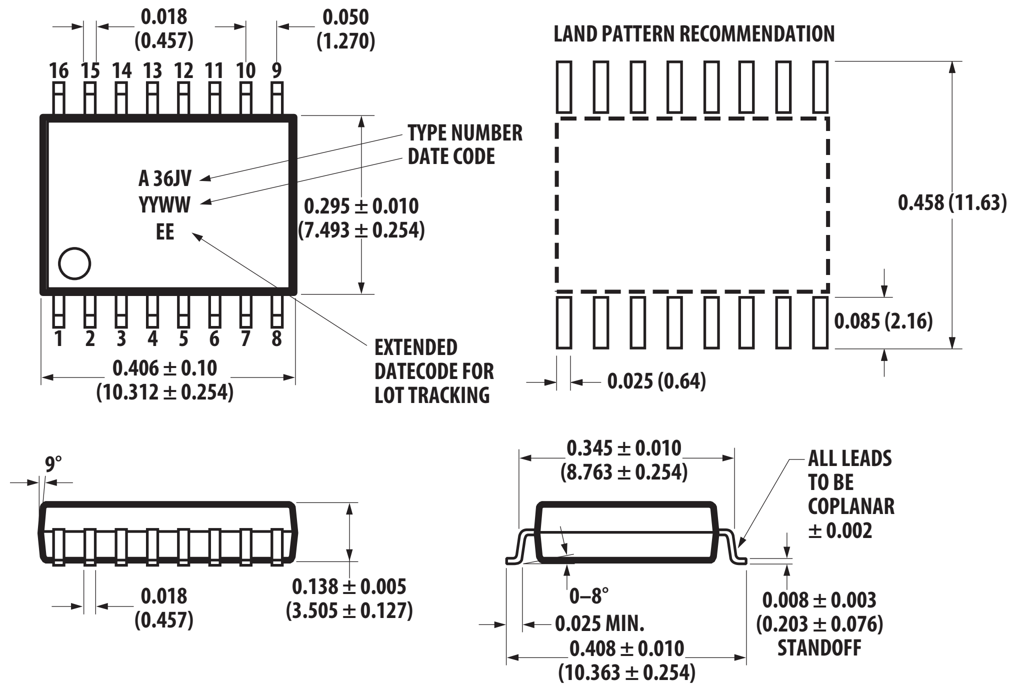


Pin Descriptions

Symbol	Description	Symbol	Description
V_{IN+}	Noninverting gate drive voltage output (V_{OUT}) control input.	V_E	Common (IGBT emitter) output supply voltage.
V_{IN-}	Inverting gate drive voltage output (V_{OUT}) control input.	V_{LED2+}	LED 2 anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)
V_{CC1}	Positive input supply voltage. (4.5 V to 5.5 V)	DESAT	Desaturation voltage input. When the voltage on DESAT exceeds an internal reference voltage of 7 V while the IGBT is on, FAULT output is changed from a high impedance state to a logic low state within 5 µs. See Note 25.
GND1	Input Ground.	V_{CC2}	Positive output supply voltage.
$\overline{RESET}$	$\overline{FAULT}$ reset input. A logic low input for at least 0.1 µs, asynchronously resets FAULT output high and enables V_{IN}. Synchronous control of RESET relative to V_{IN} is required. RESET is not affected by UVLO. Asserting RESET while V_{OUT} is high does not affect V_{OUT}.	V_C	Collector of output pull-up triple-darlington transistor. It is connected to V_{CC2} directly or through a resistor to limit output turn-on current.
$\overline{FAULT}$	Fault output. $\overline{FAULT}$ changes from a high impedance state to a logic low output within 5 µs of the voltage on the DESAT pin exceeding an internal reference voltage of 7 V. FAULT output remains low until RESET is brought low. FAULT output is an open collector which allows the FAULT outputs from all HCPL-316Js in a circuit to be connected together in a "wired OR" forming a single fault bus for interfacing directly to the micro-controller.	V_{OUT}	Gate drive voltage output.
V_{LED1+}	LED 1 anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)	V_{EE}	Output supply voltage.
V_{LED1-}	LED 1 cathode. This pin must be connected to ground.		

Package Outline Drawings

16-Lead Surface Mount



Package Characteristics

All specifications and figures are at the nominal (typical) operating conditions of V_{CC1} = 5 V, V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V, and T_A = +25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	3750			V_{RMS}	RH < 50%, t = 1 min. T_A = 25°C	1, 2, 3
Resistance (Input-Output)	R_{I-O}		$>10^9$		Ω	V_{I-O} = 500 Vdc	3
Capacitance (Input-Output)	C_{I-O}		1.3		pF	f = 1 MHz	
Output IC-to-Pins 9 & 12 Thermal Resistance	θ_{O9-12}		30		°C/W	T_A = 100°C	
Input IC-to-Pin 1 Thermal Resistance	θ_{I1}		60		°C/W	T_A = 100°C	

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

The ACPL-36JV-000E is pending approval by the following organizations:

UL

Pending approval under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS} expected prior to product release.

CSA

Pending approval under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-5

Approved under:

IEC 60747-5-5: Pending

EN 60747-5-5: Pending

DIN EN 60747-5-5: Pending

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 Vrms		I - IV	
for rated mains voltage ≤ 450 Vrms		I - III	
for rated mains voltage ≤ 600 Vrms		I - II	
Climatic Classification		55/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	891	V_{PEAK}
Input to Output Test Voltage, Method b[2] V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	1670	V_{PEAK}
Input to Output Test Voltage, Method a[2] V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial discharge < 5 pC	V_{PR}	1336	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	V_{PEAK}
Safety-limiting values – maximum values allowed in the event of a failure			
Case Temperature	T_S	175	°C
Input Current[3]	$I_{S, INPUT}$	400	mA
Output Power[3]	$P_{S, OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

Notes:
1. Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface Mount Classification is Class A in accordance with CECCOO802.
2. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.
3. Refer to the following figure for dependence of P_S and I_S on ambient temperature.

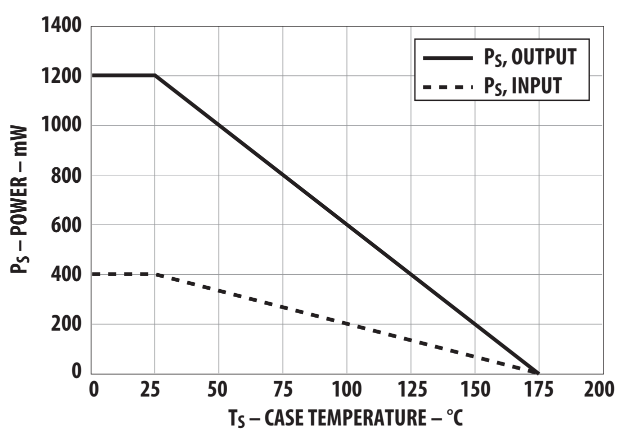


Figure 2. Dependence of safety limiting values on temperature.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	150	°C	
Operating Temperature	T_A	-40	105	°C	
Output IC Junction Temperature	T_J		140	°C	4
Peak Output Current	$\|I_{O(peak)}\|$		2.5	A	5
Fault Output Current	I_{FAULT}		8	mA	
Positive Input Supply Voltage	V_{CC1}	-0.5	5.5V	Volts	
Input Pin Voltages	V_{IN+}, V_{IN-} and $V_{\overline{RESET}}$	-0.5	V_{CC1}	Volts	
Total Output Supply Voltage	$(V_{CC2} - V_{EE})$	-0.5	35	Volts	
Negative Output Supply Voltage	$(V_E - V_{EE})$	-0.5	15	Volts	6
Positive Output Supply Voltage	$(V_{CC2} - V_E)$	-0.5	35 - $(V_E - V_{EE})$	Volts	
Gate Drive Output Voltage	$V_{o(peak)}$	-0.5	V_{CC2}	Volts	
Collector Voltage	V_C	V_{EE} + 5 V	V_{CC2}	Volts	
DESAT Voltage	V_{DESAT}	V_E	V_E + 10	Volts	
Output IC Power Dissipation	P_O		600	mW	4
Input IC Power Dissipation	P_I		150	mW	
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Input Supply Voltage	V_{CC1}	4.5	5.5	Volts	28
Total Output Supply Voltage	$(V_{CC2} - V_{EE})$	15	30	Volts	9
Negative Output Supply Voltage	$(V_E - V_{EE})$	0	15	Volts	6
Positive Output Supply Voltage	$(V_{CC2} - V_E)$	15	30 – $(V_E - V_{EE})$	Volts	
Collector Voltage	V_C	V_{EE} + 6	V_{CC2}	Volts	
Operating Temperature	T_A	-40	105	°C	

Electrical Specifications

Recommended operating conditions unless otherwise specified: T_A = -40°C to +105°C, all typical values at T_A = 25°C, V_{CC1} = 5 V, and V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Logic Low Input Voltages	V_{IN+L}, V_{IN-L}, $V_{\overline{RESET}L}$			0.8	V			
Logic High Input Voltages	V_{IN+H}, V_{IN-H}, $V_{\overline{RESET}H}$	2.0			V			
Logic Low Input Currents	I_{IN+L}, I_{IN-L}, $I_{\overline{RESET}L}$	-0.5	-0.4		mA	V_{IN} = 0.4 V		
$\overline{FAULT}$ Logic Low Output Current	$I_{\overline{FAULT}L}$	5.0	12		mA	V_{FAULT} = 0.4 V	29	
$\overline{FAULT}$ Logic High Output Current	$I_{\overline{FAULT}H}$	-40			µA	$V_{FAULT} = V_{CC1}$	30	
High Level Output Current	I_{OH}	-0.5 -2.0	-1.5		A	$V_{OUT} = V_{CC2}$ - 4 V $V_{OUT} = V_{CC2}$ - 15 V	3, 8, 31	7 5
Low Level Output Current	I_{OL}	0.5 2.0	2.3		A	$V_{OUT} = V_{EE}$ + 2.5 V $V_{OUT} = V_{EE}$ + 15 V	4, 9, 32	7 5
Low Level Output Current	I_{OLF}	90	160	230	mA	V_{OUT} - V_{EE} = 14 V	5, 33	8
High Level Output Voltage	V_{OH}	V_C - 3.5	V_C - 2.5	V_C - 1.5	V	I_{OUT} = -100 mA	6, 8,	9, 10, 11
		V_C -2.9	V_C - 2.0	V_C - 1.2	V	I_{OUT} = -650 µA	34	
				V_C	V	I_{OUT} = 0		
Low Level Output Voltage	V_{OL}		0.17	0.5	V	I_{OUT} = 100 mA	7, 9, 35	26
High Level Input Supply Current	I_{CC1H}		17	22	mA	$V_{IN+} = V_{CC1}$ = 5.5 V, V_{IN-} = 0 V	10, 36	
Low Level Input Supply Current	I_{CCIL}		6	11	mA	$V_{IN+} = V_{IN-}$ = 0 V, V_{CC1} = 5.5 V,	10, 37	
Output Supply Current	I_{CC2}		2.5	5	mA	V_{OUT} open	11, 12, 38, 39	11
Low Level Collector Current	I_{CL}		0.3	1.0	mA	I_{OUT} = 0	15, 58	27
High Level Collector Current	I_{CH}		0.3	1.3	mA	I_{OUT} = 0	15, 57	27
			1.8	3.0	mA	I_{OUT} = -650 µA	15, 56	27
V_E Low Level Supply Current	I_{EL}	-0.7	-0.4	0	mA		14, 60	
V_E High Level Supply Current	I_{EH}	-0.5	-0.14	0	mA		14, 59	25
Blanking Capacitor Charging Current	I_{CHG}	-0.13 -0.18	-0.25 -0.25	-0.33 -0.33	mA mA	V_{DESAT} = 0 - 6 V V_{DESAT} = 0 - 6 V, T_A = 25°C - 105°C	13, 40	11, 12
Blanking Capacitor Discharge Current	I_{DSCHG}	10	50		mA	V_{DESAT} = 7 V	41	
UVLO Threshold	V_{UVLO+} V_{UVLO-}	11.6	12.3 11.1	13.5 12.4	V V	V_{OUT} > 5 V V_{OUT} < 5 V	42	9, 11, 13 9, 11, 14
UVLO Hysteresis	(V_{UVLO+} V_{UVLO-})	0.4	1.2		V		42	
DESAT Threshold	V_{DESAT}	6.5	7.0	7.5	V	V_{CC2} - V_E > V_{UVLO-}	16, 43	11

Switching Specifications

Unless otherwise noted, all typical values at T_A = 25°C, V_{CC1} = 5 V, and V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V; all Minimum/ Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
V_{IN} to High Level Output Propagation Delay Time	t_{PLH}	0.10	0.30	0.50	µs	Rg = 10 Ω Cg = 10 nF f = 10 kHz Duty Cycle = 50%	17,18,19, 20,21,22, 44, 53, 54	15
V_{IN} to Low Level Output Propagation Delay Time	t_{PHL}	0.10	0.32	0.5	µs			
Pulse Width Distortion	PWD	-0.30	0.02	0.30	µs			16,17
Propagation Delay Difference Between Any 2 Parts	$(t_{PHL}-t_{PLH})$ P_{DD}	-0.35		0.35	µs			17,18
10% to 90% Rise Time	t_r		0.1		µs		44	
90% to 10% Fall Time	t_f		0.1		µs		44	
DESAT Sense to 90% V_{OUT} Delay	$t_{DESAT(90\%)}$		0.3	0.5	µs	Rg = 10 Ω Cg = 10 nF	23, 55	19
DESAT Sense to 10% V_{OUT} Delay	$t_{DESAT(10\%)}$		2.0	3.0	µs	V_{CC2} - V_{EE} = 30 V	24, 26, 27 45, 55	
DESAT Sense to Low Level $\overline{FAULT}$ Signal Delay	$t_{DESAT(\overline{FAULT})}$		1.8	5	µs		25, 46, 55	20
DESAT Sense to DESAT Low Propagation Delay	$t_{DESAT(LOW)}$		0.25		µs		55	21
$\overline{RESET}$ to High Level FAULT Signal Delay	$t_{\overline{RESET(FAULT)}}$	3	7	20	µs		28, 47, 55	22
$\overline{RESET}$ Signal Pulse Width	$PW_{\overline{RESET}}$	0.1			µs			
UVLO to VOUT High Delay	$t_{UVLO\ ON}$		4.0		µs	V_{CC2} = 1.0 ms ramp	48	13
UVLO to VOUT Low Delay	$t_{UVLO\ OFF}$		6.0		µs			14
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V, V_{CC2} = 30 V	49, 50, 51, 52	23
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V, V_{CC2} = 30 V		24

Notes:

1. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$).
2. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.
3. Device considered a two terminal device: pins 1 - 8 shorted together and pins 9 - 12 shorted together.
4. In order to achieve the absolute maximum power dissipation specified, pins 1, 9, and 12 require ground plane connections and may require airflow. See the Thermal Model section in the application notes at the end of this data sheet for details on how to estimate junction temperature and power dissipation. In most cases the absolute maximum output IC junction temperature is the limiting factor. The actual power dissipation achievable will depend on the application environment (PCB Layout, air flow, part placement, etc.). See the Recommended PCB Layout section in the application notes for layout considerations. Output IC power dissipation is derated linearly at 10 mW/°C above 90°C. Input IC power dissipation does not require de-rating.
5. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with IO peak minimum = 2.0 A. See Applications section for additional details on I_{OH} peak. De-rate linearly from 3.0 A at +25°C to 2.5 A at +105°C. This compensates for increased I_{OPEAK} due to changes in V_{OL} over temperature.
6. This supply is optional. Required only when negative gate drive is implemented.
7. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
8. See the Slow IGBT Gate Discharge During Fault Condition section in the applications notes at the end of this data sheet for further details.
9. 15 V is the recommended minimum operating positive supply voltage (V_{CC2} - V_E) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 13.5 V. For High Level Output Voltage testing, V_{OH} is measured with a dc load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero units.
10. Maximum pulse width = 1.0 ms, maximum duty cycle = 20%.
11. Once V_{OUT} of the ACPL-36JV is allowed to go high ($V_{CC2} - V_E > V_{UVLO}$), the DESAT detection feature of the ACPL-36JV will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{UVLO+} > 11.6 V, DESAT will remain functional until V_{UVLO-} < 12.4 V. Thus, the DESAT detection and UVLO features of the ACPL-36JV work in conjunction to ensure constant IGBT protection.
12. See the Blanking Time Control section in the applications notes at the end of this data sheet for further details.
13. This is the "increasing" (i.e. turn-on or "positive going" direction) of V_{CC2} - V_E.
14. This is the "decreasing" (i.e. turn-off or "negative going" direction) of V_{CC2} - V_E.
15. This load condition approximates the gate load of a 1200 V/75A IGBT.
16. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given unit.
17. As measured from V_{IN+}, V_{IN-} to V_{OUT}.
18. The difference between t_{PHL} and t_{PLH} between any two ACPL-36JV parts under the same test conditions.
19. Supply Voltage Dependent.
20. This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low.
21. This is the amount of time the DESAT threshold must be exceeded before V_{OUT} begins to go low, and the FAULT output to go low.
22. This is the amount of time from when RESET is asserted low, until FAULT output goes high. The minimum specification of 3 µs is the guaranteed minimum FAULT signal pulse width when the ACPL-36JV is configured for Auto-Reset. See the Auto-Reset section in the applications notes at the end of this data sheet for further details.
23. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15 V or FAULT > 2 V). A 100 pF and a 3KΩ pull-up resistor is needed in fault detection mode.
24. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V or FAULT < 0.8 V).
25. Does not include LED2 current during fault or blanking capacitor discharge current.
26. To clamp the output voltage at V_{CC} - 3 V_{BE}, a pull-down resistor between the output and V_{EE} is recommended to sink a static current of 650 µA while the output is high. See the Output Pull-Down Resistor section in the application notes at the end of this data sheet if an output pull-down resistor is not used.
27. The recommended output pull-down resistor between V_{OUT} and V_{EE} does not contribute any output current when $V_{OUT} = V_{EE}$.
28. In most applications V_{CC1} will be powered up first (before V_{CC2}) and powered down last (after V_{CC2}). This is desirable for maintaining control of the IGBT gate. In applications where V_{CC2} is powered up first, it is important to ensure that Vin+ remains low until V_{CC1} reaches the proper operating voltage (minimum 4.5 V) to avoid any momentary instability at the output during V_{CC1} ramp-up or ramp-down.

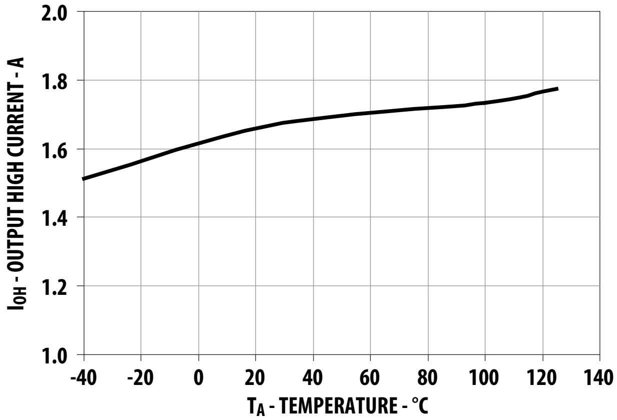


Figure 3. I_{OH} vs. temperature.

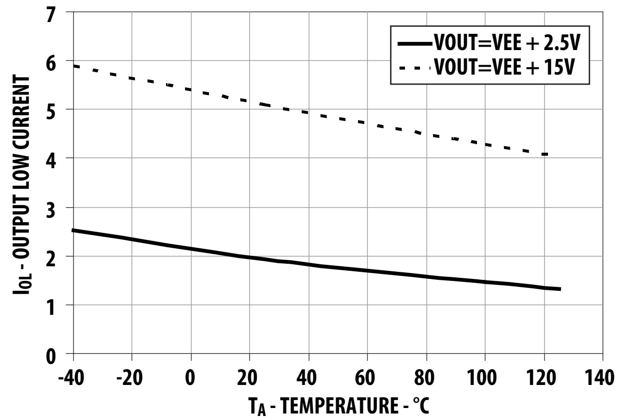


Figure 4. I_{OL} vs. temperature.

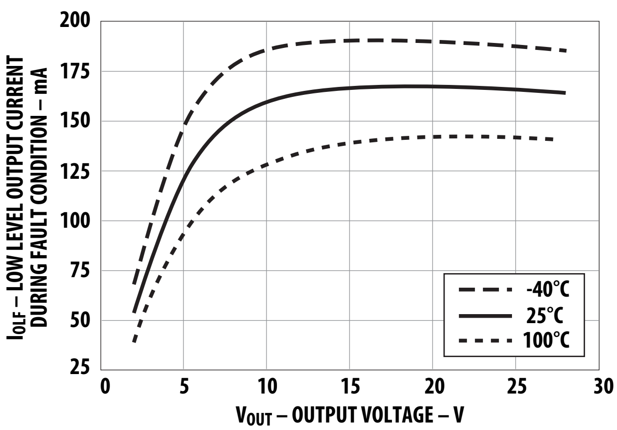


Figure 5. I_{OLF} vs. V_{OUT}.

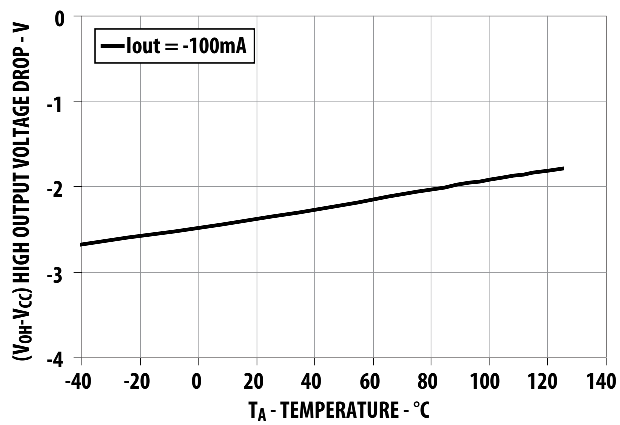


Figure 6. V_{OH} vs. Temperature.

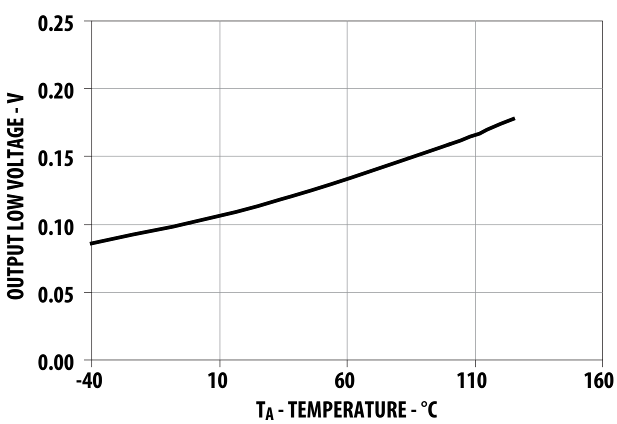


Figure 7. V_{OL} vs. Temperature.

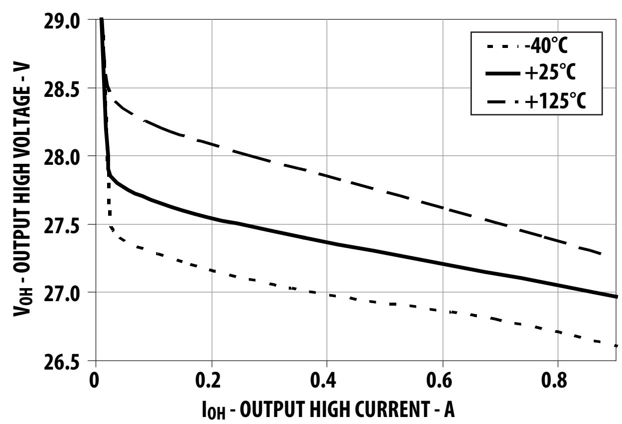


Figure 8. V_{OH} vs. I_{OH}.

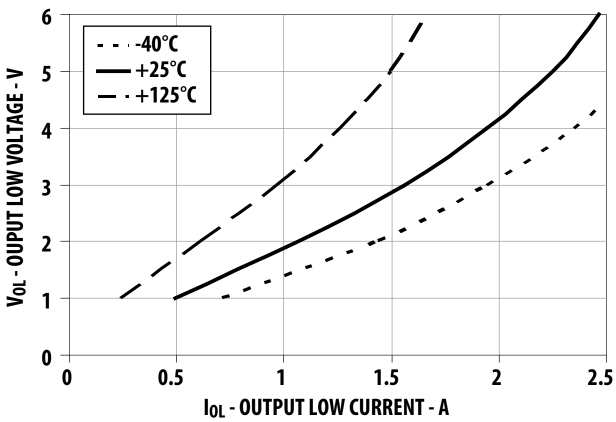


Figure 9. V_{OL} vs. I_{OL}.

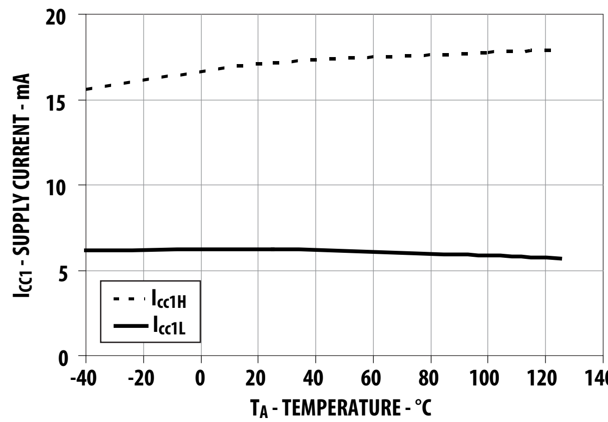


Figure 10. I_{CC1} vs. temperature.

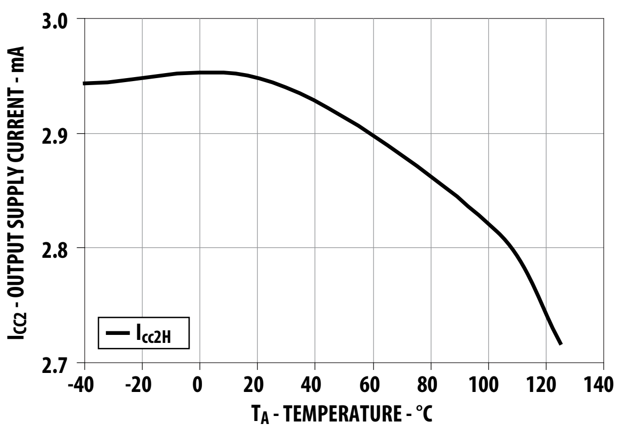


Figure 11. I_{CC2} vs. temperature.

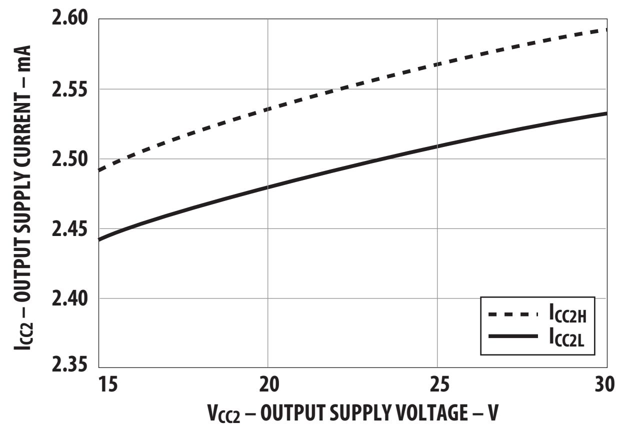


Figure 12. I_{CC2} vs. V_{CC2}.

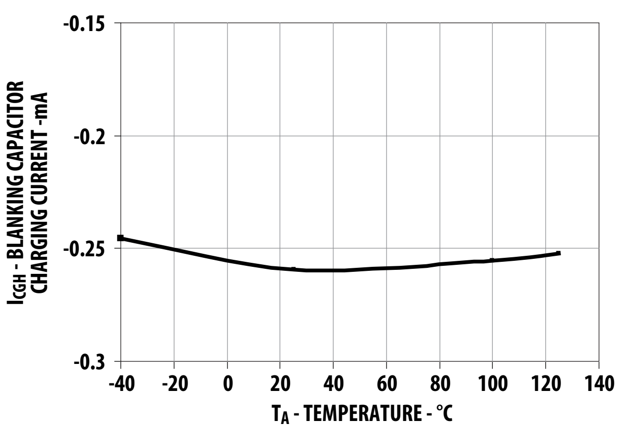


Figure 13. I_{CHG} vs. temperature.

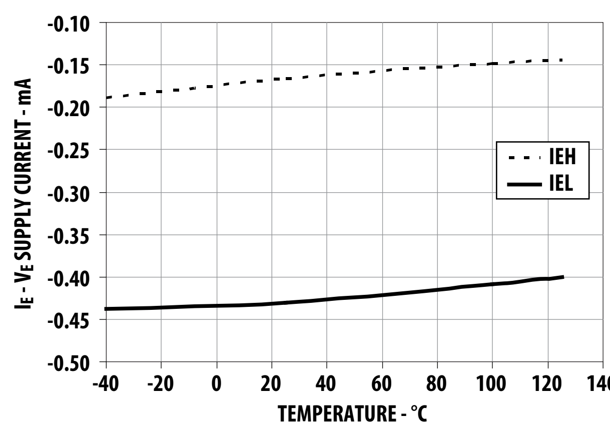


Figure 14. I_E vs. temperature.

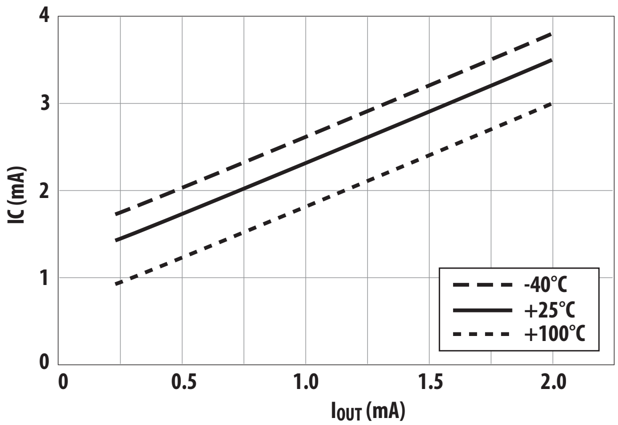


Figure 15. I_C vs. I_{OUT}.

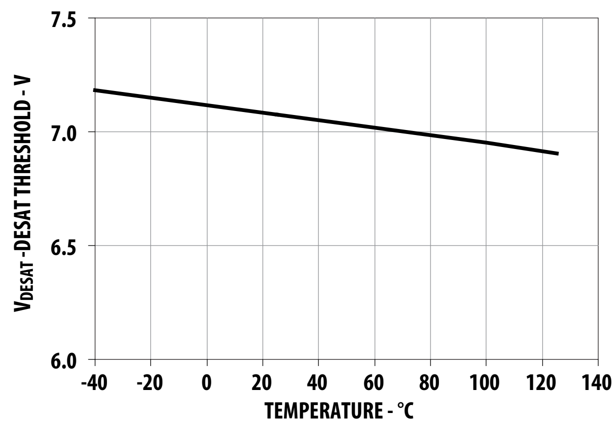


Figure 16. DESAT threshold vs. temperature.

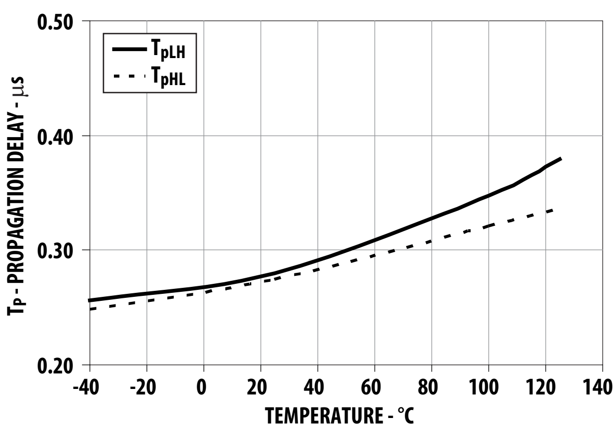


Figure 17. Propagation delay vs. temperature.

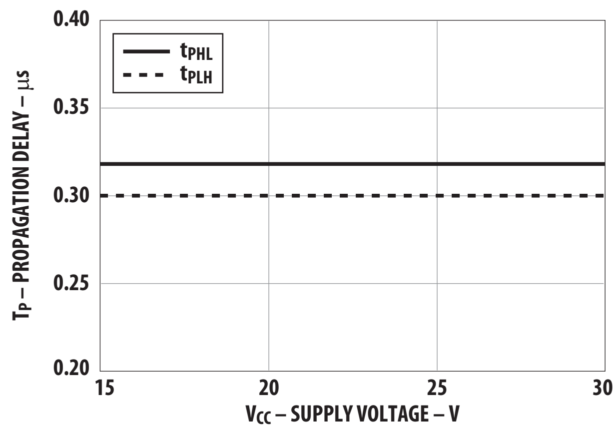


Figure 18. Propagation delay vs. supply voltage.

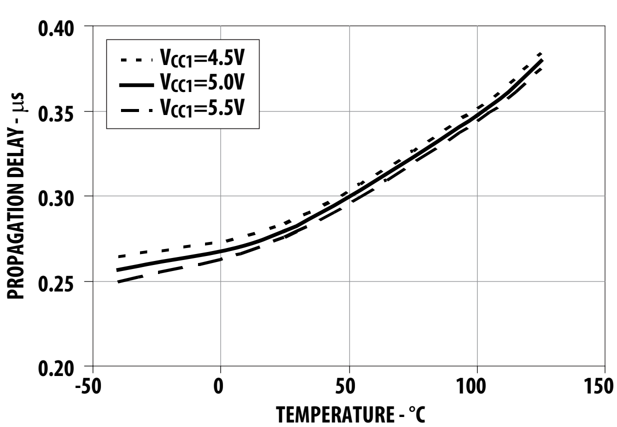


Figure 19. V_{IN} to high propagation delay vs. temperature.

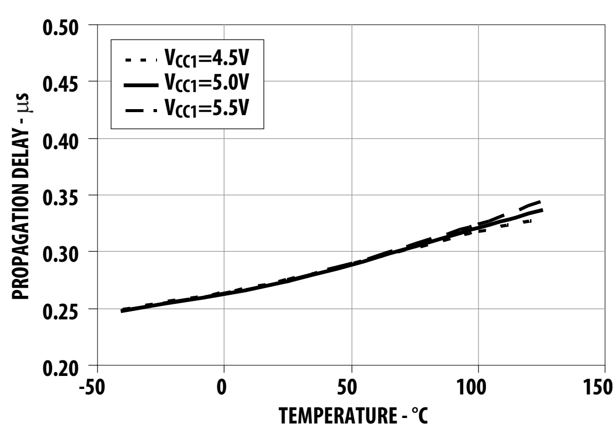


Figure 20. V_{IN} to low propagation delay vs. temperature.

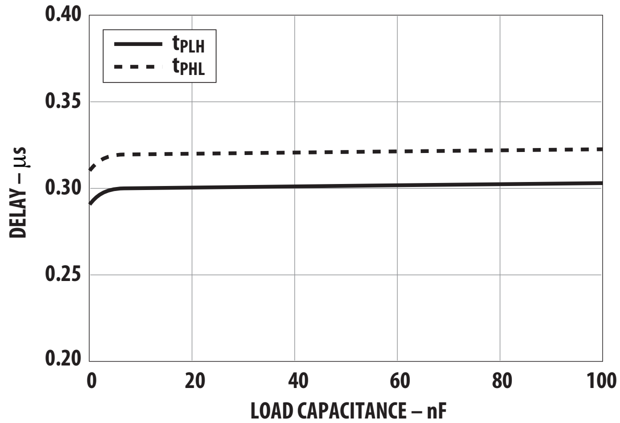


Figure 21. Propagation delay vs. load capacitance.

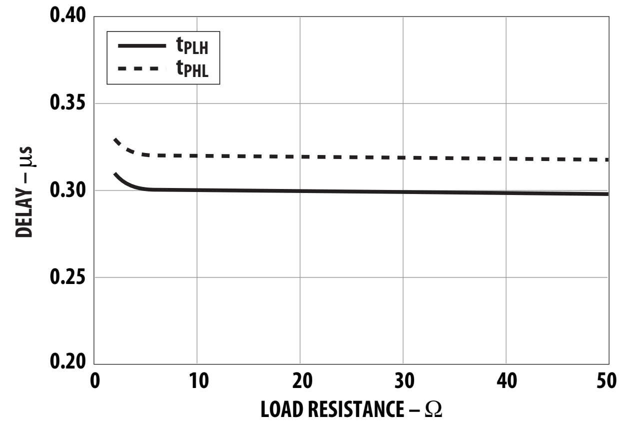


Figure 22. Propagation delay vs. load resistance.

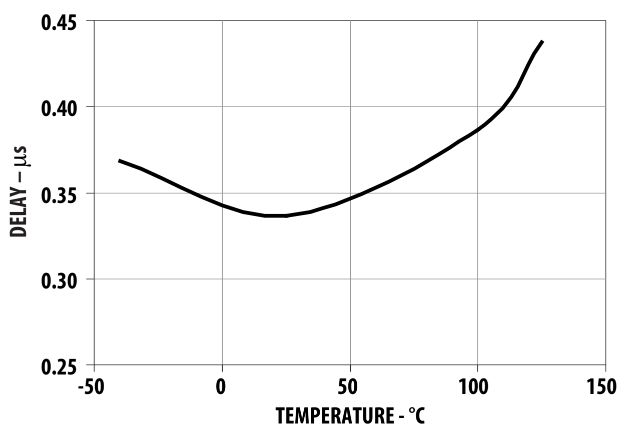


Figure 23. DESAT sense to 90% Vout delay vs. temperature.

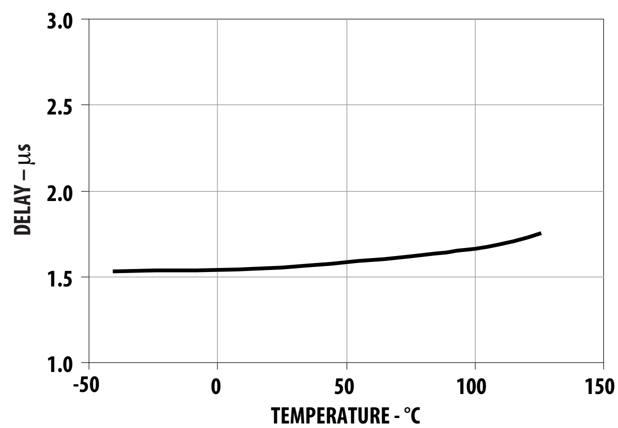


Figure 24. DESAT sense to 10% Vout delay vs. temperature.

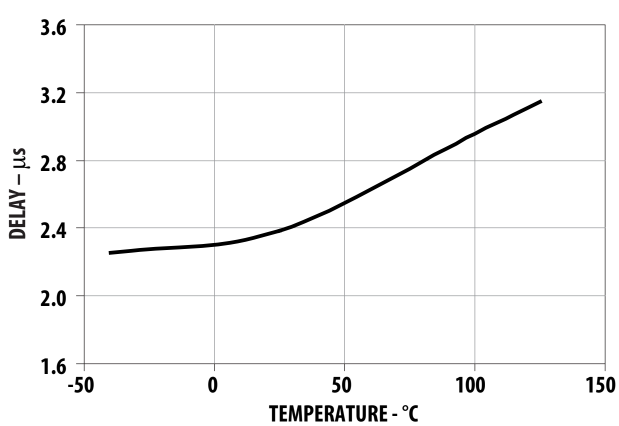


Figure 25. DESAT sense to low level fault signal delay vs. temperature.

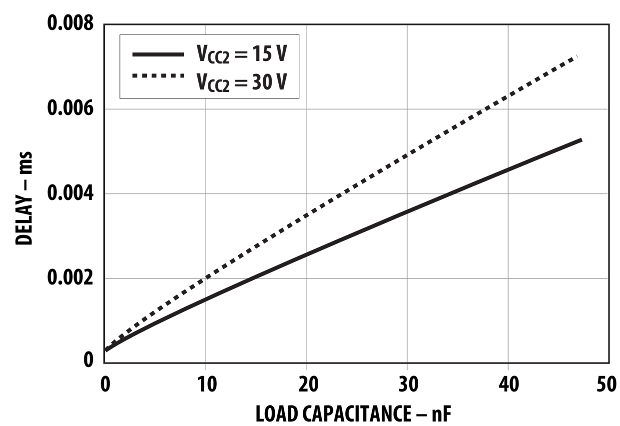


Figure 26. DESAT sense to 10% Vout delay vs. load capacitance.

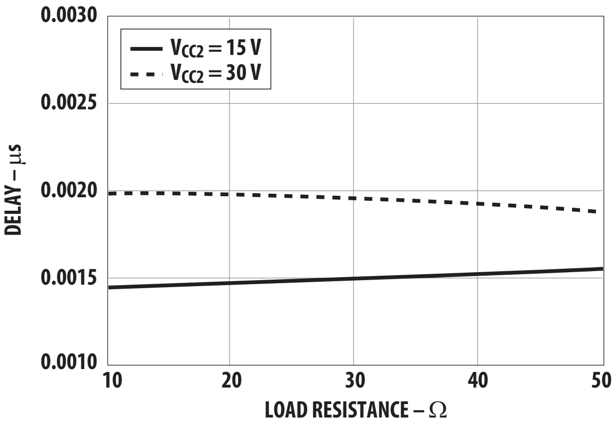


Figure 27. DESAT sense to 10% Vout delay vs. load resistance.

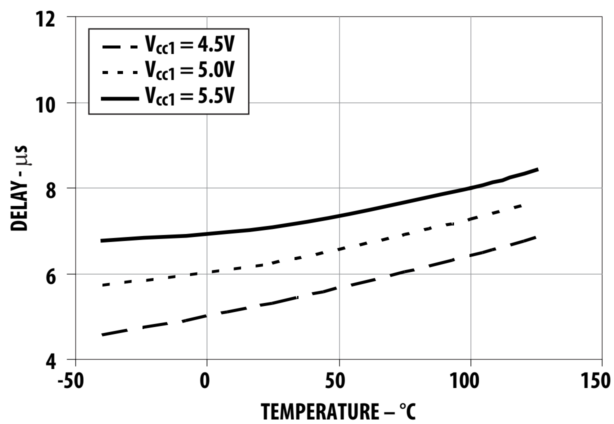


Figure 28. RESET to high level fault signal delay vs. temperature.

Test Circuit Diagrams

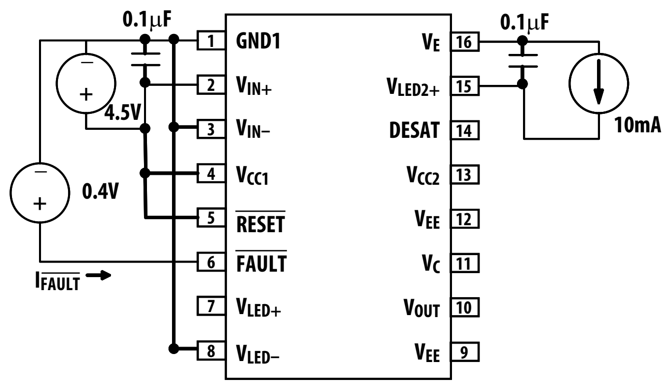


Figure 29. $I_{\overline{FAULTL}}$ test circuit.

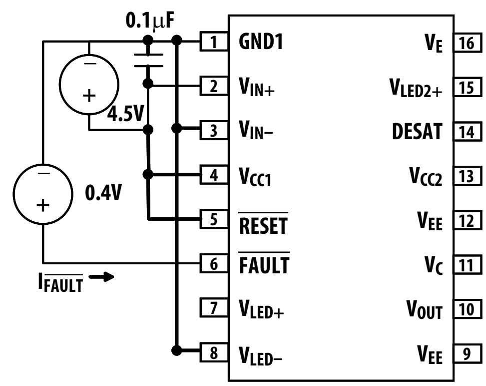


Figure 30. $I_{\overline{FAULTH}}$ test circuit.

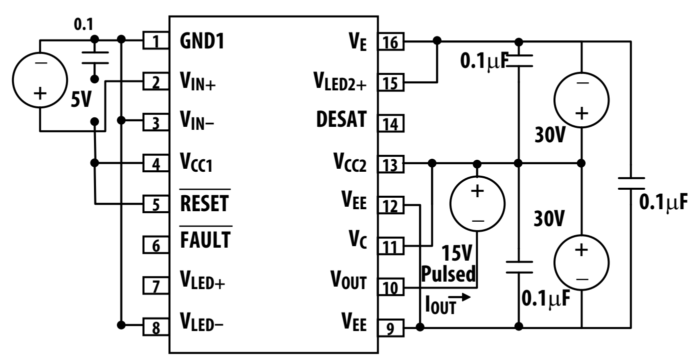


Figure 31. I_{OH} pulsed test circuit.

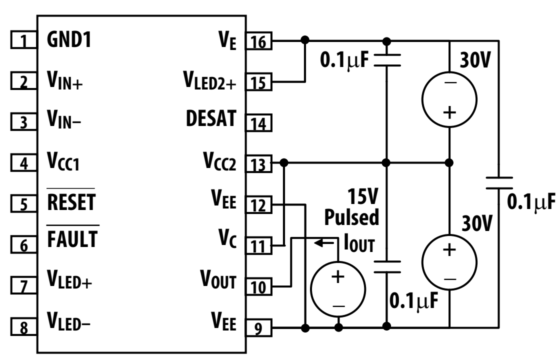


Figure 32. I_{OL} pulsed test circuit.

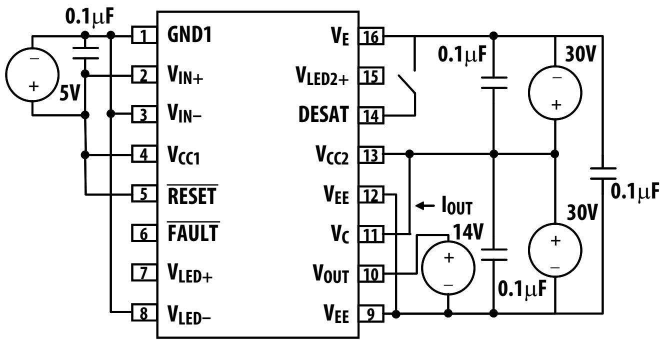


Figure 33. I_{OLF} test circuit.

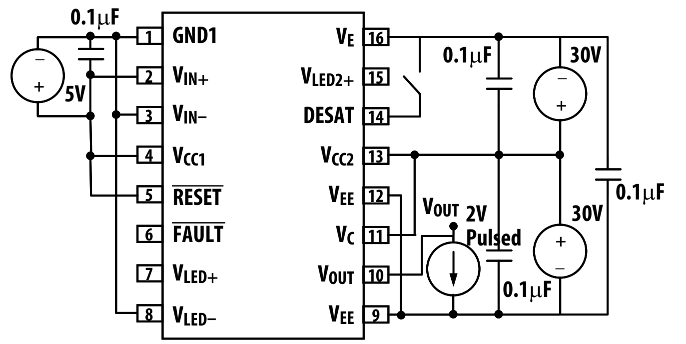


Figure 34. V_{OH} pulsed test circuit.

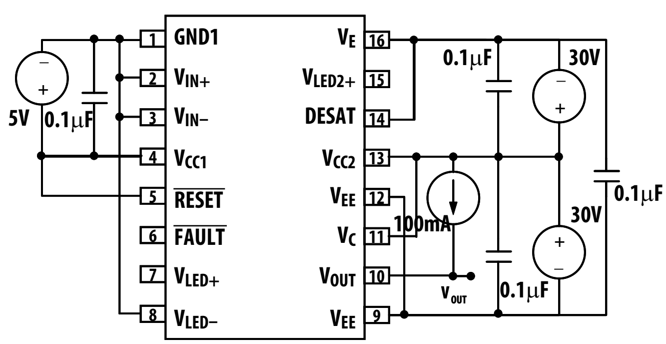


Figure 35. V_{OL} test circuit.

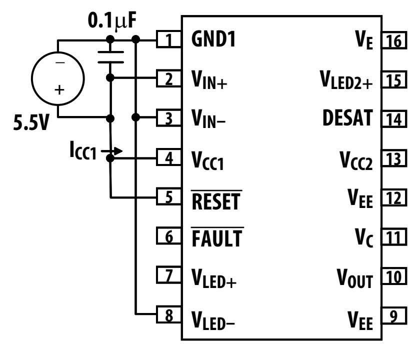


Figure 36. I_{CC1H} test circuit.

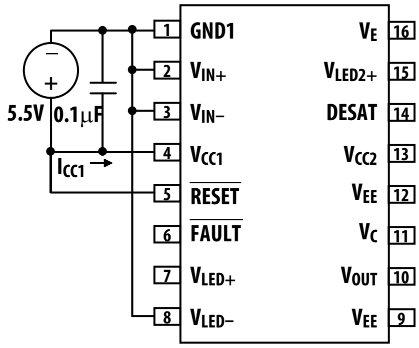


Figure 37. I_{CC1L} test circuit.

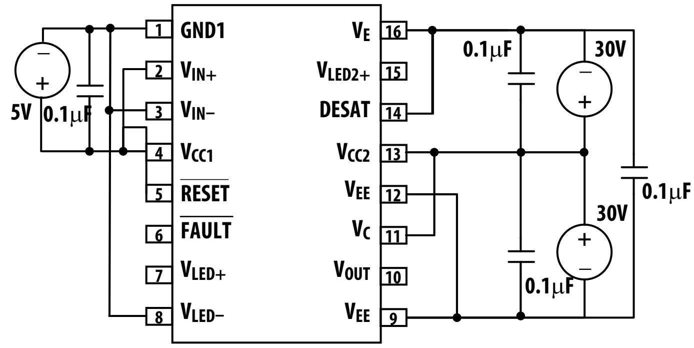


Figure 38. I_{CC2H} test circuit.

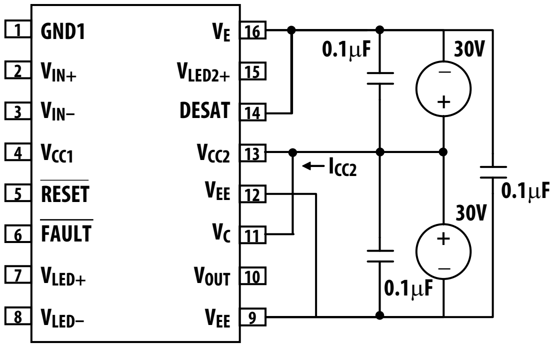


Figure 39. I_{CC2L} test circuit.

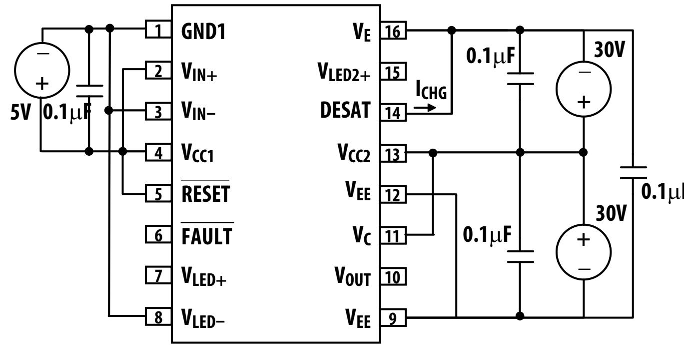


Figure 40. I_{CHG} pulsed test circuit.

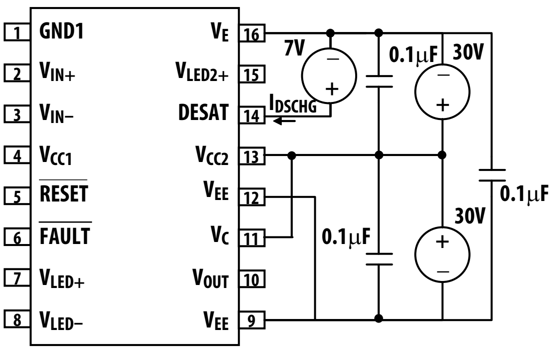


Figure 41. I_{DSCHG} test circuit.

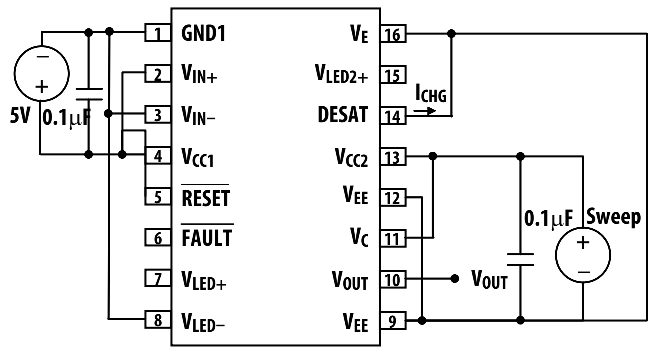


Figure 42. UVLO threshold test circuit.

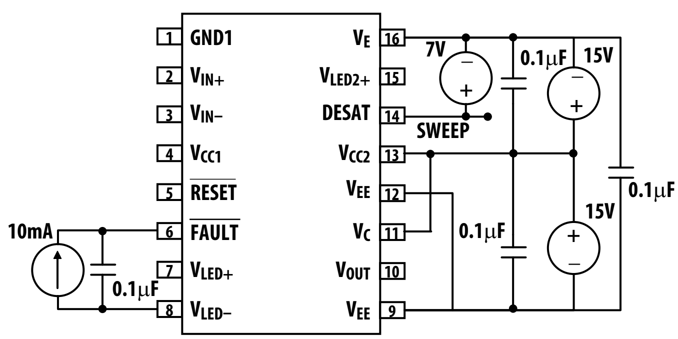


Figure 43. DESAT threshold test circuit.

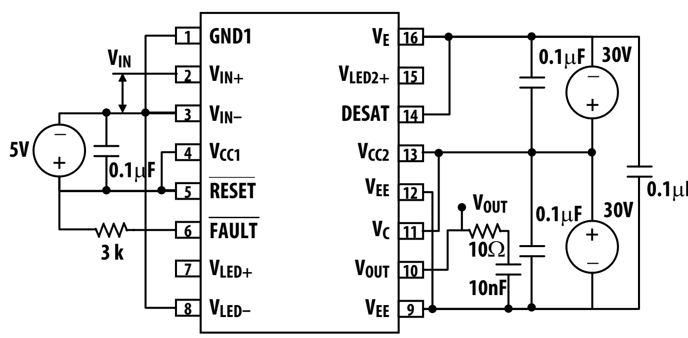


Figure 44. t_{PLH}, t_{PHL}, t_r, t_f test circuit.

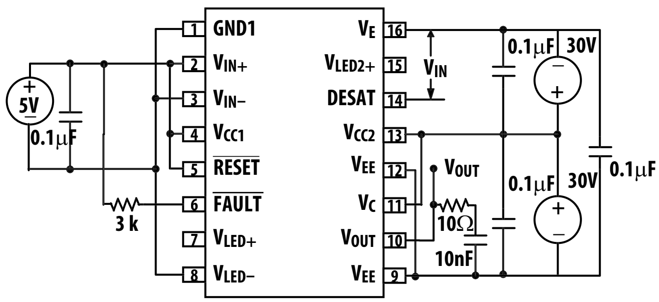


Figure 45. t_{DESAT}(10%) test circuit.

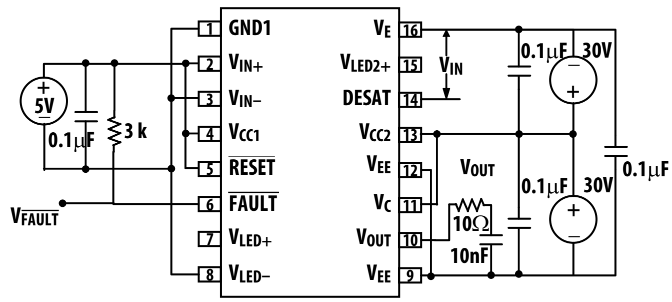


Figure 46. t_{DESAT}(FAULT) test circuit.

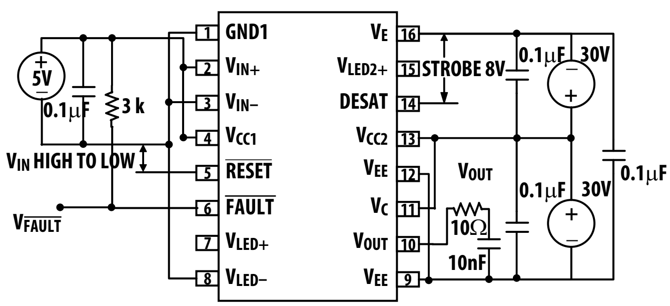


Figure 47. t_{RESET}(FAULT) test circuit.

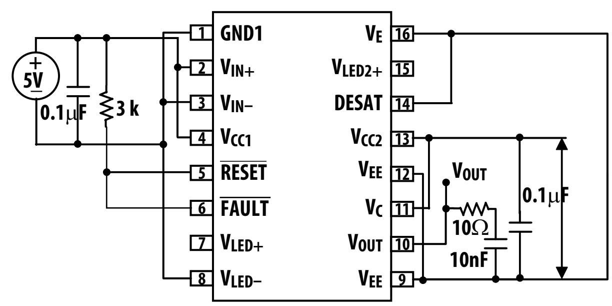


Figure 48. UVLO delay test circuit.

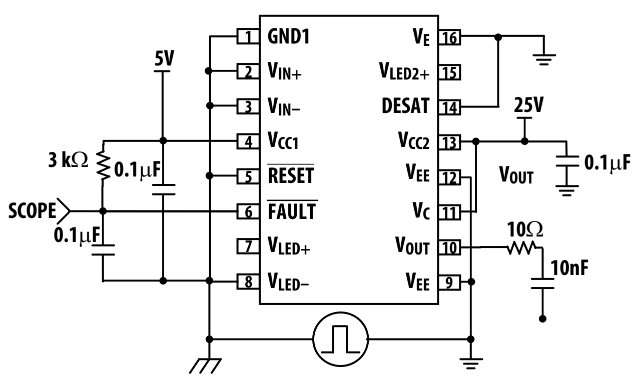


Figure 49. CMR test circuit, LED2 off.

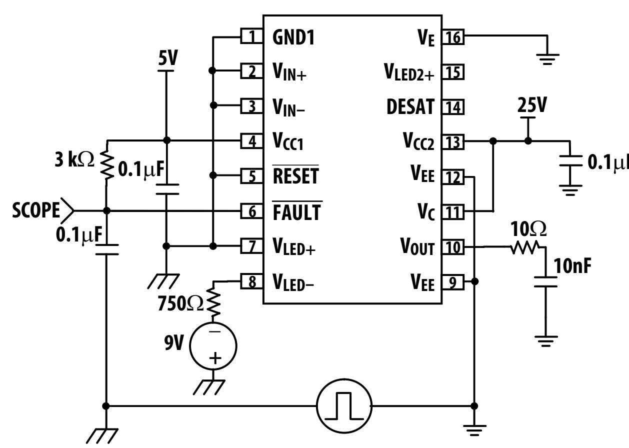


Figure 50. CMR test circuit, LED2 on.

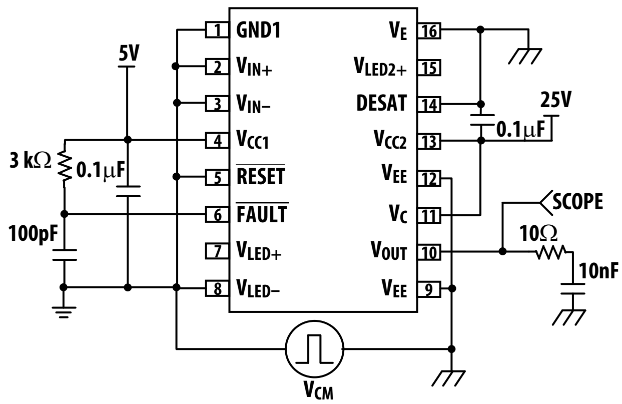


Figure 51. CMR test circuit, LED1 off.

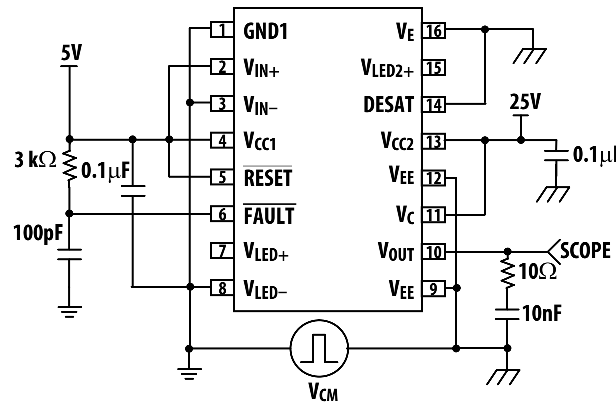


Figure 52. CMR test circuit, LED1 on.

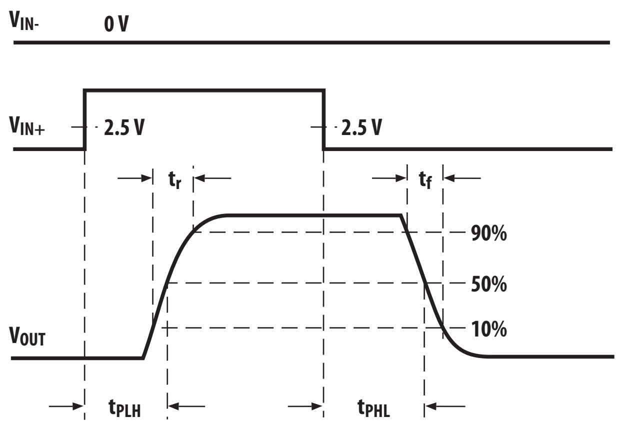


Figure 53. V_{OUT} propagation delay waveforms, noninverting configuration.

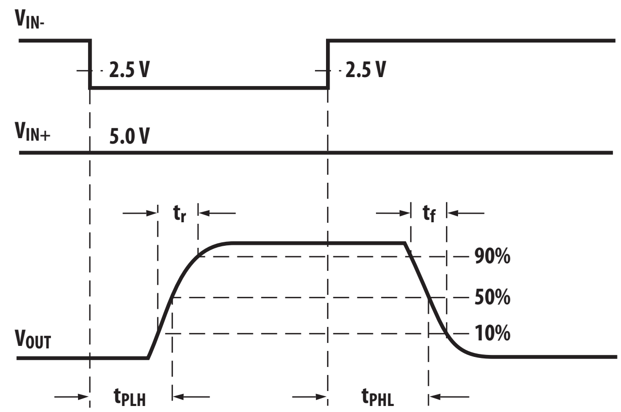


Figure 54. V_{OUT} propagation delay waveforms, inverting configuration.

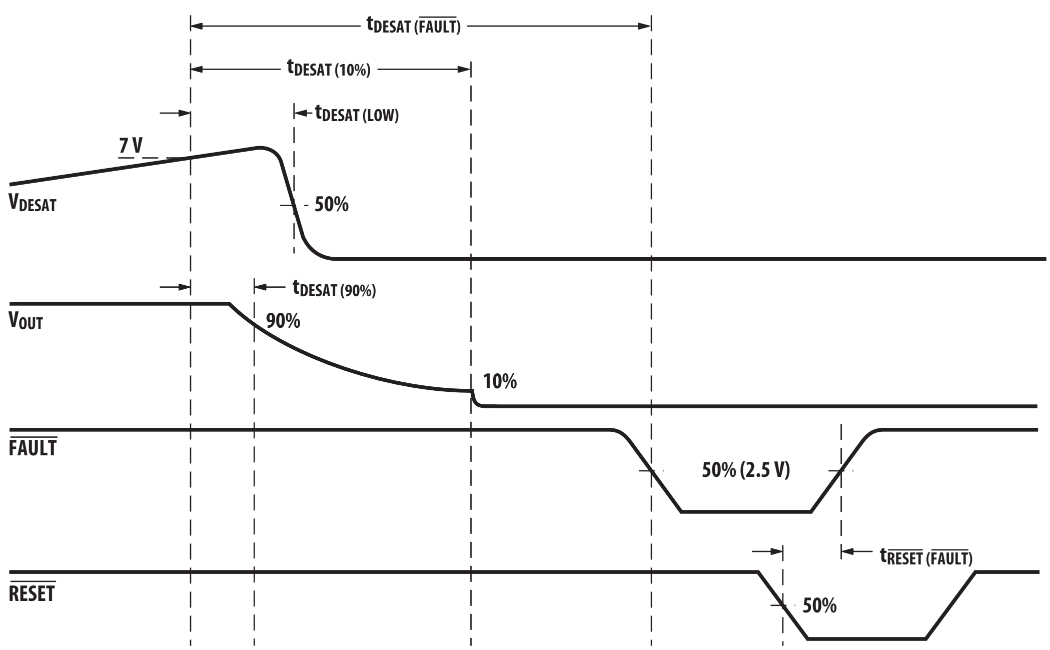


Figure 55. Desat, V_{OUT}, fault, reset delay waveforms.

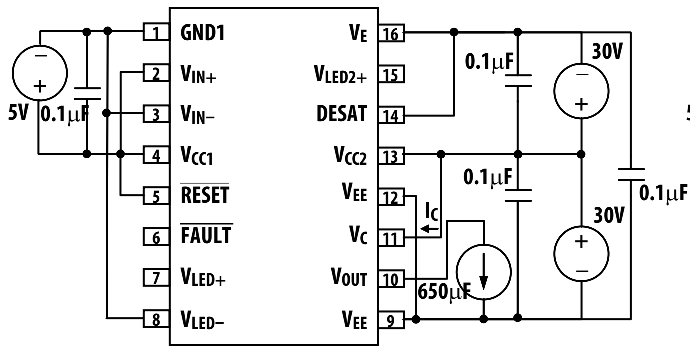


Figure 56. I_{CH} test circuit.

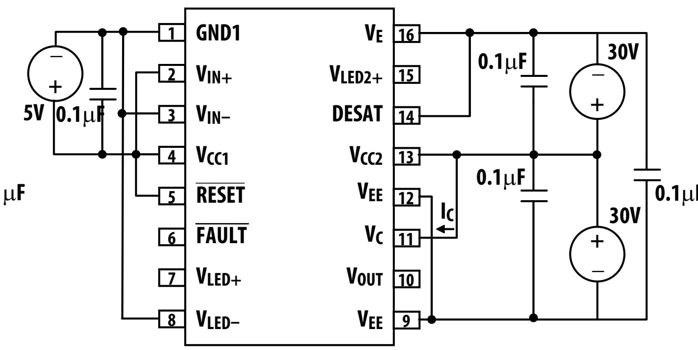


Figure 57. I_{CH} test circuit.

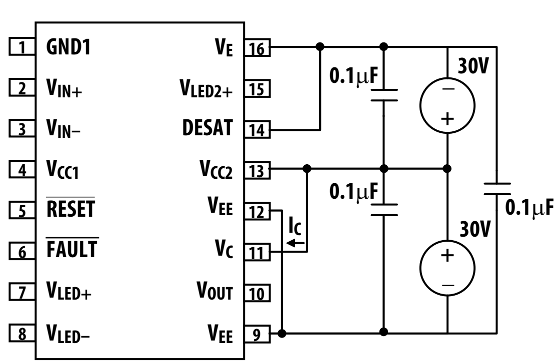


Figure 58. I_{CL} test circuit.

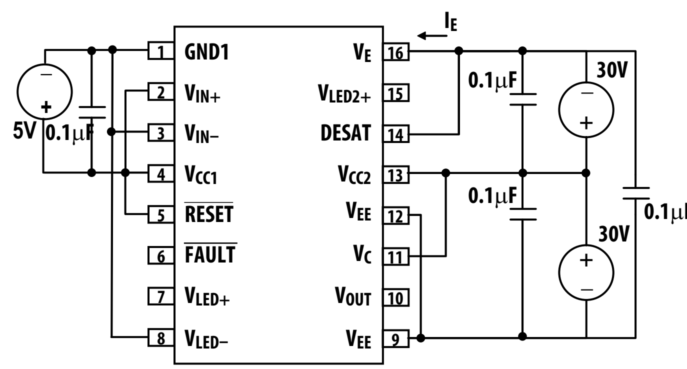


Figure 59. I_{EH} test circuit.

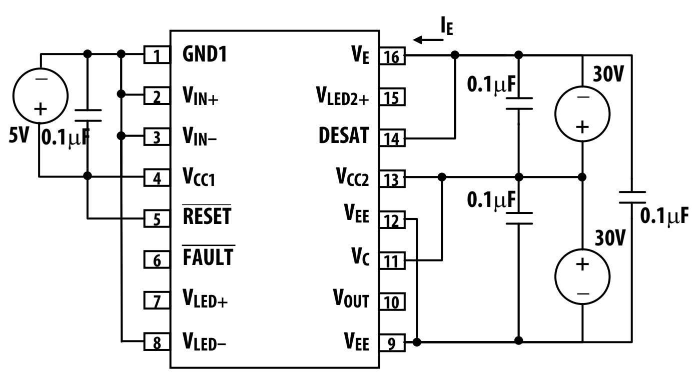


Figure 60. I_{EL} test circuit.

Typical Application/Operation

Introduction to Fault Detection and Protection

The power stage of a typical three phase inverter is susceptible to several types of failures, most of which are potentially destructive to the power IGBTs. These failure modes can be grouped into four basic categories: phase and/or rail supply short circuits due to user misconnect or bad wiring, control signal failures due to noise or computational errors, overload conditions induced by the load, and component failures in the gate drive circuitry. Under any of these fault conditions, the current through the IGBTs can increase rapidly, causing excessive power dissipation and heating. The IGBTs become damaged when the current load approaches the saturation current of the device, and the collector to emitter voltage rises above the saturation voltage level. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn--off the overcurrents during a fault condition.

A circuit providing fast local fault detection and shutdown is an ideal solution, but the number of required components, board space consumed, cost, and complexity have until now limited its use to high performance drives. The features which this circuit must have are high speed, low cost, low resolution, low power dissipation, and small size.

Applications Information

The ACPL-36JV satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shut down, and an optically isolated fault status feedback signal into a single 16-pin surface mount package.

The fault detection method, which is adopted in the ACPL-36JV, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off state of the IGBT, the fault detect circuitry is simply disabled to prevent false 'fault' signals.

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the ACPL-36JV limits the power dissipation in the IGBT even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly- conservative overcurrent threshold is not needed to protect the IGBT.

Recommended Application Circuit

The ACPL-36JV has both inverting and non-inverting gate control inputs, an active low reset input, and an open collector fault output suitable for wired 'OR' applications.

The recommended application circuit shown in Figure 61 illustrates a typical gate drive implementation using the ACPL-36JV.

The four supply bypass capacitors (0.1 μF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (5 mA) power supply suffices. The desat diode and 100pF capacitor are the necessary external components for the fault detection circuitry. The gate resistor (10 Ω) serves to limit gate charge current and indirectly control the IGBT collector voltage rise and fall times. The open collector fault output has a passive 3.3 kΩ pull-up resistor and a 330 pF filtering capacitor.

A clamping diode between V_{CC1} and $\overline{\text{RESET}}$ will prevent positive going voltage noises affecting the $\overline{\text{FAULT}}$ status.

A 47 kΩ pulldown resistor on V_{OUT} provides a more predictable high level output voltage (V_{OH}). In this application, the IGBT gate driver will shut down when a fault is detected and will not resume switching until the microcontroller applies a reset signal.

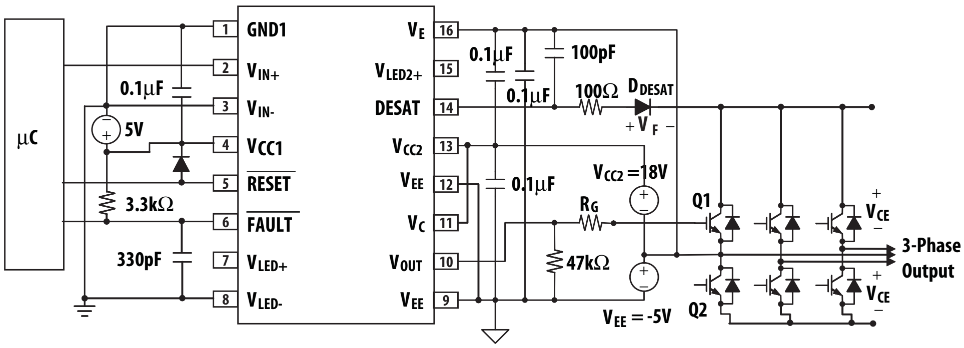


Figure 61. Recommended application circuit.

Description of Operation/Timing

Figure 62 illustrates input and output waveforms under the conditions of normal operation, a desat fault condition, and normal reset behavior.

Normal Operation

During normal operation, V_{OUT} of the ACPL-36JV is controlled by either V_{IN+} or V_{IN-}, with the IGBT collector-to-emitter voltage being monitored through D_{DESAT}. The $\overline{FAULT}$ output is high and the $\overline{RESET}$ input should be held high. See Figure 62.

Fault Condition

When the voltage on the DESAT pin exceeds 7 V while the IGBT is on, V_{OUT} is slowly brought low in order to "softly" turn-off the IGBT and prevent large di/dt induced voltages. Also activated is an internal feedback channel which brings the $\overline{FAULT}$ output low for the purpose of notifying the micro-controller of the fault condition. See Figure 62.

Reset

The $\overline{FAULT}$ output remains low until $\overline{RESET}$ is brought low. See Figure 62. While asserting the $\overline{RESET}$ pin (LOW), the input pins must be asserted for an output low state (V_{IN+} is LOW or V_{IN-} is HIGH). This may be accomplished either by software control (i.e. of the microcontroller) or hardware control (see Figures 71 and 72).

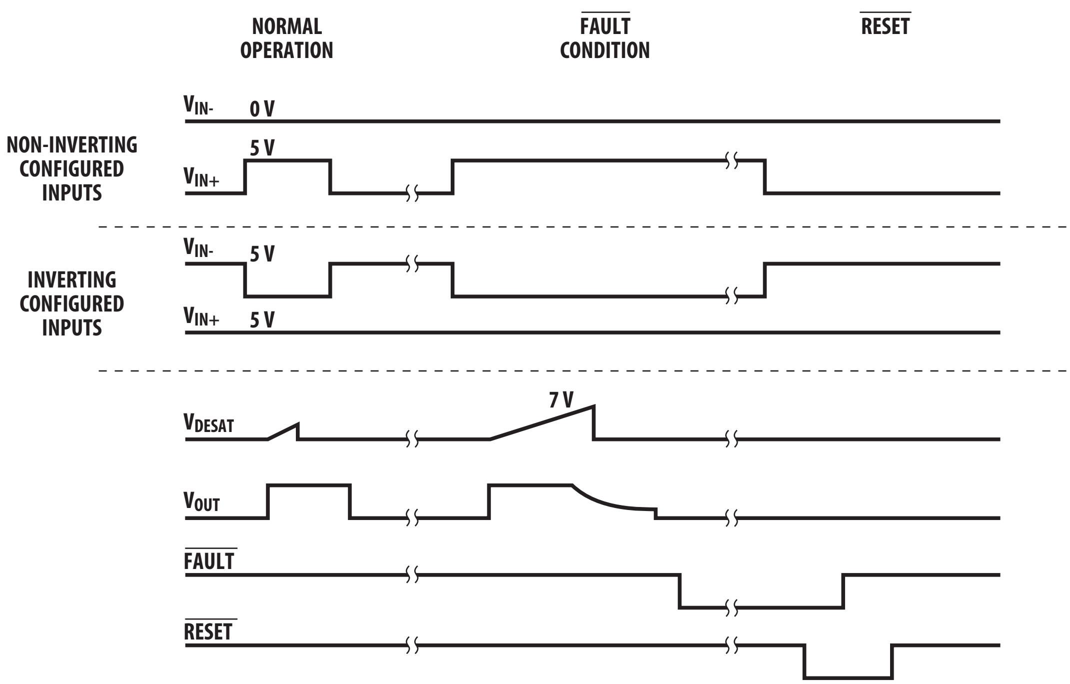


Figure 62. Timing diagram.

Slow IGBT Gate Discharge During Fault Condition

When a desaturation fault is detected, a weak pull-down device in the ACPL-36JV output drive stage will turn on to 'softly' turn off the IGBT. This device slowly discharges the IGBT gate to prevent fast changes in drain current that could cause damaging voltage spikes due to lead and wire inductance. During the slow turn off, the large output pull-down device remains off until the output voltage falls below V_{EE} + 2 Volts, at which time the large pull down device clamps the IGBT gate to V_{EE}.

DESAT Fault Detection Blanking Time

The DESAT fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT theshold. This time period, called the DESAT blanking time, is controlled by the internal DESAT charge current, the DESAT voltage threshold, and the external DESAT capacitor. The nominal blanking time is calculated in terms of external capacitance (C_{BLANK}), FAULT threshold voltage (V_{DESAT}), and DESAT charge current (ICHG) as $t_{BLANK} = C_{BLANK} \times V_{DESAT} / I_{CHG}$. The nominal blanking time with the recommended 100 pF capacitor is 100 pF * 7 V / 250 A = 2.8 μsec. The capacitance value can be scaled slightly to adjust the blanking time, though a value smaller than 100 pF is not recommended.

This nominal blanking time also represents the longest time it will take for the ACPL-36JV to respond to a DESAT fault condition. If the IGBT is turned on while the collector and emitter are shorted to the supply rails (switching into a short), the soft shut-down sequence will begin after approximately 3 μsec. If the IGBT collector and emitter are shorted to the supply rails after the IGBT is already on, the response time will be much quicker due to the parasitic parallel capacitance of the DESAT diode. The recommended 100 pF capacitor should provide adequate blanking as well as fault response times for most applications.

Under Voltage Lockout

The ACPL-36JV Under Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to the IGBT by forcing the ACPL-36JV output low during power-up. IGBTs typically require gate voltages of 15 V to achieve their rated $V_{CE(ON)}$ voltage. At gate voltages below 13 V typically, their on-voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10 V), the IGBT may operate in the linear region and quickly overheat. The UVLO function causes the output to be clamped whenever insufficient operating supply (V_{CC2}) is applied. Once V_{CC2} exceeds V_{UVLO+} (the positive-going UVLO threshold), the UVLO clamp is released to allow the device output to turn on in response to input signals. As V_{CC2} is increased from 0 V (at some level below V_{UVLO+}), first the DESAT protection circuitry becomes active. As V_{CC2} is further increased (above V_{UVLO+}), the UVLO clamp is released. Before the time the UVLO clamp is released, the DESAT protection is already active. Therefore, the UVLO and DESAT FAULT DETECTION features work together to provide seamless protection regardless of supply voltage (V_{CC2}).

Behavioral Circuit Schematic

The functional behavior of the ACPL-36JV is represented by the logic diagram in Figure 63 which fully describes the interaction and sequence of internal and external signals in the ACPL-36JV.

Input IC

In the normal switching mode, no output fault has been detected, and the low state of the fault latch allows the input signals to control the signal LED. The fault output is in the open-collector state, and the state of the Reset pin does not affect the control of the IGBT gate. When a fault is detected, the FAULT output and signal input are both latched. The fault output changes to an active low state, and the signal LED is forced off (output LOW). The latched condition will persist until the Reset pin is pulled low.

Output IC

Three internal signals control the state of the driver output: the state of the signal LED, as well as the UVLO and Fault signals. If no fault on the IGBT collector is detected, and the supply voltage is above the UVLO threshold, the LED signal will control the driver output state. The driver stage logic includes an interlock to ensure that the pull-up and pull-down devices in the output stage are never on at the same time. If an undervoltage condition is detected, the output will be actively pulled low by the 50x DMOS device, regardless of the LED state. If an IGBT desaturation fault is detected while the signal LED is on, the Fault signal will latch in the high state. The triple darlington AND the 50x DMOS device are disabled, and a smaller 1x DMOS pull-down device is activated to slowly discharge the IGBT gate. When the output drops below two volts, the 50x DMOS device again turns on, clamping the IGBT gate firmly to Vee. The Fault signal remains latched in the high state until the signal LED turns off.

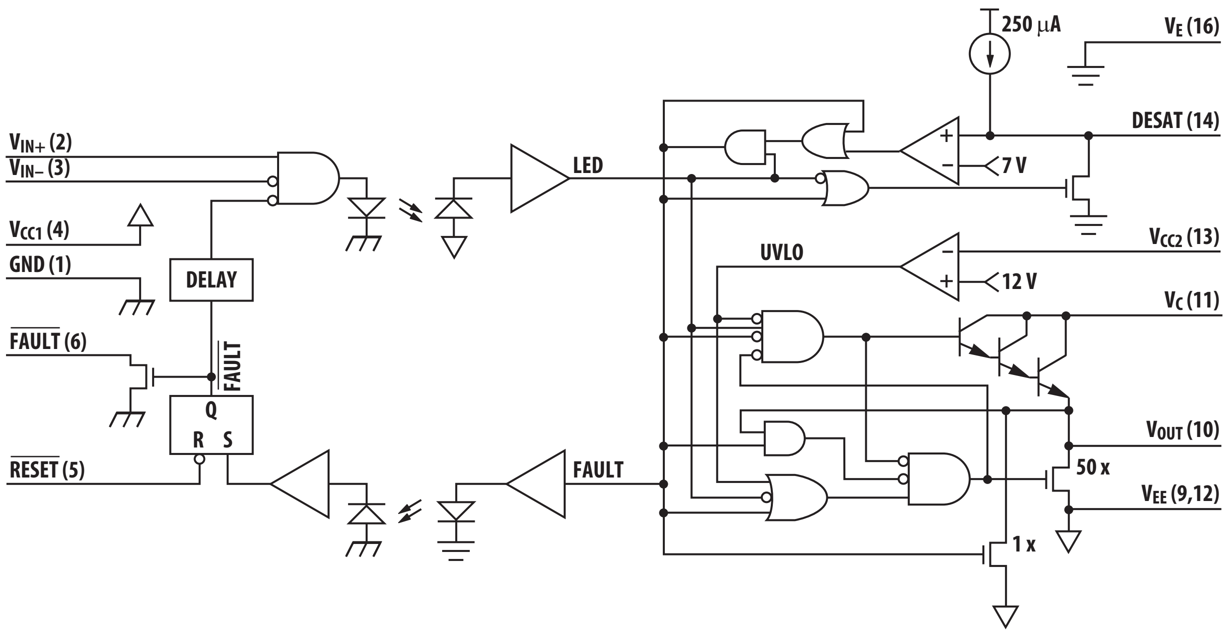


Figure 63. Behavioral circuit schematic

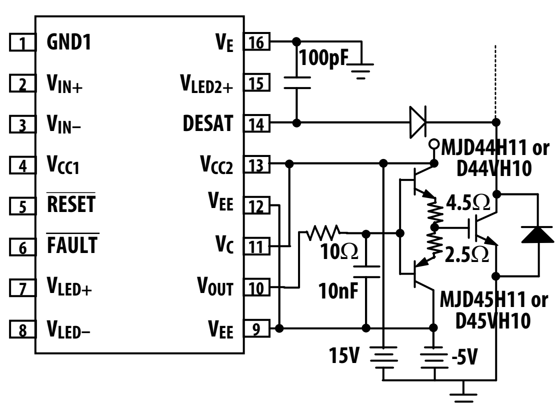


Figure 64. Output pull-down resistor.

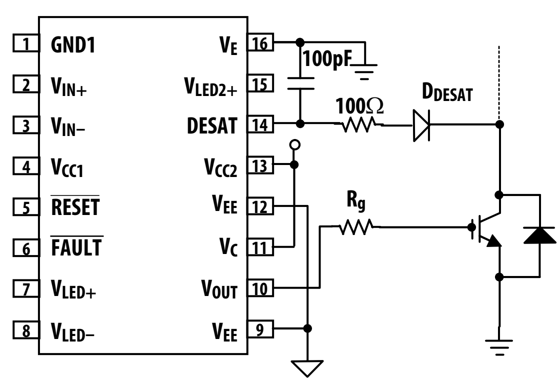


Figure 65. DESAT pin protection.

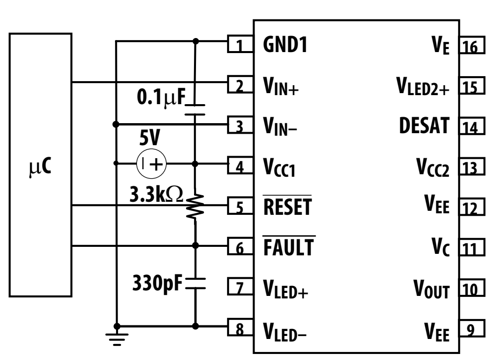


Figure 66. FAULT Pin CMR protection.